400061

National Semiconductor

Operational Amplifiers Databook

- Operational Amplifiers
- Buffers
- Voltage Comparators

OPERATIONAL AMPLIFIERS
DATABOOK

1993 Edition

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BLC™
BLX™
BMAC™
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BSI™
BSI-2™
CDD™
CIM™
CIMBUS™
CLASIC™
COMBO®
COMBO I™
COMBO II™
COPS™ microcontrollers
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DA4™
DENSPAK™
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DISCERN™
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ISE™
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ISE/16™
ISE32™
ISOPLANAR™
ISOPLANAR-Z™
LERIC™
LMCMOS™
M²CMOS™
Macrobus™
Macrocomponent™
MAPL™
MAXI-ROM®
Microbus™ data bus
MICRO-DAC™
μtalker™
Microtalker™
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MPA™
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SONIC™
SPIRE™
Staggered Refresh™
STAR™
Starlink™
STARPLEX™
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SuperChip™
SuperScript™
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VIP™
VR32™
WATCHDOG™
XMOS™
XPU™
Z STAR™
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Product Status Definitions

Definition of Terms

Data Sheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This data sheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This data sheet contains preliminary data, and supplementary data will be published at a later date. National Semiconductor Corporation reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
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Additional Available Linear Devices

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National Semiconductor

Cross Reference by Part Number

A complete interchangeability list of Linear IC's offered by most Integrated Circuit Manufacturers is listed in this section, and references the nearest National Semiconductor Corporation direct replacement or recommended replacement with either an improved or functional replacement.

The following companies are included in this cross reference:

Analog Devices	Harris (GE/RCA/Intersil)	Philips	Signetics
Burr Brown	Hitachi	Precision Monolithics Inc.	Siliconix
Cherry	Linear Technology Corp.	Raytheon	Texas Instruments
Elantec	Maxim	Samsung	Toshiba
Fairchild (NSC)	Motorola	SGS Thompson	Unitrode

Part Number	NSC Part Number		Part Number	NSC Part Number		Part Number	NSC Part Number	
ANALOG DEVICES								
AD0042	LH0042	I	AD590	LM135	S	AD7542	DAC1210	S
AD101A	LM101A	I	AD590	LM34	S	AD7545	DAC1208	S
AD201A	LM201A	I	AD590	LM35	S	AD7545	DAC1209	S
AD301A	LM301A	I	AD611	LF441	I	AD7545	DAC1210	S
AD5035	LH0042	S	AD624	LM363	S	AD7548	DAC1230	S
AD506	LH0022	S	AD650	LM331	S	AD7548	DAC1231	S
AD509	LH0003	S	AD651	LM331	S	AD7548	DAC1232	S
AD521	LH0036	S	AD654	LM331	S	AD7552	ADC1220	S
AD521	LM363	S	AD673	ADC0841	S	AD7552	ADC1225	S
AD522	LH0038	S	AD707	LM607	I	AD7575	ADC0820	S
AD524	LM363	S	AD711	LF411	S	AD7576	ADC0820	S
AD537	LM331	S	AD712	LF412	S	AD7578	ADC1205	S
AD546	LPC660	I	AD741	LM741	D	AD7578	ADC1225	S
AD546	LPC662	I	AD746	LM6218	I	AD7820	ADC0820	D
AD548	LF441	D	AD7502	LF13509	S	AD7821	ADC08061	I
AD549	LPC660	I	AD7523	DAC0830	S	AD7824	ADC08064	I
AD549	LPC662	I	AD7523	DAC0831	S	AD7828	ADC08068	I
AD562	DAC1266	S	AD7523	DAC0832	S	AD844	LM6181	I
AD563	DAC1265	S	AD7524	DAC0830	S	AD846	LM6181	I
AD565A	DAC1265	S	AD7524	DAC0831	S	AD847	LM6161	D
AD566A	DAC1266	S	AD7524	DAC0832	S	AD848	LM6164	D
AD567	DAC1230	S	AD7533	DAC1020	D	AD849	LM6165	D
AD573	ADC1005	S	AD7533	DAC1021	D	AD96685	LM6685	I
AD581	LH0070	I	AD7533	DAC1022	D	AD96687	LM6687	I
AD582	LF398	S	AD7541	DAC1218	S	ADDAC-08	DAC0800	D
AD583	LF398	S	AD7541	DAC1219	S	ADDAC-08	DAC0801	D
AD588	LM369	S	AD7541A	DAC1218	S	ADDAC-08	DAC0802	D
AD589M	LM385	I	AD7541A	DAC1219	S	ADOP07	LM607	I
AD589U	LM185	I	AD7542	DAC1208	S	HTC-0300	LH4860	S
AD590	LM134	S	AD7542	DAC1209	S			

The following notations are appended to assist you in finding the best option.
S = NSC Similar Device I = NSC Improved Device D = NSC Direct Replacement

Part Number	NSC Part Number	
BURR-BROWN		
3507	LH0003	S
3507	LM118	S
3507	LM6361	S
3507	LM709	S
3510	LM101	S
3510	LM107	S
3510	LM112	S
3510	LM725	S
3510	LM748	S
3533	LH0033	S
3542	LH0042	S
3550	LM6361	S
3551	LH0024	S
3551	LM6361	S
3553	LH0002	S
3553	LH0063	S
3554	LH0032	S
3571	LM675	S
3572	LH0021	S
3573	LM675	S
3580	LH0004	S
3580	LM143	S
3580	LM144	S
3606A6	LH0084	S
3606A6	LH0086	S
3626	LH0036	S
3629	LH0038	S
ADC80	ADC1280	S
DAC7541A	AD7521	S
DAC7541A	AD7531	S
DAC7541A	DAC1218	S
DAC7541A	DAC1219	S
DAC811	ADC1230	S
H0S-100	LH0033	S
HI-508	LF13508	S
HI-509	LF13509	S
INA101	LM163	S
INA101HP	LM363	S
INA102	LH0038	S
INA102	LM363	S

Part Number	NSC Part Number	
OPA111	LH0052	S
OPA121	LF441A	S
OPA121	LH0022	S
OPA121	LH0042	S
OPA156	LF156	S
OPA21	LM108A	S
OPA21	LM11	S
OPA2111	LF353	S
OPA2111	LF412A	S
OPA2111	LF442A	S
OPA2111	LH2011	S
OPA2111	LH2101A	S
OPA2111	LH2108A	S
OPA2111	LM1558	S
OPA2111	LM358	S
OPA2111	LM2904	S
OPA2111	LM747A	S
OPA27	LH0044	S
OPA27	LM627	S
OPA37	LM637	S
OPA404	LF444A	S
OPA404	LM837	S
OPA404	LMC660	S
OPA511	LM675	S
OPA541	LH0101	S
OPA541	LM12	S
OPA602	LF411	S
OPA605	LH0005	S
OPA605	LH0032	S
OPA633	LH0033	S
OPA633	LH4001	S
PGA100/102	LH0086	S
PGA200/201	LH0084	S
SHC298	LF298	D
SHC298	LH0043	S
SHC5320	LH0053	D
SHC80	LF398	S
SHC85	LF398	S
SHC85	LH0053	S
VFC32	LM131/331	S

Part Number	NSC Part Number	
CHERRY		
CS-189	LM1819	S
CS-2907	LM2907	D
CS-2917	LM2917	D
CS-925	LM2925	S
CS-935	LM2935	S
ELANTEC		
EHA2500	LM6161	S
EHA2502	LM6161	S
EHA2505	LM6361	S
EHA2510	LM6161	S
EHA2512	LM6161	S
EHA2515	LM6361	S
EHA2520	LM6164	S
EHA2522	LM6164	S
EHA2525	LM6364	S
EHA2600	LM6161	S
EHA2602	LM6161	S
EHA2605	LM6361	S
EHA2620	LM6164	S
EHA2622	LM6164	S
EHA2625	LM6364	S
EL2006	LM6161	S
EL2006C	LM6261	S
EL2020	LM6181	I
ELH0002	LH0002	D
ELH0021	LH0021	D
ELH0032	LH0032	D
ELH0033	LH0033	D
ELH0041	LH0041	D
ELH0101	LH0101	D

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Part Number	NSC Part Number	
FAIRCHILD (NSC)		
μA101	LM101	D
μA105	LM105	D
μA108	LM108	D
μA108A	LM108A	D
μA110	LM110	D
μA111	LM111	D
μA117	LM117	D
μA124	LM124	D
μA139	LM139	D
μA1458	LM1458	D
μA1489	DS1489	D
μA1558	LM1558	D
μA201	LM201	D
μA208	LM208	D
μA208A	LM208A	D
μA2111	LH2111	D
μA224	LM224	D
μA239	LM239	D
μA26LS31	DS26LS31	D
μA26LS32	DS26LS32	D
μA2901	LM2901	D
μA301	LM301	D
μA301A	LM301A	D
μA305	LM305	D
μA3052	TP3052	D
μA305A	LM305A	D
μA308	LM308	D
μA3086	LM3086	D
μA30S54	TP3054	D
μA30S57	TP3057	D
μA30S64	TP3064	D
μA30S67	TP3067	D
μA311	LM311	D
μA317	LM317	D
μA324	LM324	D
μA3302	LM3302	D
μA348	LM348	D
μA3486	DS3486	D
μA350	LM350	D
μA5116	TP5116	D
μA5156	TP5156	D
μA555	LM555	D
μA556	LM556	D
μA5800	TP3204	D
μA709	LM709	D
μA710	LM710	D
μA711	LM711	D
μA723	LM723	D
μA725	LM725	D
μA741	LM741	D
μA747	LM747	D
μA748	LM748	D
μA75107	DS75107	D
μA75108	DS75108	D
μA75150	DS75150	D
μA75154	DS75154	D
μA75450	DS75450	D
μA75491	DS75491	D
μA760	LM760	D
μA771	LF351	D
μA772	LF353	D
μA774	LF347	D
μA7805	LM140	D
μA7805	LM340-5	D
μA7805	LM7805	D
μA7806	LM7806	D
μA7808	LM7808	D
μA7812	LM140	D
μA7812	LM340-12	D
μA7812	LM7812	D
μA7815	LM140	D
μA7815	LM340-15	D
μA7815	LM7815	D
μA7818	LM7818	D
μA7824	LM7824	D
μA78L05	LM78L05	D
μA78L12	LM78L12	D
μA78L15	LM78L15	D
μA78LXXA	LM78LXXA	D
μA78M05	LM78M05	D
μA78M12	LM78M12	D
μA78MXX	LM341-XX	D
μA78MXX	LM78MXX	D
μA78XX	LM140-XX	D
μA78XX	LM340-XX	D
μA78XX	LM78XX	D
μA7905	LM7905	D
μA7912	LM7912	D
μA7915	LM7915	D
μA79M05	LM79M05	D
μA79M12	LM79M12	D
μA79M15	LM79M15	D
μA79MXX	LM320-XX	D
μA79XX	LM320-XX	D
μA79XX	LM79LXX	D
μA79XX	LM79MXX	D
μA79XX	LM79XX	D
DAC1508	MC1508	D
SH0002	LH0002	D
SH1605	LH1605	D
HARRIS (GE/RCA/Intersil)		
μA748	LM748	D
AD7520	DAC1021	D
AD7520	DAC1022	D
AD7521	DAC1220	D
AD7521	DAC1221	D
AD7521	DAC1222	D
AD7530	DAC1020	S
AD7530	DAC1021	S
AD7530	DAC1022	S
AD7531	DAC1220	D
AD7531	DAC1221	D
AD7531	DAC1222	D
AD7533	DAC1020	D
AD7533	DAC1021	D
AD7533	DAC1022	D
AD7541	DAC1218	S
AD7541	DAC1219	S
ADC0801	ADC0801	D
ADC0802	ADC0802	D
ADC0803	ADC0803	D

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S = NSC Similar Device I = NSC Improved Device D = NSC Direct Replacement

HARRIS (GE/RCA/Intersil) (Continued)

Part Number	NSC Part Number	
ADC0804	ADC0804	D
CA081	LF411	S
CA081	TL081	D
CA082	LF412	S
CA082	TL082	D
CA084	LF147	S
CA084	LF347	S
CA124	LM124	D
CA139	LM139	D
CA139A	LM139A	D
CA1458	LM1458	D
CA1558	LM1558	D
CA158	LM158	D
CA158A	LM158A	D
CA224	LM224	D
CA239	LM239	D
CA239A	LM239A	D
CA258	LM258	D
CA258A	LM258A	D
CA301A	LM301A	D
CA307	LM307	D
CA3105	LM675	S
CA311	LM311	D
CA324	LM324	D
CA3290	LM393	S
CA339	LM339	D
CA339A	LM339A	D
CA3401	LM3401	D
CA358	LM358	D
CA358A	LM358A	D
CA741	LM741	D
CA747	LM747	D
CA748	LM748	D
DG201	LF13201	D
DG211	LF13201	D
DG212	LF13202	D
HA-OP07	LM607	I
HA2400	LM604	S
HA2404	LM604	S
HA2405	LM604	S
HA2406	LM604	S
HA2420	LH0023	S
HA2420	LH0043	S
HA2500	LM6161	S
HA2502	LM6161	S
HA2505	LM6361	S
HA2510	LM118	S
HA2510	LM318	S
HA2510	LM6161	S
HA2512	LM6161	S
HA2515	LM6361	S
HA2520	LM6164	S
HA2520	LM6113	S
HA2522	LM6164	S
HA2522	LM6113	S
HA2525	LM6364	S
HA2525	LM6313	S
HA2529	LM6313	S
HA2530	LH0024	S
HA2535	LH0024	S
HA2540	LH0032	S
HA2541-2	LM6161	S
HA2541-5	LM6361	S
HA2542	LH0032	S
HA2620	LH4104	S
HA2620	LM6164	S
HA2622	LM118	S
HA2625	LM318	S
HA2640	LH0004	S
HA2640	LM143	S
HA2640	LM144	S
HA2645	LM343	S
HA2645	LM344	S
HA4741	LM348	S
HA5002	LH0002	S
HA5033	LH0033	S
HA5020	LM6181	I
HA5102	LM833	S
HA5104	LM837	S
HA5135	LM637	S
HA5141	LM4250	S
HA5142	LF442	D
HA5144	LF444	D
HA5160	LF357	S
HA5160	LH0062	S
HA5162	LH0062	S
HA5170	LF151	S
HA5170	LF155	S
HA5170	LF156	S
HA5170	LF157	S
HA5170	LF355	S
HA5170	LF356	S
HA5180	LH0022	S
HA5180	LH0042	S
HA5180	LH0052	S
HF-10	MF10	D
HF-201	LF13201	D
HF-300	AH5020	S
HI-201	LF13201	D
HI-508	LF13508	S
HI-509	LF13509	S
HI-5618	DAC0800	S
HI-5618	DAC0806	S
HI-5618	DAC0807	S
HI-5618	DAC0808	S
HI-565A	DAC1265	D
HI-5660	DAC1266	D
HI-5680	DAC1280	S
HI-5685	DAC1200	S
HI-5685	DAC1285	S
HI-5687	DAC1201	S
HI-5687	DAC1285	S
HI-5690	DAC1280	S
HI-5695	DAC1285	S
HI-5697	DAC1285	S
HI-574	ADC1080	S
HI-574	ADC1210	S
HI-574	ADC1211	S
HI-574	ADC1280	S
HI-674	ADC1080	S

The following notations are appended to assist you in finding the best option.

S = NSC Similar Device I = NSC Improved Device D = NSC Direct Replacement

Part Number	NSC Part Number	
HARRIS (GE/RCA/Intersil) (Continued)		
HI-674	ADC1280	S
ICH8530	LH0101	S
ICL7114	ADC1205	S
ICL7114	ADC1225	S
ICL7660	LMC7660	D
ICL8069	LM313	D
ICL8069	LM385-1.2	D
IH5009	AH5009	D
IH5010	AH5010	D
IH5011	AH5011	D
IH5012	AH5012	D
IH6106	LF13508	D
IH6206	LF13509	D
LM741	LM741	D
HITACHI		
HA12012	LM833	S
HA12411	LM3089	D
HA12412	LM3189	S
HA12413	LM1868	S
HA12417	LM1863	S
HA13421A	LM18293	S
HA1374	LM2877	S
HA1389	LM384	S
HA1394	LM2879	S
HA1397	LM1875	S
HA17082	LF353	I
HA17082A	LF412	I
HA17084	LF347	I
HA17084A	LF347B	I
HA17094	LM2904	I
HA17301	LM3301	I
HA17324	LM324	I
HA17339	LM339	I
HA17358	LM358	I
HA17393	LM393	I
HA17458	LM458	I
HA17741	LM741	I
HA17747	LM747	I
HA17901	LM2901	I
HA17902	LM2902	I
HA17903	LM2903	I

Part Number	NSC Part Number	
LINEAR TECHNOLOGY CORP.		
LF155	LF155	D
LF155A	LF155A	D
LF156	LF156	D
LF156A	LF156A	D
LF198	LF198	D
LF198A	LF198A	D
LF355A	LF355A	D
LF356A	LF356A	D
LF398	LF398	D
LF398A	LF398A	D
LF412A	LF412A	D
LH0070	LH0070	D
LH2108	LH2108	D
LH2108A	LH2108A	D
LM10	LM10	D
LM101A	LM101A	D
LM107	LM107	D
LM108	LM108	D
LM108A	LM108A	D
LM111	LM111	D
LM117	LM117	D
LM117HV	LM117HV	D
LM118	LM118	D
LM119	LM119	D
LM123	LM123	D
LM129	LM129	D
LM129A	LM129A	D
LM134	LM134	D
LM136	LM136	D
LM137	LM137	D
LM137HV	LM137HV	D
LM138	LM138	D
LM150	LM150	D
LM185	LM185	D
LM199	LM199	D
LM234	LM234	D
LM308A	LM308A	D
LM311	LM311	D
LM317	LM317	D
LM317HV	LM317HV	D

Part Number	NSC Part Number	
LM318	LM318	D
LM319	LM319	D
LM323	LM323	D
LM329	LM329	D
LM329A	LM329A	D
LM334	LM334	D
LM336	LM336	D
LM337	LM337	D
LM337HV	LM337HV	D
LM338	LM338	D
LM350	LM350	D
LM385	LM385	D
LM399	LM399	D
LM399A	LM399A	D
LT1001	LH0044	D
LT1001	LM607	I
LT1003	LM123	S
LT1003	LM323	S
LT1003	LM337	D
LT1004	LM113	D
LT1004	LM185	D
LT1004	LM385	D
LT1005	LM2935	S
LT1008	LM108	D
LT1008	LM308	D
LT1009	LM136	D
LT1009	LM336	D
LT1010	LH0002	S
LT1011	LM311	D
LT1012	LM312	D
LT1013	LM358	D
LT1014	LM324	D
LT1014	LM348	D
LT1019	LM368	D
LT1020	LP2951	S
LT1021	LM369	I
LT1022	LF356	D
LT1029	LM336	D
LT1031	LH0070	D
LT1033	LM133	D

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Part Number	NSC Part Number	
LINEAR TECHNOLOGY CORP. (Continued)		
LT1033	LM137	S
LT1033	LM333	D
LT1034	LM385	D
LT1038C	LM396	S
LT1038M	LM196	S
LT1055	LF355	D
LT1056	LF356	D
LT111	LM111	D
LM317HV	LM317HV	D
LT117	LM117	D
LT118	LM118	D
LT119	LM119	D
LT123	LM123	D
LT123A	LM123A	D
LT1223	LM6181	I
LT137	LM137	D
LT150	LM150	D
LT1524	LM1524D	D
LT311	LM311	D
LT317	LM317	D
LT317A	LM317A	D
LT318	LM318	D
LT319	LM319	D
LT323	LM323	D
LT323A	LM323A	D
LT337	LM337	D
LT338	LM338	D
LT338A	LM338A	D
LT350A	LM350A	D
LT3524	LM3524D	D
LTC1059	MF5	D
LTC1060	MF10	D
LTC1099	ADC0820	D
REF-01	LM368	S
SG1524	LM1524D	I
SG3524	LM3524D	I

Part Number	NSC Part Number	
MAXIM		
AD565	DAC1265	D
AD566	DAC1266	D
AD7523	DAC0830	S
AD7523	DAC0831	S
AD7523	DAC0832	S
AD7524	DAC0830	S
AD7524	DAC0831	S
AD7524	DAC0832	S
AD7533	DAC1020	D
AD7533	DAC1021	D
AD7533	DAC1022	D
AD7541	DAC1218	S
AD7541	DAC1219	S
AD7542	DAC1208	S
AD7542	DAC1209	S
AD7542	DAC1210	S
AD7545	DAC1208	S
AD7545	DAC1209	S
AD7545	DAC1210	S
AD7548	DAC1230	S
AD7548	DAC1231	S
AD7548	DAC1232	S
AD7820	ADC0820	D
ICL7642	LMC6044	S
MAX480	LMC6041	S
MOTOROLA		
AD562	DAC1266	S
AD563	DAC1265	S
DAC-08	DAC0800	D
DAC-08	DAC0801	D
DAC-08	DAC0802	D
LF347	LF347	D
LF351	LF351	D
LF353	LF353	D
LF355	LF355	D
LF356	LF356	D
LF357	LF357	D
LF411	LF411	D
LF412	LF412	D
LF441	LF441	D
LF442	LF442	D

Part Number	NSC Part Number	
LF444	LF444	D
LM101	LM101	D
LM108	LM108	D
LM109	LM109	D
LM11	LM11	D
LM111	LM111	D
LM117	LM117	D
LM123	LM123	D
LM124	LM124	D
LM137	LM137	D
LM139	LM139	D
LM140	LM140	D
LM148	LM148	D
LM150	LM150	D
LM158	LM158	D
LM193	LM193	D
LM201	LM201	D
LM208	LM208	D
LM209	LM109	D
LM211	LM211	D
LM217	LM117	D
LM223	LM123	D
LM224	LM224	D
LM237	LM137	D
LM239	LM239	D
LM248	LM248	D
LM250	LM150	D
LM258	LM258	D
LM285	LM285	D
LM2900	LM2900	D
LM2901	LM2901	D
LM2902	LM2902	D
LM2903	LM2903	D
LM2904	LM2904	D
LM293	LM293	D
LM2931	LM2931	D
LM301	LM301	D
LM307	LM307	D
LM308	LM308	D
LM309	LM309	D

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Part Number	NSC Part Number	
MOTOROLA (Continued)		
LM311	LM311	D
LM317	LM317	D
LM323	LM323	D
LM324	LM324	D
LM337	LM337	D
LM339	LM339	D
LM340-XX	LM340-XX	D
LM348	LM348	D
LM350	LM350	D
LM358	LM358	D
LM385	LM385	D
LM3900	LM3900	D
LM393	LM393	D
LM833	LM833	D
MC1391	LM1391	D
MC1408	DAC0806	D
MC1408	DAC0807	D
MC1408	DAC0808	D
MC1414	LM1414	D
MC1436	LM343	I
MC1437	LH2301	S
MC14442	ADC0829	S
MC14444	ADC0830	S
MC145040	ADC0811	S
MC145041	ADC0811	D
MC1455	LM555	D
MC1456	LM212	S
MC1458	LM1458	D
MC1468	LM325	S
MC1488	DS1488	D
MC1489	DS1489	D
MC1496	LM1496	D
MC1508	DAC0808	D
MC1514	LM1514	D
MC1536	LM143	I
MC1537	LH2101	S
MC1537	LH2201	S
MC1556	LM112	S
MC1558	LM1558	D
MC1568	LM125	S

Part Number	NSC Part Number	
MC1596	LM1596	D
MC1709	LM709	D
MC1710	LM710	D
MC1723	LM723	D
MC1741	LM741	D
MC1747	LM747	D
MC1748	LM748	D
MC3301	LM3301	D
MC3302	LM3302	D
MC33078	LM833	S
MC33079	LM837	S
MC3346	LM3046	D
MC3346	LM3146	I
MC3356	LM3089	S
MC3356	LM3189	S
MC3361	LM3361A	I
MC34001	LF351	I
MC34001	LF353	I
MC34001	LF411	I
MC34002	LF412	I
MC34004	LF347	I
MC3401	LM3401	D
MC3410	DAC1020	D
MC3412	DAC1265	S
MC3456	LM556	D
MC35001	LF411	I
MC35002	LF412	I
MC3510	DAC1020	D
MC4741	LM348	D
MC7812	LM7812	D
MC7815	LM7815	D
MC7824	LM7824	D
MC78LXX	LM78LXX	D
MC78LXXA	LM78LXXA	D
MC78MXX	LM341-XX	D
MC78MXX	LM78MXX	D
MC78XX	LM78XX	D
MC78XXA	LM340A-XX	D
MC79LXX	LM320L-XX	D
MC79LXX	LM79LXXA	D

Part Number	NSC Part Number	
MC79MXXA	LM79MXX	I
MC79XX	LM320-XX	I
MC79XX	LM79XX	D
MC79XXA	LM320-XX	I
PHILIPS		
μA723	LM723	D
μA741	LM741	D
μA747	LM747	D
ADC0803	ADC0803	D
ADC0804	ADC0804	D
ADC0805	ADC0805	D
ADC0820	ADC0820	D
AM26LS30	DS3691	D
CA3089	LM3089	D
DAC-08	DAC0801	D
DAC-08	DAC0800	D
DAC-08	DAC0802	D
ICM7555	LMC555	D
LF198	LF198	D
LF224	LM224	D
LF298	LF298	D
LF398	LF398	D
LM111	LM111	D
LM119	LM119	D
LM124	LM124	D
LM139	LM139	D
LM139A	LM139A	D
LM158	LM158	D
LM193	LM193	D
LM193A	LM193A	D
LM211	LM211	D
LM219	LM219	D
LM224	LM224	D
LM239	LM239	D
LM239A	LM239A	D
LM258	LM258	D
LM2901	LM2901	D
LM2903	LM2903	D
LM293	LM293	D
LM293A	LM293A	D

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Part Number	NSC Part Number	
PHILIPS (Continued)		
LM311	LM311	D
LM319	LM319	D
LM324	LM324	D
LM324A	LM324A	D
LM339	LM339	D
LM339A	LM339A	D
LM358	LM358	D
LM393	LM393	D
LM393A	LM393A	D
MC1408	DAC0807	D
MC1408	DAC0808	D
MC1458	LM1458	D
MC1488	DS1488	D
MC1488	DS14C88	I
MC1489	DS1489	D
MC1489A	DS1489A	D
MC1489A	DS14C89A	I
MC1496	LM1496	D
MC1508	DAC0808	D
MC1596	LM1596	D
MC3302	LM3302	D
MC3403	LM3403	D
NE4558	LM833	S
NE5034	ADC0841	S
NE5118	DAC0830	S
NE5119	DAC0830	S
NE5410	DAC1020	S
NE5532	LM833	D
NE5532	LM833	D
NE555	LM555	D
NE556	LM556	D
NE565	LM565	D
NE566	LM566	D
NE567	LM567	D
SA532	LM2904	I
SA534	LM2902	I
SE529	LM161	S
SE5537	LF398	D
SE555	LM555	D
SE556	LM556	D
SE567	LM567	D
SG1532	LM1524	I
SG2524	LM2524	D
SG3524	LM3524	D
PRECISION MONOLITHICS INC.		
ADC-910	ADC1025	S
ADC-910	ADC1061	S
AMP-01	LH0038	S
AMP01	LM363	S
BUF-03	LH0033	I
BUF-03	LH0002	S
CMP-08	LM260	S
CMP-08	LM360	S
DAC-02	DAC1020	S
DAC-02	DAC1021	S
DAC-02	DAC1022	S
DAC-03	DAC1020	S
DAC-03	DAC1021	S
DAC-03	DAC1022	S
DAC-05	DAC1020	S
DAC-05	DAC1021	S
DAC-05	DAC1022	S
DAC-08	DAC0800	D
DAC-08	DAC0801	D
DAC-08	DAC0802	D
DAC-100	DAC1020	S
DAC-100	DAC1021	S
DAC-100	DAC1022	S
DAC-1408	DAC0806	S
DAC-1408	DAC0807	S
DAC-1408	DAC0808	S
DAC-312	DAC1266	D
DAC-888	DAC0830	S
DAC-888	DAC0831	S
DAC-888	DAC0832	S
MAT02	LM394	S
MAT02AH	LM194H	S
MUX-08E	LF13508	D
MUX-24E	LF13509	D
OP-05	LM607	S
OP-07	LM607	I
OP-07	OP07	D
OP-15	LF411	I
OP-215	LF412	I
OP-77	LM607	I
OP02	LM741	S
OP04	LM747	S
OP06	LM725	S
OP08	LM101	S
OP09	LM4136	S
OP11	LM324	S
OP11	LM348	S
OP14	LM1458	S
OP14	LM1558	S
OP14	LM358	S
OP15	LF351	S
OP15	LM301	S
OP15	LM310	S
OP160	LM6181	I
OP177	LM607	S
OP215	LF353	S
OP22	LM4250	S
OP221	LM2904	S
OP221	LM358	S
OP42	LH0062	S
OP42	LM318	S
OP421	LM2902	S
OP421	LM324	S
OP421	LM3303	S
OP421	L2902	S
OP421	LP324	S
OP43	LM348	S
OP43GP	LF441ACN	S
OP471	LM149	S
OP471	LM837	S
OP490	LMC6044	S
OP77	LM607	S
OP97	LM311	S
PM0820	ADC0820	D
PM1008	LM308	D

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Part Number	NSC Part Number	
PRECISION MONOLITHICS INC. (Continued)		
PM1012	LM312	S
PM111	LM111	D
PM119	LM119	D
PM139	LM139	D
PM139A	LM139A	D
PM148	LM148	D
PM155	LF155	D
PM155A	LF155A	D
PM156	LF156	D
PM156A	LF156A	D
PM157	LF157	D
PM157A	LF157A	D
PM208	LM208	D
PM208A	LM208A	D
PM211	LM211	D
PM219	LM219	D
PM248	LM248	D
PM308	LM308	D
PM308A	LM308A	D
PM319	LM319	D
PM339A	LM339A	D
PM355	LF355	D
PM355A	LF355A	D
PM356	LF356	D
PM356A	LF356A	D
PM357	LF357	D
PM357A	LF357A	D
PM725	LM725	D
PM741	LM741	D
PM747	LM747	D
PM7533	DAC1020	D
PM7533	DAC1021	D
PM7533	DAC1022	D
PM7541	DAC1218	S
PM7541	DAC1219	S
REF-01	LM368	S
REF-01	LM369	S
REF-02	LM368-5.0	S
REF-03	LM336	S
REF-03	LM385-2.5	S
REF-43	LM136	D
SMP10	LF398	S
SMP10	LH0043	S
SMP11	LF398	S
SMP11	LH0023	S
SSM2139	LM833	S
SSM2210	LM394	S
SW-06	LF13333	D
SW-201	LF13201	D
SW-202	LF13202	D
RAYTHEON		
DAC-08	DAC0800	S
DAC-10	DAC-1020	S
DAC-10	DAC-1021	S
DAC-6012	DAC-1220	S
DAC-6012	DAC-1221	S
LH2101A	LH2101A	D
LH2111	LH2111	D
LM101A	LM101A	D
LM111	LM111	D
LM124	LM124	D
LM139	LM139	D
LM148	LM148	D
LM2900	LM2900	D
LM301A	LM301A	D
LM324	LM324	D
LM339	LM339	D
LM348	LM348	D
LM3900	LM3900	D
LP365	LP365	D
RC1458	LM1458	D
RC1558	LM1558	D
RC4156	LM348	S
RC4157	LM348	S
RC4195	LM325	S
RC4195	LM326	S
RC714	LM607	I
RC741	LM741	D
RC747	LM747	D
REF-01	LH0070	S
REF-01	LM368	S
REF-01	LM369	I
REF-02	LM336-5.0	S
REF-02	LM368-5	S
REF-03	LM368-5	I
SAMSUNG		
KA219	LM219	D
KA2803	LM1851	S
KA2807	LM1851	S
KA301	LM301	D
KA319	LM319	D
KA331	LM331	D
KA3524	LM3524D	D
KA431	LM431	D
KA710	LM710	D
KA78S40	LM78S40	D
KF347	LF347	D
KF351	LF351	D
KF442	LF442	D
LM224A	LM224A	D
LM239	LM239	D
LM248	LM248	D
LM258A	LM258A	S
LM2901	LM2901	D
LM2902	LM2902	D
LM2903	LM2903	D
LM2904	LM2904	D
LM293	LM293	D
LM311	LM311	D
LM324	LM324	D
LM324A	LM324A	D
LM3302	LM3302	D
LM339A	LM339A	D
LM348	LM348	D
LM358A	LM358A	D
LM393	LM393	D
LM393A	LM393A	D
LM741	LM741	D
MC1458	LM1458	D
MC78LXX	LM78LXX	D
MC78MXX	LM78MXX	D

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S = NSC Similar Device I = NSC Improved Device D = NSC Direct Replacement

Part Number	NSC Part Number	
SAMSUMG (Continued)		
MC78XX	LM78XX	D
MC79MXX	LM79MXX	D
MC79XX	LM79XX	D
NE555	LM555	D
NE556	LM556	D
SGS THOMPSON		
μA741	LM741	D
μA748	LM748	D
L293	LM18293	D
L4940	LM2940	S
L4941	LM2940	S
L78MXX	LM78MXX	D
L78S05	LM323	I
L78XX	LM340-XX	D
L78XX	LM78XX	D
L7912	LM7912	D
L79XX	LM320-XX	D
L79XX	LM79XX	D
LF198	LF198	D
LF255	LF255	D
LF256	LF256	D
LF257	LF257	D
LF298	LF298	D
LF351	LF351	D
LF353	LF353	D
LF355	LF355	D
LF355A	LF355A	D
LF356	LF356	D
LF356A	LF356A	D
LF357	LF357	D
LF357A	LF357A	D
LF398	LF398	D
LM101A	LM101A	D
LM109	LM109	D
LM117	LM117	D
LM123	LM123	D
LM124	LM124	D
LM124A	LM124A	D
LM134	LM134	D
LM135	LM135	D
LM137	LM137	D
LM139	LM139	D
LM139A	LM139A	D
LM148	LM148	D
LM158	LM158	D
LM158A	LM158A	D
LM1837	LM1837	D
LM193	LM193	D
LM193A	LM193A	D
LM201A	LM201A	D
LM208	LM208	D
LM211	LM211	D
LM218	LM218	D
LM219	LM219	D
LM223	LM223	D
LM224	LM224	D
LM224A	LM224A	D
LM234	LM234	D
LM235	LM235	D
LM236	LM236	D
LM239	LM239	D
LM239A	LM239A	D
LM246	LM246	D
LM248	LM249	D
LM258	LM258	D
LM2901	LM2901	D
LM2902	LM2902	D
LM2903	LM3903	D
LM2904	LM2904	D
LM293	LM293	D
LM2930	LM2930	D
LM2931A	LM2931A	D
LM301A	LM301A	D
LM308	LM308	D
LM308A	LM308A	D
LM311	LM311	D
LM318	LM318	D
LM319	LM319	D
LM323	LM323	D
LM324	LM324	D
LM324A	LM324A	D
LM334	LM334	D
LM335	LM335	D
LM336	LM336	D
LM336B	LM336B	D
LM339	LM339	D
LM339A	LM339A	D
LM346	LM346	D
LM348	LM348	D
LM358	LM358	D
LM358A	LM358A	D
LM393	LM393	D
LM393A	LM393A	D
NE555	LM555	D
NE556	LM556	D
SE555	LM555	D
SG556	LM556	D
SG2524	LM2524	D
SG3524	LM3524	D
SG3525	LM3525	D
SG3527	LM3527	D
TSA2040	LM1875	S
TS272	LMC662	S
TS274	LMC660	S
TS27L2	LPC662	S
TS27L4	LPC660	S
TS27M2	LMC662	S
TS27M4	LMC660	S
SIGNETICS		
μA723	LM723	D
μA741	LM741	D
μA747	LM747	D
ADC0801	ADC0801	D
ADC0802	ADC0802	D
ADC0803	ADC0803	D
ADC0804	ADC0804	D
ADC0805	ADC0805	D
ADC0820	ADC0820	D
CA3089N	LM3089	D

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Part Number	NSC Part Number	
SIGNETICS (Continued)		
DAC-08	DAC0800	D
DAC-08	DAC0801	D
DAC-08	DAC0802	D
ICM7555	LMC555	D
LF198	LF198	D
LF298	LF298	D
LF398	LF398	D
LM2901	LM2901	D
LM2903	LM2903	D
LM311	LM311	D
LM319	LM319	D
LM324	LM324	D
LM339	LM339	D
LM358	LM358	D
LM393	LM393	D
MC1408	DAC0807	D
MC1458	LM1458	D
MC1496	LM1496	D
NE5034	ADC0841	S
NE5118	DAC0830	S
NE529	LM361	S
NE532	LM358	D
NE5410	DAC1020	S
NE5517	LM13600	D
NE5537	LF398	D
NE555	LM555	D
NE565	LM565	D
NE566	LM566	D
NE567	LM567	D
SA532	LM2904	I
SA534	LM2902	I
SE5118	DAC0830	S
SE529	LM161	S
SE532	LM158	S
SE5410	DAC1020	S
SE566	LM566	D
SE567	LM567	D
SG3524	LM3524	D

Part Number	NSC Part Number	
SILICONIX		
DG201	LF13201	D
DG202	LF13202	D
DG211	LF13201	D
DG212	LF13202	D
DG508	LF13508	D
DG509	LF13509	D
TEXAS INSTRUMENTS		
UA2240	LM2240	D
μA709	LM709	D
μA723	LM723	D
μA741	LM741	D
μA747	LM747	D
μA748	LM748	D
μA78LXX	LM78LXX	D
μA78MXX	LM78MXX	D
μA78XX	LM78XX	D
μA79MXX	LM79MXX	D
μA79XX	LM79XX	D
ADC0803	ADC0803	D
ADC0804	ADC0804	D
ADC0805	ADC0805	D
ADC0808	ADC0808	D
ADC0809	ADC0809	D
ADC0820	ADC0820	D
ADC0831	ADC0831	D
ADC0832	ADC0832	D
ADC0834	ADC0834	D
ADC0838	ADC0838	D
LF198	LF198	D
LF347	LF347	D
LF351	LF351	D
LF353	LF353	D
LF398	LF398	D
LF411	LF411	D
LF412	LF412	D
LM101A	LM101A	D
LM107	LM107	D
LM108	LM108	D
LM111	LM111	D
LM124	LM124	D
LM139	LM139	D
LM148	LM148	D

Part Number	NSC Part Number	
LM158	LM158	D
LM185	LM185	D
LM193	LM193	D
LM201	LM201	D
LM207	LM207	D
LM211	LM211	D
LM217	LM217	D
LM218	LM218	D
LM224	LM224	D
LM237	LM137	D
LM239	LM239	D
LM248	LM248	D
LM258	LM258	D
LM2900	LM2900	D
LM2901	LM2901	D
LM2902	LM2902	D
LM2903	LM2903	D
LM2904	LM2904	D
LM2907	LM2907	D
LM2917	LM2917	D
LM293	LM293	D
LM2930	LM2930	D
LM2931	LM2931	D
LM301	LM301	D
LM307	LM307	D
LM317	LM317	D
LM318	LM318	D
LM324	LM324	D
LM330	LM330	D
LM337	LM337	D
LM339	LM339	D
LM348	LM348	D
LM358	LM358	D
LM385	LM385	D
LM3900	LM3900	D
LM393	LM393	D
LP111	LP311	S
LP211	LP311	S
LP239	LP339	S
LP2901	LP339	S

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Part Number	NSC Part Number	
TEXAS INSTRUMENTS (Continued)		
LP311	LP311	D
LP339	LP339	D
LT1004	LM385	D
LT1009	LM336	D
MC1458	LM1458	D
MC155	LM1558	D
MC3303	LM3303	D
MC3403	LM3403	D
MC79LXX	LM79LXX	D
MF10	MF10	D
MF4	MF4	D
NE555	LM555	D
NE555	LM556	D
NE592	LM592	D
OP07	OP07	D
OP27	LM627	I
OP37	LM63	I
RC4136	LM4136	D
RC4558	LM833	D
SA555	LM555	D
SA556	LM556	D
SE2524	LM2524D	I
SE3524	LM3524D	I
SE555	LM555	D
SE556	LM556	D
SE592	LM592	D
TL061	LF441	I
TL062	LF442	I
TL064	LF444	I
TL071	LF351	I
TL071	LF411	I
TL072	LF353	I
TL072A	LF412	I
TL074	LF347	I
TL0808	ADC0808	D
TL0809	ADC0809	D
TL081	TL081	D
TL082	TL082	D
TL084	LF347	I
TL087	LF411	S
TL088	LF411	S
TL287	LF412	S
TL288	LF412	S
TL317	LM317	D
TL431	LM431	D
TL592	LM592	D
TLC04	MF4	D
TLC0820	ADC0820	D
TLC10	MF10	D
TLC1225	ADC1225	D

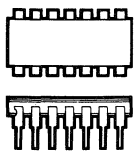
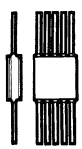
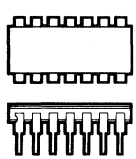
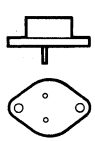
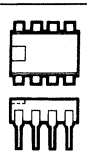
Part Number	NSC Part Number	
TLC14	MF4-100	D
TLC1541	ADC1031	S
TLC20	MF10	D
TLC252	LMC662	S
TLC254	LMC660	S
TLC25L2	LMC662	S
TLC25M2	LMC662	S
TLC25M4	LMC660	S
TLC27L2	LMC6042	I
TLC27L4	LMC6044	I
TLC27L7	LMC6062A	I
TLC27M2	LMC662	S
TLC27M4	LMC660	S
TLC271	LMC6041	I
TLC272	LMC6032	I
TLC274	LMC6034	I
TLC277	LMC6082A	I
TLC339	LP339	S
TLC532	ADC0829	S
TLC533	ADC0829	D
TLC540	ADC0811	S
TLC541	ADC0811	D
TLC545	ADC0819	S
TLC546	ADC0819	D
TLC549	ADC0831	S
TLC555	LMC555	D
TOSHIBA		
TA7133	LM1391	S
TA7140	LM386	S
TA7230	LM1877	S
TA7232	LM2896	S
TA7233	LM2877	S
TA7268	LM1875	S
TA7269	LM2878	S
TA7282	LM2896	S
TA7283	LM2896	S
TA7313	LM386	S
TA7336	LM390	S
TA7366	LM3914	S
TA7367	LM3914	S
TA7370	LM3361	S
TA7504	LM741	D
TA75061	LF441	I
TA75062	LF442	I
TA75064	LF444	I
TA75071	LF351	I
TA75072	LF353	I

Part Number	NSC Part Number	
TA75074	LF347	I
TA75092	LM2902	I
TA75092	LM324	S
TA75339	LM2901	D
TA75339	LM339	D
TA75358	LM2904	I
TA75358	LM358	D
TA75393	LM2903	I
TA75393	LM393	D
TA75458	LM1558	D
TA7555	LM555	D
TA7612	LM3914	S
TA7613	LM1868	S
TA7630	LM1036	S
TA7640	LM1868	S
TA76524	LM3624	S
TA7654	LM3914	S
TA7667	LM3915	S
TA7688	LM1896	S
TA7758	LM1868	S
TA7769	LM1896	S
TA78LXX	LM78LXX	D
TA78MXX	LM78MXX	D
TA78XXX	LM78XX	D
TA79LXXX	LM79LXX	D
TA79XXX	LM79XX	D
TA8117	LM1868	S
TA8119	LM1896	S
TA8202	LM1877	S
TA8211	LM2878	S
TC9154	LMC1982	S
UNITRODE		
L293	LM18293	D
UC117	LM117	D
UC137	LM137	D
UC150	LM150	D
UC1524	LM1524D	I
UC2524	LM2524D	I
UC317	LM317	D
UC337	LM337	D
UC350	LM350	D
UC3524	LM3524D	I
UC78XX	LM340-XX	D
UC78XX	LM78XX	D
UC79XX	LM320-XX	D
UC79XX	LM79XX	D

The following notations are appended to assist you in finding the best option.

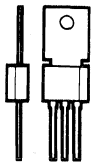
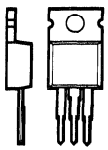
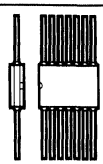
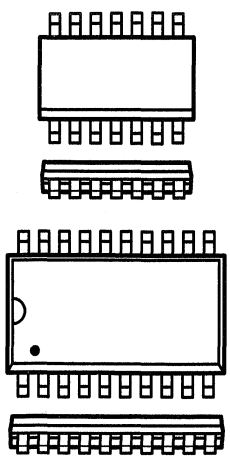
S = NSC Similar Device I = NSC Improved Device D = NSC Direct Replacement

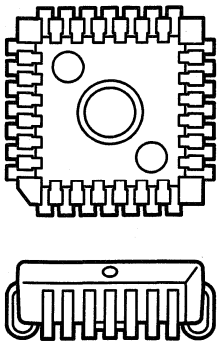
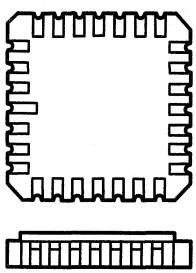
Industry Package Cross-Reference Guide

	NSC	NSC μA	Signetics	Motorola	TI	AMD	Spraque
 4/16 Lead Glass/Metal DIP	D	D	I	L		D	R
 Glass/Metal Flat Pack	F	F	Q	F	F, S	F	
 TO-99, TO-100, TO-5	H	H	T, K, L, DB	G	L	H	
 8-, 14- and 16-Lead Low Temperature Ceramic DIP	J	R, D	F	U	J	D	H
 TO-3 (Steel)	K			KS			
TO-3 (Aluminum)	KC	K	DA	K	K		
 8-, 14- and 16-Lead Plastic DIP	N	T, P	N, V	P	P, N	P	A, B, M

*With dual-in-line formed leads

**With radically formed leads

		NSC	NSC μA	Signetics	Motorola	TI	AMD	Sprague
	TO-202 (D-40, Durawatt)	P						
	TO-220 3- & 5-Lead	T	U	U		KC		
	TO-220 11-, 15- & 23-Lead	T						
	Low Temperature Glass Hermetic Flat Pack	W	F		F	W	F	
	TO-92 (Plastic)	Z	W	S	P	LP		
	SO (Narrow Body)	M	S	S, D	D	D		L
	(Wide Body)	WM				DW		LW

	NSC	NSC μA	Signetics	Motorola	TI	AMD	Spraque
 PCC	V	Q	A	FN	FN	L	EP
 LCC Leadless Ceramic Chip Carrier	E	L1	G	U	FK/ FG/FH	L	EK

Section 1

Operational Amplifiers

Section 1 Contents

Section 1 Contents (Continued)

Section 1 Contents (Continued)

National Semiconductor

Operational Amplifiers Definition of Terms

Bandwidth: That frequency at which the voltage gain is reduced to $1/\sqrt{2}$ times the low frequency value.

Common-Mode Rejection Ratio: The ratio of the input common-mode voltage range to the peak-to-peak change in input offset voltage over this range.

Harmonic Distortion: That percentage of harmonic distortion being defined as one-hundred times the ratio of the root-mean-square (rms) sum of the harmonics to the fundamental. % harmonic distortion =

$$\frac{(V2^2 + V3^2 + V4^2 + \ldots)^{1/2}\,(100\%)}{V1}$$

where V1 is the rms amplitude of the fundamental and V2, V3, V4, . . . are the rms amplitudes of the individual harmonics.

Input Bias Current: The average of the two input currents.

Input Common-Mode Voltage Range (or Input Voltage Range): The range of voltages on the input terminals for which the amplifier is operational. Note that the specifications are not guaranteed over the full common-mode voltage range unless specifically stated.

Input Impedance: The ratio of input voltage to input current under the stated conditions for source resistance (R_S) and load resistance (R_L).

Input Offset Current: The difference in the currents into the two input terminals when the output is at zero.

Input Offset Voltage: That voltage which must be applied between the input terminals through two equal resistances to obtain zero output voltage.

Input Resistance: The ratio of the change in input voltage to the change in input current on either input with the other grounded.

Large-Signal Voltage Gain: The ratio of the output voltage swing to the change in input voltage required to drive the output from zero to this voltage.

Output Impedance: The ratio of output voltage to output current under the stated conditions for source resistance (R_S) and load resistance (R_L).

Output Resistance: The small signal resistance seen at the output with the output voltage near zero.

Output Voltage Swing: The peak output voltage swing, referred to zero, that can be obtained without clipping.

Offset Voltage Temperature Drift: The average drift rate of offset voltage for a thermal variation from room temperature to the indicated temperature extreme.

Power Supply Rejection: The ratio of the change in input offset voltage to the change in power supply voltages producing it.

Settling Time: The time between the initiation of the input step function and the time when the output voltage has settled to within a specified error band of the final output voltage.

Slew Rate: The internally-limited rate of change in output voltage with a large-amplitude step function applied to the input.

Supply Current: The current required from the power supply to operate the amplifier with no load and the output midway between the supplies.

Transient Response: The closed-loop step-function response of the amplifier under small-signal conditions.

Unity Gain Bandwidth: The frequency range from dc to the frequency where the amplifier open loop gain rolls off to one.

Voltage Gain: The ratio of output voltage to input voltage under the stated conditions for source resistance (R_S) and load resistance (R_L).

National Semiconductor

General Purpose Operational Amplifier Selection Guide

Military Temperature Range (−55°C to +125°C) Specs at T_A = 25°C (Note 1)

Part #	V_{OS} mV (Max)	I_B nA (Max)	GBW MHz (Typ)	Slew Rate V/μs (Typ)	Supply Current (Note 3) mA (Max)	Supply Voltage		Special Features
						Min V	Max V	
LM607A	0.025	2	1.8	0.7	1.5	±3	±18	Improved OP-07
LH0044	0.05	30	0.4	0.06	4	±2	±20	Low Noise
LM607B	0.06	3	1.8	0.7	1.5	±3	±18	Improved OP-07
LM11	0.3	0.05	0.8	0.3	0.6	±2.5	±20	
LF411A	0.5	0.2	4	15	2.8	±6	±22	
LF441A	0.5	0.05	1	1	0.2	±6	±22	
LH2108A	0.5	2	1	0.3	1.2	±2	±20	Dual LM108A
LM108A	0.5	2	1	0.3	0.6	±2	±20	
LH0052	0.5	0.003	1	3	3.5	±5	±22	
LF412A	1	0.2	4	15	5.6	±6	±22	Dual
LF442A	1	0.05	1	1	0.4	±6	±22	Dual
LH0004	1	100	10	*	0.15	±5	±45	
LM604A	1	50	7	2	9	4	36	Multiplexed Op Amp
LH2101A	2	75	1	0.5	5	±3	±22	Dual LM101A
LF155A	2	0.05	2.5	5	4	±5	±22	
LF156A	2	0.05	5	12	7	±5	±22	
LF157A	2	0.05	20	50	7	±5	±22	Minimum Gain of 5
LF411	2	0.2	4	15	3.4	±6	±18	
LM10	2	20	0.09	0.1	0.4	±0.6	±22.5	Op Amp + Reference
LM101A	2	75	1	0.5	3	±3	±22	
LM107	2	100	1	0.5	3	±3	±22	Compensated LM101A
LM108	2	2	1	0.3	0.6	±2	±20	
LM112	2	2	1	0.2	0.4	±2	±20	Compensated LM108
LM124A	2	50	1	0.5	3	3	32	Quad
LM158A	2	50	1	0.5	2	3	32	Dual
LP124	2	4	0.1	0.05	0.13	3	32	Quad
LH0020	2.5	250	*	*	5	±5	±22	
LF412	3	0.2	4	15	6.5	±6	±18	Dual
LM741A	3	80	1.5	0.7	2.8	±3	±22	

General Purpose Operational Amplifier Selection Guide (Continued)

Military Temperature Range (−55°C to +125°C) Specs at T_A = 25°C (continued)

Part #	V_{OS} mV (Max)	I_B nA (Max)	GBW MHz (Typ)	Slew Rate V/μs (Typ)	Supply Current (Note 3) mA (Max)	Supply Voltage		Special Features
						Min V	Max V	
LH0022	4	0.01	1	3	2.5	±5	±22	
LF155	5	0.1	2.5	5	4	±5	±22	
LF156	5	0.1	5	12	7	±5	±22	
LF157	5	0.1	20	50	7	±5	±22	Minimum Gain of 5
LF147	5	0.2	4	13	11	±6	±22	Quad
LF442	5	0.1	1	1	0.5	±6	±18	Dual
LF444A	5	50	1	1	0.80	±6	±22	Quad
LM124	5	150	1	0.5	3	3	32	Quad
LM143	5	20	1	2.5	4	±4	±40	
LM144	5	20	1	2.5	4	±4	±40	Minimum Gain of 10
LM146	5	100	1.2	0.4	2.2	±1.5	±22	(Note 5)
LM148	5	100	1	0.5	3.6	±5	±22	Quad
LM149	5	100	4	2	3.6	±5	±22	Minimum Gain of 5, Quad
LM158	5	150	1	0.5	2	3	32	Dual
LM741	5	500	1	0.5	2.8	±3	±22	
LM1558	5	500	*	*	5	±3	±22	Dual
LM4250	5	50	0.2	0.2	0.1	±1	±18	(Note 5)
LH0042	20	0.025	1	3	3.5	±5	±22	

Automotive Temperature Range (−40°C to +85°C) Specs at T_A = 25°C (Note 1)

Part #	V_{OS} mV (Max)	I_B nA (Max)	GBW MHz (Typ)	Slew Rate V/μs (Typ)	Supply Current (Note 3) mA (Max)	Supply Voltage		Special Features
						Min V	Max V	
LM604	3	80	7	3	9	4	36	Multiplexed Op Amp
LP2902	4	20	0.1	0.05	0.15	3	26	Quad
LM2902	7	250	1	0.5	3	3	26	Quad
LM2904	7	250	1	0.5	2	3	26	Dual
LM2924	7	250	1	0.5	2	3	26	Comparator + Op Amp

General Purpose Operational Amplifier Selection Guide (Continued)

Industrial Temperature Range (−25°C to +85°C) Specs at T_A = 25°C (Note 1)

Part #	V_{OS} mV (Max)	I_B nA (Max)	GBW MHz (Typ)	Slew Rate V/μs (Typ)	Supply Current (Note 3) mA (Max)	Supply Voltage		Special Features
						Min V	Max V	
LM637A	0.025	10	65	14	4.5	±3.5	±18	Improved OP-37
LM627A	0.025	10	14	4.5	4.5	±3.5	±18	Improved OP-27
LH0044B	0.05	30	0.4	0.06	4	±2	±20	
LH0044C	0.1	30	0.4	0.06	4	±2	±20	
LM637	0.1	25	65	14	4.8	±3.5	±18	Improved OP-37
LM627	0.1	25	14	4.5	4.8			Improved OP-27
LM208A	0.5	2	1	0.3	0.6	±2	±20	
LM10B(L)	2	20	0.09	0.1	0.4	(Note 4)		Op Amp + Reference
LM201A	2	75	1	0.5	2.5	±3	±22	
LM207	2	75	1	0.5	2.5	±3	±22	Compensated LM201A
LM208	2	2	1	0.3	0.6	±2	±20	
LM212	2	2	1	0.3	0.4	±2	±20	Compensated LM208
LM224A	3	80	1	0.5	3	3	32	Quad
LM258A	3	80	1	0.5	2	3	32	Dual
LF255	5	0.1	2.5	5	4	±5	±22	
LF256	5	0.1	5	12	7	±5	±22	
LF257	5	0.1	20	50	7	±5	±22	Minimum Gain of 5
LM224	5	150	1	0.5	3	3	32	Quad
LM258	5	150	1	0.5	2	3	32	Dual
LH0020C	6	500	*	*	6	±5	±22	
LM246	6	250	1.2	0.4	2.5	±2	±18	(Note 5)
LM248	6	200	1	0.5	4.5	±5	±18	Quad
LM249	6	200	4	2	4.5	±5	±18	Minimum Gain of 5, Quad
LH0042C	20	0.05	1	3	4	±5	±22	

General Purpose Operational Amplifier Selection Guide (Continued)

Commercial Temperature Range (0°C to +70°C) Specs at T_A = 25°C (Notes 1 and 2)

Part #	V_{OS} mV (Max)	I_B nA (Max)	GBW MHz (Typ)	Slew Rate V/μs (Typ)	Supply Current (Note 3) mA (Max)	Supply Voltage		Special Features
						Min V	Max V	
LM607A	0.025	2	1.8	0.7	1.5	±3	±18	Improved OP-07
LM607B	0.06	3	1.8	0.7	1.5	±3	±18	Improved OP-07
LM607	0.15	10	1.8	0.7	1.8	±3	±18	Improved OP-07
LF411A	0.5	0.2	4	15	2.8	±6	±22	
LF441A	0.5	0.05	1	1	0.2	±6	±22	
LM308A	0.5	7	1	0.3	0.8	±2	±20	
LM11C	0.6	0.1	0.8	0.3	0.8	±2.5	±20	
LF412A	1	0.2	4	15	5.6	±6	±22	Dual
LF442A	1	0.05	1	1	0.4	±6	±22	Dual
LM604A	1	50	7	3	9	4	36	Multiplexed Op Amp
LF355A	2	0.05	2.5	5	4	±5	±22	
LF356A	2	0.05	5	12	10	±5	±22	
LF357A	2	0.05	20	50	10	±5	±22	Minimum Gain of 5
LF411	2	0.2	4	15	3.4	±6	±22	
LF412	3	0.2	4	15	6.5	±6	±22	Dual
LM324A	3	100	1	0.5	3	3	32	Quad
LM358A	3	100	1	0.5	2	3	32	Dual
LM604	3	80	7	7	9	4	36	Multiplexed Op Amp
LM741E	3	80	1.5	0.7	2.8	±3	±22	
LM10C(L)	4	30	0.09	0.1	0.5	(Note 4)		Op Amp + Reference
LP324	4	10	0.1	0.05	0.15	3	32	
LF347B	5	0.2	4	13	11	±6	±22	Quad
LF355B	5	0.1	2.5	5	4	±5	±22	
LF356B	5	0.1	5	12	4	±5	±22	
LF357B	5	0.1	20	50	7	±5	±22	
LF441	5	0.1	1	1	0.25	±6	±22	
LF442	5	0.1	1	1	0.5	±6	±22	Dual
LM11CL	5	0.2	0.8	0.3	0.8	±2.5	±20	
LF451	5	0.2	4	13	3.4	10	32	SO Pkg
LF453	5	0.2	4	13	6.5	10	32	SO Pkg Dual
LM611	5	35	0.8	0.7	0.35	4	36	Op Amp + Ref
LM613	5	35	0.8	0.7	1	4	36	2 Op Amps + 2 Comparators + Ref

General Purpose Operational Amplifier Selection Guide (Continued)

Commercial Temperature Range (0°C to +70°C) (Notes 1 and 2) (Continued)

Part #	V_{OS} mV (Max)	I_B nA (Max)	GBW MHz (Typ)	Slew Rate V/μs (Typ)	Supply Current (Note 3) mA (Max)	Supply Voltage		Special Features
						Min V	Max V	
LM614	5	35	0.8	0.7	1	4	36	Quad Op Amp + Ref
LM392	5	250	1	0.5	2	3	32	
LM833	5	1000	15	7	8	±5	±18	Dual Low Noise
LM346	6	250	1.2	0.4	2.5	±1.5	±22	(Note 5)
LM348	6	200	1	0.5	4.5	±5	±18	
LM349	6	200	4	2	4.5	±5	±18	
LM741C	6	500	1.5	0.5	2.8	±3	±18	
LM1458	6	500	*	*	5.6	±3	±18	
LM4250C	6	75	0.2	0.2	0.1	±1	±18	(Note 5)
LM324	7	250	1	0.5	3	3	32	
LM358	7	250	1	0.5	2	3	32	
LM301A	7.5	250	1	0.5	3	±3	±18	
LM307	7.5	250	1	0.5	3	±3	±18	Compensated LM301A
LM308	7.5	7	1	0.3	0.8	±2	±18	
LM312	7.5	7	1	0.2	0.8	±2	±18	Compensated LM308
LM343	8	40	1	2.5	5	±4	±34	
LM344	8	40	1	2.5	5	±4	±34	Minimum Gain of 10
LF347	10	0.2	4	13	11	±6	±18	Quad
LF351	10	0.2	4	13	3.4	±6	±18	
LF353	10	0.2	4	13	6.8	±6	±18	Dual
LF355	10	0.2	2.5	5	4	±5	±18	
LF356	10	0.2	5	12	10	±5	±18	
LF357	10	0.2	20	50	10	±5	±18	Minimum Gain of 5
LF444	10	0.1	1	1	1	±6	±18	Quad
TL081C	15	0.2	4	13	2.8	±6	±18	
TL082C	15	0.2	4	13	5.6	±6	±18	Dual

*Not Specified.

Note 1: Datasheet should be referred to for test conditions and more detailed information.

Note 2: Those looking for a commercial part should also look at the Industrial Temp Range guide as many Hybrids are listed there.

Note 3: Supply current is for all amplifiers in a package.

Note 4: The LM10 has 2 versions: one a high voltage part, good to 45V and a low voltage part, good to 7V. Refer to the datasheet for more information.

Note 5: The LM146 and LM4250 are programmable amplifiers. The data shown is for $V_S = \pm 15V$ and $I_{SET} = 10\ \mu A$. Refer to the datasheets for more information.

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Low I_{BIAS} Selection Guide

<5 pA*	≤20 pA	≤50 pA	≤100 pA	≤200 pA	≤500 pA
T_A = 25°C					
LMC660*	LH0042	LH0032A	LH0032	TL081	LH0032C
LMC662*	LH0042C	LF155A/156A/	LF155/156/	LH0032AC	LH4004
LMC6041*		LF157A	LF157	LF351	
LMC6042*		LF355A/356A/	LF255/256/	LF411A/411	
LMC6044*		LF357A	LF257	LF355/356/	
LMC6062*		LF441A	LF355B/356B/	LF357	
LMC6082*		LF442A	LF357B	LF147/347B/347	
LPC660*		LF444A	LF441	LF353	
LPC661*		LM11	LF442	LF412A/412	
LPC662*			LF444	LM11CL	
LMC6061*			LM11C	LMC6022*	
LMC6081*			LH0101	LMC6024*	
LMC6064*				LMC6032*	
LMC6084*				LMC6034*	
LMC6482*				LH4104	
LMC6484*				LH4104C	

Note: Datasheet should be referred to for conditions and more detailed information.

*Guaranteed over industrial temperature range (−40°C to +85°C). Typical value is ≤ 40 fA.

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High Speed Operational Amplifier Selection Guide

Part #	Slew Rate V/μs (Typ)	GBW MHz (Typ)	V_{OS} mV (Max)	I_S mA (Max) (Note 1)	Notes
GBW ≥ 4 MHz, T_A = 25°C					
LH4118A	2400	250	2	±25	Low V_{OS}, Current Feedback
LM6181	2000	100	7.0	10	Current Feedback, VIP
LH0024	500	70	4	±15	
LH0032	500	70	5	±20	FET Input
LM6161	300	50	7	6.8	Unity Gain Stable, VIP™
LM6162	300	100	5	6.8	Min Gain of 2, VIP
LM6164	300	175	4	6.8	Min Gain of 5, VIP
LM6165	300	725	3	6.8	Min Gain of 25, VIP
LM6313	250	35	20	23	Hi Speed Hi Power
LM6218A	140	17	1	7	Fast Settling Dual, VIP
LM6218	140	17	3	7	Fast Settling Dual, VIP
LH0003	70	30	3	±3	
LM118	70	15	4	7	
LF157A	50	20	2	7	Min Gain of 5, JFET
LH4104	40	18	10	±25	Medium Power Fast Settling JFET
LM359	30	30	*	22	Dual Current Mode (Norton) Amp
LF411A	15	4	0.5	2.8	JFET
LF412A	15	4	1.0	5.6	Dual JFET
LF147	13	4	5	11	Quad JFET
LF451	13	4	5	3.4	SO Pkg
LF453	13	4	5	6.5	SO Pkg Dual
LF351	13	4	10	3.4	JFET
LF353	13	4	10	6.5	Dual JFET
LF156A	12	5	2	7	JFET
LM833	7	15	5	8	Dual Low Noise

*Not specified.

Note 1: Supply current is for all amplifiers in a package.

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Precision Operational Amplifier Selection Guide

Part #	V_{OS} mV (Max)	I_B nA (Max)	GBW MHz (typ)	Slew Rate V/μs (Typ)	Supply Current (Note 1) mA (Max)	Notes
Singles						
LM637A	0.025	10	65	14	4.5	Improved OP-37
LM627A	0.025	10	14	4.5	4.5	Improved OP-27
LM607A	0.025	2	1.8	0.7	1.5	Improved OP-07
LM637	0.1	25	65	14	4.8	Improved OP-37
LM627	0.1	25	14	4.5	4.8	Improved OP-27
LM607	0.15	10	1.8	0.7	1.8	Improved OP-07
LM11	0.3	0.05	0.8	0.3	0.6	
LMC6081A	0.35	0.00001*	1.3	1.5	0.750	Low power
LMC6061A	0.35	0.00001*	0.1	0.035	0.024	Micropower
LM308A	0.5	7	1	0.3	0.8	
LM208A	0.5	2	1	0.3	0.6	
LM108A	0.5	2	1	0.3	0.6	
LF441A	0.5	0.05	1	1	0.2	
LF411A	0.5	0.2	4	15	2.8	
LM11C	0.6	0.1	0.8	0.3	0.8	
LMC6081	0.8	0.00001*	1.3	1.5	0.750	Low power
LMC6061	0.8	0.00001*	0.1	0.035	0.032	Micropower
Duals						
LMC6082A	0.35	0.00001*	1.3	1.5	1.5	Dual LMC6081A
LMC6062A	0.35	0.00001*	0.1	0.035	0.038	Dual LMC6061A
LMC6482A	0.5	0.00002*	1.3	1	1*	Rail to Rail Input/Output
LMC6082	0.8	0.00001*	1.3	1.5	1.5	Dual LMC6081
LMC6062	0.8	0.00001*	0.1	0.035	0.046	Dual LMC6061
Quads						
LMC6084A	0.35	0.00001*	1.3	1.5	3.0	Quad LMC6081A
LMC6064A	0.35	0.00001*	0.1	0.035	0.076	Quad LMC6061A
LMC6484A	0.5	0.00002*	1.3	1	2*	Rail to Rail Input/Output
LMC6084	0.8	0.00001*	1.3	1.5	3.0	Quad LMC6081
LMC6064	0.8	0.00001*	0.1	0.35	0.114	Quad LMC6061

*Typical Value

Note 1: Supply current is for all amplifiers in a package.

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Low Power Operational Amplifier Selection Guide

Part #	I_S μA Typ	V_{OS} mV Max	I_B fA Typ	CMVR V Typ	Output Swing V Typ with RL = 100 kΩ	GBW MHz Typ	Supply Voltage Min V	Supply Voltage Max V
Specs at T_A = 25°C and Vs = +5V								
Singles								
LMC6041A	14	3	2	−0.4 to 3.1	0.004 to 4.987	0.075	5	15
LMC6041	14	6	2	−0.4 to 3.1	0.004 to 4.987	0.075	5	15
LMC6061A	20	0.35	10	−0.4 to 3.1	0.005 to 4.995	0.1	5	15
LMC6061	20	0.8	10	−0.4 to 3.1	0.005 to 4.995	0.1	5	15
LPC661A	55	3	2	−0.4 to 3.1	0.004 to 4.987	0.35	5	15
LPC661	55	6	2	−0.4 to 3.1	0.004 to 4.987	0.35	5	15
LMC6081A	450	0.35	10	−0.4 to 3.1	0.02 to 4.98	1.3	5	15
LMC6081	450	0.8	10	−0.4 to 3.1	0.02 to 4.98	1.3	5	15
Duals								
LMC6042A	20	3	2	−0.4 to 3.1	0.004 to 4.987	0.1	5	15
LMC6042	20	6	2	−0.4 to 3.1	0.004 to 4.987	0.1	5	15
LMC6062A	32	0.35	10	−0.4 to 3.1	0.005 to 4.995	0.1	5	15
LMC6062	32	0.8	10	−0.4 to 3.1	0.005 to 4.995	0.1	5	15
LPC662A	86	3	2	−0.4 to 3.1	0.004 to 4.987	0.35	5	15
LPC662	86	6	2	−0.4 to 3.1	0.004 to 4.987	0.35	5	15
LMC6022	86	9	40	−0.4 to 3.1	0.004 to 4.987	0.35	5	15
LMC662A	750	3	2	−0.4 to 3.1	0.02 to 4.98	1.4	5	15
LMC662	750	6	2	−0.4 to 3.1	0.02 to 4.98	1.4	5	15
LMC6032	750	9	40	−0.4 to 3.1	0.02 to 4.98	1.4	5	15
LMC6082A	900	0.35	10	−0.4 to 3.1	0.02 to 4.98	1.3	5	15
LMC6082	900	0.8	10	−0.4 to 3.1	0.02 to 4.98	1.3	5	15
LMC6482A	1000	0.5	20	0 to 5	0.03 to 4.97	1.3	3	15
LMC6482	1000	3	20	0 to 5	0.03 to 4.97	1.3	3	15
Quads								
LMC6044A	40	3	2	−0.4 to 3.1	0.004 to 4.987	0.1	5	15
LMC6044	40	6	2	−0.4 to 3.1	0.004 to 4.987	0.1	5	15
LMC6064A	64	0.35	10	−0.4 to 3.1	0.005 to 4.995	0.1	5	15
LMC6064	64	0.8	10	−0.4 to 3.1	0.005 to 4.995	0.1	5	15
LPC660A	160	3	2	−0.4 to 3.1	0.004 to 4.987	0.35	5	15
LPC660	160	6	2	−0.4 to 3.1	0.004 to 4.987	0.35	5	15

Low Power Operational Amplifier Selection Guide (Continued)

Part #	I_S μA Typ	V_{OS} mV Max	I_B fA Typ	CMVR V Typ	Output Swing V Typ with RL = 100 kΩ	GBW MHz Typ	Supply Voltage Min V	Supply Voltage Max V
Specs at T_A = 25°C and Vs = +5V								
Quads (Continued)								
LMC6024	160	9	40	−0.4 to 3.1	0.004 to 4.987	0.35	5	15
LMC660A	1500	3	2	−0.4 to 3.1	0.02 to 4.98	1.4	5	15
LMC660	1500	6	2	−0.4 to 3.1	0.02 to 4.98	1.4	5	15
LMC6034	1500	9	40	−0.4 to 3.1	0.02 to 4.98	1.4	5	15
LMC6084A	1800	0.35	10	−0.4 to 3.1	0.02 to 4.98	1.3	5	15
LMC6084	1800	0.8	10	−0.4 to 3.1	0.02 to 4.98	1.3	5	15
LMC6484A	2000	0.5	20	0 to 5	0.03 to 4.97	1.3	3	15
LMC6484	2000	3	20	0 to 5	0.03 to 4.97	1.3	3	15

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Medium and High Power Operational Amplifier Selection Guide ($\geq$ 0.1A Output) (T_A = 25°C, Note 1)

Part #	I_{OUT} A (Typ)	V_{OS} mV (Max)	I_S mA (Max)	Slew Rate V/μS (Typ)	PBW (Typ)
LH4104	0.1	5	25	40	600 kHz
LH4118	0.1	2	25	2400	68 MHz
LM6181	0.1	7.0	10	2000	60 MHz
LH0041	0.2	3	3.5	3	20 kHz
LH0021	1.2	3	3.5	3	20 kHz
LH0101A	2.2	3	35	10	300 kHz
LH0101	2.2	10	35	10	300 kHz
LM675	3	10	50	8	*
LM12(L)	(Note 2)	7	80	9	60 kHz
LM12C(L)	(Note 2)	15	120	9	60 kHz

*Not Specified

Note 1: Refer to Datasheet for conditions and more detailed information.

Note 2: I_{OUT} for the LM12 is dependent on the amount of power dissipated in the output transistor. The datasheet should be referred to, to determine amount of current available.

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Special Amplifier Selection Guide

Amplifiers with Added Functions

Featuring the new Super-Block™ family, these amplifiers have additional special functions within their packages which help minimize the number of components required in an application. These devices are often used in control circuits, power supplies, and automatic test systems.

LH0045	Two-Wire Transmitter
LM10	Op Amp and Adjustable Voltage Reference
LM392	Op Amp and Comparator
LM604	Super-Block Multiplexed Op Amp (4 Inputs, 1 Output)
LM611	Super-Block Op Amp and Adjustable Voltage Reference
LM612	Super-Block Dual Comparator and Voltage Reference
LM613	Super-Block Dual Op Amp, Dual Comparator, and Adjustable Voltage Reference
LM614	Super-Block Quad Op Amp and Adjustable Voltage Reference
LM615	Super-Block Quad Comparator and Adjustable Voltage Reference

Transconductance Amplifiers (Voltage In, Current Out)

These amplifiers provide a transconductance (g_m) proportional to their bias current, which is controlled externally. This programmable gain makes the amplifiers useful in applications such as voltage-controlled amplifiers, current-controlled amplifiers, AGC circuits, and voltage multipliers.

LM3080	Operational Transconductance Amplifier
LM13600	Dual Operational Transconductance Amplifier with Linearizing Diodes and Buffers
LM13700	Improved Dual Operational Transconductance Amplifier with Linearizing Diodes and Buffers

Transimpedance Amplifiers (Current In, Voltage Out)

Transimpedance amplifiers are widely used to amplify photo-diode signals, and to ground-reference differential voltage signals which have high common-mode voltages. The LH0082 was designed to receive and amplify analog and digital signals transmitted by fiber optics. Like the LM359, the LH0082 can also be used as a video amplifier. The LM2900 series has found popularity in filter applications, as well as general-purpose amplifiers.

LH0082	20 MHz Transimpedance Amplifier/Comparator
LM359	Dual Current Mode (Norton) Amplifier
LM2900 LM3900 LM3301 LM3401	Quad Current Mode (Norton) Amplifier

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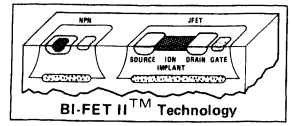


LF147/LF347 Wide Bandwidth Quad JFET Input Operational Amplifiers

General Description

The LF147 is a low cost, high speed quad JFET input operational amplifier with an internally trimmed input offset voltage (BI-FET II™ technology). The device requires a low supply current and yet maintains a large gain bandwidth product and a fast slew rate. In addition, well matched high voltage JFET input devices provide very low input bias and offset currents. The LF147 is pin compatible with the standard LM148. This feature allows designers to immediately upgrade the overall performance of existing LF148 and LM124 designs.

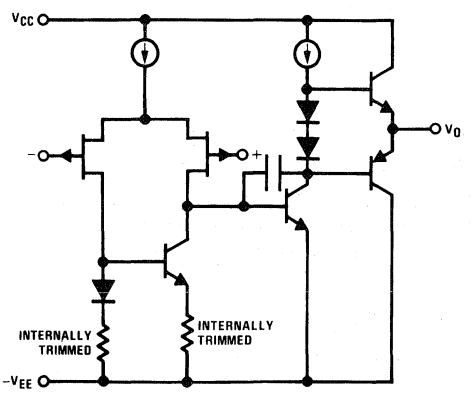
The LF147 may be used in applications such as high speed integrators, fast D/A converters, sample-and-hold circuits and many other circuits requiring low input offset voltage, low input bias current, high input impedance, high slew rate and wide bandwidth. The device has low noise and offset voltage drift.

Features

■ Internally trimmed offset voltage	5 mV max
■ Low input bias current	50 pA
■ Low input noise current	0.01 pA/$\sqrt{\text{Hz}}$
■ Wide gain bandwidth	4 MHz
■ High slew rate	13 V/μs
■ Low supply current	7.2 mA
■ High input impedance	$10^{12}\Omega$
■ Low total harmonic distortion $A_V = 10$, $R_L = 10k$, $V_O = 20$ Vp-p, BW = 20 Hz – 20 kHz	<0.02%
■ Low 1/f noise corner	50 Hz
■ Fast settling time to 0.01%	2 μs

Simplified Schematic

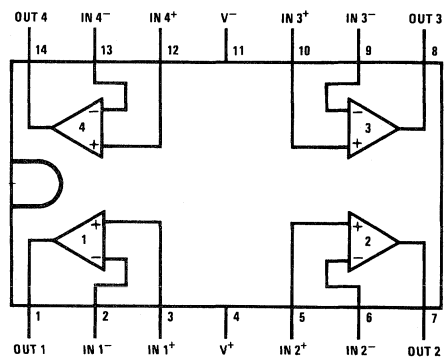
¼ Quad



TL/H/5647–13

Connection Diagram

Dual-In-Line Package



TL/H/5647–1

Top View

Order Number LF147J, LF347J, LF347M, LF347BN, LF347N, LF147D/883 or LF147J/883*
See NS Package Number D14E, J14A, M14A or N14A

*Available per SMD #8102306, JM38510/11906.

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

	LF147	LF347B/LF347
Supply Voltage	±22V	±18V
Differential Input Voltage	±38V	±30V
Input Voltage Range (Note 1)	±19V	±15V
Output Short Circuit Duration (Note 2)	Continuous	Continuous
Power Dissipation (Notes 3 and 9)	900 mW	1000 mW
T_j max	150°C	150°C
θ_{jA}		
Cavity DIP (D) Package		80°C/W
Ceramic DIP (J) Package		70°C/W
Plastic DIP (N) Package		75°C/W
Surface Mount Narrow (M)		100°C/W
Surface Mount Wide (WM)		85°C/W

	LF147	LF347B/LF347
Operating Temperature Range	(Note 4)	(Note 4)
Storage Temperature Range	$-65°C \le T_A \le 150°C$	
Lead Temperature (Soldering, 10 sec.)	260°C	260°C
Soldering Information		
Dual-In-Line Package		
Soldering (10 seconds)		260°C
Small Outline Package		
Vapor Phase (60 seconds)		215°C
Infrared (15 seconds)		220°C

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

ESD Tolerance (Note 10) 900V

DC Electrical Characteristics (Note 5)

Symbol	Parameter	Conditions	LF147			LF347B			LF347			Units
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_{OS}	Input Offset Voltage	$R_S = 10\ k\Omega$, $T_A = 25°C$ Over Temperature		1	5 8		3	5 7		5	10 13	mV mV
$\Delta V_{OS}/\Delta T$	Average TC of Input Offset Voltage	$R_S = 10\ k\Omega$		10			10			10		μV/°C
I_{OS}	Input Offset Current	$T_j = 25°C$, (Notes 5, 6) Over Temperature		25	100 25		25	100 4		25	100 4	pA nA
I_B	Input Bias Current	$T_j = 25°C$, (Notes 5, 6) Over Temperature		50	200 50		50	200 8		50	200 8	pA nA
R_{IN}	Input Resistance	$T_j = 25°C$		10^{12}			10^{12}			10^{12}		Ω
A_{VOL}	Large Signal Voltage Gain	$V_S = \pm 15V$, $T_A = 25°C$ $V_O = \pm 10V$, $R_L = 2\ k\Omega$ Over Temperature	50 25	100		50 25	100		25 15	100		V/mV V/mV
V_O	Output Voltage Swing	$V_S = \pm 15V$, $R_L = 10\ k\Omega$	±12	±13.5		±12	±13.5		±12	±13.5		V
V_{CM}	Input Common-Mode Voltage Range	$V_S = \pm 15V$	±11	+15 −12		±11	+15 −12		±11	+15 −12		V V
CMRR	Common-Mode Rejection Ratio	$R_S \le 10\ k\Omega$	80	100		80	100		70	100		dB
PSRR	Supply Voltage Rejection Ratio	(Note 7)	80	100		80	100		70	100		dB
I_S	Supply Current			7.2	11		7.2	11		7.2	11	mA

AC Electrical Characteristics (Note 5)

Symbol	Parameter	Conditions	LF147			LF347B			LF347			Units
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
	Amplifier to Amplifier Coupling	$T_A = 25°C$, f = 1 Hz − 20 kHz (Input Referred)		−120			−120			−120		dB
SR	Slew Rate	$V_S = \pm 15V$, $T_A = 25°C$	8	13		8	13		8	13		V/μs
GBW	Gain-Bandwidth Product	$V_S = \pm 15V$, $T_A = 25°C$	2.2	4		2.2	4		2.2	4		MHz
e_n	Equivalent Input Noise Voltage	$T_A = 25°C$, $R_S = 100\Omega$, f = 1000 Hz		20			20			20		$nV/\sqrt{Hz}$
i_n	Equivalent Input Noise Current	$T_j = 25°C$, f = 1000 Hz		0.01			0.01			0.01		$pA/\sqrt{Hz}$

Note 1: Unless otherwise specified the absolute maximum negative input voltage is equal to the negative power supply voltage.

Note 2: Any of the amplifier outputs can be shorted to ground indefinitely, however, more than one should not be simultaneously shorted as the maximum junction temperature will be exceeded.

Note 3: For operating at elevated temperature, these devices must be derated based on a thermal resistance of θ_{jA}.

Note 4: The LF147 is available In the military temperature range $-55°C \leq T_A \leq 125°C$, while the LF347B and the LF347 are available in the commercial temperature range $0°C \leq T_A \leq 70°C$. Junction temperature can rise to T_j max = 150°C.

Note 5: Unless otherwise specified the specifications apply over the full temperature range and for $V_S = \pm 20V$ for the LF147 and for $V_S = \pm 15V$ for the LF347B/LF347. V_{OS}, I_B, and I_{OS} are measured at $V_{CM} = 0$.

Note 6: The input bias currents are junction leakage currents which approximately double for every 10°C increase in the junction temperature, T_j. Due to limited production test time, the input bias currents measured are correlated to junction temperature. In normal operation the junction temperature rises above the ambient temperature as a result of internal power dissipation, P_D. $T_j = T_A + \theta_{jA} P_D$ where θ_{jA} is the thermal resistance from junction to ambient. Use of a heat sink is recommended if input bias current is to be kept to a minimum.

Note 7: Supply voltage rejection ratio is measured for both supply magnitudes increasing or decreasing simultaneously in accordance with common practice from $V_S = \pm 5V$ to $\pm 15V$ for the LF347 and LF347B and from $V_S = \pm 20V$ to $\pm 5V$ for the LF147.

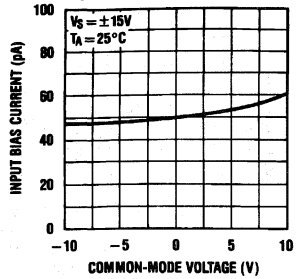
Note 8: Refer to RETS147X for LF147D and LF147J military specifications.

Note 9: Max. Power Dissipation is defined by the package characteristics. Operating the part near the Max. Power Dissipation may cause the part to operate outside guaranteed limits.

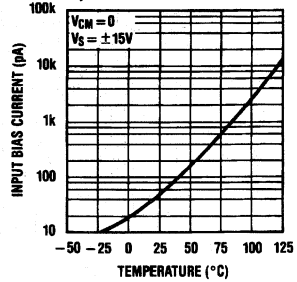
Note 10: Human body model, 1.5 kΩ in series with 100 pF.

Typical Performance Characteristics

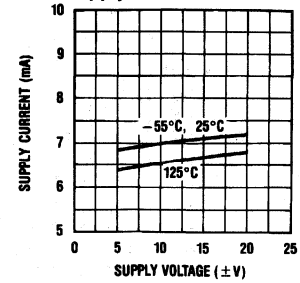
Input Bias Current



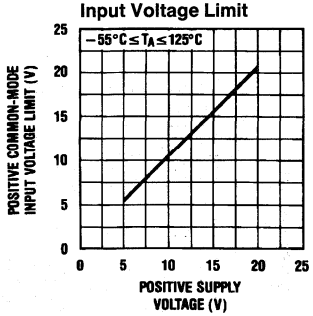
Input Bias Current



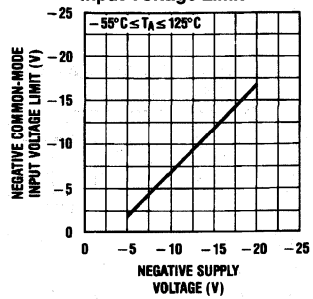
Supply Current



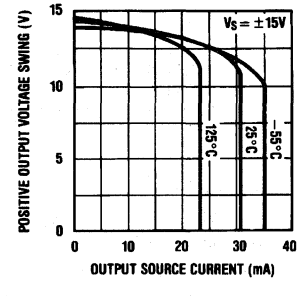
Positive Common-Mode Input Voltage Limit



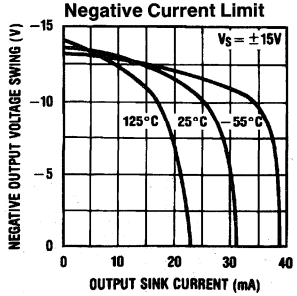
Negative Common-Mode Input Voltage Limit



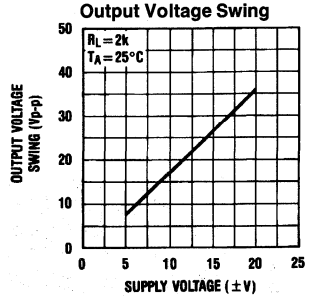
Positive Current Limit



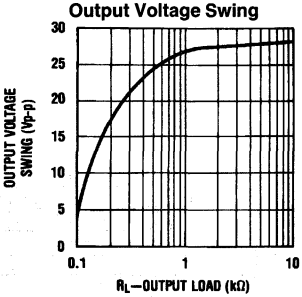
Negative Current Limit



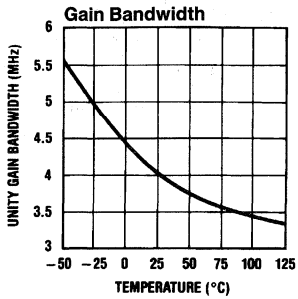
Output Voltage Swing



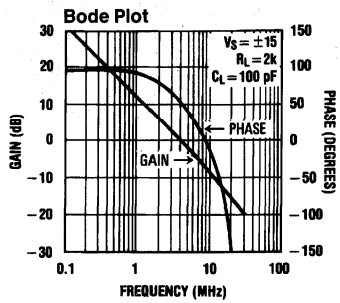
Output Voltage Swing



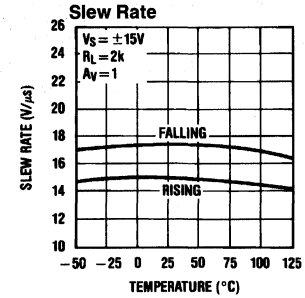
Gain Bandwidth



Bode Plot



Slew Rate

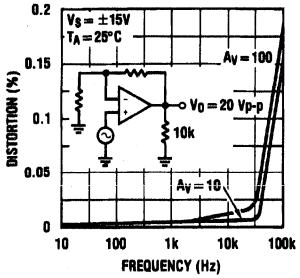


TL/H/5647–2

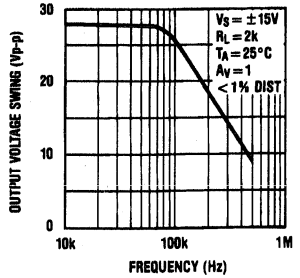
1

Typical Performance Characteristics (Continued)

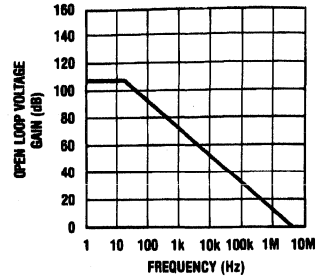
Distortion vs Frequency



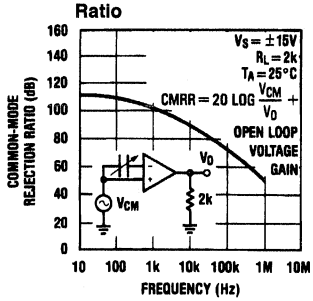
Undistorted Output Voltage Swing



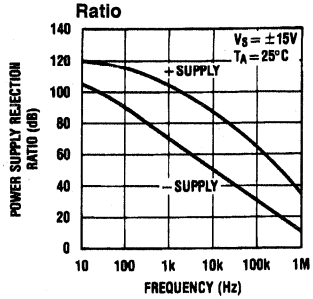
Open Loop Frequency Response



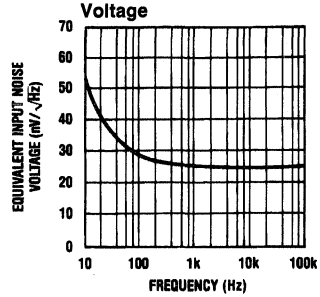
Common-Mode Rejection Ratio



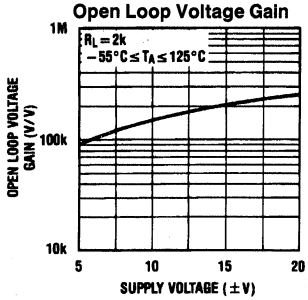
Power Supply Rejection Ratio



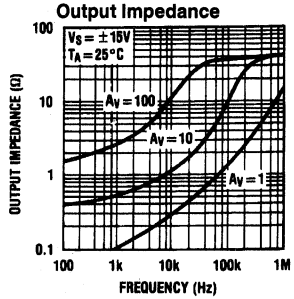
Equivalent Input Noise Voltage



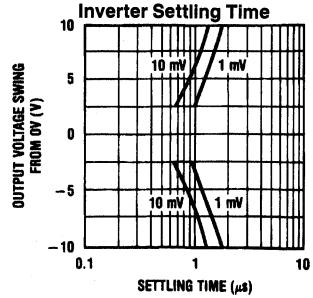
Open Loop Voltage Gain



Output Impedance



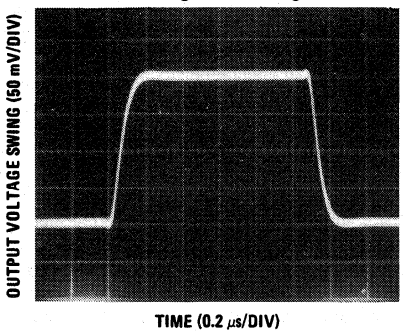
Inverter Settling Time



TL/H/5647–3

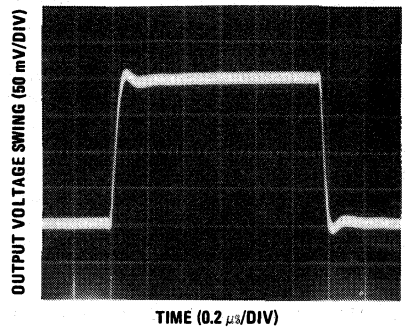
Pulse Response $R_L = 2\ k\Omega$, $C_L = 10\ pF$

Small Signal Inverting



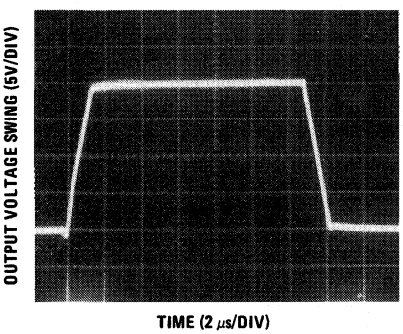
TL/H/5647–4

Small Signal Non-Inverting



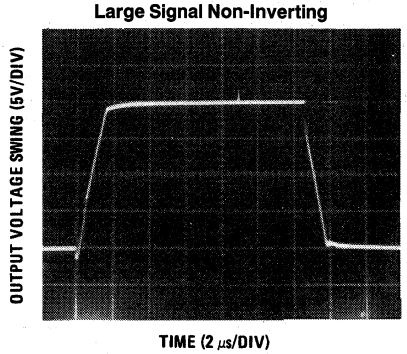
TL/H/5647–5

Large Signal Inverting



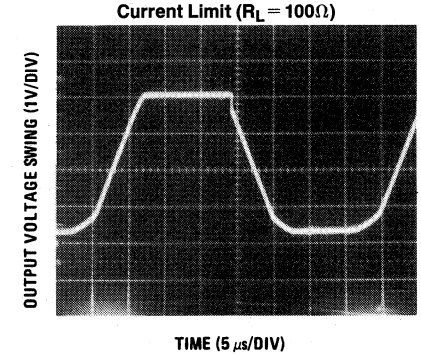
TL/H/5647–6

Large Signal Non-Inverting



TL/H/5647–7

Current Limit ($R_L = 100\Omega$)



TL/H/5647–8

Application Hints

The LF147 is an op amp with an internally trimmed input offset voltage and JFET input devices (BI-FET II™). These JFETs have large reverse breakdown voltages from gate to source and drain eliminating the need for clamps across the inputs. Therefore, large differential input voltages can easily be accommodated without a large increase in input current. The maximum differential input voltage is independent of the supply voltages. However, neither of the input voltages should be allowed to exceed the negative supply as this will cause large currents to flow which can result in a destroyed unit.

Exceeding the negative common-mode limit on either input will force the output to a high state, potentially causing a reversal of phase to the output. Exceeding the negative common-mode limit on both inputs will force the amplifier

Application Hints (Continued)

output to a high state. In neither case does a latch occur since raising the input back within the common-mode range again puts the input stage and thus the amplifier in a normal operating mode.

Exceeding the positive common-mode limit on a single input will not change the phase of the output; however, if both inputs exceed the limit, the output of the amplifier will be forced to a high state.

The amplifiers will operate with a common-mode input voltage equal to the positive supply; however, the gain bandwidth and slew rate may be decreased in this condition. When the negative common-mode voltage swings to within 3V of the negative supply, an increase in input offset voltage may occur.

Each amplifier is individually biased by a zener reference which allows normal circuit operation on ±4.5V power supplies. Supply voltages less than these may result in lower gain bandwidth and slew rate.

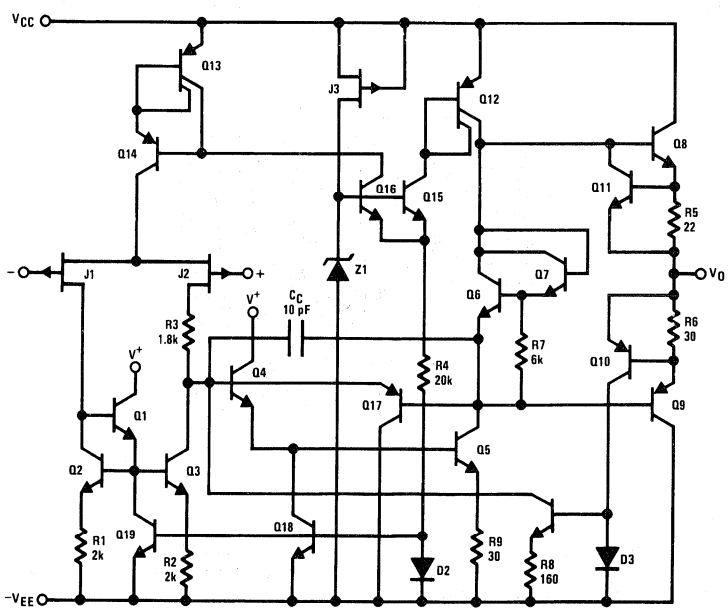
The LF147 will drive a 2 kΩ load resistance to ±10V over the full temperature range. If the amplifier is forced to drive heavier load currents, however, an increase in input offset voltage may occur on the negative voltage swing and finally reach an active current limit on both positive and negative swings.

Precautions should be taken to ensure that the power supply for the integrated circuit never becomes reversed in polarity or that the unit is not inadvertently installed backwards in a socket as an unlimited current surge through the resulting forward diode within the IC could cause fusing of the internal conductors and result in a destroyed unit.

As with most amplifiers, care should be taken with lead dress, component placement and supply decoupling in order to ensure stability. For example, resistors from the output to an input should be placed with the body close to the input to minimize "pick-up" and maximize the frequency of the feedback pole by minimizing the capacitance from the input to ground.

A feedback pole is created when the feedback around any amplifier is resistive. The parallel resistance and capacitance from the input of the device (usually the inverting input) to AC ground set the frequency of the pole. In many instances the frequency of this pole is much greater than the expected 3 dB frequency of the closed loop gain and consequently there is negligible effect on stability margin. However, if the feedback pole is less than approximately 6 times the expected 3 dB frequency a lead capacitor should be placed from the output to the input of the op amp. The value of the added capacitor should be such that the RC time constant of this capacitor and the resistance it parallels is greater than or equal to the original feedback pole time constant.

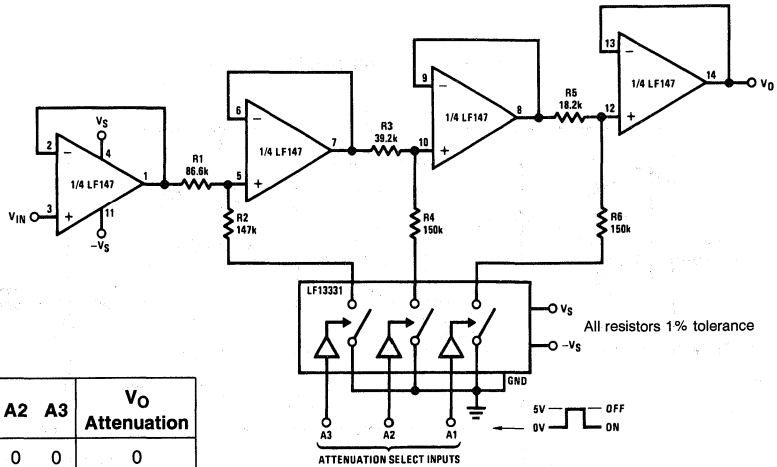
Detailed Schematic



TL/H/5647–9

Typical Applications

Digitally Selectable Precision Attenuator

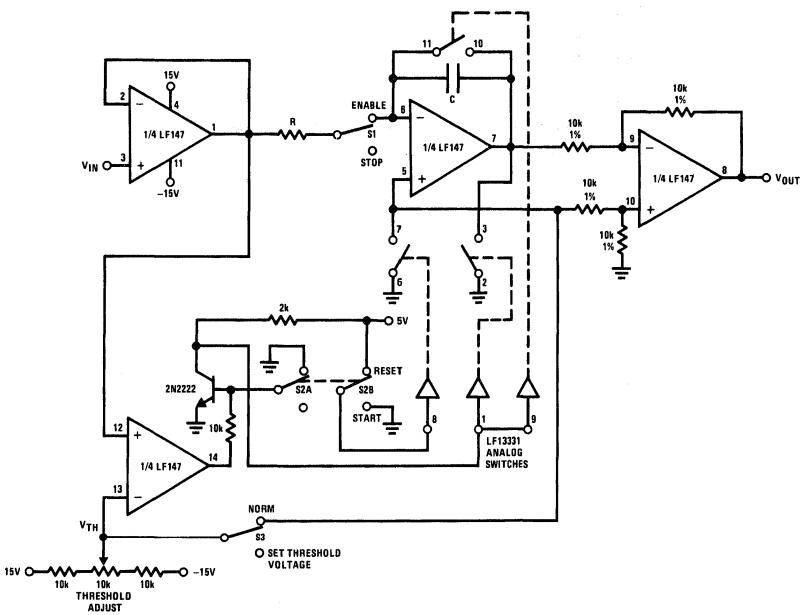


A1	A2	A3	V_O Attenuation
0	0	0	0
0	0	1	−1 dB
0	1	0	−2 dB
0	1	1	−3 dB
1	0	0	−4 dB
1	0	1	−5 dB
1	1	0	−6 dB
1	1	1	−7 dB

TL/H/5647–10

- Accuracy of better than 0.4% with standard 1% value resistors
- No offset adjustment necessary
- Expandable to any number of stages
- Very high input impedance

Long Time Integrator with Reset, Hold and Starting Threshold Adjustment



TL/H/5647–11

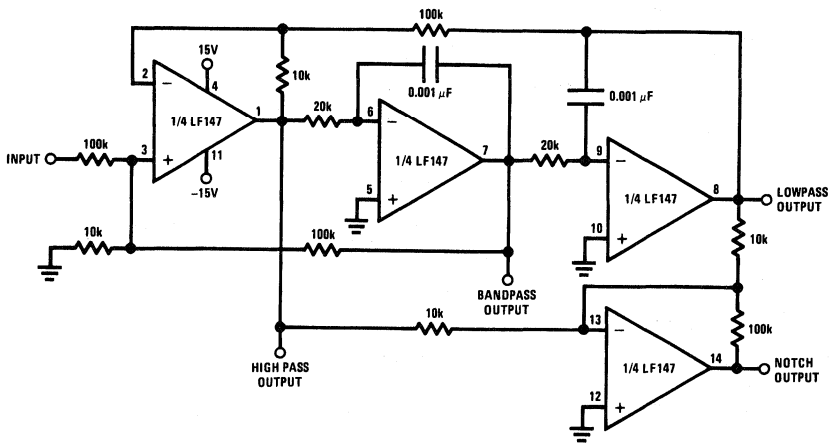
- V_{OUT} starts from zero and is equal to the integral of the input voltage with respect to the threshold voltage:

$$V_{OUT}=\frac{1}{RC}\int_0^t (V_{IN}-V_{TH})dt$$

- Output starts when $V_{IN} \geq V_{TH}$
- Switch S1 permits stopping and holding any output value
- Switch S2 resets system to zero

Typical Applications (Continued)

Universal State Variable Filter



TL/H/5647–12

For circuit shown:

$f_o = 3$ kHz, $f_{NOTCH} = 9.5$ kHz

$Q = 3.4$

Passband gain:

Highpass—0.1

Bandpass—1

Lowpass—1

Notch—10

- $f_o \times Q \leq 200$ kHz
- 10V peak sinusoidal output swing without slew limiting to 200 kHz
- See LM148 data sheet for design equations

National Semiconductor

LF155/LF156/LF157 Series Monolithic JFET Input Operational Amplifiers

General Description

These are the first monolithic JFET input operational amplifiers to incorporate well matched, high voltage JFETs on the same chip with standard bipolar transistors (BI-FET™ Technology). These amplifiers feature low input bias and offset currents/low offset voltage and offset voltage drift, coupled with offset adjust which does not degrade drift or common-mode rejection. The devices are also designed for high slew rate, wide bandwidth, extremely fast settling time, low voltage and current noise and a low 1/f noise corner.

Advantages

- Replace expensive hybrid and module FET op amps
- Rugged JFETs allow blow-out free handling compared with MOSFET input devices
- Excellent for low noise applications using either high or low source impedance—very low 1/f corner
- Offset adjust does not degrade drift or common-mode rejection as in most monolithic amplifiers
- New output stage allows use of large capacitive loads (5,000 pF) without stability problems
- Internal compensation and large differential input voltage capability

Applications

- Precision high speed integrators
- Fast D/A and A/D converters
- High impedance buffers
- Wideband, low noise, low drift amplifiers
- Logarithmic amplifiers
- Photocell amplifiers
- Sample and Hold circuits

Common Features

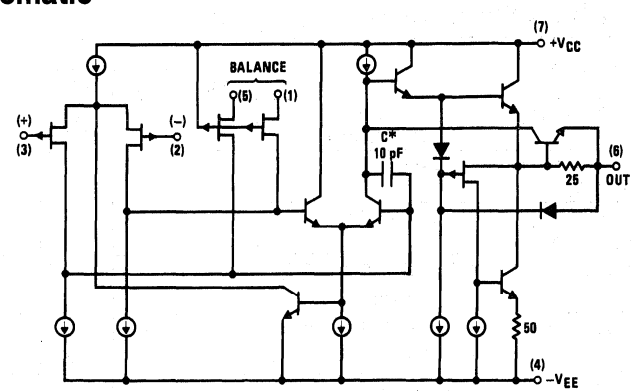
(LF155A, LF156A, LF157A)

■ Low input bias current	30 pA
■ Low input Offset Current	3 pA
■ High input impedance	$10^{12}\Omega$
■ Low input offset voltage	1 mV
■ Low input offset voltage temp. drift	3 μV/°C
■ Low input noise current	0.01 pA/$\sqrt{\text{Hz}}$
■ High common-mode rejection ratio	100 dB
■ Large dc voltage gain	106 dB

Uncommon Features

	LF155A	LF156A	LF157A ($A_V=5$)	Units
■ Extremely fast settling time to 0.01%	4	1.5	1.5	μs
■ Fast slew rate	5	12	50	V/μs
■ Wide gain bandwidth	2.5	5	20	MHz
■ Low input noise voltage	20	12	12	nV/$\sqrt{\text{Hz}}$

Simplified Schematic



*3 pF in LF157 series.

TL/H/5646–1

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/Distributors for availability and specifications.
(Note 8)

	LF155A/6A/7A	LF155/6/7	LF355B/6B/7B LF255/6/7	LF355/6/7 LF355A/6A/7A
Supply Voltage	±22V	±22V	±22V	±18V
Differential Input Voltage	±40V	±40V	±40V	±30V
Input Voltage Range (Note 2)	±20V	±20V	±20V	±16V
Output Short Circuit Duration	Continuous	Continuous	Continuous	Continuous
T_{jMAX}				
H-Package	150°C	150°C	115°C	115°C
N-Package			100°C	100°C
M-Package			100°C	100°C
Power Dissipation at T_A = 25°C (Notes 1 and 9)				
H-Package (Still Air)	560 mW	560 mW	400 mW	400 mW
H-Package (400 LF/Min Air Flow)	1200 mW	1200 mW	1000 mW	1000 mW
N-Package			670 mW	670 mW
M-Package			380 mW	380 mW
Thermal Resistance (Typical) θ_{JA}				
H-Package (Still Air)	160°C/W	160°C/W	160°C/W	160°C/W
H-Package (400 LF/Min Air Flow)	65°C/W	65°C/W	65°C/W	65°C/W
N-Package			130°C/W	130°C/W
M-Package			195°C/W	195°C/W
(Typical) θ_{JC}				
H-Package	23°C/W	23°C/W	23°C/W	23°C/W
Storage Temperature Range	−65°C to +150°C	−65°C to +150°C	−65°C to +150°C	−65°C to +150°C
Soldering Information (Lead Temp.)				
Metal Can Package				
Soldering (10 sec.)	300°C	300°C	300°C	300°C
Dual-In-Line Package				
Soldering (10 sec.)		260°C	260°C	260°C
Small Outline Package				
Vapor Phase (60 sec.)			215°C	215°C
Infrared (15 sec.)			220°C	220°C
See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.				
ESD tolerance				
(100 pF discharged through 1.5 kΩ)	1200V	1200V	1200V	1200V

DC Electrical Characteristics (Note 3) $T_A = T_j = 25°C$

Symbol	Parameter	Conditions	LF155A/6A/7A			LF355A/6A/7A			Units
			Min	Typ	Max	Min	Typ	Max	
V_{OS}	Input Offset Voltage	R_S=50Ω, T_A=25°C Over Temperature		1	2 2.5		1	2 2.3	mV mV
$\Delta V_{OS}/\Delta T$	Average TC of Input Offset Voltage	R_S=50Ω		3	5		3	5	µV/°C
$\Delta TC/\Delta V_{OS}$	Change in Average TC with V_{OS} Adjust	R_S=50Ω, (Note 4)		0.5			0.5		µV/°C per mV
I_{OS}	Input Offset Current	T_j=25°C, (Notes 3, 5) $T_j \leq T_{HIGH}$		3	10 10		3	10 1	pA nA
I_B	Input Bias Current	T_j=25°C, (Notes 3, 5) $T_j \leq T_{HIGH}$		30	50 25		30	50 5	pA nA
R_{IN}	Input Resistance	T_j=25°C		10^{12}			10^{12}		Ω
A_{VOL}	Large Signal Voltage Gain	V_S=±15V, T_A=25°C V_O=±10V, R_L=2k Over Temperature	50 25	200		50 25	200		V/mV V/mV
V_O	Output Voltage Swing	V_S=±15V, R_L=10k V_S=±15V, R_L=2k	±12 ±10	±13 ±12		±12 ±10	±13 ±12		V V

DC Electrical Characteristics (Note 3) $T_A = T_j = 25°C$ (Continued)

Symbol	Parameter	Conditions	LF155A/6A/7A			LF355A/6A/7A			Units
			Min	Typ	Max	Min	Typ	Max	
V_{CM}	Input Common-Mode Voltage Range	$V_S = \pm 15V$	±11	+15.1 −12		±11	+15.1 −12		V V
CMRR	Common-Mode Rejection Ratio		85	100		85	100		dB
PSRR	Supply Voltage Rejection Ratio	(Note 6)	85	100		85	100		dB

AC Electrical Characteristics $T_A = T_j = 25°C$, $V_S = \pm 15V$

Symbol	Parameter	Conditions	LF155A/355A			LF156A/356A			LF157A/357A			Units
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
SR	Slew Rate	LF155A/6A; $A_V = 1$, LF157A; $A_V = 5$	3	5		10	12		 40	 50		V/μs V/μs
GBW	Gain Bandwidth Product			2.5		4	4.5		15	20		MHz
t_s	Settling Time to 0.01%	(Note 7)		4			1.5			1.5		μs
e_n	Equivalent Input Noise Voltage	$R_S = 100\Omega$ f = 100 Hz f = 1000 Hz		 25 20			 15 12			 15 12		 nV/√Hz nV/√Hz
i_n	Equivalent Input Noise Current	f = 100 Hz f = 1000 Hz		0.01 0.01			0.01 0.01			0.01 0.01		pA/√Hz pA/√Hz
C_{IN}	Input Capacitance			3			3			3		pF

DC Electrical Characteristics (Note 3)

Symbol	Parameter	Conditions	LF155/6/7			LF255/6/7 LF355B/6B/7B			LF355/6/7			Units
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_{OS}	Input Offset Voltage	$R_S = 50\Omega$, $T_A = 25°C$ Over Temperature		3	5 7		3	5 6.5		3	10 13	mV mV
$\Delta V_{OS}/\Delta T$	Average TC of Input Offset Voltage	$R_S = 50\Omega$		5			5			5		μV/°C
$\Delta TC/\Delta V_{OS}$	Change in Average TC with V_{OS} Adjust	$R_S = 50\Omega$, (Note 4)		0.5			0.5			0.5		μV/°C per mV
I_{OS}	Input Offset Current	$T_j = 25°C$, (Notes 3, 5) $T_j \leq T_{HIGH}$		3	20 20		3	20 1		3	50 2	pA nA
I_B	Input Bias Current	$T_j = 25°C$, (Notes 3, 5) $T_j \leq T_{HIGH}$		30	100 50		30	100 5		30	200 8	pA nA
R_{IN}	Input Resistance	$T_j = 25°C$		10^{12}			10^{12}			10^{12}		Ω
A_{VOL}	Large Signal Voltage Gain	$V_S = \pm 15V$, $T_A = 25°C$ $V_O = \pm 10V$, $R_L = 2k$ Over Temperature	50 25	200		50 25	200		25 15	200		V/mV V/mV
V_O	Output Voltage Swing	$V_S = \pm 15V$, $R_L = 10k$ $V_S = \pm 15V$, $R_L = 2k$	±12 ±10	±13 ±12		±12 ±10	±13 ±12		±12 ±10	±13 ±12		V V
V_{CM}	Input Common-Mode Voltage Range	$V_S = \pm 15V$	±11	+15.1 −12		±11	±15.1 −12		+10	+15.1 −12		V V
CMRR	Common-Mode Rejection Ratio		85	100		85	100		80	100		dB
PSRR	Supply Voltage Rejection Ratio	(Note 6)	85	100		85	100		80	100		dB

DC Electrical Characteristics $T_A = T_j = 25°C$, $V_S = \pm 15V$

Parameter	LF155A/155, LF255, LF355A/355B		LF355		LF156A/156, LF256/356B		LF356A/356		LF157A/157 LF257/357B		LF357A/357		Units
	Typ	Max	Typ	Max	Typ	Max	Typ	Max	Typ	Max	Typ	Max	
Supply Current	2	4	2	4	5	7	5	10	5	7	5	10	mA

AC Electrical Characteristics $T_A = T_j = 25°C$, $V_S = \pm 15V$

Symbol	Parameter	Conditions	LF155/255/ 355/355B	LF156/256, LF356B	LF156/256/ 356/356B	LF157/257, LF357B	LF157/257/ 357/357B	Units
			Typ	Min	Typ	Min	Typ	
SR	Slew Rate	LF155/6: $A_V = 1$, LF157: $A_V = 5$	5	7.5	12	30	50	V/μs V/μs
GBW	Gain Bandwidth Product		2.5		5		20	MHz
t_s	Settling Time to 0.01%	(Note 7)	4		1.5		1.5	μs
e_n	Equivalent Input Noise Voltage	$R_S = 100\Omega$ f = 100 Hz f = 1000 Hz	25 20		15 12		15 12	nV/√Hz nV/√Hz
i_n	Equivalent Input Current Noise	f = 100 Hz f = 1000 Hz	0.01 0.01		0.01 0.01		0.01 0.01	pA/√Hz pA/√Hz
C_{IN}	Input Capacitance		3		3		3	pF

Notes for Electrical Characteristics

Note 1: The maximum power dissipation for these devices must be derated at elevated temperatures and is dictated by T_{JMAX}, θ_{jA}, and the ambient temperature, T_A. The maximum available power dissipation at any temperature is $P_d = (T_{JMAX} - T_A)/\theta_{jA}$ or the 25°C P_{dMAX}, whichever is less.

Note 2: Unless otherwise specified the absolute maximum negative input voltage is equal to the negative power supply voltage.

Note 3: Unless otherwise stated, these test conditions apply:

	LF155A/6A/7A LF155//6/7	LF255//6/7	LF355A/6A/7A	LF355B/6B/7B	LF355//6/7
Supply Voltage, V_S	$\pm 15V \le V_S \le \pm 20V$	$\pm 15V \le V_S \le \pm 20V$	$\pm 15V \le V_S \le \pm 18V$	$\pm 15V \le V_S \pm 20V$	$V_S = \pm 15V$
T_A	$-55°C \le T_A \le +125°C$	$-25°C \le T_A \le +85°C$	$0°C \le T_A \le +70°C$	$0°C \le T_A \le +70°C$	$0°C \le T_A \le +70°C$
T_{HIGH}	+125°C	+85°C	+70°C	+70°C	+70°C

and V_{OS}, I_B and I_{OS} are measured at $V_{CM} = 0$.

Note 4: The Temperature Coefficient of the adjusted input offset voltage changes only a small amount (0.5μV/°C typically) for each mV of adjustment from its original unadjusted value. Common-mode rejection and open loop voltage gain are also unaffected by offset adjustment.

Note 5: The input bias currents are junction leakage currents which approximately double for every 10°C increase in the junction temperature, T_J. Due to limited production test time, the input bias currents measured are correlated to junction temperature. In normal operation the junction temperature rises above the ambient temperature as a result of internal power dissipation, Pd. $T_j = T_A + \theta_{jA}$ Pd where θ_{jA} is the thermal resistance from junction to ambient. Use of a heat sink is recommended if input bias current is to be kept to a minimum.

Note 6: Supply Voltage Rejection is measured for both supply magnitudes increasing or decreasing simultaneously, in accordance with common practice.

Note 7: Settling time is defined here, for a unity gain inverter connection using 2 kΩ resistors for the LF155/6. It is the time required for the error voltage (the voltage at the inverting input pin on the amplifier) to settle to within 0.01% of its final value from the time a 10V step input is applied to the inverter. For the LF157, $A_V = -5$, the feedback resistor from output to input is 2 kΩ and the output step is 10V (See Settling Time Test Circuit).

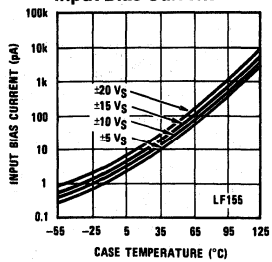
Note 8: Refer to RETS155AX for LF155A, RETS155X for LF155, RETS156AX for LF156A, RETS156X for LF156, RETS157A for LF157A and RETS157X for LF157 military specifications.

Note 9: Max. Power Dissipation is defined by the package characteristics. Operating the part near the Max. Power Dissipation may cause the part to operate outside guaranteed limits.

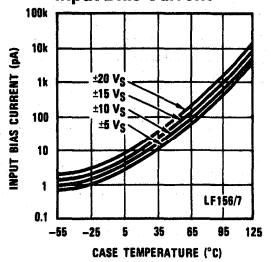
Typical DC Performance Characteristics

Curves are for LF155, LF156 and LF157 unless otherwise specified.

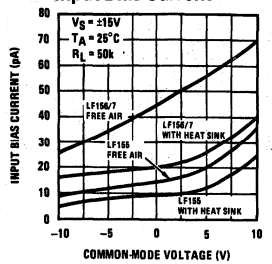
Input Bias Current



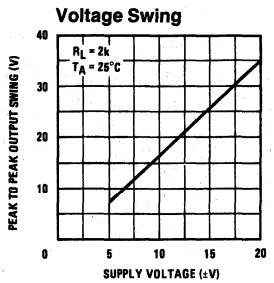
Input Bias Current



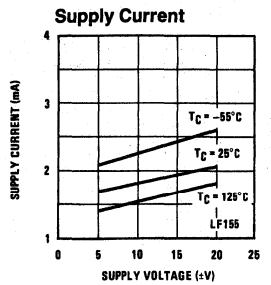
Input Bias Current



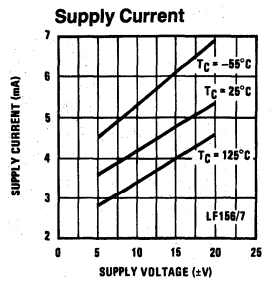
Voltage Swing



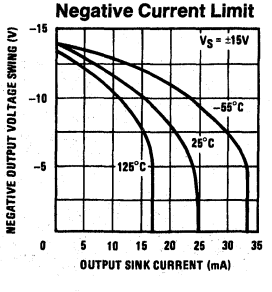
Supply Current



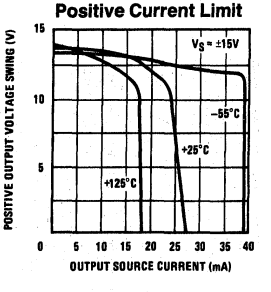
Supply Current



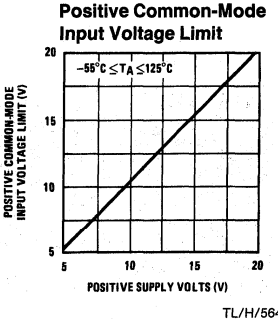
Negative Current Limit



Positive Current Limit

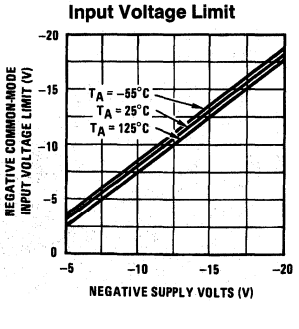


Positive Common-Mode Input Voltage Limit

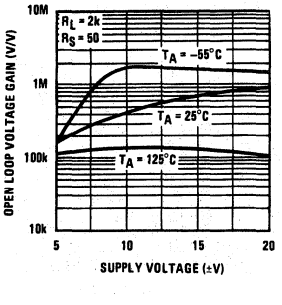


TL/H/5646–2

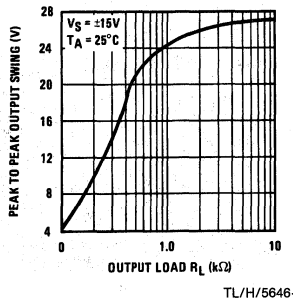
Negative Common-Mode Input Voltage Limit



Open Loop Voltage Gain



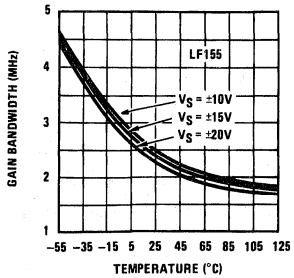
Output Voltage Swing



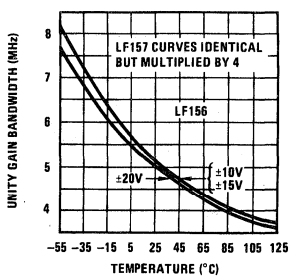
TL/H/5646–3

Typical AC Performance Characteristics

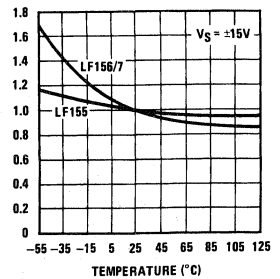
Gain Bandwidth



Gain Bandwidth

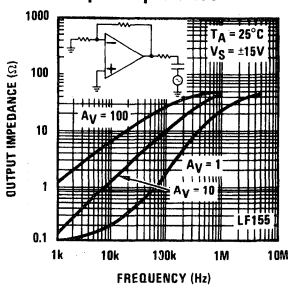


Normalized Slew Rate

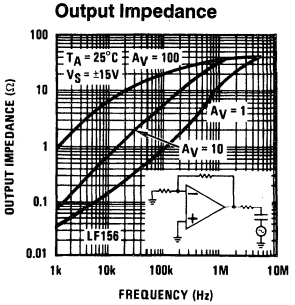


TL/H/5646–4

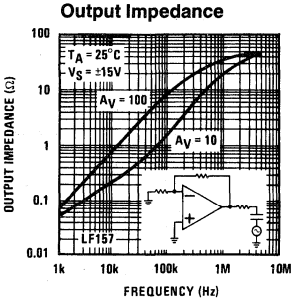
Output Impedance



Output Impedance

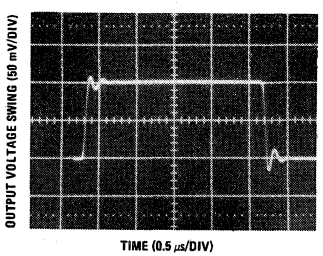


Output Impedance



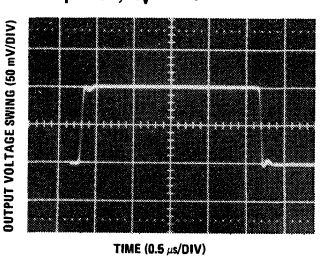
TL/H/5646–12

LF155 Small Signal Pulse Response, $A_V = +1$



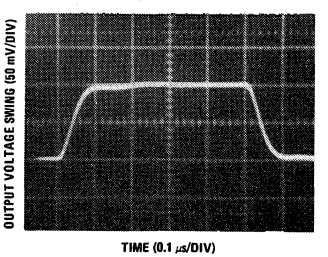
TL/H/5646–5

LF156 Small Signal Pulse Response, $A_V = +1$



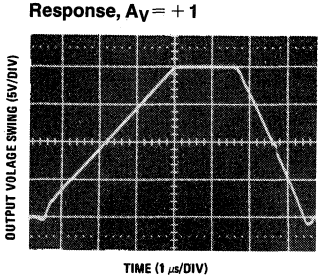
TL/H/5646–6

Small Signal Pulse Response, $A_V = +5$



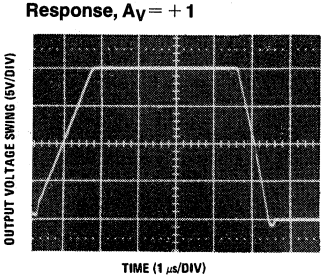
TL/H/5646–7

LF155 Large Signal Pulse Response, $A_V = +1$



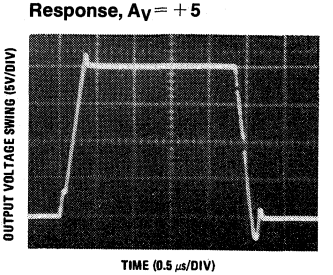
TL/H/5646–8

LF156 Large Signal Pulse Response, $A_V = +1$



TL/H/5646–9

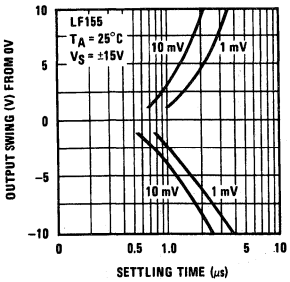
LF157 Large Signal Pulse Response, $A_V = +5$



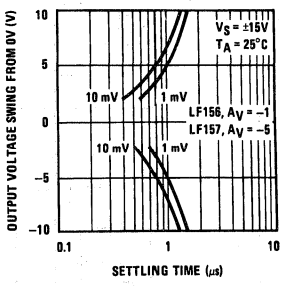
TL/H/5646–10

Typical AC Performance Characteristics (Continued)

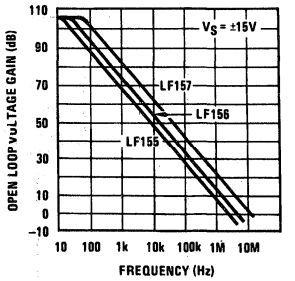
Inverter Settling Time



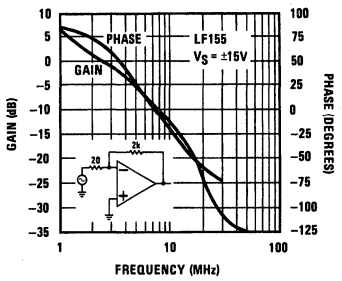
Inverter Settling Time



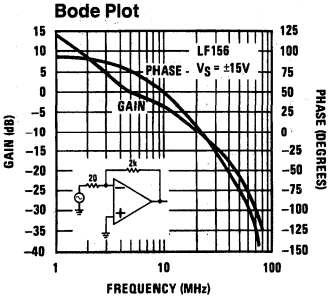
Open Loop Frequency Response



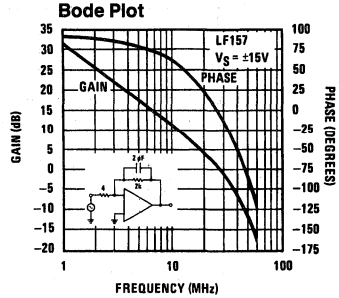
Bode Plot



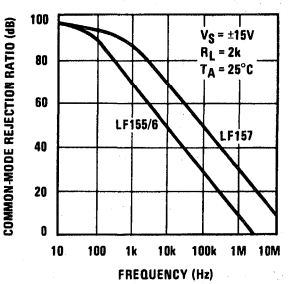
Bode Plot



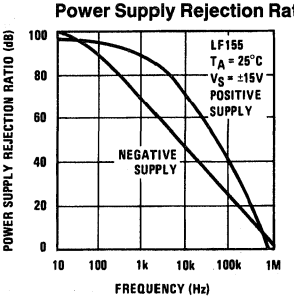
Bode Plot



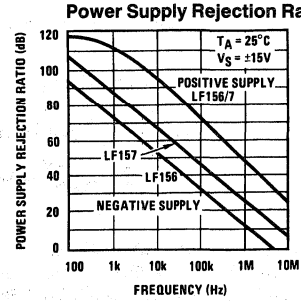
Common-Mode Rejection Ratio



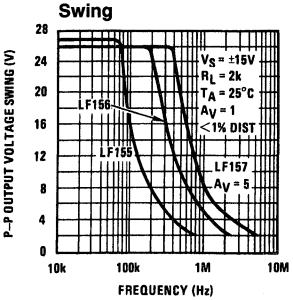
Power Supply Rejection Ratio



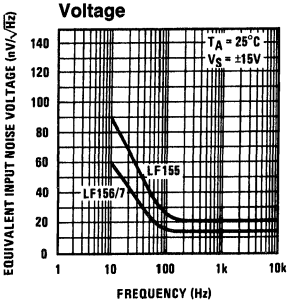
Power Supply Rejection Ratio



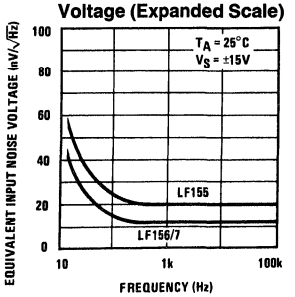
Undistorted Output Voltage Swing



Equivalent Input Noise Voltage



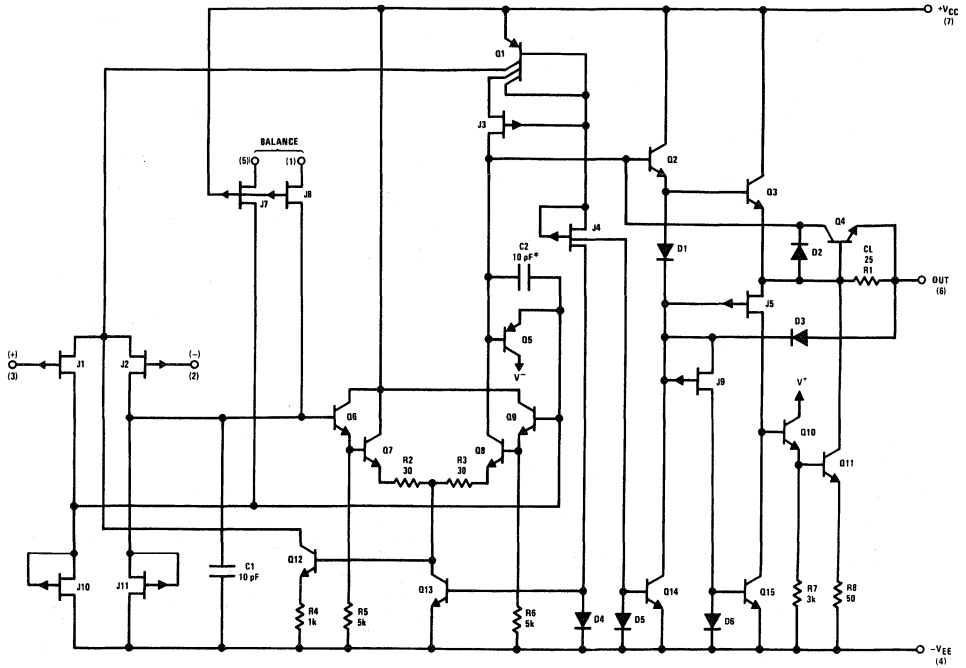
Equivalent Input Noise Voltage (Expanded Scale)



TL/H/5646–11

1

Detailed Schematic

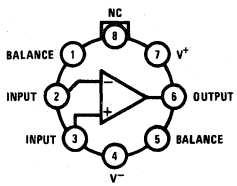


*C = 3 pF in LF157 series.

TL/H/5646–13

Connection Diagrams (Top Views)

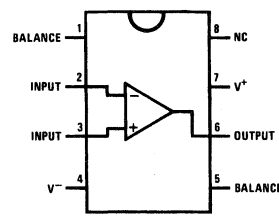
Metal Can Package (H)



TL/H/5646–14

Order Number LF155AH, LF156AH, LF157AH, LF155H, LF156H, LF157H, LF255H, LF256H, LF257H, LF355AH, LF356AH, LF357AH, LF356BH, LF355H, LF356H, LF357H, LM155AH/883, LM155H/883, LM156AH/883, LM156H/883, LM157AH/883 or LM157H/883*
See NS Package Number H08C

Dual-In-Line Package (M and N)



TL/H/5646–29

Order Number LF355M, LF356M, LF357M, LF355BM, LF356BM, LF355BN, LF356BN, LF357BN, LF355N, LF356N or LF357N
See NS Package Number M08A or N08E

*Available per JM38510/11401 or JM38510/11402

Application Hints

The LF155/6/7 series are op amps with JFET input devices. These JFETs have large reverse breakdown voltages from gate to source and drain eliminating the need for clamps across the inputs. Therefore large differential input voltages can easily be accomodated without a large increase in input current. The maximum differential input voltage is independent of the supply voltages. However, neither of the input voltages should be allowed to exceed the negative supply as this will cause large currents to flow which can result in a destroyed unit.

Exceeding the negative common-mode limit on either input will force the output to a high state, potentially causing a reversal of phase to the output. Exceeding the negative common-mode limit on both inputs will force the amplifier output to a high state. In neither case does a latch occur since raising the input back within the common-mode range again puts the input stage and thus the amplifier in a normal operating mode.

Exceeding the positive common-mode limit on a single input will not change the phase of the output however, if both inputs exceed the limit, the output of the amplifier will be forced to a high state.

These amplifiers will operate with the common-mode input voltage equal to the positive supply. In fact, the common-mode voltage can exceed the positive supply by approximately 100 mV independent of supply voltage and over the full operating temperature range. The positive supply can therefore be used as a reference on an input as, for example, in a supply current monitor and/or limiter.

Precautions should be taken to ensure that the power supply for the integrated circuit never becomes reversed in polarity or that the unit is not inadvertently installed backwards in a socket as an unlimited current surge through the resulting forward diode within the IC could cause fusing of the internal conductors and result in a destroyed unit.

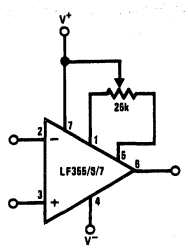
All of the bias currents in these amplifiers are set by FET current sources. The drain currents for the amplifiers are therefore essentially independent of supply voltage.

As with most amplifiers, care should be taken with lead dress, component placement and supply decoupling in order to ensure stability. For example, resistors from the output to an input should be placed with the body close to the input to minimize "pickup" and maximize the frequency of the feedback pole by minimizing the capacitance from the input to ground.

A feedback pole is created when the feedback around any amplifier is resistive. The parallel resistance and capacitance from the input of the device (usually the inverting input) to ac ground set the frequency of the pole. In many instances the frequency of this pole is much greater than the expected 3 dB frequency of the closed loop gain and consequently there is negligible effect on stability margin. However, if the feedback pole is less than approximately six times the expected 3 dB frequency a lead capacitor should be placed from the output to the input of the op amp. The value of the added capacitor should be such that the RC time constant of this capacitor and the resistance it parallels is greater than or equal to the original feedback pole time constant.

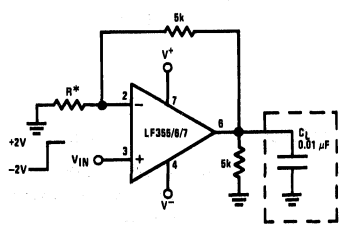
Typical Circuit Connections

V_{OS} Adjustment



- V_{OS} is adjusted with a 25k potentiometer
- The potentiometer wiper is connected to V^+
- For potentiometers with temperature coefficient of 100 ppm/°C or less the additional drift with adjust is ≈ 0.5 μV/°C/mV of adjustment
- Typical overall drift: 5 μV/°C ±(0.5 μV/°C/mV of adj.)

Driving Capacitive Loads



*LF155/6 R = 5k

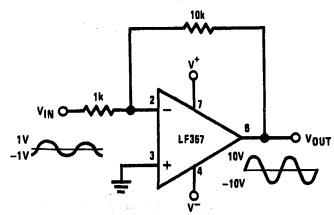
LF157 R = 1.25k

Due to a unique output stage design, these amplifiers have the ability to drive large capacitive loads and still maintain stability. $C_{L(MAX)} \cong 0.01$ μF.

Overshoot ≤ 20%

Settling time (t_s) ≅ 5 μs

LF157. A Large Power BW Amplifier

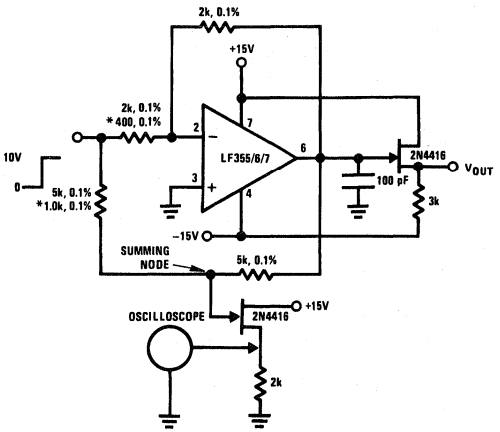


TL/H/5646–15

For distortion ≤ 1% and a 20 Vp-p V_{OUT} swing, power bandwidth is: 500 kHz.

Typical Applications

Settling Time Test Circuit

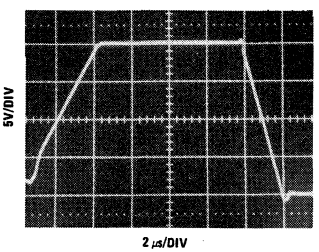


- Settling time is tested with the LF155/6 connected as unity gain inverter and LF157 connected for $A_V = -5$
- FET used to isolate the probe capacitance
- Output = 10V step
- $A_V = -5$ for LF157

TL/H/5646–16

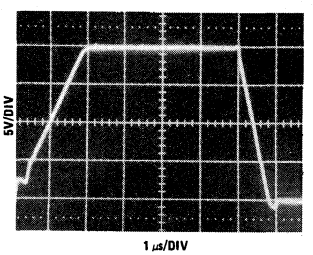
Large Signal Inverter Output, V_{OUT} (from Settling Time Circuit)

LF355



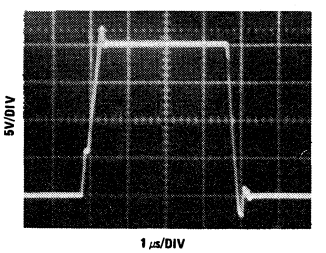
TL/H/5646–17

LF356



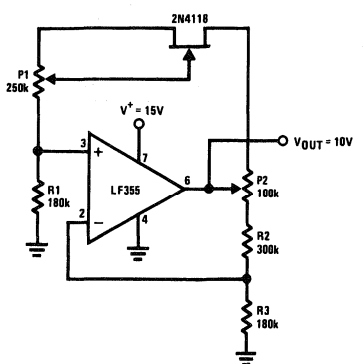
TL/H/5646–18

LF357



TL/H/5646–19

Low Drift Adjustable Voltage Reference

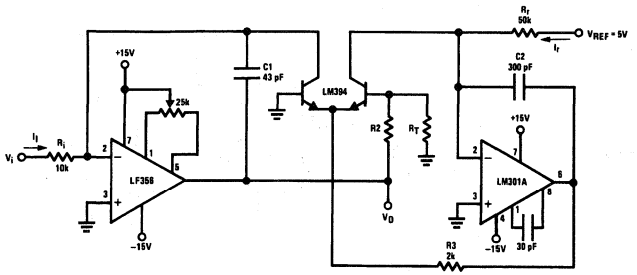


- $\Delta V_{OUT}/\Delta T = \pm 0.002\%/°C$
- All resistors and potentiometers should be wire-wound
- P1: drift adjust
- P2: V_{OUT} adjust
- Use LF155 for
  - Low I_B
  - Low drift
  - Low supply current

TL/H/5646–20

Typical Applications (Continued)

Fast Logarithmic Converter

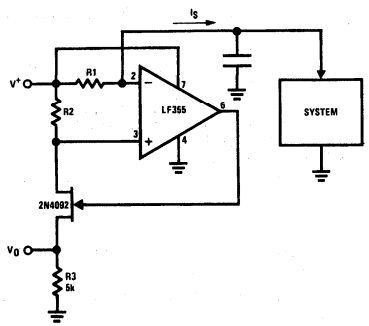


TL/H/5646–21

- Dynamic range: 100 μA ≤ I_i ≤ 1 mA (5 decades), $|V_O|$ = 1V/decade
- Transient response: 3 μs for ΔI_i = 1 decade
- C1, C2, R2, R3: added dynamic compensation
- V_{OS} adjust the LF156 to minimize quiescent error
- R_T: Tel Labs type Q81 + 0.3%/°C

$$|V_{OUT}| = \left[1 + \frac{R2}{R_T}\right]\frac{kT}{q}\ln V_i\left[\frac{R_r}{V_{REF}\,R_i}\right] = \log V_i \frac{1}{R_i I_r} \quad R2 = 15.7k,\ R_T = 1k,\ 0.3\%/°C \text{ (for temperature compensation)}$$

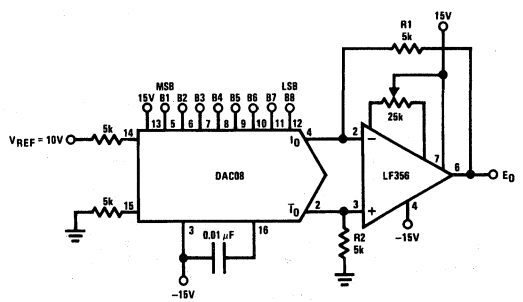
Precision Current Monitor



TL/H/5646–31

- V_O = 5 R1/R2 (V/mA of I_S)
- R1, R2, R3: 0.1% resistors
- Use LF155 for
  - Common-mode range to supply range
  - Low I_B
  - Low V_{OS}
  - Low Supply Current

8-Bit D/A Converter with Symmetrical Offset Binary Operation



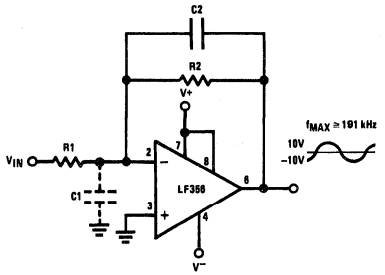
TL/H/5646–32

- R1, R2 should be matched within ±0.05%
- Full-scale response time: 3μs

E_O	B1	B2	B3	B4	B5	B6	B7	B8	Comments
+9.920	1	1	1	1	1	1	1	1	Positive Full-Scale
+0.040	1	0	0	0	0	0	0	0	(+) Zero-Scale
−0.040	0	1	1	1	1	1	1	1	(−) Zero-Scale
−9.920	0	0	0	0	0	0	0	0	Negative Full-Scale

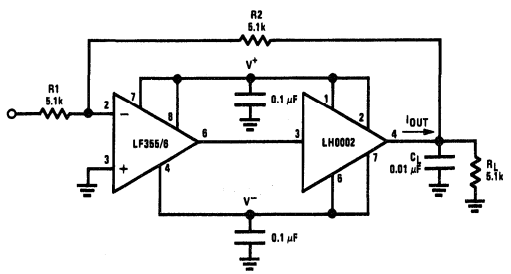
Typical Applications (Continued)

Wide BW Low Noise, Low Drift Amplifier



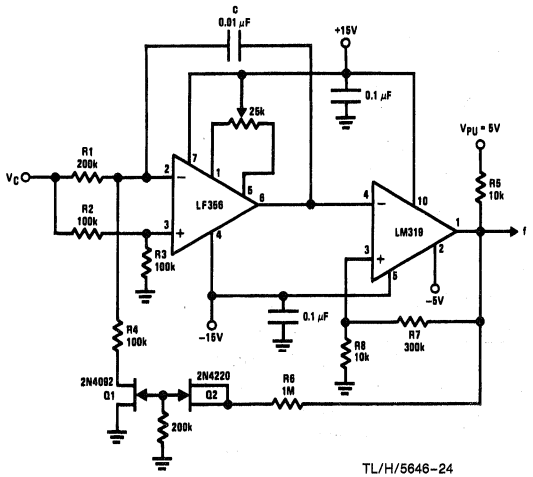
- Power BW: $f_{MAX} = \frac{S_r}{2\pi V_P} \cong 191$ kHz
- Parasitic input capacitance C1 ≅ (3 pF for LF155, LF156 and LF157 plus any additional layout capacitance) interacts with feedback elements and creates undesirable high frequency pole. To compensate add C2 such that: R2 C2 ≅ R1 C1.

Boosting the LF156 with a Current Amplifier



- $I_{OUT(MAX)} \cong 150$ mA (will drive $R_L \geq 100\Omega$)
- $\frac{\Delta V_{OUT}}{\Delta T} = \frac{0.15}{10^{-2}}$ V/µs (with C_L shown)
- No additional phase shift added by the current amplifier

3 Decades VCO

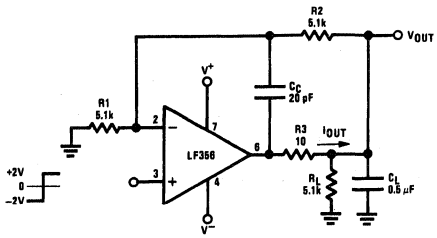


TL/H/5646–24

$f = \frac{V_C (R8 + R7)}{(8\ V_{PU}\ R8\ R1)\ C}$, $0 \leq V_C \leq 30$V, 10 Hz ≤ f ≤ 10 kHz

R1, R4 matched. Linearity 0.1% over 2 decades.

Isolating Large Capacitive Loads

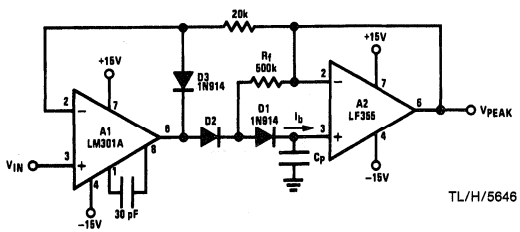


TL/H/5646–22

- Overshoot 6%
- t_s 10 µs
- When driving large C_L, the V_{OUT} slew rate determined by C_L and $I_{OUT(MAX)}$:

$\frac{\Delta V_{OUT}}{\Delta T} = \frac{I_{OUT}}{C_L} \cong \frac{0.02}{0.5}$ V/µs = 0.04 V/µs (with C_L shown)

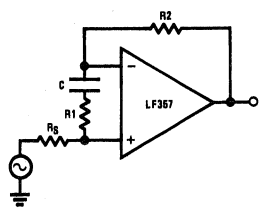
Low Drift Peak Detector



TL/H/5646

- By adding D1 and R_f, $V_{D1} = 0$ during hold mode. Leakage of D2 provided by feedback path through R_f.
- Leakage of circuit is essentially I_b (LF155, LF156) plus capacitor leakage of Cp.
- Diode D3 clamps V_{OUT} (A1) to $V_{IN} - V_{D3}$ to improve speed and to limit reverse bias of D2.
- Maximum input frequency should be $<< \frac{1}{2\pi R_f C_{D2}}$ where C_{D2} is the shunt capacitance of D2.

Non-Inverting Unity Gain Operation for LF157



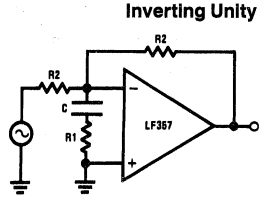
$R1C \geq \frac{1}{(2\pi)\ (5\ \text{MHz})}$

$R1 = \frac{R2 + R_S}{4}$

$A_{V(DC)} = 1$

$f_{-3\ dB} \approx 5$ MHz

Inverting Unity Gain for LF157



$R1C \geq \frac{1}{(2\pi)\ (5\ \text{MHz})}$

$R1 = \frac{R2}{4}$

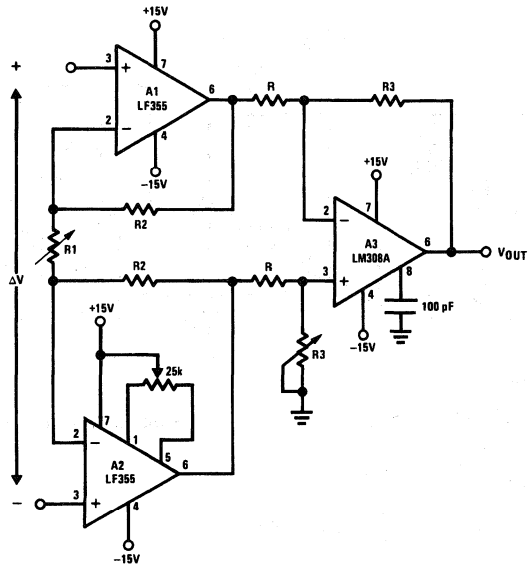
$A_{V(DC)} = -1$

$f_{-3\ dB} \approx 5$ MHz

TL/H/5646–25

Typical Applications (Continued)

High Impedance, Low Drift Instrumentation Amplifier

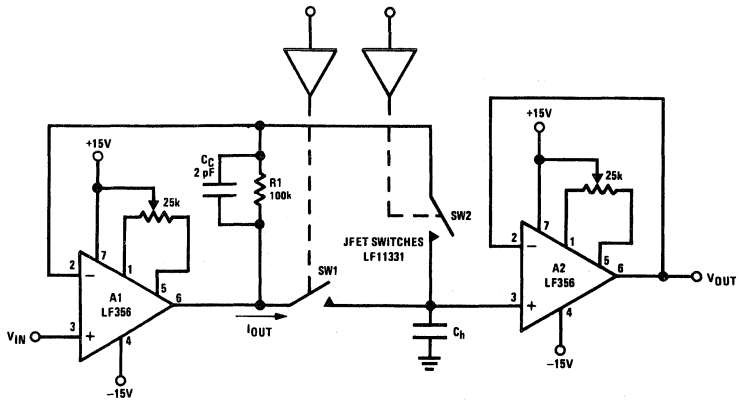


TL/H/5646–26

- $V_{OUT} = \frac{R3}{R}\left[\frac{2R2}{R1} + 1\right] \Delta V, V^- + 2V \leq V_{IN}$ common-mode $\leq V^+$
- System V_{OS} adjusted via A2 V_{OS} adjust
- Trim R3 to boost up CMRR to 120 dB. Instrumentation amplifier resistor array recommended for best accuracy and lowest drift

Typical Applications (Continued)

Fast Sample and Hold



TL/H/5646–33

- Both amplifiers (A1, A2) have feedback loops individually closed with stable responses (overshoot negligible)
- Acquisition time T_A, estimated by:

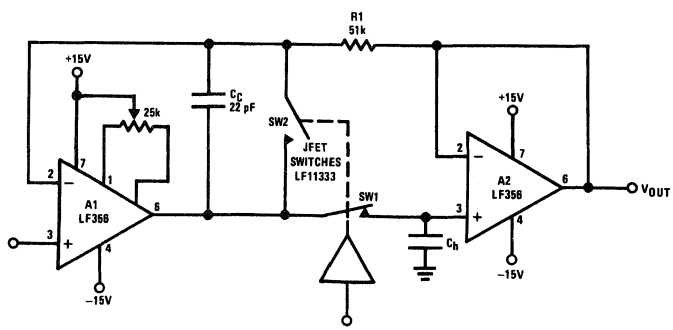
$$T_A \cong \left[\frac{2R_{ON}, V_{IN}, C_h}{S_r}\right] \text{½ provided that:}$$

$$V_{IN} < 2\pi S_r R_{ON} C_h \text{ and } T_A > \frac{V_{IN} C_h}{I_{OUT(MAX)}}, R_{ON} \text{ is of SW1}$$

$$\text{If inequality not satisfied: } T_A \cong \frac{V_{IN} C_h}{20 \text{ mA}}$$

- LF156 develops full S_r output capability for $V_{IN} \geq 1V$
- Addition of SW2 improves accuracy by putting the voltage drop across SW1 inside the feedback loop
- Overall accuracy of system determined by the accuracy of both amplifiers, A1 and A2

High Accuracy Sample and Hold

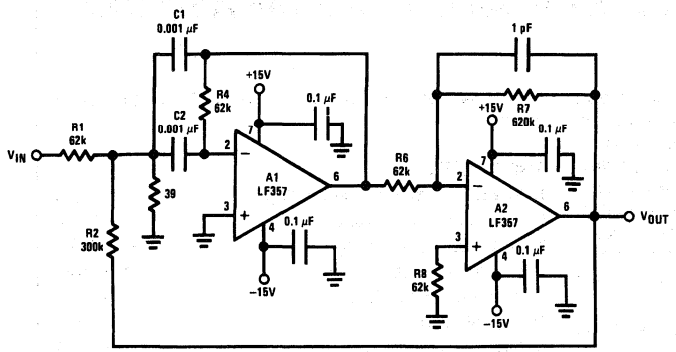


TL/H/5646–27

- By closing the loop through A2, the V_{OUT} accuracy will be determined uniquely by A1. No V_{OS} adjust required for A2.
- T_A can be estimated by same considerations as previously but, because of the added propagation delay in the feedback loop (A2) the overshoot is not negligible.
- Overall system slower than fast sample and hold
- R1, C_C: additional compensation
- Use LF156 for
  - Fast settling time
  - Low V_{OS}

Typical Applications (Continued)

High Q Band Pass Filter



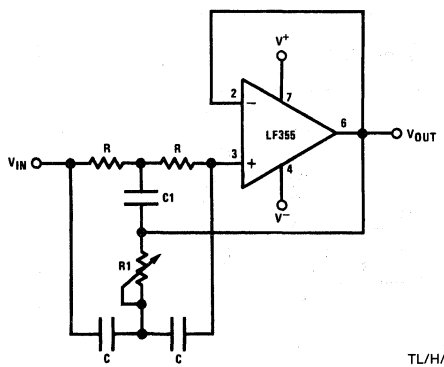
TL/H/5646–28

- By adding positive feedback (R2) Q increases to 40
- $f_{BP} = 100$ kHz

$$\frac{V_{OUT}}{V_{IN}} = 10\sqrt{Q}$$

- Clean layout recommended
- Response to a 1 Vp-p tone burst: 300 μs

High Q Notch Filter



TL/H/5646–34

- $2R1 = R = 10\ M\Omega$
  $2C = C1 = 300$ pF
- Capacitors should be matched to obtain high Q
- $f_{NOTCH} = 120$ Hz, notch = −55 dB, Q > 100
- Use LF155 for
  - Low I_B
  - Low supply current

National Semiconductor

LF351 Wide Bandwidth JFET Input Operational Amplifier

General Description

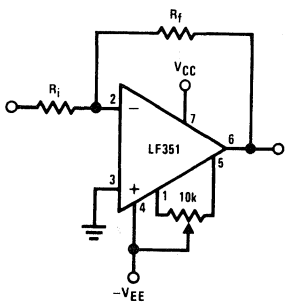
The LF351 is a low cost high speed JFET input operational amplifier with an internally trimmed input offset voltage (BI-FET II™ technology). The device requires a low supply current and yet maintains a large gain bandwidth product and a fast slew rate. In addition, well matched high voltage JFET input devices provide very low input bias and offset currents. The LF351 is pin compatible with the standard LM741 and uses the same offset voltage adjustment circuitry. This feature allows designers to immediately upgrade the overall performance of existing LM741 designs.

The LF351 may be used in applications such as high speed integrators, fast D/A converters, sample-and-hold circuits and many other circuits requiring low input offset voltage, low input bias current, high input impedance, high slew rate and wide bandwidth. The device has low noise and offset voltage drift, but for applications where these requirements are critical, the LF356 is recommended. If maximum supply current is important, however, the LF351 is the better choice.

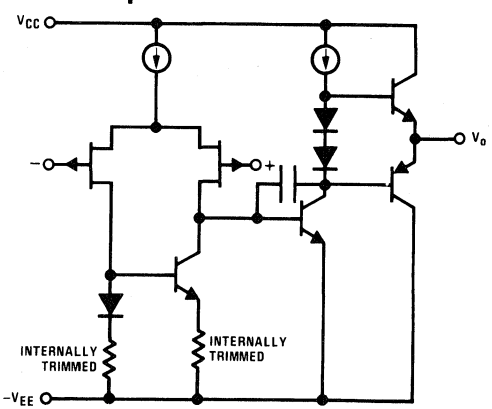
Features

■ Internally trimmed offset voltage	10 mV
■ Low input bias current	50 pA
■ Low input noise voltage	25 nV/$\sqrt{Hz}$
■ Low input noise current	0.01 pA/$\sqrt{Hz}$
■ Wide gain bandwidth	4 MHz
■ High slew rate	13 V/μs
■ Low supply current	1.8 mA
■ High input impedance	$10^{12}\Omega$
■ Low total harmonic distortion $A_V=10$, $R_L=10k$, $V_O=20$ Vp-p, BW=20 Hz–20 kHz	<0.02%
■ Low 1/f noise corner	50 Hz
■ Fast settling time to 0.01%	2 μs

Typical Connection

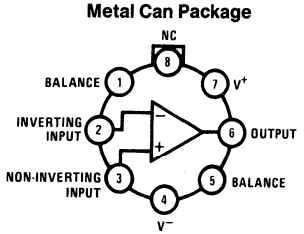


Simplified Schematic



Connection Diagrams (Top Views)

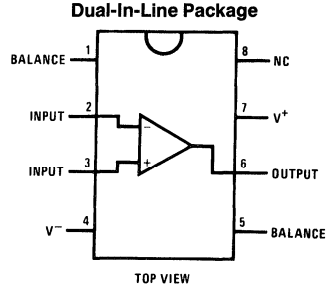
Metal Can Package



Note. Pin 4 connected to case.

Order Number LF351H
See NS Package Number H08C

Dual-In-Line Package



TOP VIEW

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Order Number LF351M or LF351N
See NS Package Number M08A or N08E

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	±18V
Power Dissipation (Notes 1 and 6)	670 mW
Operating Temperature Range	0°C to +70°C
$T_{j(MAX)}$	115°C
Differential Input Voltage	±30V
Input Voltage Range (Note 2)	±15V
Output Short Circuit Duration	Continuous
Storage Temperature Range	−65°C to +150°C
Lead Temp. (Soldering, 10 sec.)	
Metal Can	300°C
DIP	260°C

	H Package	N Package	M Package
θ_{jA}	164°C/W (Still Air) 66°C/W (400 LF/min Air Flow)	120°C/W	TBD
θ_{jC}	21°C/W		

Soldering Information

Dual-In-Line Package	
Soldering (10 sec.)	260°C
Small Outline Package	
Vapor Phase (60 sec.)	215°C
Infrared (15 sec.)	220°C

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

ESD rating to be determined.

DC Electrical Characteristics (Note 3)

Symbol	Parameter	Conditions	LF351			Units
			Min	Typ	Max	
V_{OS}	Input Offset Voltage	R_S = 10 kΩ, T_A = 25°C Over Temperature		5	10 13	mV mV
$\Delta V_{OS}/\Delta T$	Average TC of Input Offset Voltage	R_S = 10 kΩ		10		μV/°C
I_{OS}	Input Offset Current	T_j = 25°C, (Notes 3, 4) $T_j \leq$ 70°C		25	100 4	pA nA
I_B	Input Bias Current	T_j = 25°C, (Notes 3, 4) $T_j \leq$ 70°C		50	200 8	pA nA
R_{IN}	Input Resistance	T_j = 25°C		10^{12}		Ω
A_{VOL}	Large Signal Voltage Gain	V_S = ±15V, T_A = 25°C V_O = ±10V, R_L = 2 kΩ Over Temperature	25 15	100		V/mV V/mV
V_O	Output Voltage Swing	V_S = ±15V, R_L = 10 kΩ	±12	±13.5		V
V_{CM}	Input Common-Mode Voltage Range	V_S = ±15V	±11	+15 −12		V V
CMRR	Common-Mode Rejection Ratio	$R_S \leq$ 10 kΩ	70	100		dB
PSRR	Supply Voltage Rejection Ratio	(Note 5)	70	100		dB
I_S	Supply Current			1.8	3.4	mA

AC Electrical Characteristics (Note 3)

Symbol	Parameter	Conditions	LF351			Units
			Min	Typ	Max	
SR	Slew Rate	$V_S = \pm 15V$, $T_A = 25°C$		13		$V/\mu s$
GBW	Gain Bandwidth Product	$V_S = \pm 15V$, $T_A = 25°C$		4		MHz
e_n	Equivalent Input Noise Voltage	$T_A = 25°C$, $R_S = 100\Omega$, $f = 1000$ Hz		25		$nV/\sqrt{Hz}$
i_n	Equivalent Input Noise Current	$T_j = 25°C$, $f = 1000$ Hz		0.01		$pA/\sqrt{Hz}$

Note 1: For operating at elevated temperature, the device must be derated based on the thermal resistance, θ_{JA}.

Note 2: Unless otherwise specified the absolute maximum negative input voltage is equal to the negative power supply voltage.

Note 3: These specifications apply for $V_S = \pm 15V$ and $0°C \leq T_A \leq +70°C$. V_{OS}, I_B and I_{OS} are measured at $V_{CM} = 0$.

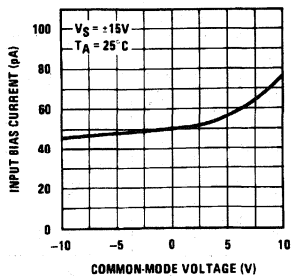
Note 4: The input bias currents are junction leakage currents which approximately double for every 10°C increase in the junction temperature, T_j. Due to the limited production test time, the input bias currents measured are correlated to junction temperature. In normal operation the junction temperature rises above the ambient temperature as a result of internal power dissipation, P_D. $T_j = T_A + \theta_{jA} P_D$ where θ_{jA} is the thermal resistance from junction to ambient. Use of a heat sink is recommended if input bias current is to be kept to a minimum.

Note 5: Supply voltage rejection ratio is measured for both supply magnitudes increasing or decreasing simultaneously in accordance with common practice. From $\pm 15V$ to $\pm 5V$.

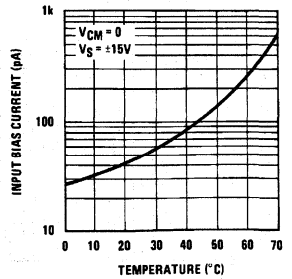
Note 6: Max. Power Dissipation is defined by the package characteristics. Operating the part near the Max. Power Dissipation may cause the part to operate outside guaranteed limits.

Typical Performance Characteristics

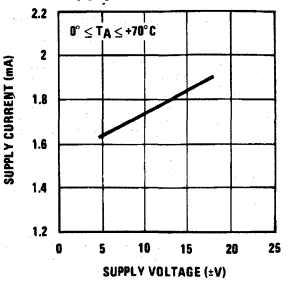
Input Bias Current



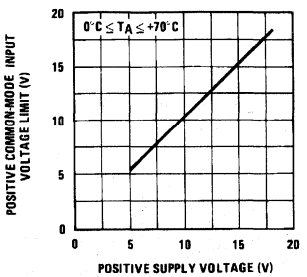
Input Bias Current



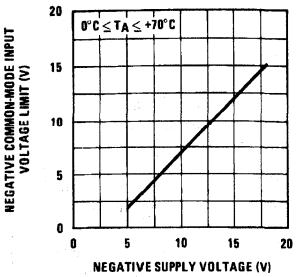
Supply Current



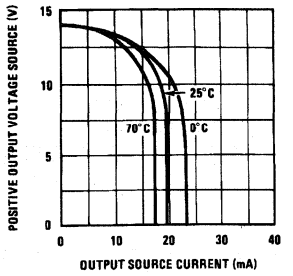
Positive Common-Mode Input Voltage Limit



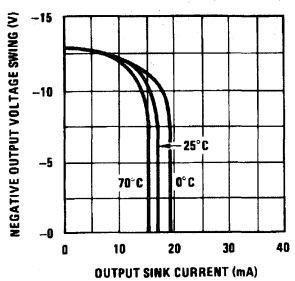
Negative Common-Mode Input Voltage Limit



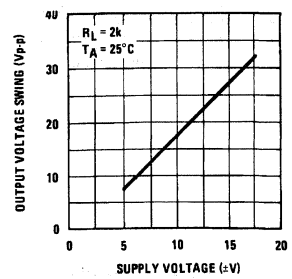
Positive Current Limit



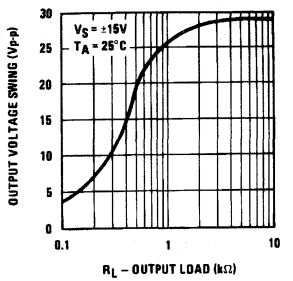
Negative Current Limit



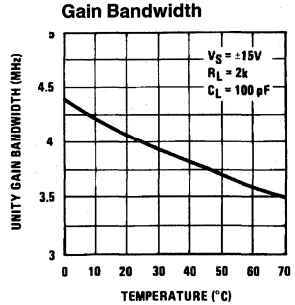
Voltage Swing



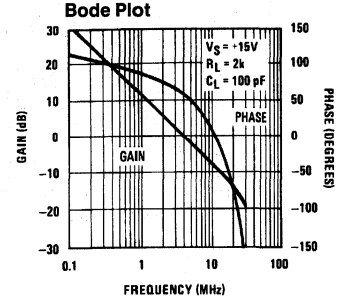
Output Voltage Swing



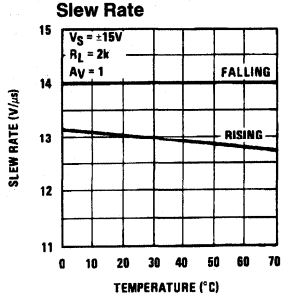
Gain Bandwidth



Bode Plot



Slew Rate



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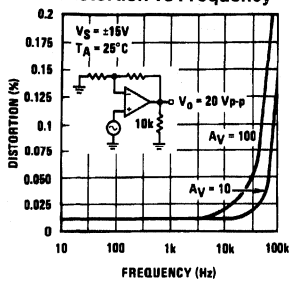
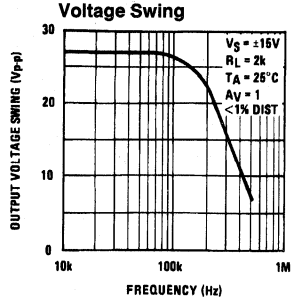
Typical Performance Characteristics (Continued)

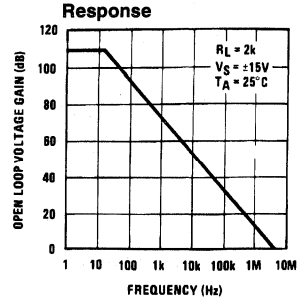
Distortion vs Frequency



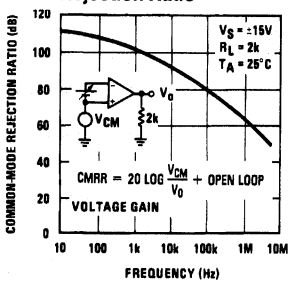
Undistorted Output Voltage Swing



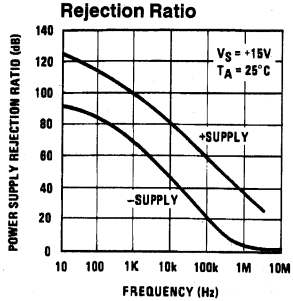
Open Loop Frequency Response



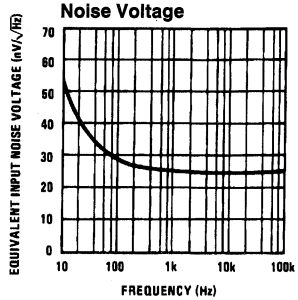
Common-Mode Rejection Ratio



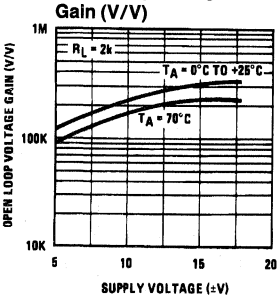
Power Supply Rejection Ratio



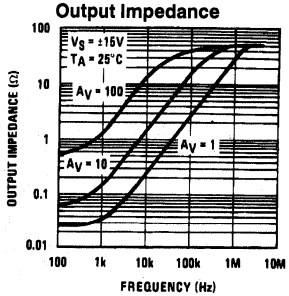
Equivalent Input Noise Voltage



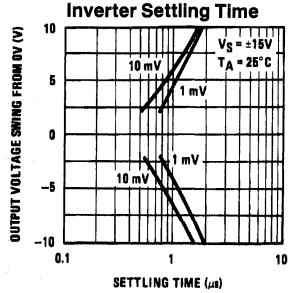
Open Loop Voltage Gain (V/V)



Output Impedance



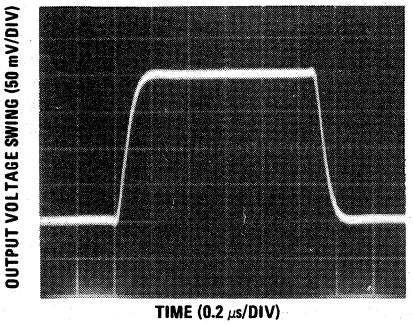
Inverter Settling Time



TL/H/5648–3

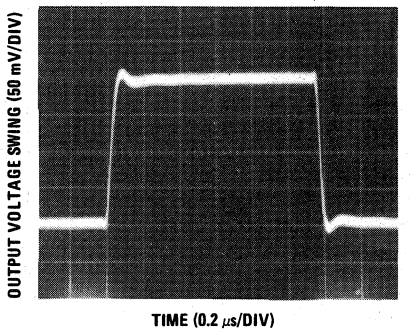
Pulse Response

Small Signal Inverting



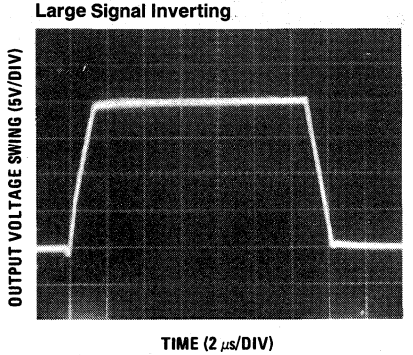
TL/H/5648–4

Small Signal Non-Inverting



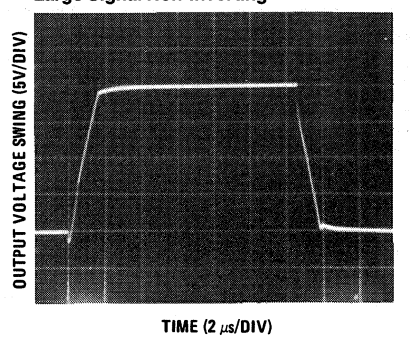
TL/H/5648–5

Large Signal Inverting



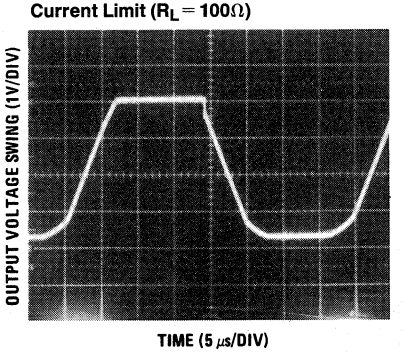
TL/H/5648–6

Large Signal Non-Inverting



TL/H/5648–7

Current Limit ($R_L = 100\Omega$)



TL/H/5648–8

Application Hints

The LF351 is an op amp with an internally trimmed input offset voltage and JFET input devices (BI-FET II™). These JFETs have large reverse breakdown voltages from gate to source and drain eliminating the need for clamps across the inputs. Therefore, large differential input voltages can easily be accommodated without a large increase in input current. The maximum differential input voltage is independent of the supply voltages. However, neither of the input voltages should be allowed to exceed the negative supply as this will cause large currents to flow which can result in a destroyed unit.

Exceeding the negative common-mode limit on either input will force the output to a high state, potentially causing a reversal of phase to the output.

Exceeding the negative common-mode limit on both inputs will force the amplifier output to a high state. In neither case does a latch occur since raising the input back within the

Application Hints (Continued)

common-mode range again puts the input stage and thus the amplifier in a normal operating mode.

Exceeding the positive common-mode limit on a single input will not change the phase of the output; however, if both inputs exceed the limit, the output of the amplifier will be forced to a high state.

The amplifier will operate with a common-mode input voltage equal to the positive supply; however, the gain bandwidth and slew rate may be decreased in this condition. When the negative common-mode voltage swings to within 3V of the negative supply, an increase in input offset voltage may occur.

The LF351 is biased by a zener reference which allows normal circuit operation on ±4V power supplies. Supply voltages less than these may result in lower gain bandwidth and slew rate.

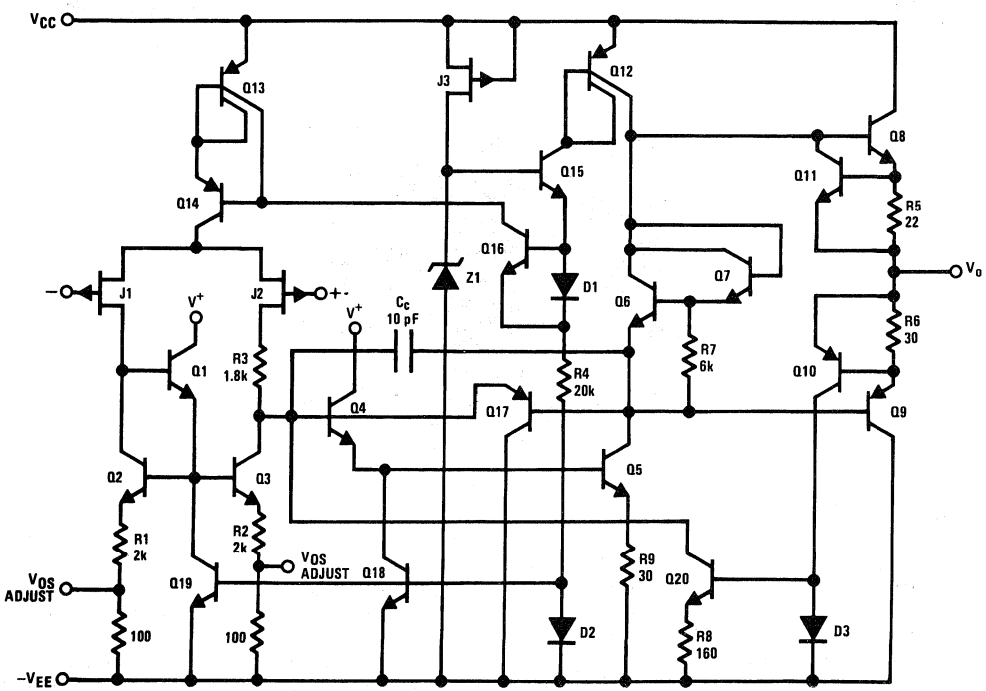
The LF351 will drive a 2 kΩ load resistance to ±10V over the full temperature range of 0°C to +70°C. If the amplifier is forced to drive heavier load currents, however, an increase in input offset voltage may occur on the negative voltage swing and finally reach an active current limit on both positive and negative swings.

Precautions should be taken to ensure that the power supply for the integrated circuit never becomes reversed in polarity or that the unit is not inadvertently installed backwards in a socket as an unlimited current surge through the resulting forward diode within the IC could cause fusing of the internal conductors and result in a destroyed unit.

As with most amplifiers, care should be taken with lead dress, component placement and supply decoupling in order to ensure stability. For example, resistors from the output to an input should be placed with the body close to the input to minimize "pick-up" and maximize the frequency of the feedback pole by minimizing the capacitance from the input to ground.

A feedback pole is created when the feedback around any amplifier is resistive. The parallel resistance and capacitance from the input of the device (usually the inverting input) to AC ground set the frequency of the pole. In many instances the frequency of this pole is much greater than the expected 3 dB frequency of the closed loop gain and consequently there is negligible effect on stability margin. However, if the feedback pole is less than approximately 6 times the expected 3 dB frequency a lead capacitor should be placed from the output to the input of the op amp. The value of the added capacitor should be such that the RC time constant of this capacitor and the resistance it parallels is greater than or equal to the original feedback pole time constant.

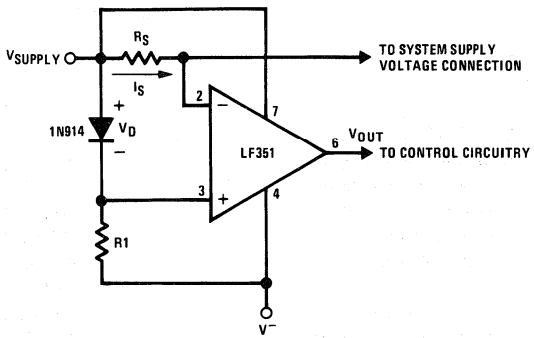
Detailed Schematic



TL/H/5648–9

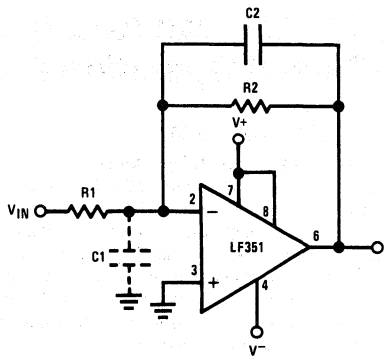
Typical Applications

Supply Current Indicator/Limiter



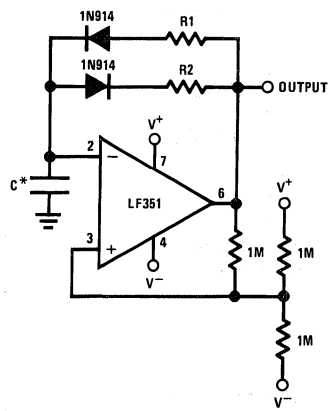
• V_{OUT} switches high when $R_S I_S > V_D$

Hi-Z_{IN} Inverting Amplifier



Parasitic input capacitance C1 ≅ (3 pF for LF351 plus any additional layout capacitance) interacts with feedback elements and creates undesirable high frequency pole. To compensate, add C2 such that: R2C2 ≅ R1C1.

Ultra-Low (or High) Duty Cycle Pulse Generator



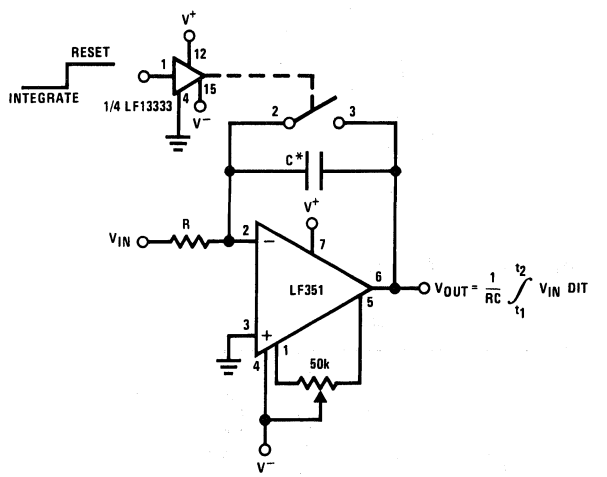
• $t_{OUTPUT\ HIGH} \approx R1C\ \ell n \frac{4.8 - 2V_S}{4.8 - V_S}$

• $t_{OUTPUT\ LOW} \approx R2C\ \ell n \frac{2V_S - 7.8}{V_S - 7.8}$

where $V_S = V^+ + |V^-|$

*low leakage capacitor

Long Time Integrator



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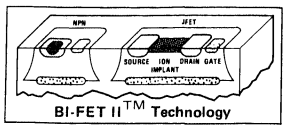
*Low leakage capacitor

• 50k pot used for less sensitive V_{OS} adjust

National Semiconductor



LF353 Wide Bandwidth Dual JFET Input Operational Amplifier

General Description

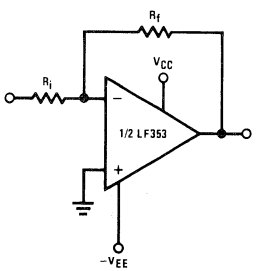
These devices are low cost, high speed, dual JFET input operational amplifiers with an internally trimmed input offset voltage (BI-FET II™ technology). They require low supply current yet maintain a large gain bandwidth product and fast slew rate. In addition, well matched high voltage JFET input devices provide very low input bias and offset currents. The LF353 is pin compatible with the standard LM1558 allowing designers to immediately upgrade the overall performance of existing LM1558 and LM358 designs.

These amplifiers may be used in applications such as high speed integrators, fast D/A converters, sample and hold circuits and many other circuits requiring low input offset voltage, low input bias current, high input impedance, high slew rate and wide bandwidth. The devices also exhibit low noise and offset voltage drift.

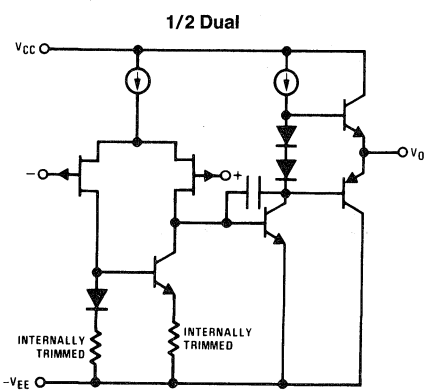
Features

■ Internally trimmed offset voltage	10 mV
■ Low input bias current	50pA
■ Low input noise voltage	16 nV/$\sqrt{Hz}$
■ Low input noise current	0.01 pA/$\sqrt{Hz}$
■ Wide gain bandwidth	4 MHz
■ High slew rate	13 V/μs
■ Low supply current	3.6 mA
■ High input impedance	$10^{12}\Omega$
■ Low total harmonic distortion $A_V = 10$, $R_L = 10k$, $V_O = 20Vp-p$, BW = 20 Hz-20 kHz	<0.02%
■ Low 1/f noise corner	50 Hz
■ Fast settling time to 0.01%	2 μs

Typical Connection

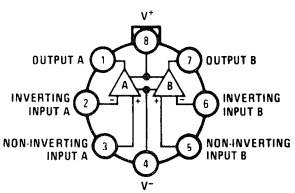


Simplified Schematic



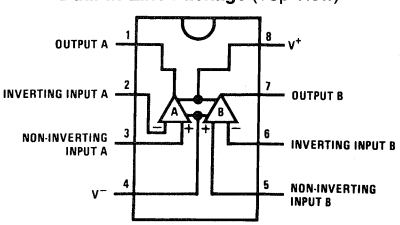
Connection Diagrams

Metal Can Package (Top View)



Order Number LF353H
See NS Package Number H08B

Dual-In-Line Package (Top View)



Order Number LF353M or LF353N
See NS Package Number M08A or N08E

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Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	±18V
Power Dissipation	(Note 1)
Operating Temperature Range	0°C to +70°C
T_j(MAX)	150°C
Differential Input Voltage	±30V
Input Voltage Range (Note 2)	±15V
Output Short Circuit Duration	Continuous
Storage Temperature Range	−65°C to +150°C
Lead Temp. (Soldering, 10 sec.)	260°C
Soldering Information	
Dual-In-Line Package	
Soldering (10 sec.)	260°C
Small Outline Package	
Vapor Phase (60 sec.)	215°C
Infrared (15 sec.)	220°C

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

ESD Tolerance (Note 7)	1700V
θ_{JA} M Package	TBD

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	LF353			Units
			Min	Typ	Max	
V_{OS}	Input Offset Voltage	R_S=10kΩ, T_A=25°C Over Temperature		5	10 13	mV mV
$\Delta V_{OS}/\Delta T$	Average TC of Input Offset Voltage	R_S=10 kΩ		10		µV/°C
I_{OS}	Input Offset Current	T_j=25°C, (Notes 4, 5) $T_j \leq 70°C$		25	100 4	pA nA
I_B	Input Bias Current	T_j=25°C, (Notes 4, 5) $T_j \leq 70°C$		50	200 8	pA nA
R_{IN}	Input Resistance	T_j=25°C		10^{12}		Ω
A_{VOL}	Large Signal Voltage Gain	V_S=±15V, T_A=25°C V_O=±10V, R_L=2 kΩ Over Temperature	25 15	100		V/mV V/mV
V_O	Output Voltage Swing	V_S=±15V, R_L=10kΩ	±12	±13.5		V
V_{CM}	Input Common-Mode Voltage Range	V_S=±15V	±11	+15 −12		V V
CMRR	Common-Mode Rejection Ratio	$R_S \leq$ 10kΩ	70	100		dB
PSRR	Supply Voltage Rejection Ratio	(Note 6)	70	100		dB
I_S	Supply Current			3.6	6.5	mA

AC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	LF353			Units
			Min	Typ	Max	
	Amplifier to Amplifier Coupling	T_A=25°C, f=1 Hz−20 kHz (Input Referred)		−120		dB
SR	Slew Rate	V_S=±15V, T_A=25°C	8.0	13		V/µs
GBW	Gain Bandwidth Product	V_S=±15V, T_A=25°C	2.7	4		MHz
e_n	Equivalent Input Noise Voltage	T_A=25°C, R_S=100Ω, f=1000 Hz		25		nV/$\sqrt{Hz}$
i_n	Equivalent Input Noise Current	T_j=25°C, f=1000 Hz		0.01		pA/$\sqrt{Hz}$

Note 1: For operating at elevated temperatures, the device must be derated based on a thermal resistance of 115°C/W typ junction to ambient for the N package, and 158°C/W typ junction to ambient for the H package.

Note 2: Unless otherwise specified the absolute maximum negative input voltage is equal to the negative power supply voltage.

Note 3: The power dissipation limit, however, cannot be exceeded.

Note 4: These specifications apply for V_S=±15V and 0°C≤T_A≤+70°C. V_{OS}, I_B and I_{OS} are measured at V_{CM}=0.

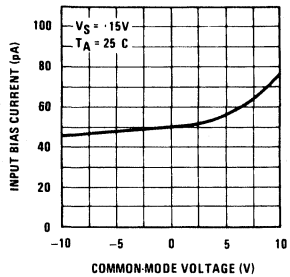
Note 5: The input bias currents are junction leakage currents which approximately double for every 10°C increase in the junction temperature, T_j. Due to the limited production test time, the input bias currents measured are correlated to junction temperature. In normal operation the junction temperature rises above the ambient temperature as a result of internal power dissipation, P_D. $T_j=T_A+\theta_{jA} P_D$ where θ_{jA} is the thermal resistance from junction to ambient. Use of a heat sink is recommended if input bias current is to be kept to a minimum.

Note 6: Supply voltage rejection ratio is measured for both supply magnitudes increasing or decreasing simultaneously in accordance with common practice. V_S = ±6V to ±15V.

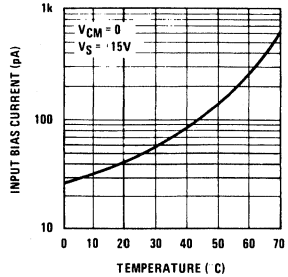
Note 7: Human body model, 1.5 kΩ in series with 100 pF.

Typical Performance Characteristics

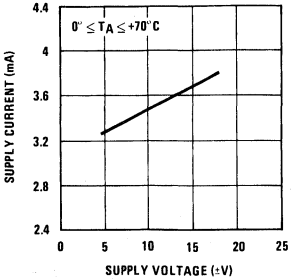
Input Bias Current



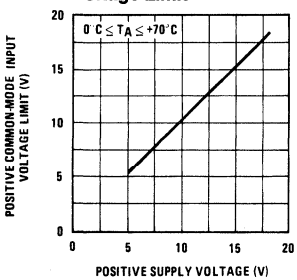
Input Bias Current



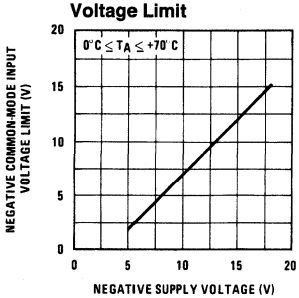
Supply Current



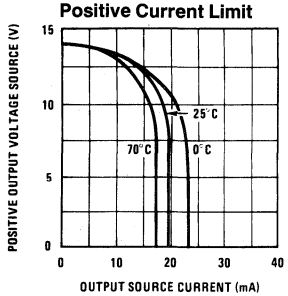
Positive Common-Mode Input Voltage Limit



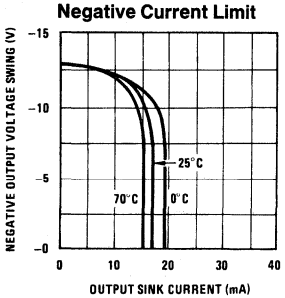
Negative Common-Mode Input Voltage Limit



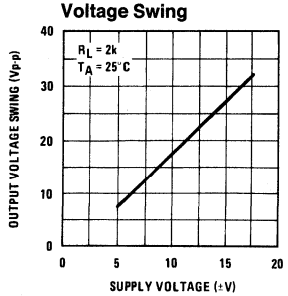
Positive Current Limit



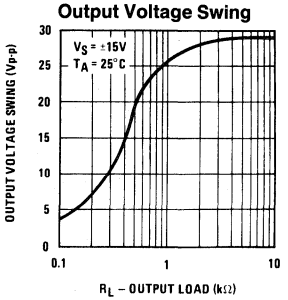
Negative Current Limit



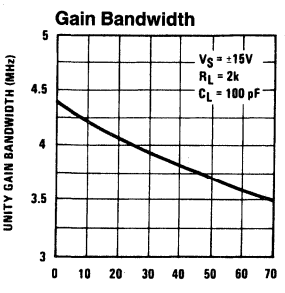
Voltage Swing



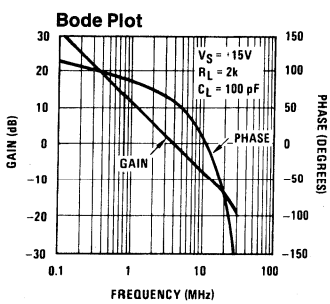
Output Voltage Swing



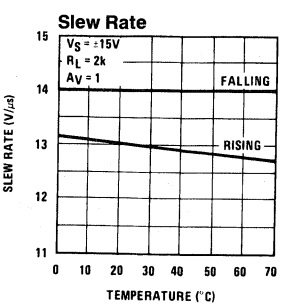
Gain Bandwidth



Bode Plot



Slew Rate



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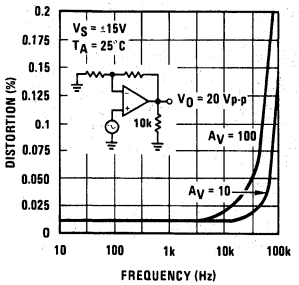
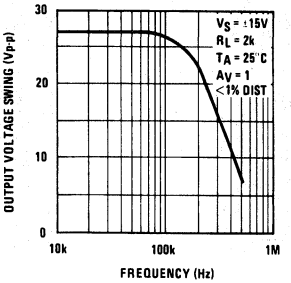
Typical Performance Characteristics (Continued)

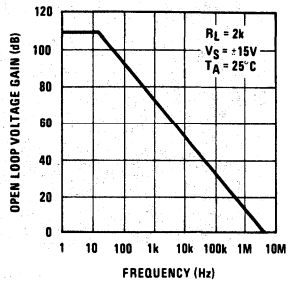
Distortion vs Frequency



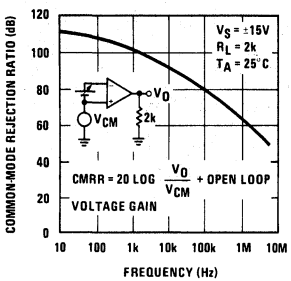
Undistorted Output Voltage Swing



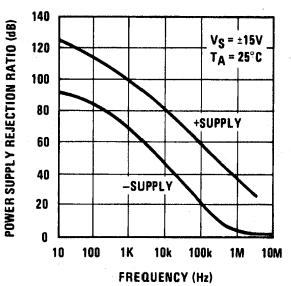
Open Loop Frequency Response



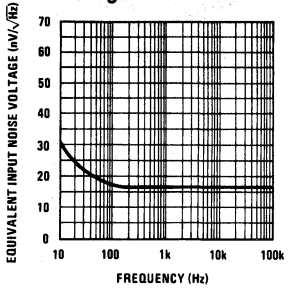
Common-Mode Rejection Ratio



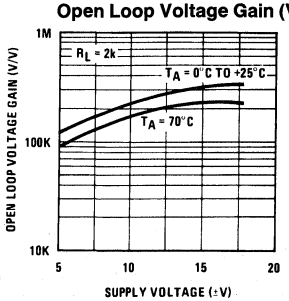
Power Supply Rejection Ratio



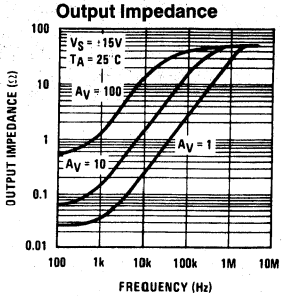
Equivalent Input Noise Voltage



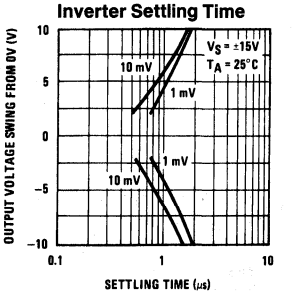
Open Loop Voltage Gain (V/V)



Output Impedance



Inverter Settling Time



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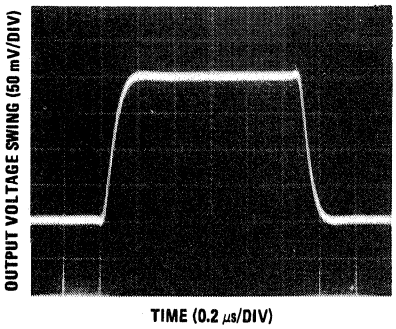
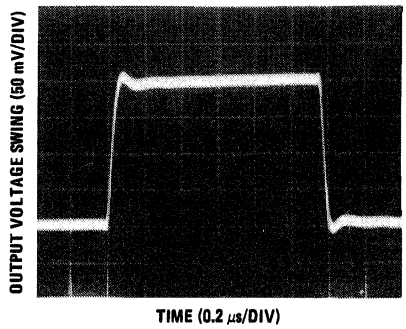
Pulse Response

Small Signaling Inverting



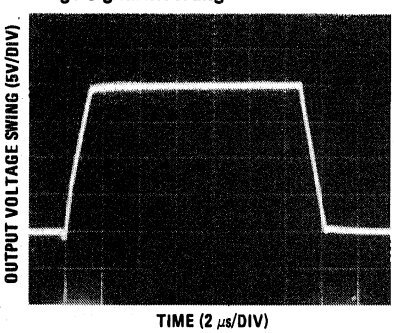
TL/H/5649-4

Small Signal Non-Inverting



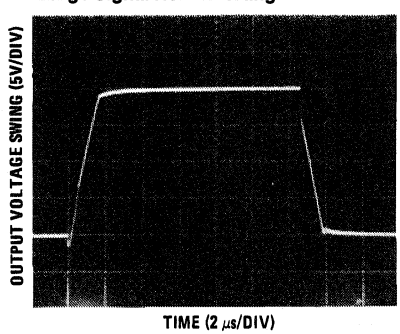
TL/H/5649-5

Large Signal Inverting



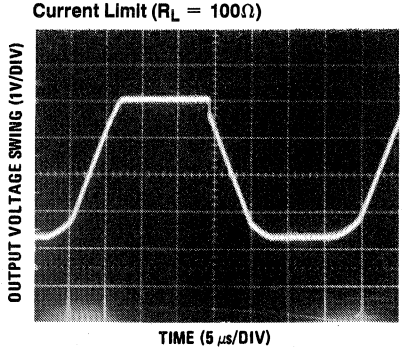
TL/H/5649-6

Large Signal Non-Inverting



TL/H/5649-7

Current Limit (R_L = 100Ω)



TL/H/5649-8

Application Hints

These devices are op amps with an internally trimmed input offset voltage and JFET input devices (BI-FET II). These JFETs have large reverse breakdown voltages from gate to source and drain eliminating the need for clamps across the inputs. Therefore, large differential input voltages can easily be accommodated without a large increase in input current. The maximum differential input voltage is independent of the supply voltages. However, neither of the input voltages should be allowed to exceed the negative supply as this will cause large currents to flow which can result in a destroyed unit.

Exceeding the negative common-mode limit on either input will force the output to a high state, potentially causing a reversal of phase to the output. Exceeding the negative common-mode limit on both inputs will force the amplifier output to a high state. In neither case does a latch occur since raising the input back within the common-mode range again puts the input stage and thus the amplifier in a normal operating mode.

Application Hints (Continued)

Exceeding the positive common-mode limit on a single input will not change the phase of the output; however, if both inputs exceed the limit, the output of the amplifier will be forced to a high state.

The amplifiers will operate with a common-mode input voltage equal to the positive supply; however, the gain bandwidth and slew rate may be decreased in this condition. When the negative common-mode voltage swings to within 3V of the negative supply, an increase in input offset voltage may occur.

Each amplifier is individually biased by a zener reference which allows normal circuit operation on ±6V power supplies. Supply voltages less than these may result in lower gain bandwidth and slew rate.

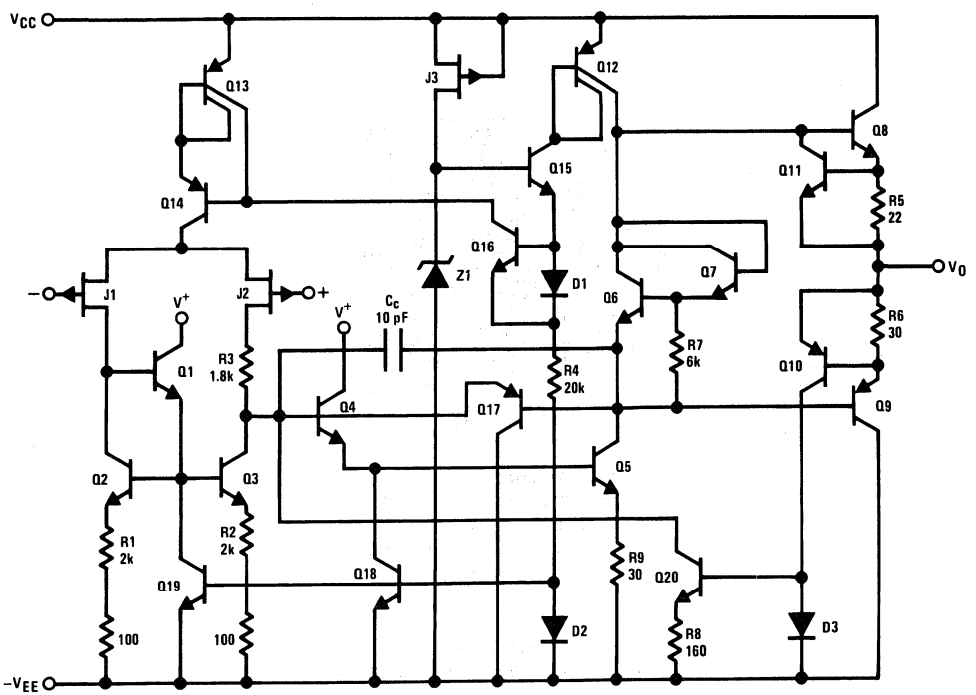
The amplifiers will drive a 2 kΩ load resistance to ±10V over the full temperature range of 0°C to +70°C. If the amplifier is forced to drive heavier load currents, however, an increase in input offset voltage may occur on the negative voltage swing and finally reach an active current limit on both positive and negative swings.

Precautions should be taken to ensure that the power supply for the integrated circuit never becomes reversed in polarity or that the unit is not inadvertently installed backwards in a socket as an unlimited current surge through the resulting forward diode within the IC could cause fusing of the internal conductors and result in a destroyed unit.

As with most amplifiers, care should be taken with lead dress, component placement and supply decoupling in order to ensure stability. For example, resistors from the output to an input should be placed with the body close to the input to minimize "pick-up" and maximize the frequency of the feedback pole by minimizing the capacitance from the input to ground.

A feedback pole is created when the feedback around any amplifier is resistive. The parallel resistance and capacitance from the input of the device (usually the inverting input) to AC ground set the frequency of the pole. In many instances the frequency of this pole is much greater than the expected 3 dB frequency of the closed loop gain and consequently there is negligible effect on stability margin. However, if the feedback pole is less than approximately 6 times the expected 3 dB frequency a lead capacitor should be placed from the output to the input of the op amp. The value of the added capacitor should be such that the RC time constant of this capacitor and the resistance it parallels is greater than or equal to the original feedback pole time constant.

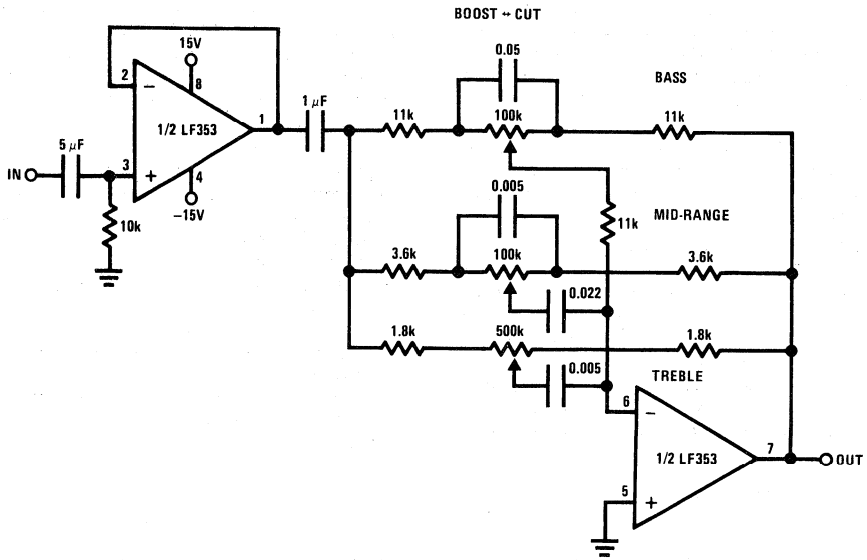
Detailed Schematic

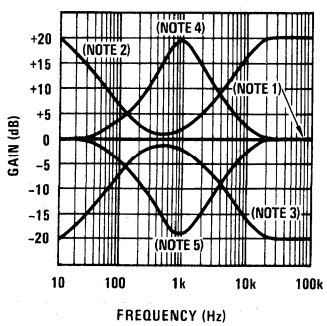


TL/H/5649–9

Typical Applications

Three-Band Active Tone Control





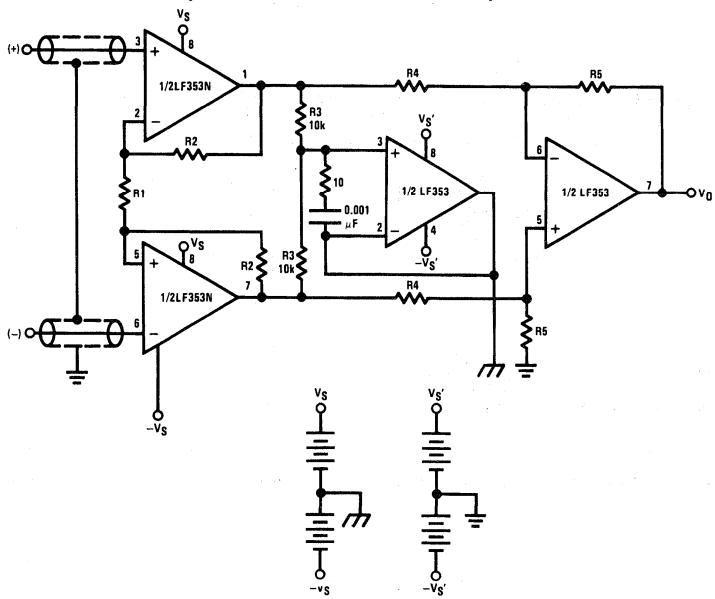
TL/H/5649–10

Note 1: All controls flat.
Note 2: Bass and treble boost, mid flat.
Note 3: Bass and treble cut, mid flat.
Note 4: Mid boost, bass and treble flat.
Note 5: Mid cut, bass and treble flat.

- All potentiometers are linear taper
- Use the LF347 Quad for stereo applications

Typical Applications (Continued)

Improved CMRR Instrumentation Amplifier



$$A_V = \left(\frac{2R2}{R1} + 1\right) \frac{R5}{R4}$$

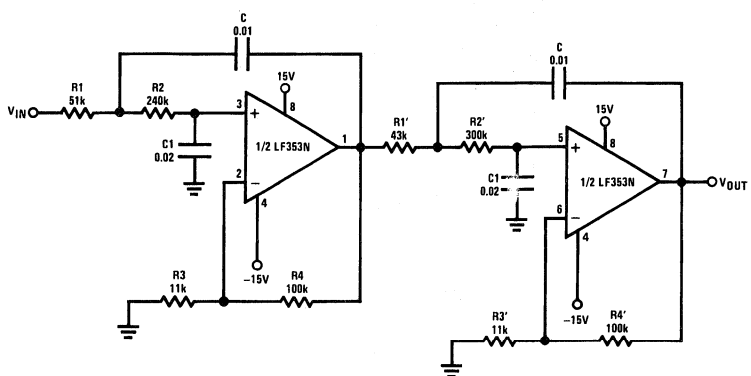
and are separate isolated grounds

Matching of R2's, R4's and R5's control CMRR

With A_{V_T} = 1400, resistor matching = 0.01%: CMRR = 136 dB

- Very high input impedance
- Super high CMRR

Fourth Order Low Pass Butterworth Filter

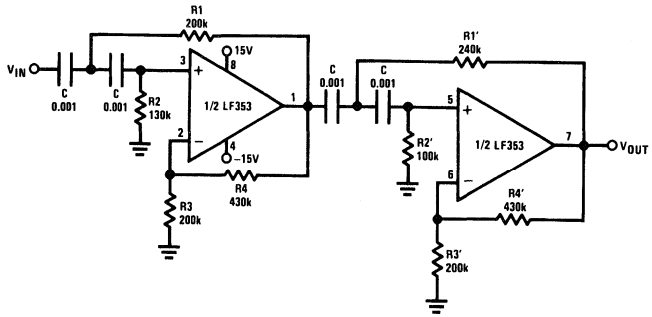


- Corner frequency (f_c) = $\sqrt{\frac{1}{R1R2CC1}} \cdot \frac{1}{2\pi} = \sqrt{\frac{1}{R1'R2'CC1}} \cdot \frac{1}{2\pi}$
- Passband gain (H_O) = (1 + R4/R3) (1 + R4'/R3')
- First stage Q = 1.31
- Second stage Q = 0.541
- Circuit shown uses nearest 5% tolerance resistor values for a filter with a corner frequency of 100 Hz and a passband gain of 100
- Offset nulling necessary for accurate DC performance

TL/H/5649–11

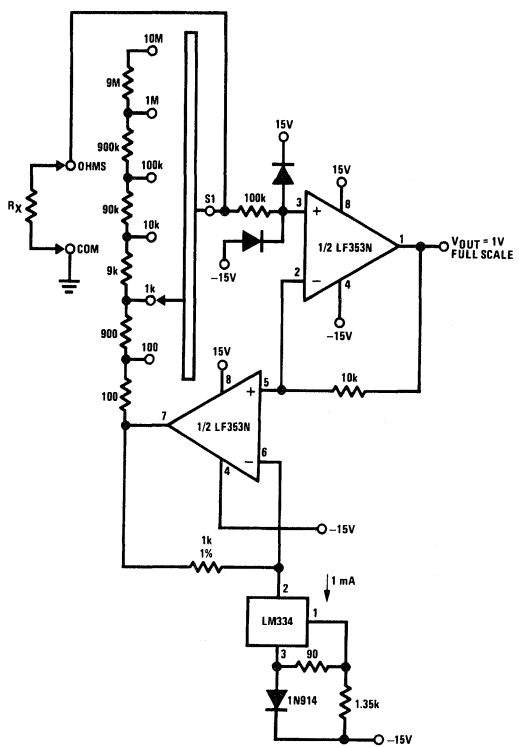
Typical Applications (Continued)

Fourth Order High Pass Butterworth Filter



- Corner frequency (f_c) $= \sqrt{\frac{1}{R1R2C^2}} \cdot \frac{1}{2\pi} = \sqrt{\frac{1}{R1'R2'C^2}} \cdot \frac{1}{2\pi}$
- Passband gain (H_O) $= (1 + R4/R3)\ (1 + R4'/R3')$
- First stage Q = 1.31
- Second stage Q = 0.541
- Circuit shown uses closest 5% tolerance resistor values for a filter with a corner frequency of 1 kHz and a passband gain of 10.

Ohms to Volts Converter

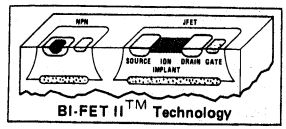


TL/H/5649–13

$$V_O = \frac{1V}{R_{LADDER}} \times R_X$$

Where R_{LADDER} is the resistance from switch S1 pole to pin 7 of the LF353.

National Semiconductor



LF411 Low Offset, Low Drift JFET Input Operational Amplifier

General Description

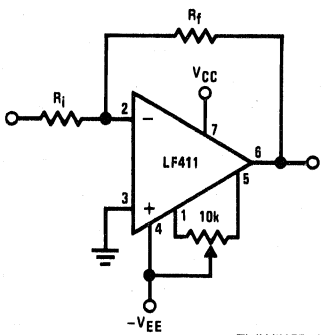
These devices are low cost, high speed, JFET input operational amplifiers with very low input offset voltage and guaranteed input offset voltage drift. They require low supply current yet maintain a large gain bandwidth product and fast slew rate. In addition, well matched high voltage JFET input devices provide very low input bias and offset currents. The LF411 is pin compatible with the standard LM741 allowing designers to immediately upgrade the overall performance of existing designs.

These amplifiers may be used in applications such as high speed integrators, fast D/A converters, sample and hold circuits and many other circuits requiring low input offset voltage and drift, low input bias current, high input impedance, high slew rate and wide bandwidth.

Features

■ Internally trimmed offset voltage	0.5 mV(max)
■ Input offset voltage drift	10 μV/°C(max)
■ Low input bias current	50 pA
■ Low input noise current	0.01 pA/√Hz
■ Wide gain bandwidth	3 MHz(min)
■ High slew rate	10V/μs(min)
■ Low supply current	1.8 mA
■ High input impedance	$10^{12}\Omega$
■ Low total harmonic distortion $A_V = 10$, $R_L = 10k$, $V_O = 20$ Vp-p, BW = 20 Hz–20 kHz	<0.02%
■ Low 1/f noise corner	50 Hz
■ Fast settling time to 0.01%	2 μs

Typical Connection



TL/H/5655–1

Ordering Information

LF411XYZ

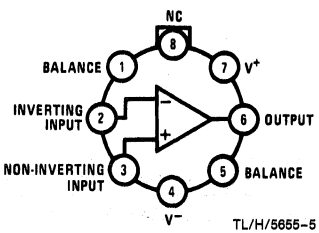
X indicates electrical grade

Y indicates temperature range
"M" for military
"C" for commercial

Z indicates package type
"H" or "N"

Connection Diagrams

Metal Can Package



TL/H/5655–5

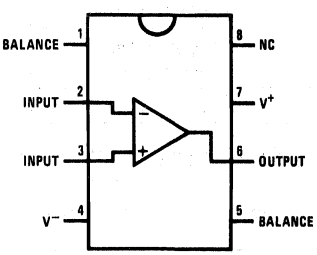
Top View

Note: Pin 4 connected to case.

Order Number LF411AMH, LF411MH, LF411ACH, LF411CH or LF411MH/883*

See NS Package Number H08B

Dual-In-Line Package



TL/H/5655–7

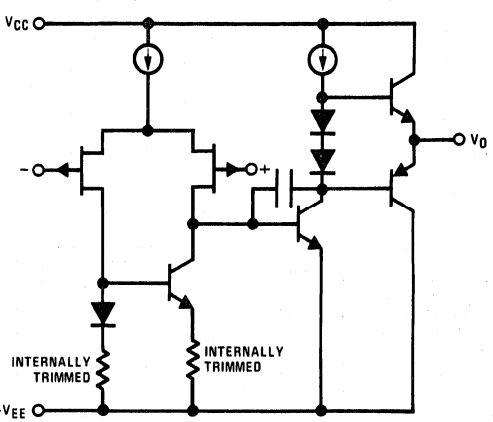
Top View

Order Number LF411ACN, LF411CN or LF411MJ/883*

See NS Package Number N08E or J08A

*Available per JM38510/11904

Simplified Schematic



TL/H/5655–6

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications. (Note 8)

	LF411A	LF411
Supply Voltage	±22V	±18V
Differential Input Voltage	±38V	±30V
Input Voltage Range (Note 1)	±19V	±15V
Output Short Circuit Duration	Continuous	Continuous

	H Package	N Package
Power Dissipation (Notes 2 and 9)	670 mW	670 mW
$T_j$max	150°C	115°C
θ_jA	162°C/W (Still Air) 65°C/W (400 LF/min Air Flow)	120°C/W
θ_jC	20°C/W	
Operating Temp. Range	(Note 3)	(Note 3)
Storage Temp. Range	$-65°C \le T_A \le 150°C$	$-65°C \le T_A \le 150°C$
Lead Temp. (Soldering, 10 sec.)	260°C	260°C
ESD Tolerance		Rating to be determined.

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions		LF411A			LF411			Units
				Min	Typ	Max	Min	Typ	Max	
V_{OS}	Input Offset Voltage	$R_S = 10\ k\Omega$, $T_A = 25°C$			0.3	0.5		0.8	2.0	mV
$\Delta V_{OS}/\Delta T$	Average TC of Input Offset Voltage	$R_S = 10\ k\Omega$ (Note 5)			7	10		7	20 (Note 5)	µV/°C
I_{OS}	Input Offset Current	$V_S = \pm 15V$ (Notes 4, 6)	$T_j = 25°C$		25	100		25	100	pA
			$T_j = 70°C$			2			2	nA
			$T_j = 125°C$			25			25	nA
I_B	Input Bias Current	$V_S = \pm 15V$ (Notes 4, 6)	$T_j = 25°C$		50	200		50	200	pA
			$T_j = 70°C$			4			4	nA
			$T_j = 125°C$			50			50	nA
R_{IN}	Input Resistance	$T_j = 25°C$			10^{12}			10^{12}		Ω
A_{VOL}	Large Signal Voltage Gain	$V_S = \pm 15V$, $V_O = \pm 10V$, $R_L = 2k$, $T_A = 25°C$		50	200		25	200		V/mV
		Over Temperature		25	200		15	200		V/mV
V_O	Output Voltage Swing	$V_S = \pm 15V$, $R_L = 10k$		±12	±13.5		±12	±13.5		V
V_{CM}	Input Common-Mode Voltage Range			±16	+19.5		±11	+14.5		V
					−16.5			−11.5		V
CMRR	Common-Mode Rejection Ratio	$R_S \le 10k$		80	100		70	100		dB
PSRR	Supply Voltage Rejection Ratio	(Note 7)		80	100		70	100		dB
I_S	Supply Current				1.8	2.8		1.8	3.4	mA

AC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	LF411A			LF411			Units
			Min	Typ	Max	Min	Typ	Max	
SR	Slew Rate	$V_S = \pm 15V$, $T_A = 25°C$	10	15		8	15		V/µs
GBW	Gain-Bandwidth Product	$V_S = \pm 15V$, $T_A = 25°C$	3	4		2.7	4		MHz
e_n	Equivalent Input Noise Voltage	$T_A = 25°C$, $R_S = 100\Omega$, f = 1 kHz		25			25		$nV/\sqrt{Hz}$
i_n	Equivalent Input Noise Current	$T_A = 25°C$, f = 1 kHz		0.01			0.01		$pA/\sqrt{Hz}$

Note 1: Unless otherwise specified the absolute maximum negative input voltage is equal to the negative power supply voltage.

Note 2: For operating at elevated temperature, these devices must be derated based on a thermal resistance of θ_jA.

Note 3: These devices are available in both the commercial temperature range $0°C \leq T_A \leq 70°C$ and the military temperature range $-55°C \leq T_A \leq 125°C$. The temperature range is designated by the position just before the package type in the device number. A "C" indicates the commercial temperature range and an "M" indicates the military temperature range. The military temperature range is available in "H" package only.

Note 4: Unless otherwise specified, the specifications apply over the full temperature range and for $V_S = \pm 20V$ for the LF411A and for $V_S = \pm 15V$ for the LF411. V_{OS}, I_B, and I_{OS} are measured at $V_{CM} = 0$.

Note 5: The LF411A is 100% tested to this specification. The LF411 is sample tested to insure at least 90% of the units meet this specification.

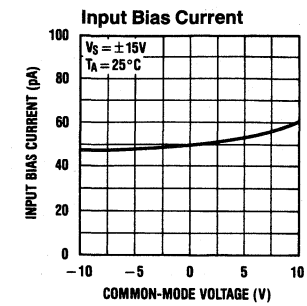
Note 6: The input bias currents are junction leakage currents which approximately double for every 10°C increase in the junction temperature, T_j. Due to limited production test time, the input bias currents measured are correlated to junction temperature. In normal operation the junction temperature rises above the ambient temperature as a result of internal power dissipation, P_D. $T_j = T_A + \theta_{jA} P_D$ where θ_{jA} is the thermal resistance from junction to ambient. Use of a heat sink is recommended if input bias current is to be kept to a minimum.

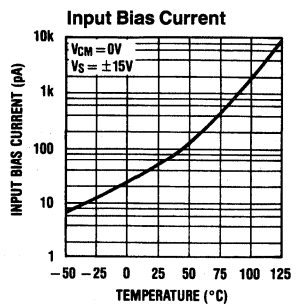
Note 7: Supply voltage rejection ratio is measured for both supply magnitudes increasing or decreasing simultaneously in accordance with common practice, from $\pm 15V$ to $\pm 5V$ for the LF411 and from $\pm 20V$ to $\pm 5V$ for the LF411A.

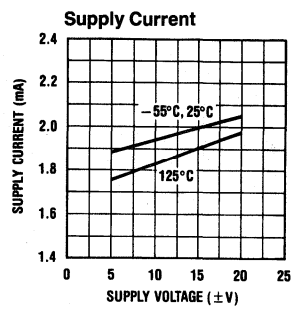
Note 8: RETS 411X for LF411MH and LF411MJ military specifications.

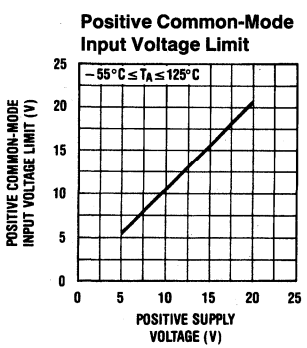
Note 9: Max. Power Dissipation is defined by the package characteristics. Operating the part near the Max. Power Dissipation may cause the part to operate outside guaranteed limits.

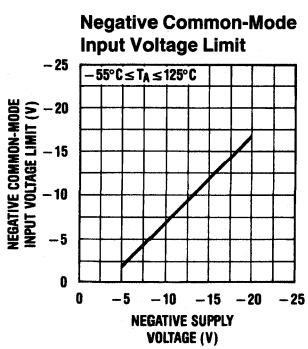
Typical Performance Characteristics

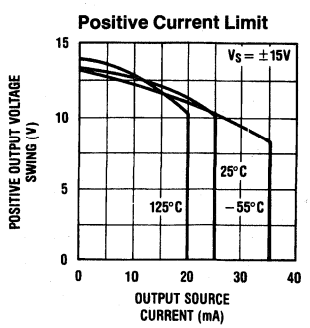


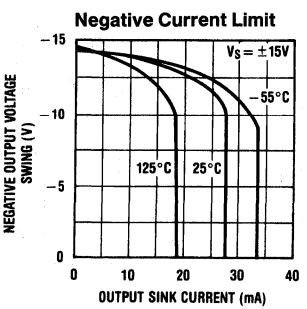


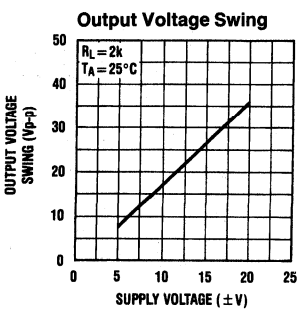


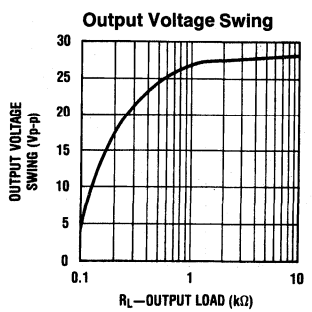








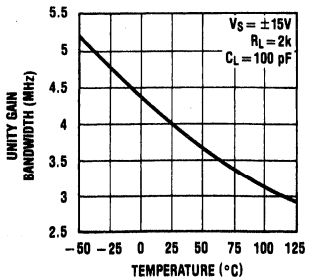




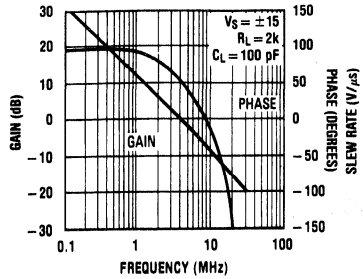
TL/H/5655–2

Typical Performance Characteristics (Continued)

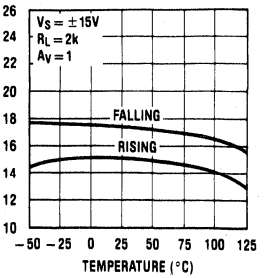
Gain Bandwidth



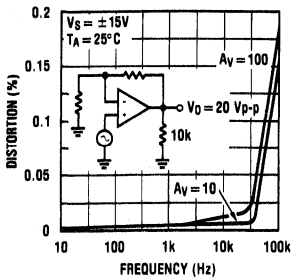
Bode Plot



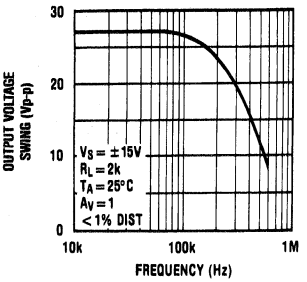
Slew Rate



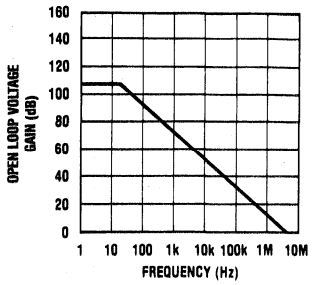
Distortion vs Frequency



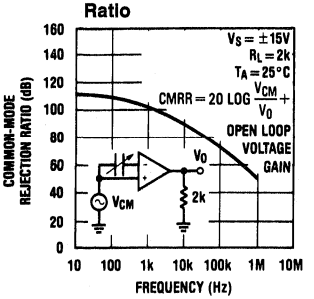
Undistorted Output Voltage Swing



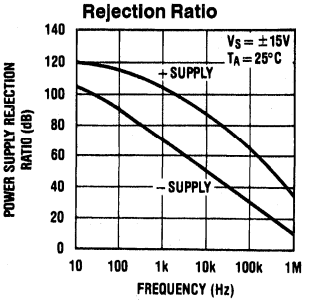
Open Loop Frequency Response



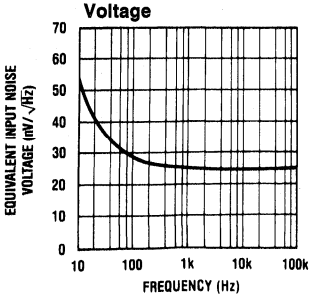
Common-Mode Rejection Ratio



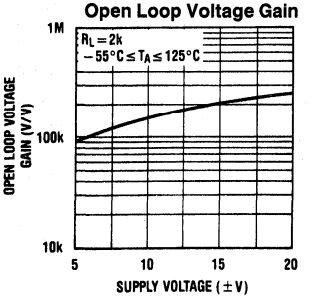
Power Supply Rejection Ratio



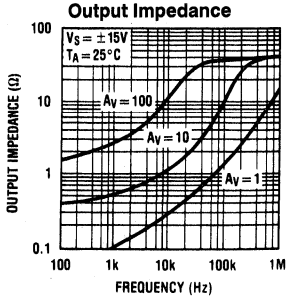
Equivalent Input Noise Voltage



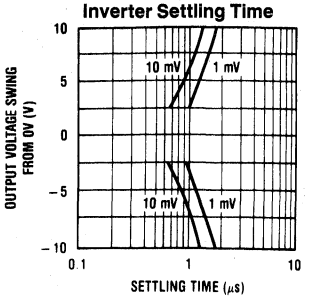
Open Loop Voltage Gain



Output Impedance



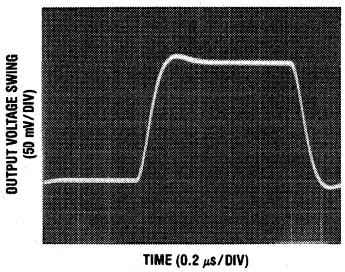
Inverter Settling Time



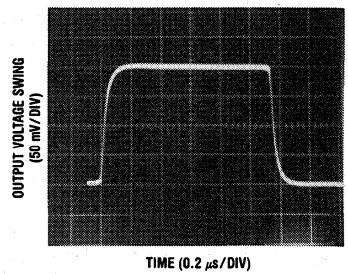
TL/H/5655–3

Pulse Response $R_L = 2\,k\Omega$, C_L 10 pF

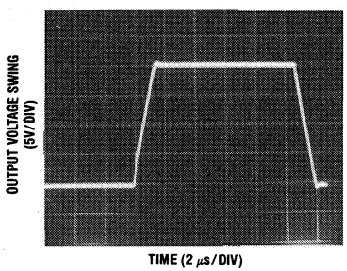
Small Signal Inverting



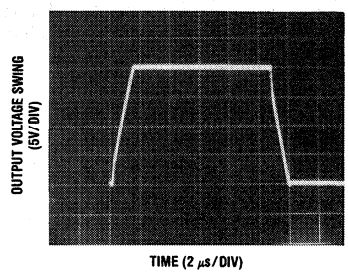
Small Signal Non-Inverting



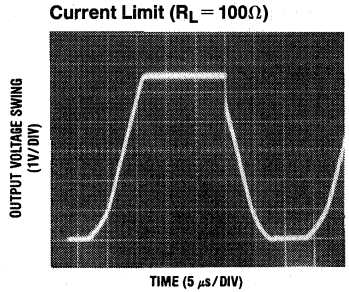
Large Signal Inverting



Large Signal Non-Inverting



Current Limit ($R_L = 100\Omega$)



TL/H/5655–4

Application Hints

The LF411 series of internally trimmed JFET input op amps (BI-FET II™) provide very low input offset voltage and guaranteed input offset voltage drift. These JFETs have large reverse breakdown voltages from gate to source and drain eliminating the need for clamps across the inputs. Therefore, large differential input voltages can easily be accommodated without a large increase in input current. The maximum differential input voltage is independent of the supply voltages. However, neither of the input voltages should be allowed to exceed the negative supply as this will cause large currents to flow which can result in a destroyed unit.

Exceeding the negative common-mode limit on either input will force the output to a high state, potentially causing a reversal of phase to the output. Exceeding the negative common-mode limit on both inputs will force the amplifier output to a high state. In neither case does a latch occur since raising the input back within the common-mode range again puts the input stage and thus the amplifier in a normal operating mode.

Exceeding the positive common-mode limit on a single input will not change the phase of the output; however, if both inputs exceed the limit, the output of the amplifier may be forced to a high state.

Application Hints (Continued)

The amplifier will operate with a common-mode input voltage equal to the positive supply; however, the gain bandwidth and slew rate may be decreased in this condition. When the negative common-mode voltage swings to within 3V of the negative supply, an increase in input offset voltage may occur.

The LF411 is biased by a zener reference which allows normal circuit operation on ±4.5V power supplies. Supply voltages less than these may result in lower gain bandwidth and slew rate.

The LF411 will drive a 2 kΩ load resistance to ±10V over the full temperature range. If the amplifier is forced to drive heavier load currents, however, an increase in input offset voltage may occur on the negative voltage swing and finally reach an active current limit on both positive and negative swings.

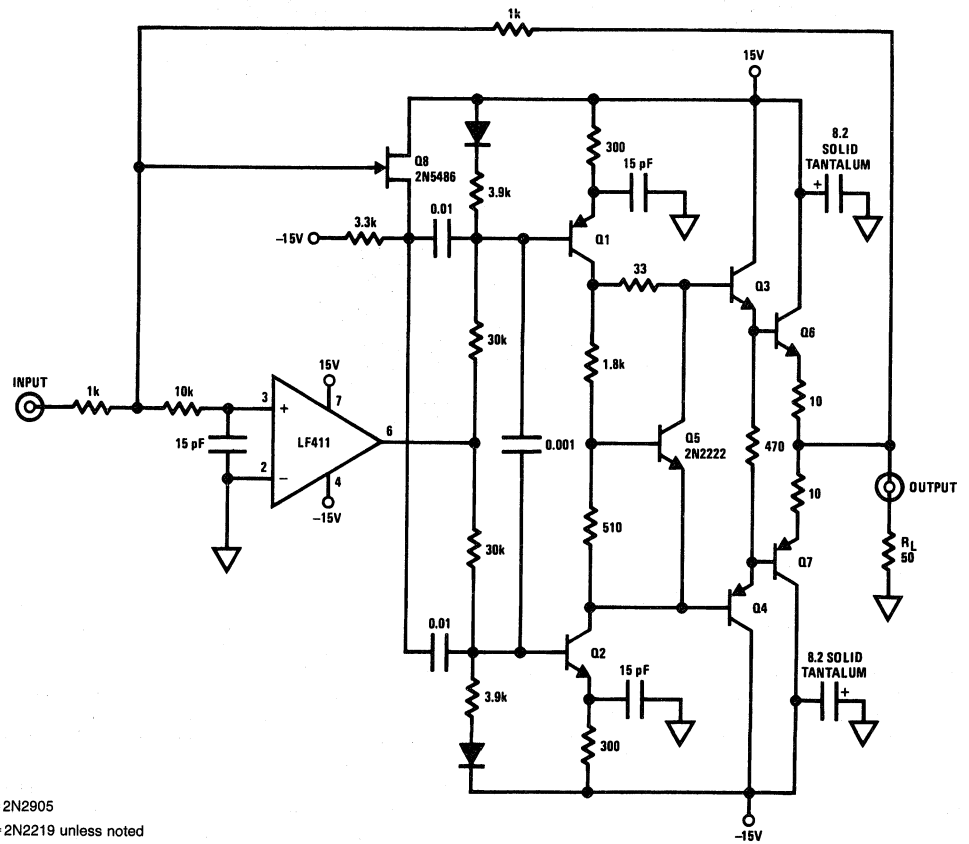
Precautions should be taken to ensure that the power supply for the integrated circuit never becomes reversed in polarity or that the unit is not inadvertently installed backwards in a socket as an unlimited current surge through the resulting forward diode within the IC could cause fusing of the internal conductors and result in a destroyed unit.

As with most amplifiers, care should be taken with lead dress, component placement and supply decoupling in order to ensure stability. For example, resistors from the output to an input should be placed with the body close to the input to minimize "pick-up" and maximize the frequency of the feedback pole by minimizing the capacitance from the input to ground.

A feedback pole is created when the feedback around any amplifier is resistive. The parallel resistance and capacitance from the input of the device (usually the inverting input) to AC ground set the frequency of the pole. In many instances the frequency of this pole is much greater than the expected 3 dB frequency of the closed loop gain and consequently there is negligible effect on stability margin. However, if the feedback pole is less than approximately 6 times the expected 3 dB frequency, a lead capacitor should be placed from the output to the input of the op amp. The value of the added capacitor should be such that the RC time constant of this capacitor and the resistance it parallels is greater than or equal to the original feedback pole time constant.

Typical Applications

High Speed Current Booster

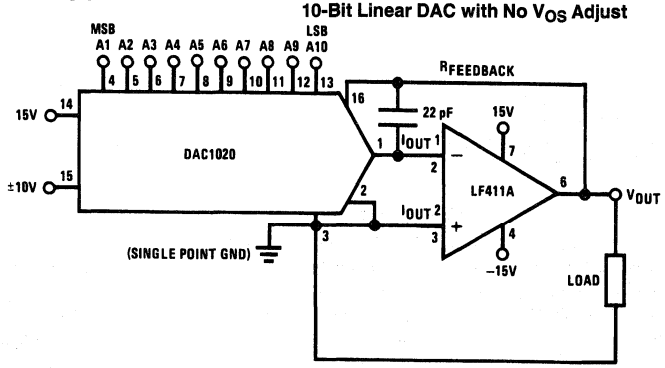


PNP = 2N2905
NPN = 2N2219 unless noted
TO-5 heat sinks for Q6-Q7

TL/H/5655–9

Typical Applications (Continued)

10-Bit Linear DAC with No V_{OS} Adjust



$$V_{OUT} = -V_{REF}\left(\frac{A1}{2} + \frac{A2}{4} + \frac{A3}{8} + \cdots \frac{A10}{1024}\right)$$

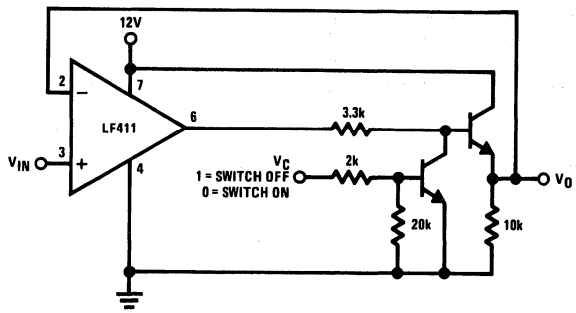
$-10V \le V_{REF} \le 10V$

$$0 \le V_{OUT} \le -\frac{1023}{1024} V_{REF}$$

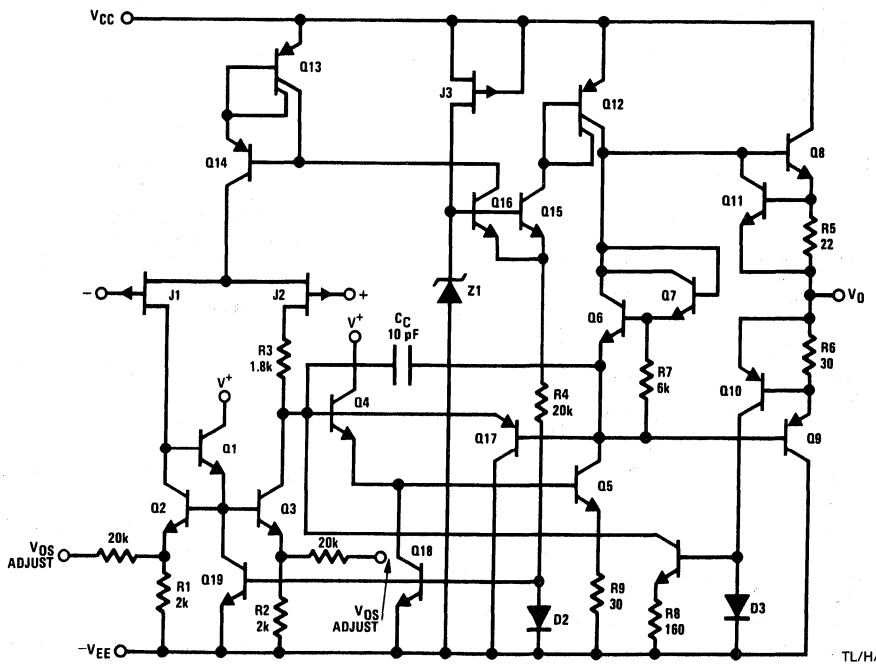
where $A_N = 1$ if the A_N digital input is high

$A_N = 0$ if the A_N digital input is low

Single Supply Analog Switch with Buffered Output



Detailed Schematic



TL/H/5655–10

National Semiconductor

LF412 Low Offset, Low Drift Dual JFET Input Operational Amplifier

General Description

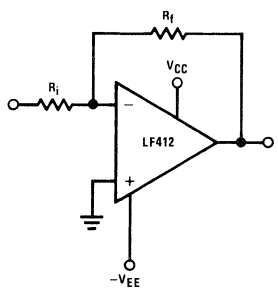
These devices are low cost, high speed, JFET input operational amplifiers with very low input offset voltage and guaranteed input offset voltage drift. They require low supply current yet maintain a large gain bandwidth product and fast slew rate. In addition, well matched high voltage JFET input devices provide very low input bias and offset currents. LF412 dual is pin compatible with the LM1558, allowing designers to immediately upgrade the overall performance of existing designs.

These amplifiers may be used in applications such as high speed integrators, fast D/A converters, sample and hold circuits and many other circuits requiring low input offset voltage and drift, low input bias current, high input impedance, high slew rate and wide bandwidth.

Features

■ Internally trimmed offset voltage	1 mV (max)
■ Input offset voltage drift	10 μV/°C (max)
■ Low input bias current	50 pA
■ Low input noise current	0.01 pA/√Hz
■ Wide gain bandwidth	3 MHz (min)
■ High slew rate	10V/μs (min)
■ Low supply current	1.8 mA/Amplifier
■ High input impedance	$10^{12}\Omega$
■ Low total harmonic distortion $A_V = 10$, $R_L = 10k$, $V_O = 20$ Vp-p, BW = 20 Hz-20 kHz	≤0.02%
■ Low 1/f noise corner	50 Hz
■ Fast settling time to 0.01%	2 μs

Typical Connection



Ordering Information

LF412XYZ

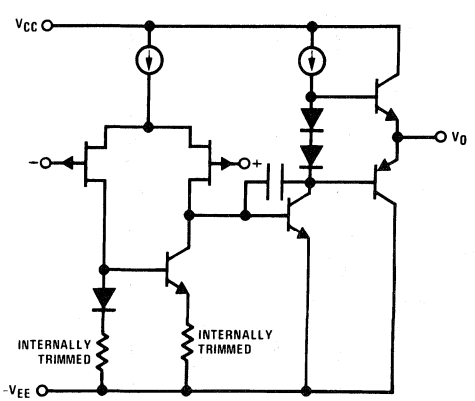
X indicates electrical grade

Y indicates temperature range
"M" for military
"C" for commercial

Z indicates package type
"H" or "N"

Simplified Schematic

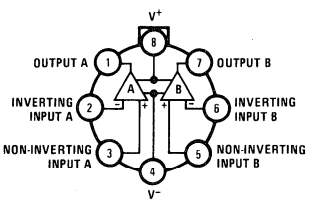
1/2 Dual



*Available per JM38510/11905

Connection Diagrams

Metal Can Package

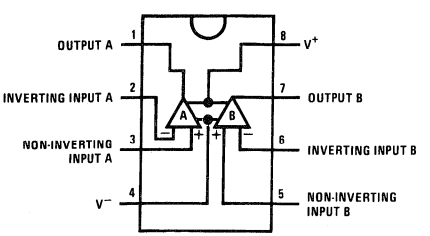


Note. Pin 4 connected to case.

TOP VIEW

Order Number LF412AMH, LF412MH, LF412ACH, LF412CH or LF412MH/883*
See NS Package Number H08B

Dual-In-Line Package



TOP VIEW

TL/H/5656–1

Order Number LF412ACN, LF412CN or LF412MJ/883*
See NS Package Number J08A or N08E

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.
(Note 9)

	LF412A	LF412
Supply Voltage	±22V	±18V
Differential Input Voltage	±38V	±30V
Input voltage Range (Note 1)	±19V	±15V
Output Short Circuit Duration (Note 2)	Continuous	Continuous

	H Package	N Package
Power Dissipation (Note 10)	(Note 3)	670 mW
T_j max	150°C	115°C
θ_{jA} (Typical)	152°C/W	115°C/W
Operating Temp. Range	(Note 4)	(Note 4)
Storage Temp. Range	$-65°C \leq T_A \leq 150°C$	$-65°C \leq T_A \leq 150°C$
Lead Temp. (Soldering, 10 sec.)	260°C	260°C
ESD Tolerance (Note 11)	1700V	1700V

DC Electrical Characteristics (Note 5)

Symbol	Parameter	Conditions		LF412A Min	LF412A Typ	LF412A Max	LF412 Min	LF412 Typ	LF412 Max	Units
V_{OS}	Input Offset Voltage	$R_S = 10\ k\Omega$, $T_A = 25°C$			0.5	1.0		1.0	3.0	mV
$\Delta V_{OS}/\Delta T$	Average TC of Input Offset Voltage	$R_S = 10\ k\Omega$ (Note 6)			7	10		7	20	μV/°C
I_{OS}	Input Offset Current	$V_S = \pm 15V$ (Notes 5 and 7)	$T_j = 25°C$		25	100		25	100	pA
			$T_j = 70°C$			2			2	nA
			$T_j = 125°C$			25			25	nA
I_B	Input Bias Current	$V_S = \pm 15V$ (Notes 5 and 7)	$T_j = 25°C$		50	200		50	200	pA
			$T_j = 70°C$			4			4	nA
			$T_j = 125°C$			50			50	nA
R_{IN}	Input Resistance	$T_j = 25°C$			10^{12}			10^{12}		Ω
A_{VOL}	Large Signal Voltage Gain	$V_S = \pm 15V$, $V_O = \pm 10V$, $R_L = 2k$, $T_A = 25°C$		50	200		25	200		V/mV
		Over Temperature		25	200		15	200		V/mV
V_O	Output Voltage Swing	$V_S = \pm 15V$, $R_L = 10k$		±12	±13.5		±12	±13.5		V
V_{CM}	Input Common-Mode Voltage Range			±16	+19.5		±11	+14.5		V
					−16.5			−11.5		V
CMRR	Common-Mode Rejection Ratio	$R_S \leq 10k$		80	100		70	100		dB
PSRR	Supply Voltage Rejection Ratio	(Note 8)		80	100		70	100		dB
I_S	Supply Current	$V_O = 0V$, $R_L = \infty$			3.6	5.6		3.6	6.5	mA

AC Electrical Characteristics (Note 5)

Symbol	Parameter	Conditions	LF412A Min	LF412A Typ	LF412A Max	LF412 Min	LF412 Typ	LF412 Max	Units
	Amplifier to Amplifier Coupling	$T_A = 25°C$, f = 1 Hz-20 kHz (Input Referred)		−120			−120		dB
SR	Slew Rate	$V_S = \pm 15V$, $T_A = 25°C$	10	15		8	15		V/μs
GBW	Gain-Bandwidth Product	$V_S = \pm 15V$, $T_A = 25°C$	3	4		2.7	4		MHz
e_n	Equivalent Input Noise Voltage	$T_A = 25°C$, $R_S = 100\Omega$, f = 1 kHz		25			25		$nV/\sqrt{Hz}$
i_n	Equivalent Input Noise Current	$T_A = 25°C$, f = 1 kHz		0.01			0.01		$pA/\sqrt{Hz}$

Note 1: Unless otherwise specified the absolute maximum negative input voltage is equal to the negative power supply voltage.

Note 2: Any of the amplifier outputs can be shorted to ground indefintely, however, more than one should not be simultaneously shorted as the maximum junction temperature will be exceeded.

Note 3: For operating at elevated temperature, these devices must be derated based on a thermal resistance of θ_{jA}.

Note 4: These devices are available in both the commercial temperature range $0°C \leq T_A \leq 70°C$ and the military temperature range $-55°C \leq T_A \leq 125°C$. The temperature range is designated by the position just before the package type in the device number. A "C" indicates the commercial temperature range and an "M" indicates the military temperature range. The military temperature range is available in "H" package only. In all cases the maximum operating temperature is limited by internal junction temperature T_j max.

Note 5: Unless otherwise specified, the specifications apply over the full temperature range and for $V_S = \pm 20V$ for the LF412A and for $V_S = \pm 15V$ for the LF412. V_{OS}, I_B, and I_{OS} are measured at $V_{CM} = 0$.

Note 6: The LF412A is 100% tested to this specification. The LF412 is sample tested on a per amplifier basis to insure at least 85% of the amplifiers meet this specification.

Note 7: The input bias currents are junction leakage currents which approximately double for every 10°C increase in the junction temperature, T_j. Due to limited production test time, the input bias currents measured are correlated to junction temperature. In normal operation the junction temperature rises above the ambient temperature as a result of internal power dissipation, P_D. $T_j = T_A + \theta_{jA} P_D$ where θ_{jA} is the thermal resistance from junction to ambient. Use of a heat sink is recommended if input bias current is to be kept to a minimum.

Note 8: Supply voltage rejection ratio is measured for both supply magnitudes increasing or decreasing simultaneously in accordance with common practice. $V_S = \pm 6V$ to $\pm 15V$.

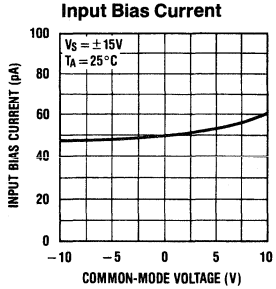
Note 9: Refer to RETS412X for LF412MH and LF412MJ military specifications.

Note 10: Max. Power Dissipation is defined by the package characteristics. Operating the part near the Max. Power Dissipation may cause the part to operate outside guaranteed limits.

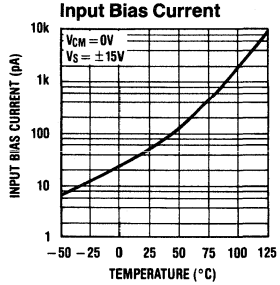
Note 11: Human body model, 1.5 kΩ in series with 100 pF.

Typical Performance Characteristics

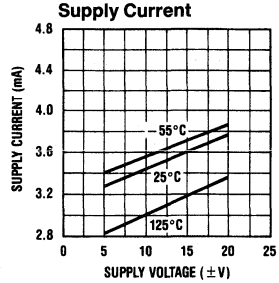
Input Bias Current



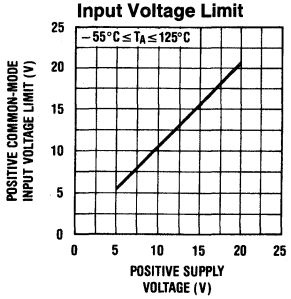
Input Bias Current



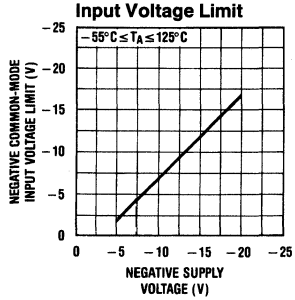
Supply Current



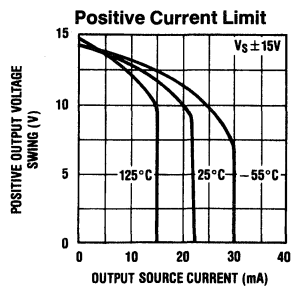
Positive Common-Mode Input Voltage Limit



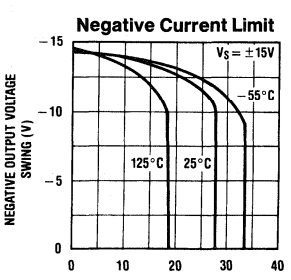
Negative Common-Mode Input Voltage Limit



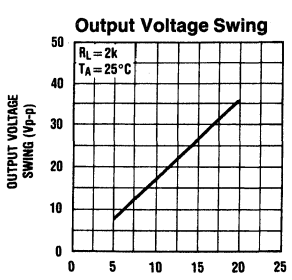
Positive Current Limit



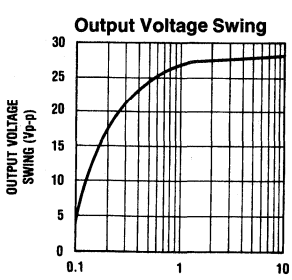
Negative Current Limit



Output Voltage Swing



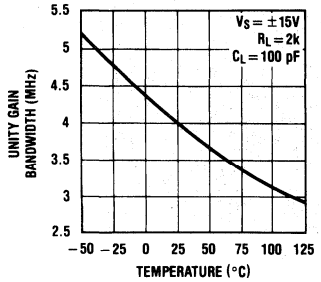
Output Voltage Swing



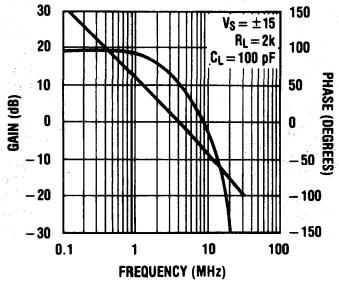
TL/H/5656–2

Typical Performance Characteristics (Continued)

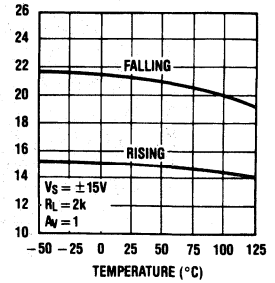
Gain Bandwidth



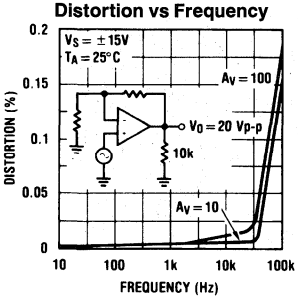
Bode Plot



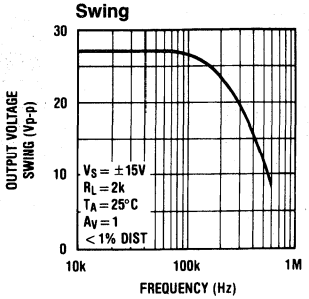
Slew Rate



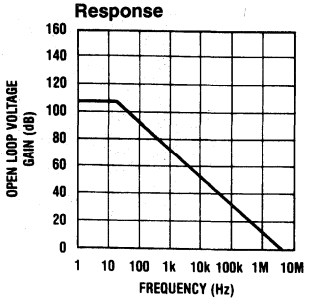
Distortion vs Frequency



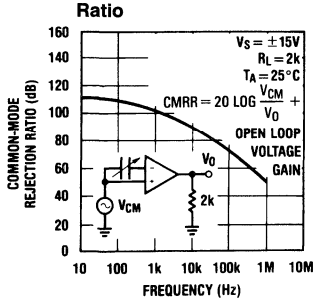
Undistorted Output Voltage Swing



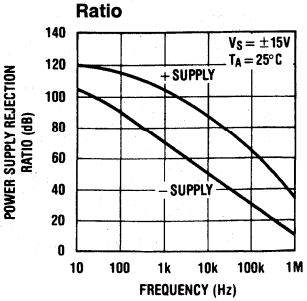
Open Loop Frequency Response



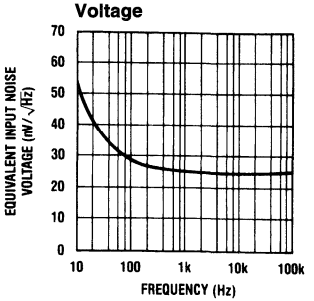
Common-Mode Rejection Ratio



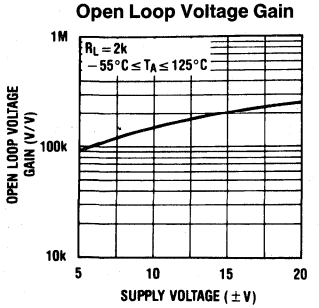
Power Supply Rejection Ratio



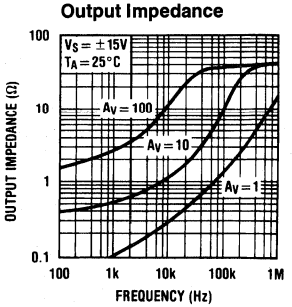
Equivalent Input Noise Voltage



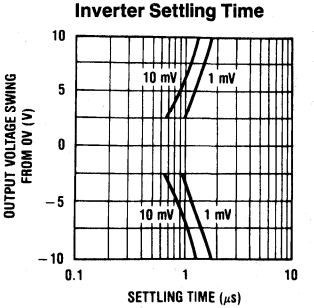
Open Loop Voltage Gain



Output Impedance



Inverter Settling Time



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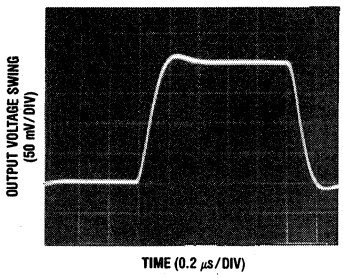
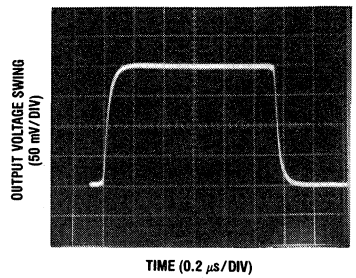
Pulse Response $R_L = 2\,k\Omega$, $C_L = 10\,pF$

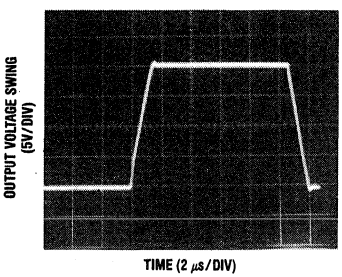
Small Signal Inverting



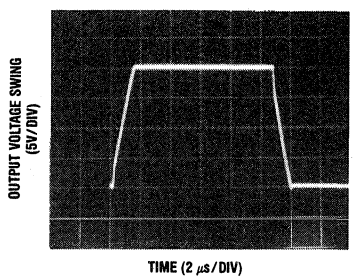
Small Signal Non-Inverting



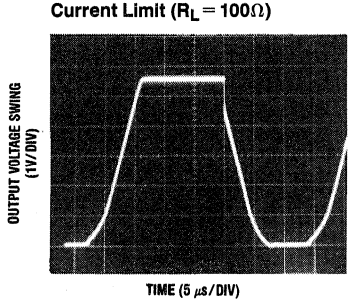
Large Signal Inverting



Large Signal Non-Inverting



Current Limit ($R_L = 100\Omega$)



TL/H/5656–4

Application Hints

The LF412 series of JFET input dual op amps are internally trimmed (BI-FET II™) providing very low input offset voltages and guaranteed input offset voltage drift. These JFETs have large reverse breakdown voltages from gate to source and drain eliminating the need for clamps across the inputs. Therefore, large differential input voltages can easily be accommodated without a large increase in input current. The maximum differential input voltage is independent of the supply voltages. However, neither of the input voltages should be allowed to exceed the negative supply as this will cause large currents to flow which can result in a destroyed unit.

Exceeding the negative common-mode limit on either input will cause a reversal of the phase to the output and force the amplifier output to the corresponding high or low state. Exceeding the negative common-mode limit on both inputs will force the amplifier output to a high state. In neither case does a latch occur since raising the input back within the common-mode range again puts the input stage and thus the amplifier in a normal operating mode.

Exceeding the positive common-mode limit on a single input will not change the phase of the output, however, if both inputs exceed the limit, the output of the amplifier may be forced to a high state.

The amplifiers will operate with a common-mode input voltage equal to the positive supply; however, the gain bandwidth and slew rate may be decreased in this condition. When the negative common-mode voltage swings to within 3V of the negative supply, an increase in input offset voltage may occur.

Application Hints (Continued)

Each amplifier is individually biased by a zener reference which allows normal circuit operation on ±6.0V power supplies. Supply voltages less than these may result in lower gain bandwidth and slew rate.

The amplifiers will drive a 2 kΩ load resistance to ±10V over the full temperature range. If the amplifier is forced to drive heavier load currents, however, an increase in input offset voltage may occur on the negative voltage swing and finally reach an active current limit on both positive and negative swings.

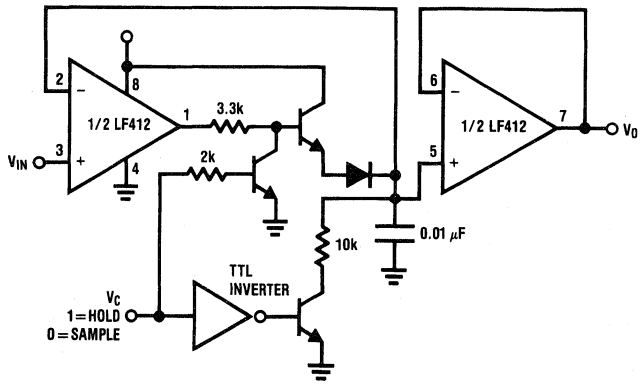
Precautions should be taken to ensure that the power supply for the integrated circuit never becomes reversed in polarity or that the unit is not inadvertently installed backwards in a socket as an unlimited current surge through the resulting forward diode within the IC could cause fusing of the internal conductors and result in a destroyed unit.

As with most amplifiers, care should be taken with lead dress, component placement and supply decoupling in order to ensure stability. For example, resistors from the output to an input should be placed with the body close to the input to minimize "pick-up" and maximize the frequency of the feedback pole by minimizing the capacitance from the input to ground.

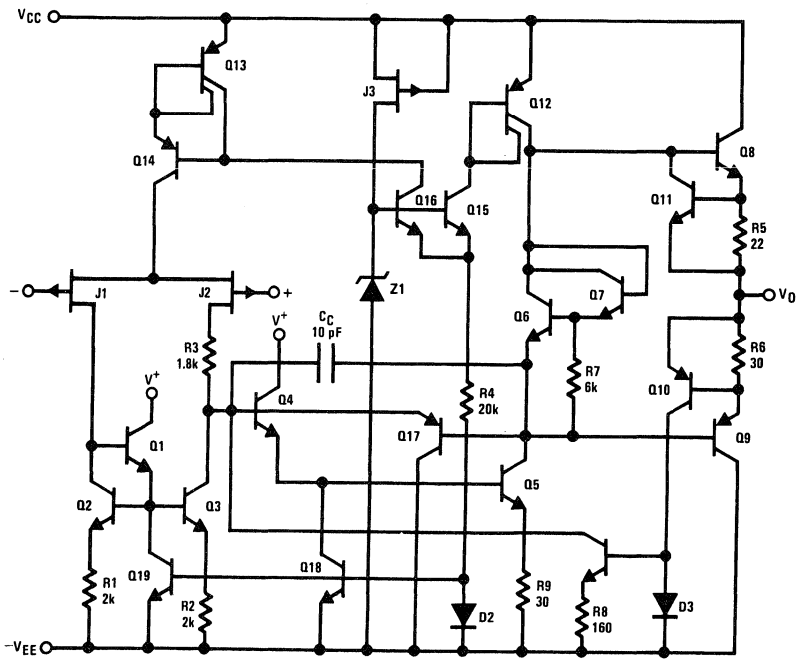
A feedback pole is created when the feedback around any amplifier is resistive. The parallel resistance and capacitance from the input of the device (usually the inverting input) to AC ground set the frequency of the pole. In many instances the frequency of this pole is much greater than the expected 3 dB frequency of the closed loop gain and consequently there is negligible effect on stability margin. However, if the feedback pole is less than approximately 6 times the expected 3 dB frequency a lead capacitor should be placed from the output to the input of the op amp. The value of the added capacitor should be such that the RC time constant of this capacitor and the resistance it parallels is greater than or equal to the original feedback pole time constant.

Typical Application

Single Supply Sample and Hold



Detailed Schematic



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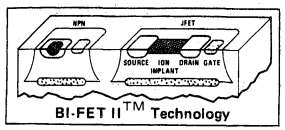
National Semiconductor



LF441 Low Power JFET Input Operational Amplifier

General Description

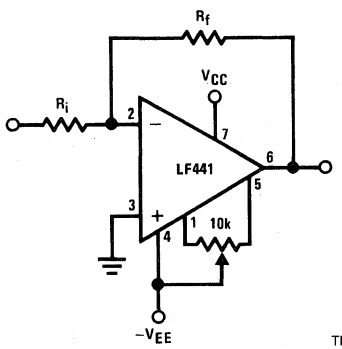
The LF441 low power operational amplifier provides many of the same AC characteristics as the industry standard LM741 while greatly improving the DC characteristics of the LM741. The amplifier has the same bandwidth, slew rate, and gain (10 kΩ load) as the LM741 and only draws one tenth the supply current of the LM741. In addition, the well matched high voltage JFET input devices of the LF441 reduce the input bias and offset currents by a factor of 10,000 over the LM741. A combination of careful layout design and internal trimming guarantees very low input offset voltage and voltage drift. The LF441 also has a very low equivalent input noise voltage for a low power amplifier.

The LF441 is pin compatible with the LM741, allowing an immediate 10 times reduction in power drain in many applications. The LF441 should be used where low power dissipation and good electrical characteristics are the major considerations.

Features

■ 1/10 supply current of a LM741	200 μA (max)
■ Low input bias current	50 pA (max)
■ Low input offset voltage	0.5 mV (max)
■ Low input offset voltage drift	10 μV/°C (max)
■ High gain bandwidth	1 MHz
■ High slew rate	1 V/μs
■ Low noise voltage for low power	35 nV/√Hz
■ Low input noise current	0.01 pA/√Hz
■ High input impedance	$10^{12}\Omega$
■ High gain $V_O = \pm 10V$, $R_L = 10k$	50k (min)

Typical Connection



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Ordering Information

LF441XYZ

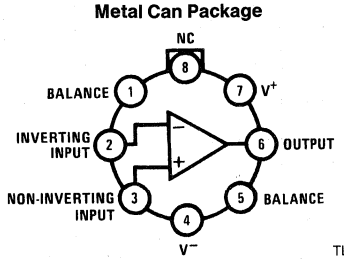
X indicates electrical grade

Y indicates temperature range
"M" for military,
"C" for commercial

Z indicates package type
"H" or "N"

Connection Diagrams

Metal Can Package



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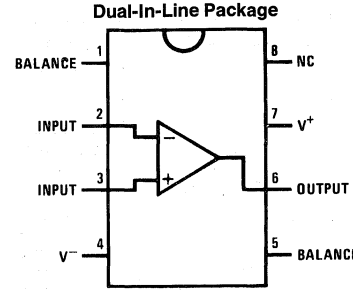
Top View

Note: Pin 4 connected to case.

Order Number LF441AMH, LF441MH/883, LF441ACH or LF441CH
See NS Package Number H08B

Dual-In-Line Package



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Top View

Order Number LF441ACN, LF441CM or LF441CN
See NS Package Number M08A or N08E

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

	LF441A	LF441
Supply Voltage	±22V	±18V
Differential Input Voltage	±38V	±30V
Input Voltage Range (Note 1)	±19V	±15V
Output Short Circuit Duration	Continuous	Continuous

	H Package	N Package	M Package
Power Dissipation (Notes 2 and 9)	670 mW	670 mW	
$T_{j\,max}$	150°C	115°C	
θ_{jA}(Typical)		130°C/W	185°C/W
Board Mount in still air	165°C/W		
Board Mount in 400 LF/min air flow	65°C/W		
θ_{jC}	25°C/W		
Operating Temp. Range	(Note 3)	(Note 3)	
Storage Temp. Range	$-65°C \le T_A \le 150°C$	$-65°C \le T_A \le 150°C$	
Lead Temperature (Soldering, 10 seconds)	300°C	260°C	

	LF441A	LF441
Soldering Information		
Dual-In-Line Package		
Soldering (10 sec.)	260°C	260°C
Small Outline Package		
Vapor Phase (60 sec.)	215°C	215°C
Infrared (15 sec.)	220°C	220°C

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

ESD Tolerance (Note 10) Rating to be Determined

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions		LF441A			LF441			Units
				Min	Typ	Max	Min	Typ	Max	
V_{OS}	Input Offset Voltage	$R_S = 10\,k\Omega$, $T_A = 25°C$			0.3	0.5		1	5	mV
		Over Temperature							7.5	mV
$\Delta V_{OS}/\Delta T$	Average TC of Input Offset Voltage	$R_S = 10\,k\Omega$ (Note 5)			7	10		10		µV/°C
I_{OS}	Input Offset Current	$V_S = \pm 15V$ (Notes 4 and 6)	$T_j = 25°C$		5	25		5	50	pA
			$T_j = 70°C$			1.5			1.5	nA
			$T_j = 125°C$			10				nA
I_B	Input Bias Current	$V_S = \pm 15V$ (Notes 4 and 6)	$T_j = 25°C$		10	50		10	100	pA
			$T_j = 70°C$			3			3	nA
			$T_j = 125°C$			20				nA
R_{IN}	Input Resistance	$T_j = 25°C$			10^{12}			10^{12}		Ω
A_{VOL}	Large Signal Voltage Gain	$V_S = \pm 15V$, $V_O = \pm 10V$, $R_L = 10\,k\Omega$, $T_A = 25°C$		50	100		25	100		V/mV
		Over Temperature		25			15			V/mV
V_O	Output Voltage Swing	$V_S = \pm 15V$, $R_L = 10\,k\Omega$		±12	±13		±12	±13		V
V_{CM}	Input Common-Mode Voltage Range			±16	+18, −17		±11	+14, −12		V
CMRR	Common-Mode Rejection Ratio	$R_S \le 10\,k\Omega$		80	100		70	95		dB

DC Electrical Characteristics (Note 4) (Continued)

Symbol	Parameter	Conditions	LF441A			LF441			Units
			Min	Typ	Max	Min	Typ	Max	
PSRR	Supply Voltage Rejection Ratio	(Note 7)	80	100		70	90		dB
I_S	Supply Current			150	200		150	250	μA

AC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	LF441A			LF441			Units
			Min	Typ	Max	Min	Typ	Max	
SR	Slew Rate	$V_S = \pm 15V$, $T_A = 25°C$	0.8	1		0.6	1		V/μs
GBW	Gain-Bandwidth Product	$V_S = \pm 15V$, $T_A = 25°C$	0.8	1		0.6	1		MHz
e_n	Equivalent Input Noise Voltage	$T_A = 25°C$, $R_S = 100\Omega$, f = 1 kHz		35			35		nV/$\sqrt{Hz}$
i_n	Equivalent Input Noise Current	$T_A = 25°C$, f = 1 kHz		0.01			0.01		pA/$\sqrt{Hz}$

Note 1: Unless otherwise specified the absolute maximum negative input voltage is equal to the negative power supply voltage.

Note 2: For operating at elevated temperature, these devices must be derated based on a thermal resistance of θ_{jA}.

Note 3: The temperature range is designated by the position just before the package type in the device number. A "C" indicates the commercial temperature range and an "M" indicates the military temperature range. The military temperature range is available in "H" package only.

Note 4: Unless otherwise specified the specifications apply over the full temperature range and for $V_S = \pm 20V$ for the LF441A and for $V_S = \pm 15V$ for the LF441. V_{OS}, I_B, and I_{OS} are measured at $V_{CM} = 0$.

Note 5: The LF441A is 100% tested to this specification.

Note 6: The input bias currents are junction leakage currents which approximately double for every 10°C increase in the junction temperature, T_j. Due to limited production test time, the input bias currents measured are correlated to junction temperature. In normal operation the junction temperature rises above the ambient temperature as a result of internal power dissipation, P_D. $T_j = T_A + \theta_{jA} P_D$ where θ_{jA} is the thermal resistance from junction to ambient. Use of a heat sink is recommended if input bias current is to be kept to a minimum.

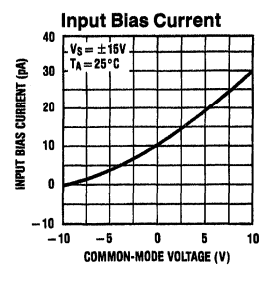
Note 7: Supply voltage rejection ratio is measured for both supply magnitudes increasing or decreasing simultaneously in accordance with common practice. From ±15V to ±5V for the LF441 and from ±20V to ±5V for the LF441A.

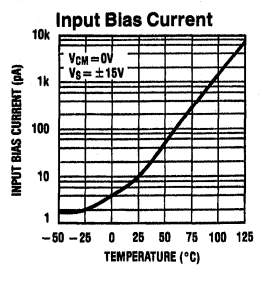
Note 8: Refer to RETS441X for LF441MH military specifications.

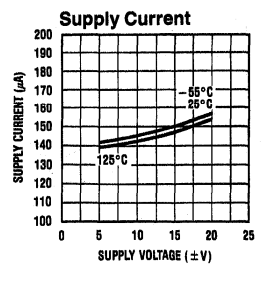
Note 9: Max. Power Dissipation is defined by the package characteristics. Operating the part near the Max. Power Dissipation may cause the part to operate outside guaranteed limits.

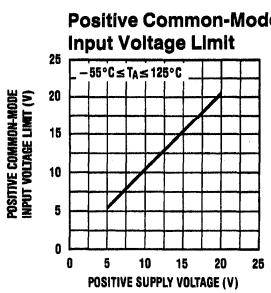
Note 10: Human body model, 1.5 kΩ in series with 100 pF.

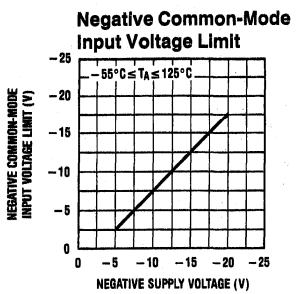
Typical Performance Characteristics

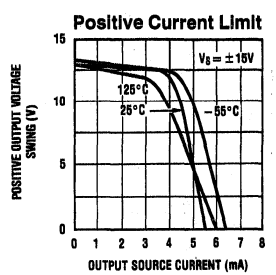












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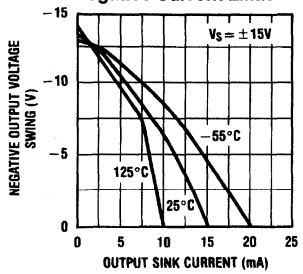
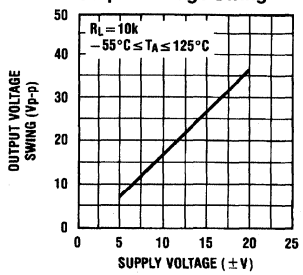
Typical Performance Characteristics (Continued)

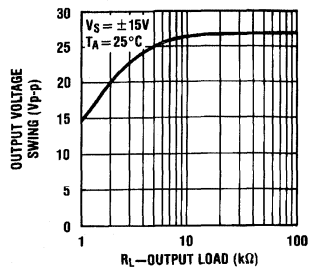
Negative Current Limit



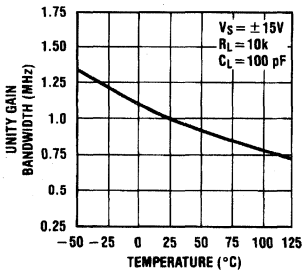
Output Voltage Swing



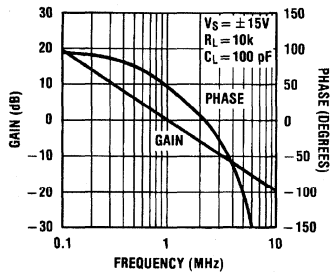
Output Voltage Swing



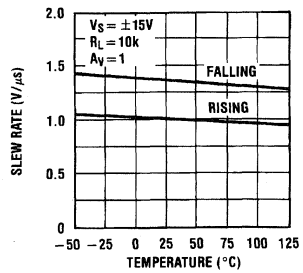
Gain Bandwidth



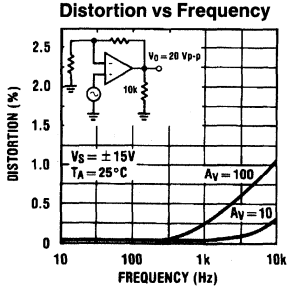
Bode Plot



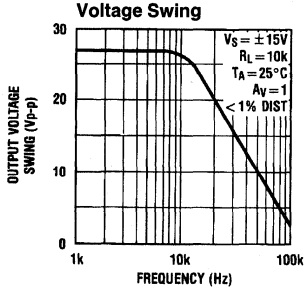
Slew Rate



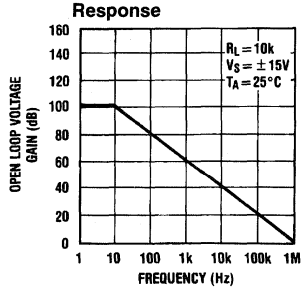
Distortion vs Frequency



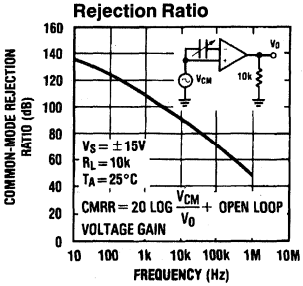
Undistorted Output Voltage Swing



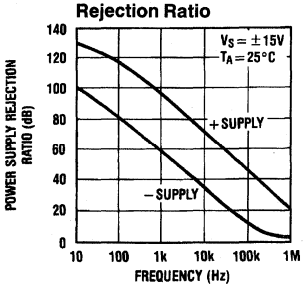
Open Loop Frequency Response



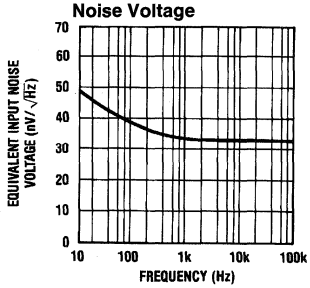
Common-Mode Rejection Ratio



Power Supply Rejection Ratio

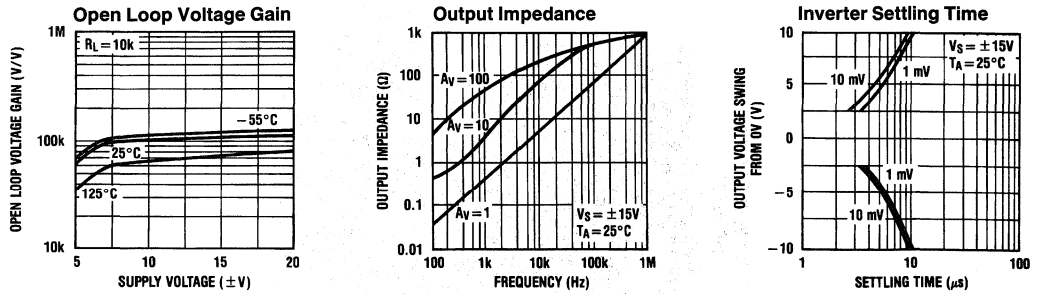


Equivalent Input Noise Voltage



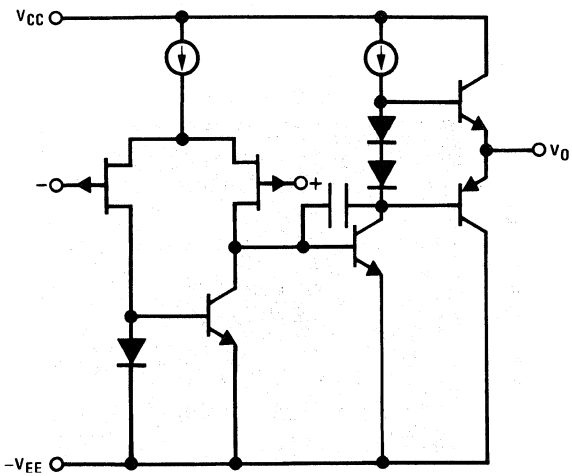
TL/H/9297–6

Typical Performance Characteristics (Continued)



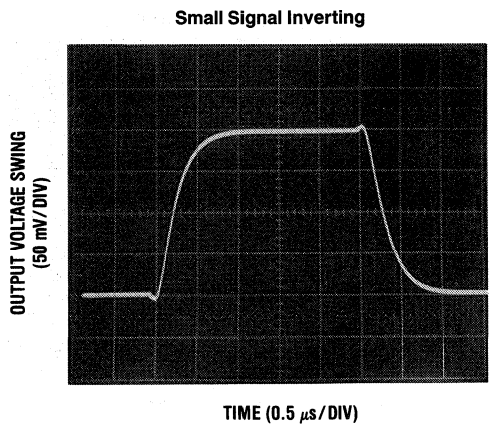
TL/H/9297–7

Simplified Schematic



TL/H/9297–3

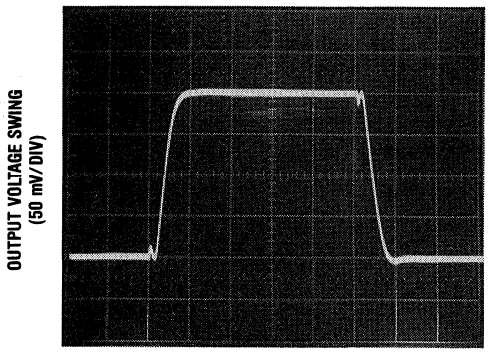
Pulse Response $R_L = 10\,k\Omega$, $C_L = 10\,pF$



TL/H/9297–8

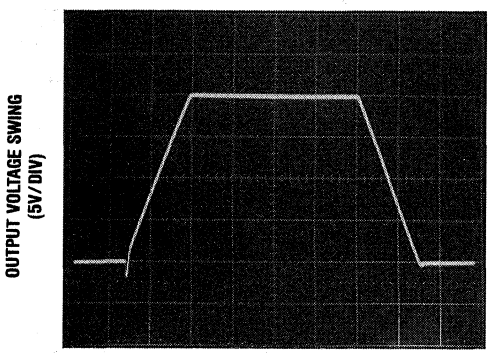
Pulse Response $R_L = 10\ k\Omega$, $C_L = 10\ pF$ (Continued)

Small Signal Non-Inverting



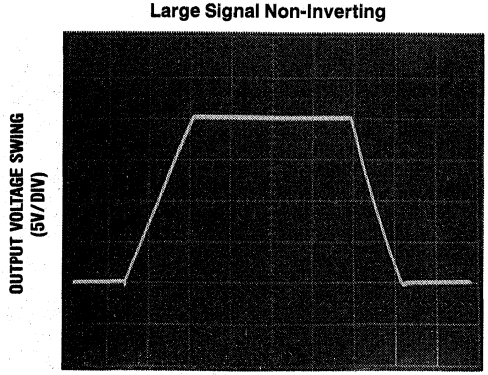
TL/H/9297–9

Large Signal Inverting



TL/H/9297–10

Large Signal Non-Inverting



TL/H/9297–11

Application Hints

This device is a low power op amp with an internally trimmed input offset voltage and JFET input devices (BI-FET II). These JFETs have large reverse breakdown voltages from gate to source and drain, eliminating the need for clamps across the inputs. Therefore, large differential input voltages can easily be accommodated without a large increase in input current. The maximum differential input voltage is independent of the supply voltages. However, neither of the input voltages should be allowed to exceed the negative supply as this will cause large currents to flow which can result in a destroyed unit.

Exceeding the negative common-mode limit on either input will force the output to a high state, potentially causing a reversal of phase to the output. Exceeding the negative common-mode limit on both inputs will force the amplifier output to a high state. In neither case does a latch occur since raising the input back within the common-mode range again puts the input stage and thus the amplifier in a normal operating mode.

Exceeding the positive common-mode limit on a single input will not change the phase of the output; however, if both inputs exceed the limit, the output of the amplifier will be forced to a high state.

The amplifier will operate with a common-mode input voltage equal to the positive supply; however, the gain bandwidth and slew rate may be decreased in this condition. When the negative common-mode voltage swings to within 3V of the negative supply, an increase in input offset voltage may occur.

The amplifier is biased to allow normal circuit operation with power supplies of $\pm 3V$. Supply voltages less than these may degrade the common-mode rejection and restrict the output voltage swing.

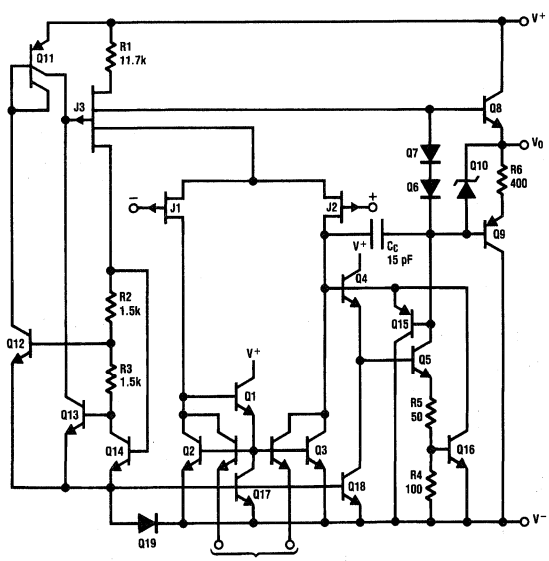
The amplifier will drive a 10 kΩ load resistance to $\pm 10V$ over the full temperature range.

Precautions should be taken to ensure that the power supply for the integrated circuit never becomes reversed in polarity or that the unit is not inadvertently installed backwards in a socket, as an unlimited current surge through the resulting forward diode within the IC could cause fusing of the internal conductors and result in a destroyed unit.

As with most amplifiers, care should be taken with lead dress, component placement and supply decoupling in order to ensure stability. For example, resistors from the output to an input should be placed with the body close to the input to minimize "pick-up" and maximize the frequency of the feedback pole by minimizing the capacitance from the input to ground.

A feedback pole is created when the feedback around any amplifier is resistive. The parallel resistance and capacitance from the input of the device (usually the inverting input to AC ground) set the frequency of this pole. In many instances the frequency of this pole is much greater than the expected 3 dB frequency, of the closed loop gain and consequently there is negligible effect on stability margin. However, if the feedback pole is less than approximately 6 times the expected 3 dB frequency, a lead capacitor should be placed from the output to the input of the op amp. The value of the added capacitor should be such that the RC time constant of this capacitor and the resistance it parallels is greater than or equal to the original feedback pole time constant.

Detailed Schematic



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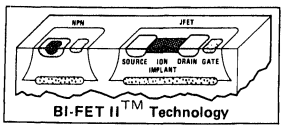
National Semiconductor



LF442 Dual Low Power JFET Input Operational Amplifier

General Description

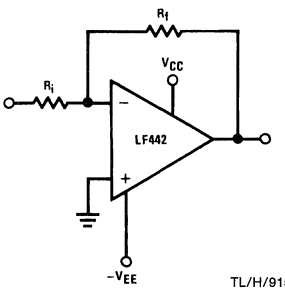
The LF442 dual low power operational amplifiers provide many of the same AC characteristics as the industry standard LM1458 while greatly improving the DC characteristics of the LM1458. The amplifiers have the same bandwidth, slew rate, and gain (10 kΩ load) as the LM1458 and only draw one tenth the supply current of the LM1458. In addition the well matched high voltage JFET input devices of the LF442 reduce the input bias and offset currents by a factor of 10,000 over the LM1458. A combination of careful layout design and internal trimming guarantees very low input offset voltage and voltage drift. The LF442 also has a very low equivalent input noise voltage for a low power amplifier.

The LF442 is pin compatible with the LM1458 allowing an immediate 10 times reduction in power drain in many applications. The LF442 should be used where low power dissipation and good electrical characteristics are the major considerations.

Features

■ 1/10 supply current of a LM1458	400 μA (max)
■ Low input bias current	50 pA (max)
■ Low input offset voltage	1 mV (max)
■ Low input offset voltage drift	10 μV/°C (max)
■ High gain bandwidth	1 MHz
■ High slew rate	1 V/μs
■ Low noise voltage for low power	35 nV/√Hz
■ Low input noise current	0.01 pA/√Hz
■ High input impedance	$10^{12}\Omega$
■ High gain $V_O = \pm 10V$, $R_L = 10k$	50k (min)

Typical Connection



TL/H/9155-1

Ordering Information

LF442XYZ

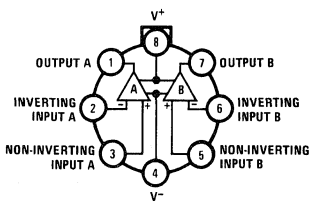
X indicates electrical grade

Y indicates temperature range
"M" for military
"C" for commercial

Z indicates package type
"H" or "N"

Connection Diagrams

Metal Can Package



TL/H/9155-2

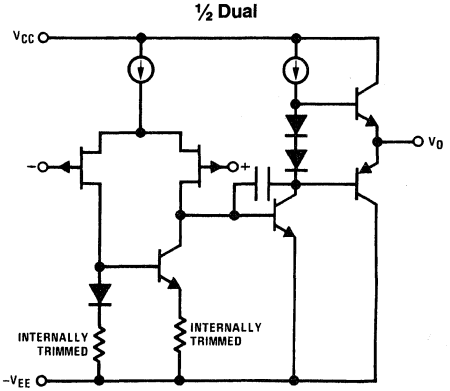
Top View

Note: Pin 4 connected to case

Order Number LF442AMH, LF442ACH, LF442CH, LF442MH or LF442MH/883
See NS Package Number H08B

Simplified Schematic

½ Dual



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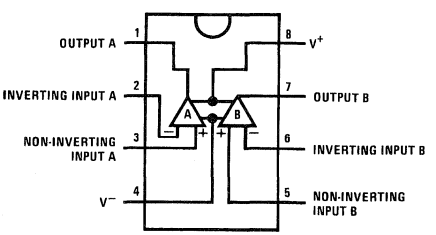
Dual-In-Line Package



TL/H/9155-4

Top View

Order Number LF442ACN or LF442CN
See NS Package Number N08E

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications. (Note 9)

	LF442A	LF442
Supply Voltage	±22V	±18V
Differential Input Voltage	±38V	±30V
Input Voltage Range (Note 1)	±19V	±15V
Output Short Circuit Duration (Note 2)	Continuous	Continuous

	H Package	N Package
T_j max	150°C	115°C
θ_{JA} (Typical) (Note 3)	65°C/W	114°C/W
θ_{JA} (Typical) (Note 4)	165°C/W	152°C/W
θ_{JC} (Typical)	21°C/W	
Operating Temperature Range	(Note 4)	(Note 4)
Storage Temperature Range	$-65°C \le T_A \le 150°C$	$-65°C \le T_A \le 150°C$
Lead Temperature (Soldering, 10 sec.)	260°C	260°C
ESD Tolerance	Rating to be determined	

DC Electrical Characteristics (Note 6)

Symbol	Parameter	Conditions		LF442A			LF442			Units
				Min	Typ	Max	Min	Typ	Max	
V_{OS}	Input Offset Voltage	$R_S = 10\ k\Omega$, $T_A = 25°C$			0.5	1.0		1.0	5.0	mV
		Over Temperature							7.5	mV
$\Delta V_{OS}/\Delta T$	Average TC of Input Offset Voltage	$R_S = 10\ k\Omega$			7	10		7		μV/°C
I_{OS}	Input Offset Current	$V_S = \pm 15V$ (Notes 6 and 7)	$T_j = 25°C$		5	25		5	50	pA
			$T_j = 70°C$			1.5			1.5	nA
			$T_j = 125°C$			10				nA
I_B	Input Bias Current	$V_S = \pm 15V$ (Notes 6 and 7)	$T_j = 25°C$		10	50		10	100	pA
			$T_j = 70°C$			3			3	nA
			$T_j = 125°C$			20				nA
R_{IN}	Input Resistance	$T_j = 25°C$			10^{12}			10^{12}		Ω
A_{VOL}	Large Signal Voltage Gain	$V_S = \pm 15V$, $V_O = \pm 10V$, $R_L = 10\ k\Omega$, $T_A = 25°C$		50	200		25	200		V/mV
		Over Temperature		25	200		15	200		V/mV
V_O	Output Voltage Swing	$V_S = \pm 15V$, $R_L = 10\ k\Omega$		±12	±13		±12	±13		V
V_{CM}	Input Common-Mode Voltage Range			±16	+18 −17		±11	+14 −12		V V
CMRR	Common-Mode Rejection Ratio	$R_S \le 10\ k\Omega$		80	100		70	95		dB
PSRR	Supply Voltage Rejection Ratio	(Note 8)		80	100		70	90		dB
I_S	Supply Current				300	400		400	500	μA

AC Electrical Characteristics (Note 6)

Symbol	Parameter	Conditions	LF442A			LF442			Units
			Min	Typ	Max	Min	Typ	Max	
	Amplifier to Amplifier Coupling	$T_A = 25°C$, f = 1 Hz-20 kHz (Input Referred)		−120			−120		dB
SR	Slew Rate	$V_S = \pm 15V$, $T_A = 25°C$	0.8	1		0.6	1		V/μs
GBW	Gain-Bandwidth Product	$V_S = \pm 15V$, $T_A = 25°C$	0.8	1		0.6	1		MHz
e_n	Equivalent Input Noise Voltage	$T_A = 25°C$, $R_S = 100\Omega$, f = 1 kHz		35			35		$nV/\sqrt{Hz}$
i_n	Equivalent Input Noise Current	$T_A = 25°C$, f = 1 kHz		0.01			0.01		$pA/\sqrt{Hz}$

Note 1: Unless otherwise specified the absolute maximum negative input voltage is equal to the negative power supply voltage.

Note 2: Any of the amplifier outputs can be shorted to ground indefinitely, however, more than one should not be simultaneously shorted as the maximum junction temperature will be exceeded.

Note 3: The value given is in 400 linear feet/min air flow.

Note 4: The value given is in static air.

Note 5: These devices are available in both the commercial temperature range $0°C \leq T_A \leq 70°C$ and the military temperature range $-55°C \leq T_A \leq 125°C$. The temperature range is designated by the position just before the package type in the device number. A "C" indicates the commercial temperature range and an "M" indicates the military temperature range. The military temperature range is available in "H" package only.

Note 6: Unless otherwise specified, the specifications apply over the full temperature range and for $V_S = \pm 20V$ for the LF442A and for $V_S = \pm 15V$ for the LF442. V_{OS}, I_B, and I_{OS} are measured at $V_{CM} = 0$.

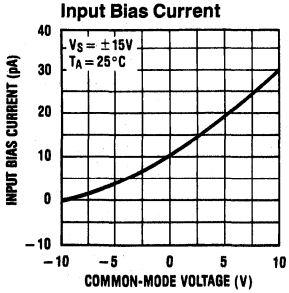
Note 7: The input bias currents are junction leakage currents which approximately double for every 10°C increase in the junction temperature, T_j. Due to limited production test time, the input bias currents measured are correlated to junction temperature. In normal operation the junction temperature rises above the ambient temperature as a result of internal power dissipation, P_D. $T_j = T_A + \theta_{jA} P_D$ where θ_{jA} is the thermal resistance from junction to ambient. Use of a heat sink is recommended if input bias current is to be kept to a minimum.

Note 8: Supply voltage rejection ratio is measured for both supply magnitudes increasing or decreasing simultaneously in accordance with common practice from ±15V to ±5V for the LF442 and ±20V to ±5V for the LF442A.

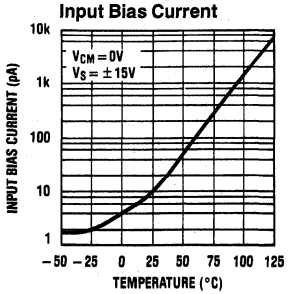
Note 9: Refer to RETS442X for LF442MH military specifications.

Typical Performance Characteristics

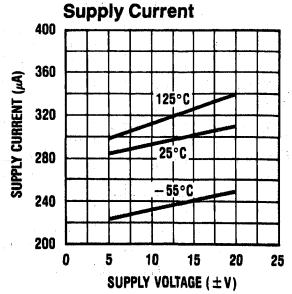
Input Bias Current



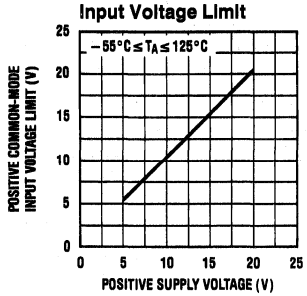
Input Bias Current



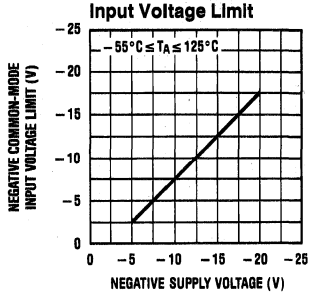
Supply Current



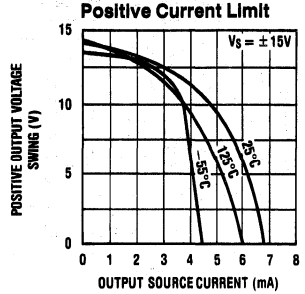
Positive Common-Mode Input Voltage Limit



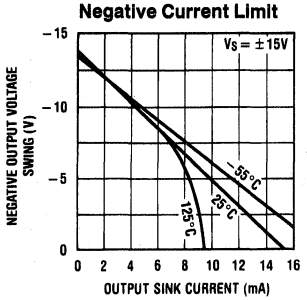
Negative Common-Mode Input Voltage Limit



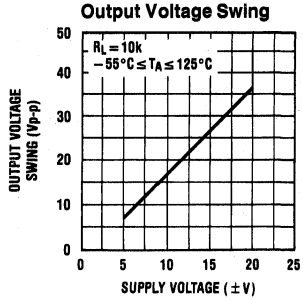
Positive Current Limit



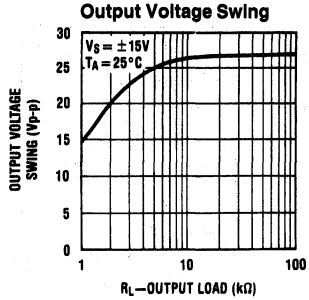
Negative Current Limit



Output Voltage Swing



Output Voltage Swing



TL/H/9155–5

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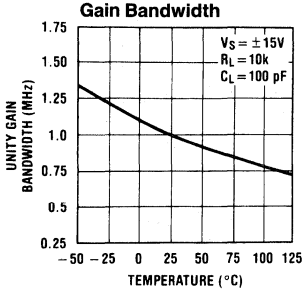
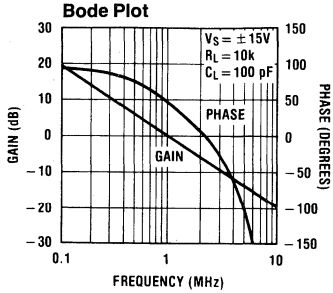
Typical Performance Characteristics (Continued)

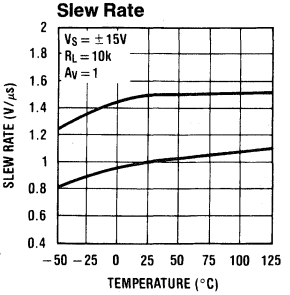
Gain Bandwidth



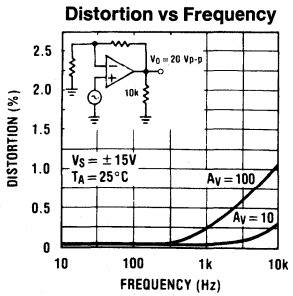
Bode Plot



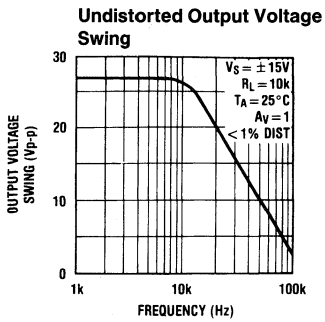
Slew Rate



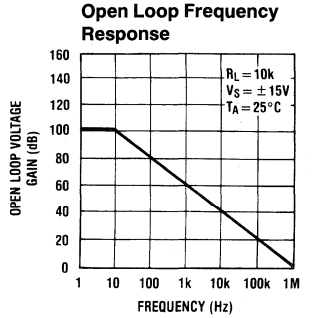
Distortion vs Frequency



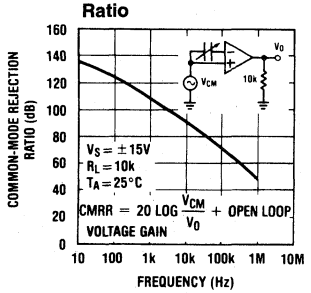
Undistorted Output Voltage Swing



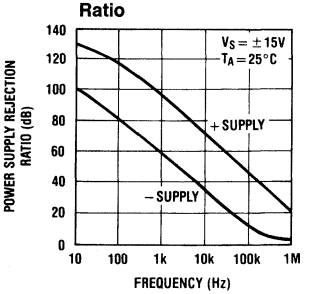
Open Loop Frequency Response



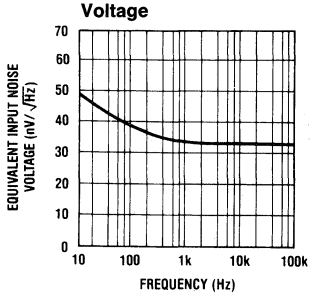
Common-Mode Rejection Ratio



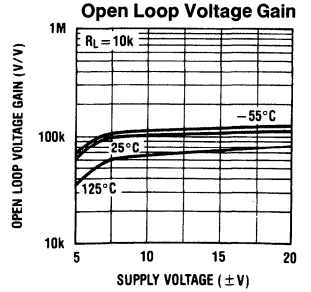
Power Supply Rejection Ratio



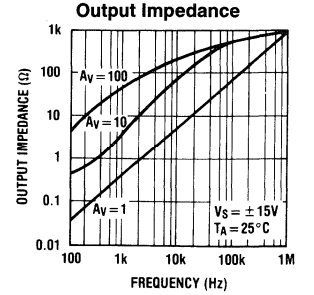
Equivalent Input Noise Voltage



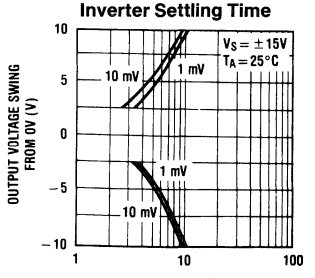
Open Loop Voltage Gain



Output Impedance



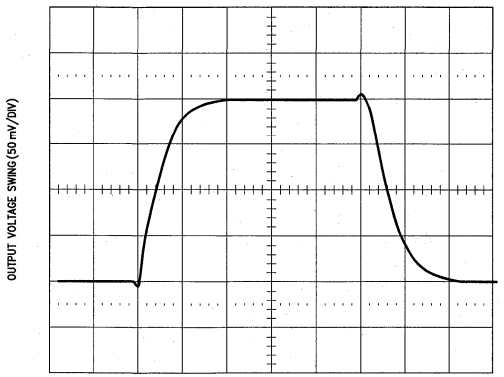
Inverter Settling Time



TL/H/9155–6

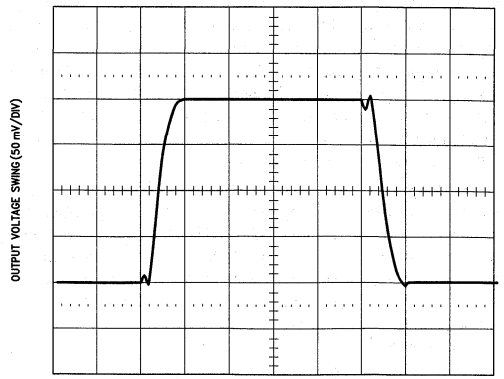
Pulse Response $R_L = 10\ k\Omega$, $C_L = 10\ pF$

Small Signal Inverting



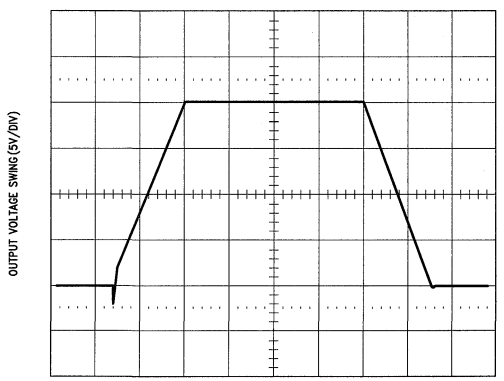
TL/H/9155–7

Small Signal Non-Inverting



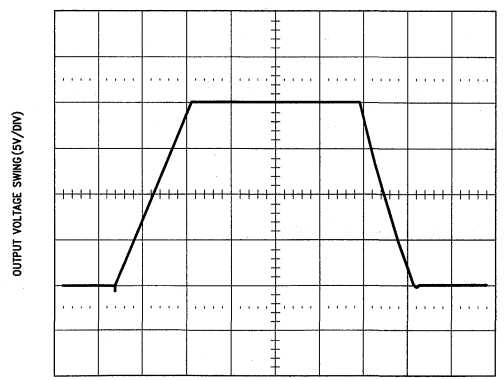
TL/H/9155–8

Large Signal Inverting



TL/H/9155–9

Large Signal Non-Inverting



TL/H/9155–10

Application Hints

This device is a dual low power op amp with internally trimmed input offset voltages and JFET input devices (BI-FET II). These JFETs have large reverse breakdown voltages from gate to source and drain eliminating the need for clamps across the inputs. Therefore, large differential input voltages can easily be accommodated without a large increase in input current. The maximum differential input voltage is independent of the supply voltages. However, neither of the input voltages should be allowed to exceed the negative supply as this will cause large currents to flow which can result in a destroyed unit.

Exceeding the negative common-mode limit on either input will force the output to a high state, potentially causing a reversal of phase to the output. Exceeding the negative common-mode limit on both inputs will force the amplifier output to a high state. In neither case does a latch occur since raising the input back within the common-mode range again puts the input stage and thus the amplifier in a normal operating mode.

Exceeding the positive common-mode limit on a single input will not change the phase of the output; however, if both inputs exceed the limit, the output of the amplifier will be forced to a high state.

The amplifiers will operate with a common-mode input voltage equal to the positive supply; however, the gain bandwidth and slew rate may be decreased in this condition. When the negative common-mode voltage swings to within 3V of the negative supply, an increase in input offset voltage may occur.

Each amplifier is individually biased to allow normal circuit operation with power supplies of ±3.0V. Supply voltages less than these may degrade the common-mode rejection and restrict the output voltage swing.

The amplifiers will drive a 10 kΩ load resistance to ± 10V over the full temperature range.

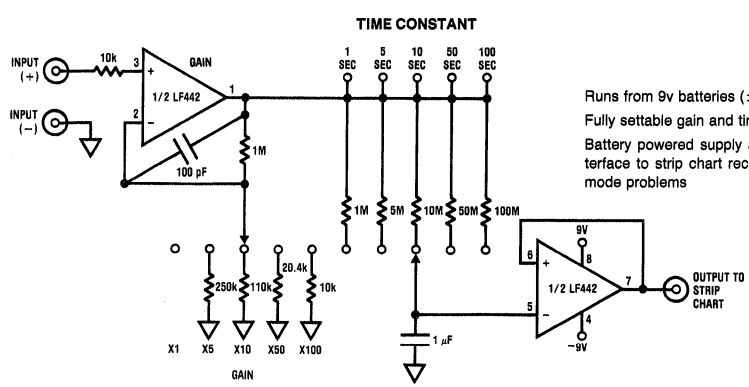
Precautions should be taken to ensure that the power supply for the integrated circuit never becomes reversed in polarity or that the unit is not inadvertently installed backwards in a socket as an unlimited current surge through the resulting forward diode within the IC could cause fusing of the internal conductors and result in a destroyed unit.

As with most amplifiers, care should be taken with lead dress, component placement and supply decoupling in order to ensure stability. For example, resistors from the output to an input should be placed with the body close to the input to minimize "pick-up" and maximize the frequency of the feedback pole by minimizing the capacitance from the input to ground.

A feedback pole is created when the feedback around any amplifier is resistive. The parallel resistance and capacitance from the input of the device (usually the inverting input) to AC ground set the frequency of the pole. In many instances the frequency of this pole is much greater than the expected 3 dB frequency of the closed loop gain and consequenty there is negligible effect on stability margin. However, if the feedback pole is less than approximately 6 times the expected 3 dB frequency a lead capacitor should be placed from the output to the input of the op amp. The value of the added capacitor should be such that the RC time constant of this capacitor and the resistance it parallels is greater than or equal to the original feedback pole time constant.

Typical Applications

Battery Powered Strip Chart Preamplifier



Runs from 9v batteries (±9V supplies)

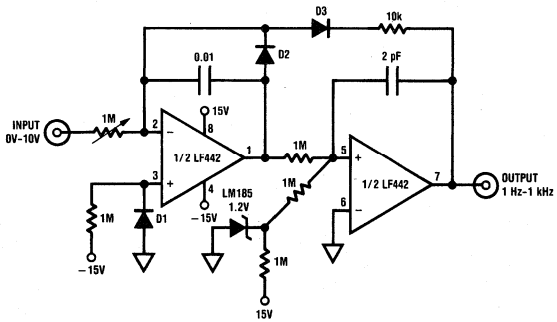
Fully settable gain and time constant

Battery powered supply allows direct plug-in interface to strip chart recorder without common-mode problems

TL/H/9155–11

Typical Applications (Continued)

"No FET" Low Power V → F Converter



Trim 1M pot for 1 kHz full-scale output

15 mW power drain

No integrator reset FET required

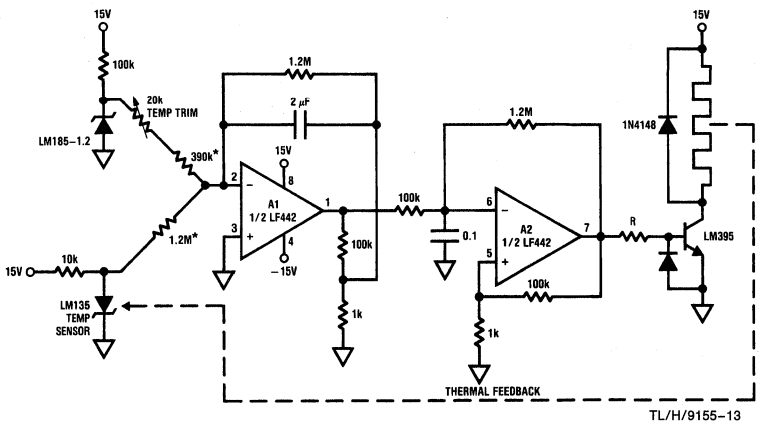
Mount D1 and D2 in close proximity

1% linearity to 1 kHz

TL/H/9155-12

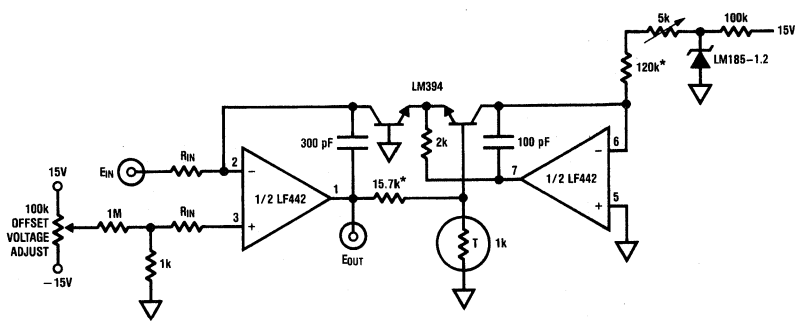
High Efficiency Crystal Oven Controller

- $T_{control}$ = 75°C
- A1's output represents the amplified difference between the LM335 temperature sensor and the crystal oven's temperature
- A2, a free running duty cycle modulator, drives the LM395 to complete a servo loop
- Switched mode operation yields high efficiency
- 1% metal film resistor



TL/H/9155-13

Conventional Log Amplifier



TL/H/9155-14

$$E_{OUT} = -\left[\log 10\left(\frac{E_{IN}}{R_{IN}}\right) + 5\right]$$

R_T = Tel Labs type Q81

Trim 5k for 10 µA through the 5k–120k combination

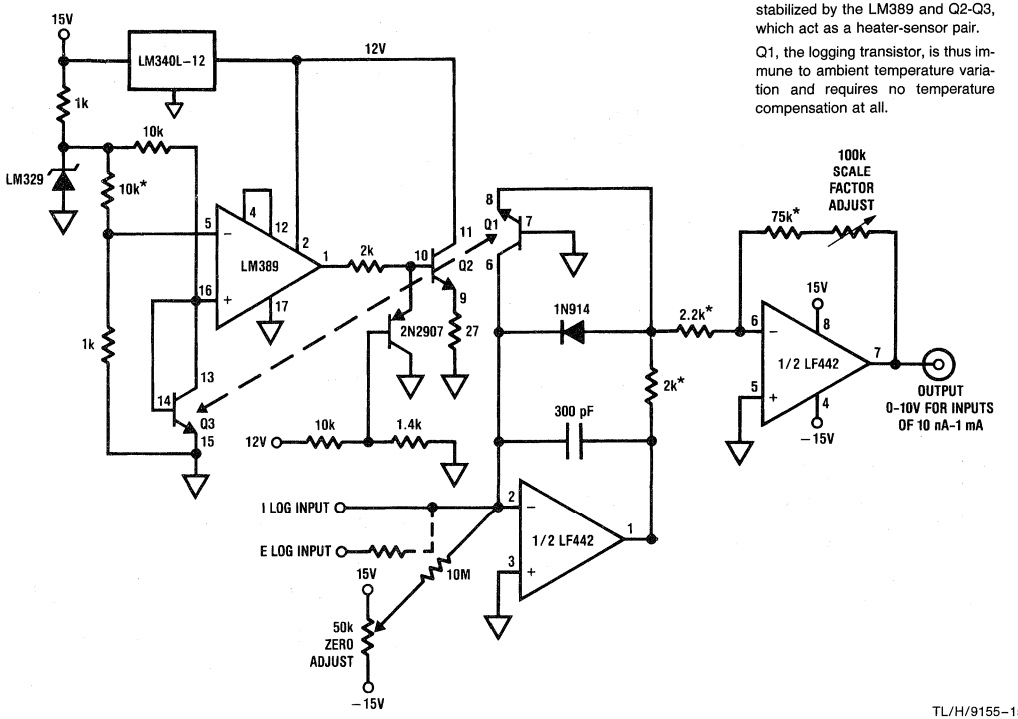
*1% film resistor

Typical Applications (Continued)

Unconventional Log Amplifier

Q1, Q2, Q3 are included on LM389 amplifier chip which is temperature-stabilized by the LM389 and Q2-Q3, which act as a heater-sensor pair.

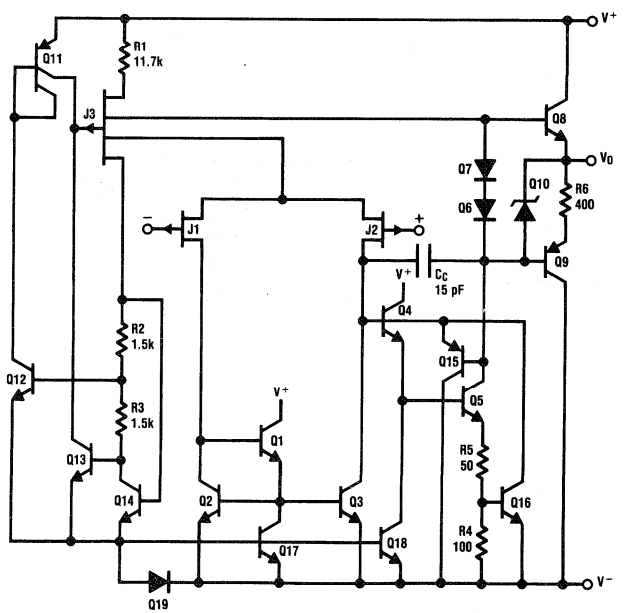
Q1, the logging transistor, is thus immune to ambient temperature variation and requires no temperature compensation at all.



TL/H/9155–15

Detailed Schematic

½ Dual



TL/H/9155–16

National Semiconductor

LF444 Quad Low Power JFET Input Operational Amplifier

General Description

The LF444 quad low power operational amplifier provides many of the same AC characteristics as the industry standard LM148 while greatly improving the DC characteristics of the LM148. The amplifier has the same bandwidth, slew rate, and gain (10 kΩ load) as the LM148 and only draws one fourth the supply current of the LM148. In addition the well matched high voltage JFET input devices of the LF444 reduce the input bias and offset currents by a factor of 10,000 over the LM148. The LF444 also has a very low equivalent input noise voltage for a low power amplifier.

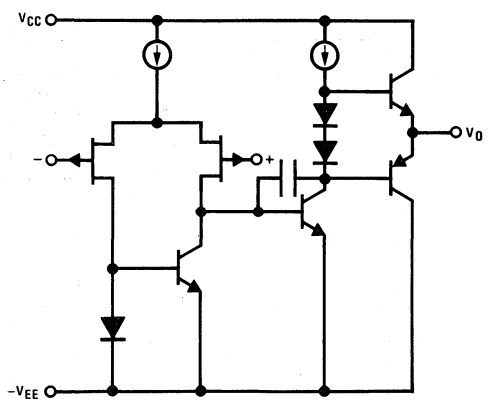
The LF444 is pin compatible with the LM148 allowing an immediate 4 times reduction in power drain in many applications. The LF444 should be used wherever low power dissipation and good electrical characteristics are the major considerations.

Features

■ ¼ supply current of a LM148	200 μA/Amplifier (max)
■ Low input bias current	50 pA (max)
■ High gain bandwidth	1 MHz
■ High slew rate	1 V/μs
■ Low noise voltage for low power	35 nV/√Hz
■ Low input noise current	0.01 pA/√Hz
■ High input impedance	$10^{12}\Omega$
■ High gain $V_O = \pm 10V$, $R_L = 10k$	50k (min)

Simplified Schematic

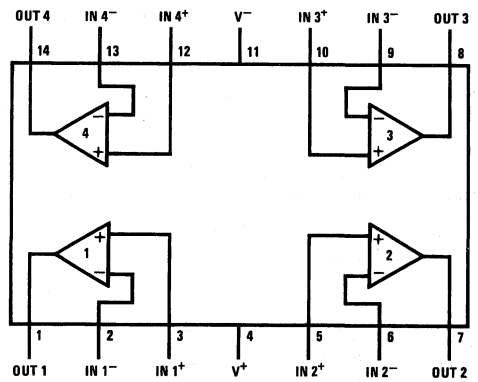
¼ Quad



TL/H/9156–1

Connection Diagram

Dual-In-Line Package



TL/H/9156–2

Top View

Order Number LF444AMD, LF444CD, LF444CM, LF444ACN, LF444CN or LF444MD/883
See NS Package Number D14E, M14A or N14A

Ordering Information

LF444XYZ

X indicates electrical grade

Y indicates temperature range
"M" for military, "C" for commercial

Z indicates package type "D", "M" or "N"

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

	LF444A	LF444
Supply Voltage	±22V	±18V
Differential Input Voltage	±38V	±30V
Input Voltage Range (Note 1)	±19V	±15V
Output Short Circuit Duration (Note 2)	Continuous	Continuous
	D Package	**N, M Packages**
Power Dissipation (Notes 3 and 9)	900 mW	670 mW
T_j max	150°C	115°C
θ_{jA} (Typical)	100°C/W	85°C/W

	LF444A/LF444
Operating Temperature Range	(Note 4)
Storage Temperature Range	$-65°C \le T_A \le 150°C$
ESD Tolerance (Note 10)	Rating to be determined
Soldering Information	
Dual-In-Line Packages (Soldering, 10 sec.)	260°C
Small Outline Package	
Vapor Phase (60 sec.)	215°C
Infrared (15 sec.)	220°C

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

DC Electrical Characteristics (Note 5)

Symbol	Parameter	Conditions		LF444A			LF444			Units
				Min	Typ	Max	Min	Typ	Max	
V_{OS}	Input Offset Voltage	$R_S = 10k, T_A = 25°C$			2	5		3	10	mV
		$0°C \le T_A \le +70°C$				6.5			12	mV
		$-55°C \le T_A \le +125°C$				8				mV
$\Delta V_{OS}/\Delta T$	Average TC of Input Offset Voltage	$R_S = 10\ k\Omega$			10			10		$\mu V/°C$
I_{OS}	Input Offset Current	$V_S = \pm 15V$ (Notes 5, 6)	$T_j = 25°C$		5	25		5	50	pA
			$T_j = 70°C$			1.5			1.5	nA
			$T_j = 125°C$			10				nA
I_B	Input Bias Current	$V_S = \pm 15V$ (Notes 5, 6)	$T_j = 25°C$		10	50		10	100	pA
			$T_j = 70°C$			3			3	nA
			$T_j = 125°C$			20				nA
R_{IN}	Input Resistance	$T_j = 25°C$			10^{12}			10^{12}		Ω
A_{VOL}	Large Signal Voltage Gain	$V_S = \pm 15V, V_O = \pm 10V$ $R_L = 10\ k\Omega, T_A = 25°C$		50	100		25	100		V/mV
		Over Temperature		25			15			V/mV
V_O	Output Voltage Swing	$V_S = \pm 15V, R_L = 10\ k\Omega$		±12	±13		±12	±13		V
V_{CM}	Input Common-Mode Voltage Range			±16	+18 −17		±11	+14 −12		V V
CMRR	Common-Mode Rejection Ratio	$R_S \le 10\ k\Omega$		80	100		70	95		dB
PSRR	Supply Voltage Rejection Ratio	(Note 7)		80	100		70	90		dB
I_S	Supply Current				0.6	0.8		0.8	1.0	mA

AC Electrical Characteristics (Note 5)

Symbol	Parameter	Conditions	LF444A			LF444			Units
			Min	Typ	Max	Min	Typ	Max	
	Amplifier-to-Amplifier Coupling			−120			−120		dB
SR	Slew Rate	$V_S = \pm 15V, T_A = 25°C$		1			1		V/μs
GBW	Gain-Bandwidth Product	$V_S = \pm 15V, T_A = 25°C$		1			1		MHz
e_n	Equivalent Input Noise Voltage	$T_A = 25°C, R_S = 100\Omega$, f = 1 kHz		35			35		nV/√Hz
i_n	Equivalent Input Noise Current	$T_A = 25°C$, f = 1 kHz		0.01			0.01		pA/√Hz

Note 1: Unless otherwise specified the absolute maximum negative input voltage is equal to the negative power supply voltage.

Note 2: Any of the amplifier outputs can be shorted to ground indefinitely, however, more than one should not be simultaneously shorted as the maximum junction temperature will be exceeded.

Note 3: For operating at elevated temperature, these devices must be derated based on a thermal resistance of θ_{jA}.

Note 4: The LF444A is available in both the commercial temperature range $0°C \le T_A \le 70°C$ and the military temperature range $-55°C \le T_A \le 125°C$. The LF444 is available in the commercial temperature range only. The temperature range is designated by the position just before the package type in the device number. A "C" indicates the commercial temperature range and an "M" indicates the military temperature range. The military temperature range is available in "D" package only.

Note 5: Unless otherwise specified the specifications apply over the full temperature range and for $V_S = \pm 20V$ for the LF444A and for $V_S = \pm 15V$ for the LF444. V_{OS}, I_B, and I_{OS} are measured at $V_{CM} = 0$.

Note 6: The input bias currents are junction leakage currents which approximately double for every 10°C increase in the junction temperature, T_j. Due to limited production test time, the input bias currents measured are correlated to junction temperature. In normal operation the junction temperature rises above the ambient temperature as a result of internal power dissipation, P_D. $T_j = T_A + \theta_{jA}P_D$ where θ_{jA} is the thermal resistance from junction to ambient. Use of a heat sink is recommended if input bias current is to be kept to a minimum.

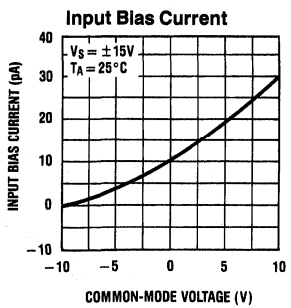
Note 7: Supply voltage rejection ratio is measured for both supply magnitudes increasing or decreasing simultaneously in accordance with common practice from ±15V to ±5V for the LF444 and from ±20V to ±5V for the LF444A.

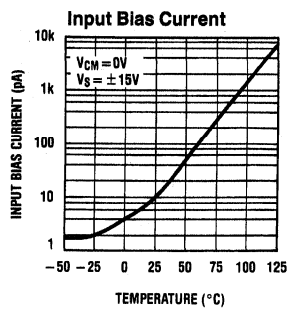
Note 8: Refer to RETS444X for LF444MD military specifications.

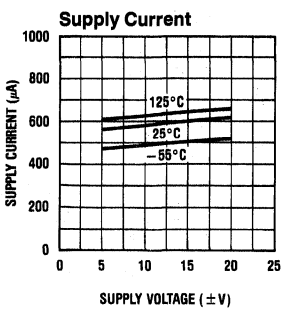
Note 9: Max. Power Dissipation is defined by the package characteristics. Operating the part near the Max. Power Dissipation may cause the part to operate outside guaranteed limits.

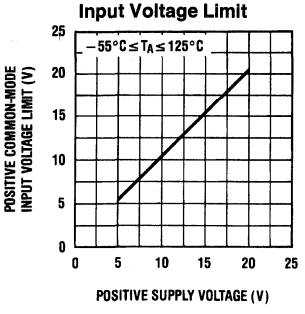
Note 10: Human body model, 1.5 kΩ in series with 100 pF.

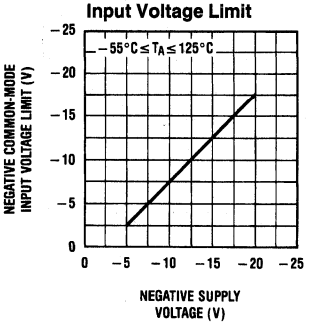
Typical Performance Characteristics

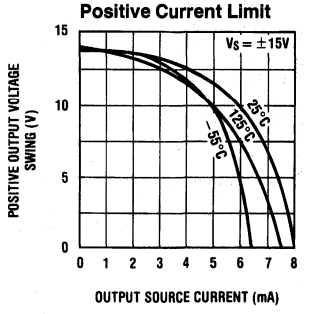








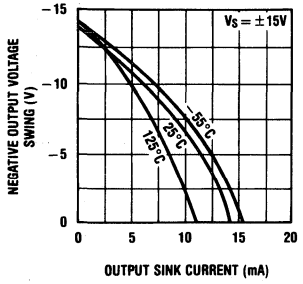




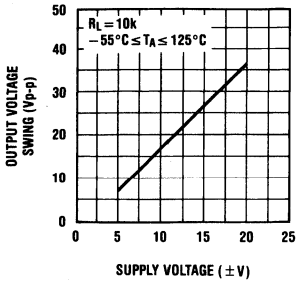
TL/H/9156–3

Typical Performance Characteristics (Continued)

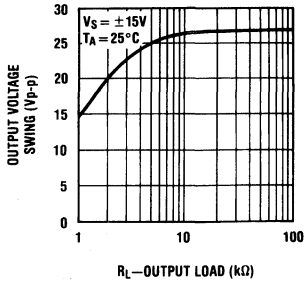
Negative Current Limit



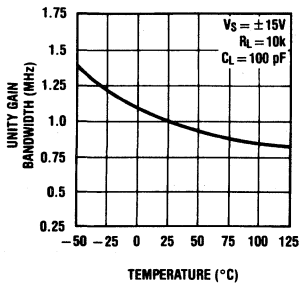
Output Voltage Swing



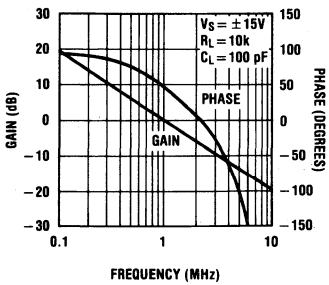
Output Voltage Swing



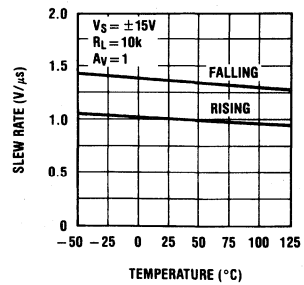
Gain Bandwidth



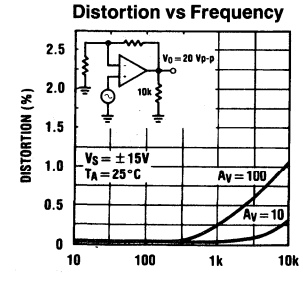
Bode Plot



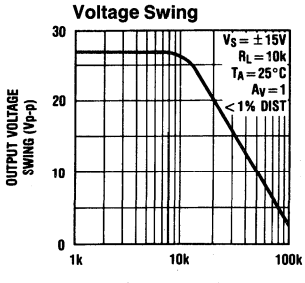
Slew Rate



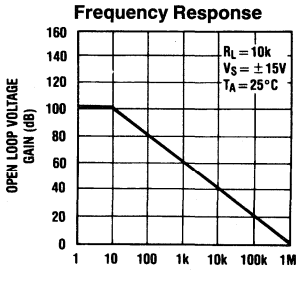
Distortion vs Frequency



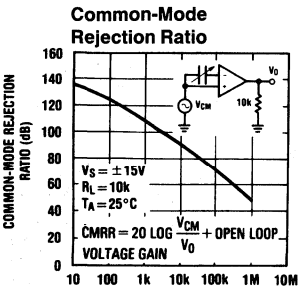
Undistorted Output Voltage Swing



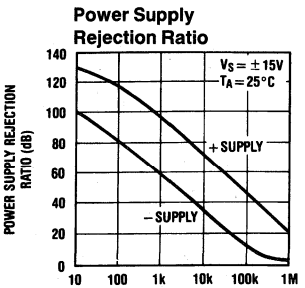
Open Loop Frequency Response



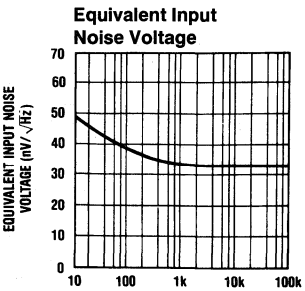
Common-Mode Rejection Ratio



Power Supply Rejection Ratio



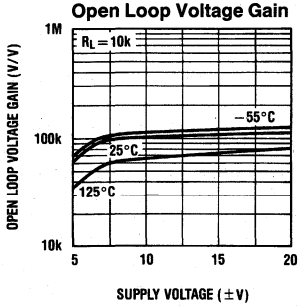
Equivalent Input Noise Voltage



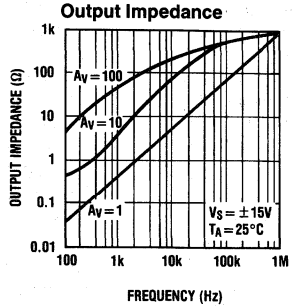
TL/H/9156–4

Typical Performance Characteristics (Continued)

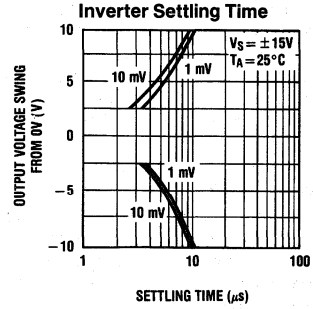
Open Loop Voltage Gain



Output Impedance



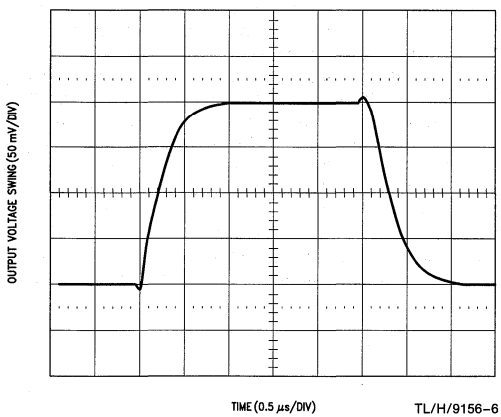
Inverter Settling Time



TL/H/9156–5

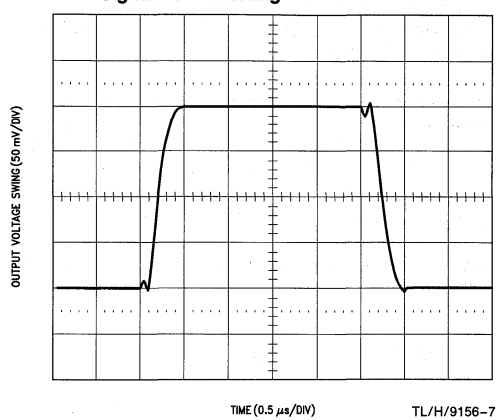
Pulse Response $R_L = 10\ k\Omega$, $C_L = 10\ pF$

Small Signal Inverting



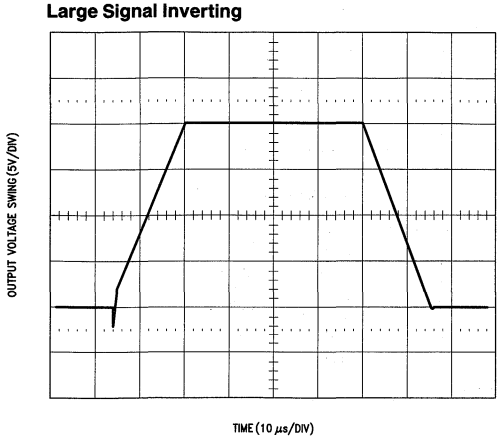
TL/H/9156–6

Small Signal Non-Inverting



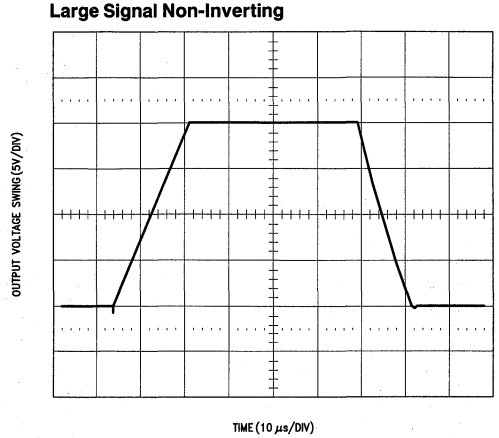
TL/H/9156–7

Large Signal Inverting



TL/H/9156–8

Large Signal Non-Inverting



TL/H/9156–9

Application Hints

This device is a quad low power op amp with JFET input devices (BI-FET™). These JFETs have large reverse breakdown voltages from gate to source and drain eliminating the need for clamps across the inputs. Therefore, large differential input voltages can easily be accommodated without a large increase in input current. The maximum differential input voltage is independent of the supply voltages. However, neither of the input voltages should be allowed to exceed the negative supply as this will cause large currents to flow which can result in a destroyed unit.

Exceeding the negative common-mode limit on either input will force the output to a high state, potentially causing a reversal of phase to the output. Exceeding the negative common-mode limit on both inputs will force the amplifier output to a high state. In neither case does a latch occur since raising the input back within the common-mode range again puts the input stage and thus the amplifier in a normal operating mode.

Exceeding the positive common-mode limit on a single input will not change the phase of the output; however, if both inputs exceed the limit, the output of the amplifier will be forced to a high state.

The amplifiers will operate with a common-mode input voltage equal to the positive supply; however, the gain bandwidth and slew rate may be decreased in this condition. When the negative common-mode voltage swings to within 3V of the negative supply, an increase in input offset voltage may occur.

Each amplifier is individually biased to allow normal circuit operation with power supplies of ±3.0V. Supply voltages less than these may degrade the common-mode rejection and restrict the output voltage swing.

The amplifiers will drive a 10 kΩ load resistance to ±10V over the full temperature range. If the amplifier is forced to drive heavier load currents, however, an increase in input offset voltage may occur on the negative voltage swing and finally reach an active current limit on both positive and negative swings.

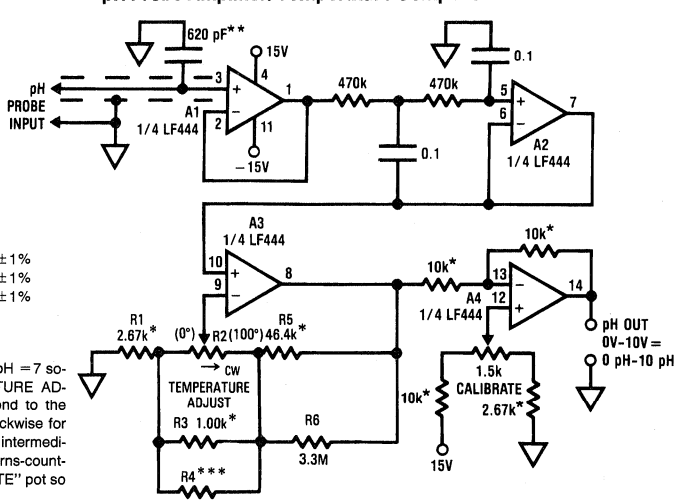
Precautions should be taken to ensure that the power supply for the integrated circuit never becomes reversed in polarity or that the unit is not inadvertently installed backwards in a socket as an unlimited current surge through the resulting forward diode within the IC could cause fusing of the internal conductors and result in a destroyed unit.

As with most amplifiers, care should be taken with lead dress, component placement and supply decoupling in order to ensure stability. For example, resistors from the output to an input should be placed with the body close to the input to minimize "pick-up" and maximize the frequency of the feedback pole by minimizing the capacitance from the input to ground.

A feedback pole is created when the feedback around any amplifier is resistive. The parallel resistance and capacitance from the input of the device (usually the inverting input) to AC ground set the frequency of the pole. In many instances the frequency of this pole is much greater than the expected 3 dB frequency of the closed loop gain and consequently there is negligible effect on stability margin. However, if the feedback pole is less than approximately 6 times the expected 3 dB frequency a lead capacitor should be placed from the output to the input of the op amp. The value of the added capacitor should be such that the RC time constant of this capacitor and the resistance it parallels is greater than or equal to the original feedback pole time constant.

Typical Application

pH Probe Amplifier/Temperature Compensator



***For R2 = 50k, R4 = 330k ±1%
For R2 = 100k, R4 = 75k ±1%
For R2 = 200k, R4 = 56k ±1%

**Polystyrene

*Film resistor type RN60C

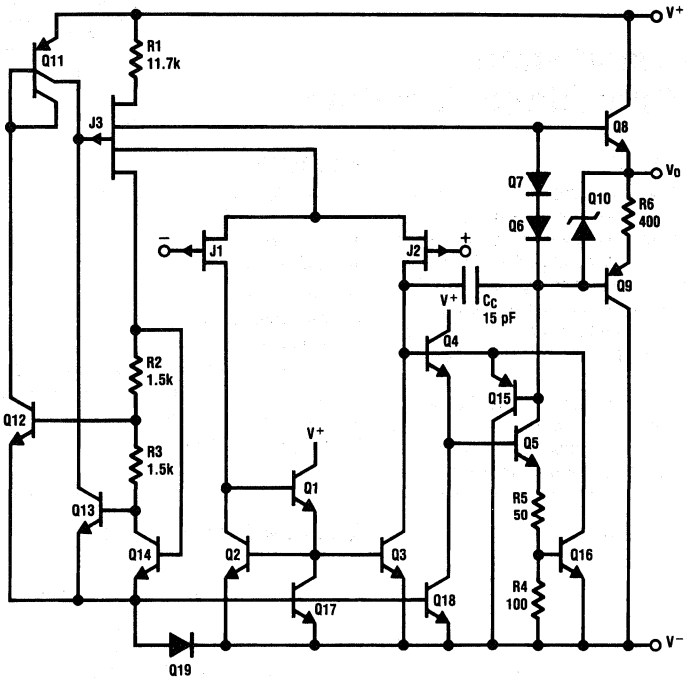
To calibrate, insert probe in pH = 7 solution. Set the "TEMPERATURE ADJUST" pot, R2, to correspond to the solution temperature: full clockwise for 0°C, and proportionately for intermediate temperatures, using a turns-counting dial. Then set "CALIBRATE" pot so output reads 7V.

Typical probe = Ingold Electrodes #465-35

TL/H/9156–10

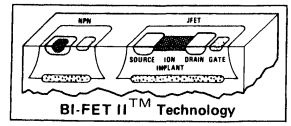
Detailed Schematic

¼ Quad



TL/H/9156–11

National Semiconductor



LF451 Wide-Bandwidth JFET-Input Operational Amplifier

General Description

The LF451 is a low-cost high-speed JFET-input operational amplifier with an internally trimmed input offset voltage (BI-FET II™ technology). The device requires a low supply current and yet maintains a large gain bandwidth product and a fast slew rate. In addition, well matched high voltage JFET input devices provide very low input bias and offset currents. The LF451 is pin compatible with the standard LM741, allowing designers to upgrade the overall performance of existing designs.

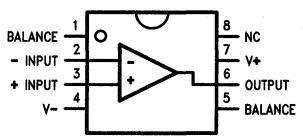
The LF451 may be used in such applications as high-speed integrators, fast D/A converters, sample-and-hold circuits and many other circuits requiring low input bias current, high input impedance, high slew rate and wide bandwidth.

Features

- Internally trimmed offset voltage — 5.0 mV (max)
- Low input bias current — 50 pA (typ)
- Low input noise current — 0.01 pA/$\sqrt{Hz}$ (typ)
- Wide gain bandwidth — 4 MHz (typ)
- High slew rate — 13 V/μs (typ)
- Low supply current — 3.4 mA (max)
- High input impedance — $10^{12}\Omega$ (typ)
- Low total harmonic distortion A_V = 10, R_L = 10k, V_O = 20 V_{p-p}, f = 20 Hz–20 kHz — <0.02% (typ)
- Low 1/f noise corner — 50 Hz (typ)
- Fast settling time to 0.01% — 2 μs (typ)

Connection Diagram

S.O. Package

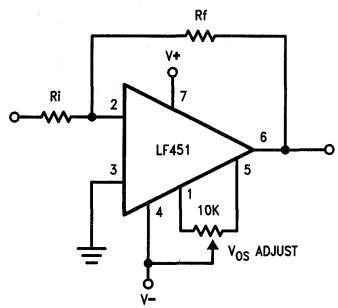


TL/H/9660–2

Top View

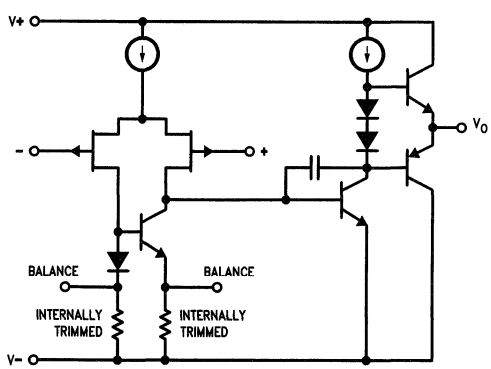
Order Number LF451CM
See NS Package Number M08A

Typical Connection



TL/H/9660–1

Simplified Schematic



TL/H/9660–3

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage ($V^+ - V^-$)	36V
Input Voltage Range	$V^- \le V_{IN} \le V+$
Differential Input Voltage (Note 2)	±30V
Junction Temperature (T_J MAX)	150°C
Output Short Circuit Duration	Continuous
Power Dissipation (Note 3)	500 mW
ESD Tolerance	TBD
Soldering Information (Note 5)	
SO Package: Vapor Phase (60 sec)	215°C
Infrared (15 sec)	220°C

Operating Ratings (Note 1)

Temperature Range	$T_{MIN} \le T_A \le T_{MAX}$
LF451CM	$0°C \le T_A \le +70°C$
Junction Temperature ($T_{J\,max}$)	125°C
Supply Voltage ($V^+ - V^-$)	10V to 32V

DC Electrical Characteristics

The following specifications apply for $V^+ = +15V$ and $V^- = -15V$. **Boldface limits apply for T_{MIN} to T_{MAX};** all other limits $T_A = T_J = 25°C$.

Symbol	Parameter	Conditions	LF451CM			Units
			Typical (Note 6)	Tested Limit (Note 7)	Design Limit (Note 8)	
V_{OS}	Maximum Input Offset Voltage	$R_S = 10\,k\Omega$, (Note 10)	0.3	5		mV
I_{OS}	Maximum Input Offset Current	(Notes 9, 10) $T_J = 25°C$ $T_J = 70°C$	25	100	 **2**	pA nA
I_B	Maximum Input Bias Current	(Notes 9, 10) $T_J = 25°C$ $T_J = 70°C$	50	200	 **4**	pA nA
R_{IN}	Input Resistance	$T_J = 25°C$	10^{12}			Ω
AVOL	Minimum Large Signal Voltage Gain	$V_O = \pm 10V$, $R_L = 2\,k\Omega$ (Note 10)	200	50	**25**	V/mV
V_O	Minimum Output Voltage Swing	$R_L = 10k$	±13.5	±12	**±12**	V
V_{CM}	Minimum Input Common Mode Voltage Range		+14.5 −11.5	+11 −11	**+11** **−11**	V V
CMRR	Minimum Common-Mode Rejection Ratio	$R_S \le 10\,k\Omega$	100	80	**80**	dB
PSRR	Minimum Supply Voltage Rejection Ratio	(Note 11)	100	80	**80**	dB
I_S	Maximum Supply Current			3.4	**3.4**	mA

AC Electrical Characteristics

The following specifications apply for $V^+ = +15V$ and $V^- = -15V$. **Boldface limits apply for T_{MIN} to T_{MAX};** all other limits $T_A = T_J = 25°C$.

Symbol	Parameter	Conditions	LF451CM			Units
			Typical (Note 6)	Tested Limit (Note 7)	Design Limit (Note 8)	
SR	Slew Rate	$A_V = +1$	13	8		V/μs
GBW	Minimum Gain-Bandwidth Product	f = 100 kHz	4	2.7		MHz
e_n	Equivalent Input Noise Voltage	$R_S = 100\Omega$, f = 1 kHz	25			$nV/\sqrt{Hz}$
i_n	Equivalent Input Noise Current	$R_S = 100\Omega$, f = 1 kHz	0.01			$pA/\sqrt{Hz}$

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its specified operating ratings.

Note 2: When the input voltage exceeds the power supplies, the current should be limited to 1 mA.

Note 3: The maximum power dissipation must be derated at elevated temperatures and is dictated by T_J MAX, θ_{JA} and the ambient temperature, T_A. The maximum allowable power dissipation at any temperature is $P_D = (T_J \text{ MAX} - T_A)/\theta_{JA}$ or the number given in the Absolute Maximum Ratings, whichever is lower. For guaranteed operation $T_{J\,max} = 125°C$. The typical thermal resistance (θ_{JA}) of the LF451CM when board-mounted is 170°C/W.

Note 5: See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" (Appendix D) for other methods of soldering surface mount devices.

Note 6: Typicals are at $T_J = 25°C$ and represent most likely parametric norm.

Note 7: Tested limits are guaranteed to National's AOQL (Average Outgoing Quality Level).

Note 8: Design limits are guaranteed to National's AOQL, but not 100% tested.

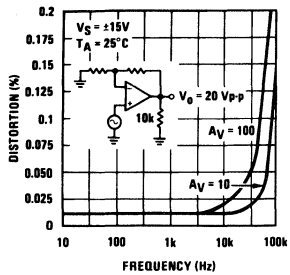
Note 9: The input bias currents are junction leakage currents which approximately double for every 10°C increase in the junction temperature T_J. Due to limited production test time, the input bias currents are correlated to junction temperature. In normal operation the junction temperature rises above the ambient temperature as a result of internal power dissipation, P_D. $T_J = T_A + \theta_{JA}P_D$ where θ_{JA} is the thermal resistance from junction to ambient.

Note 10: V_{OS}, I_B, AVOL, and I_{OS} are measured at $V_{CM} = 0V$.

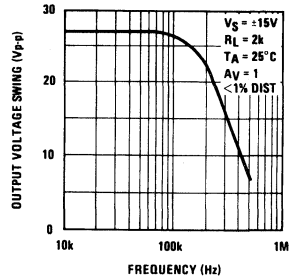
Note 11: Supply voltage rejection ratio is measured for both supply magnitudes increasing or decreasing simultaneously in accordance with common practice.

Typical Performance Characteristics

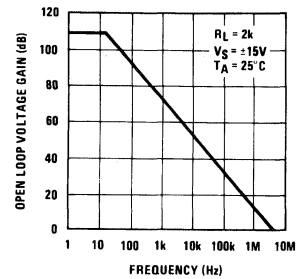
Distortion vs Frequency



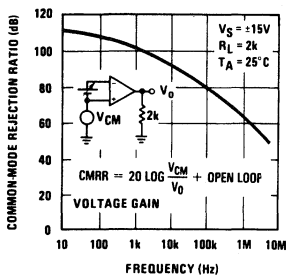
Undistorted Output Voltage Swing



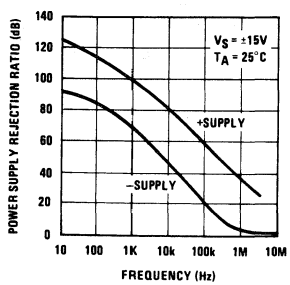
Open Loop Frequency Response



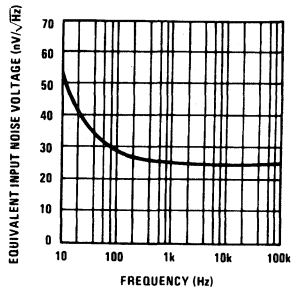
Common-Mode Rejection Ratio



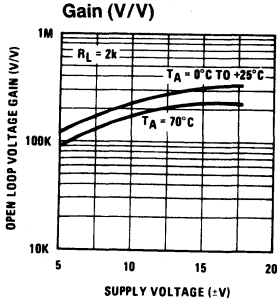
Power Supply Rejection Ratio



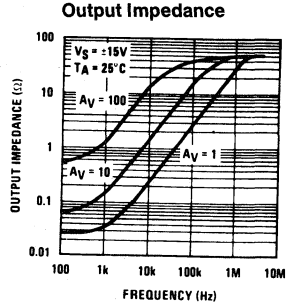
Equivalent Input Noise Voltage



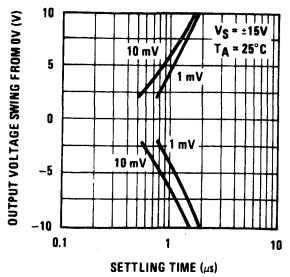
Open Loop Voltage Gain (V/V)



Output Impedance



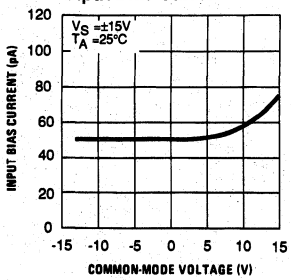
Inverter Settling Time



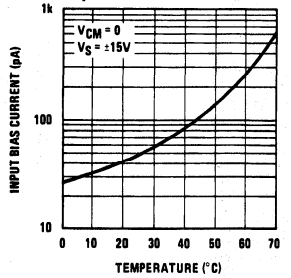
TL/H/9660–5

Typical Performance Characteristics (Continued)

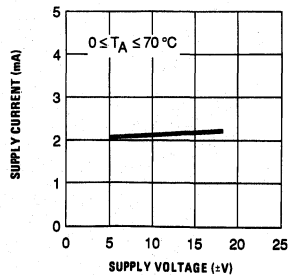
Input Bias Current



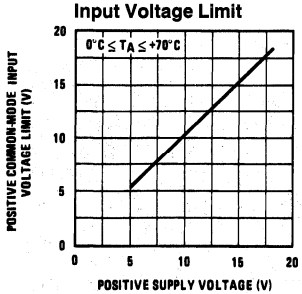
Input Bias Current



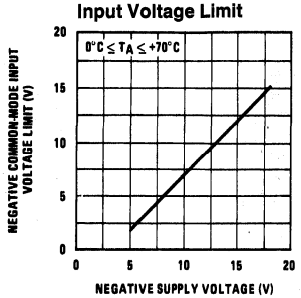
Supply Current



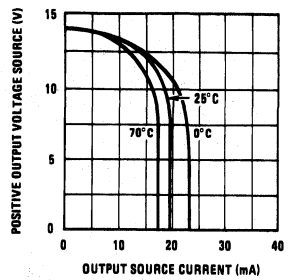
Positive Common-Mode Input Voltage Limit



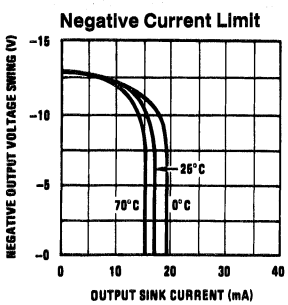
Negative Common-Mode Input Voltage Limit



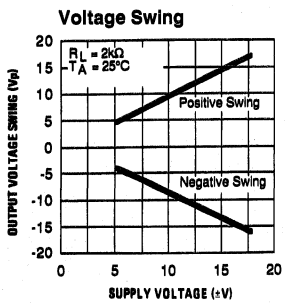
Positive Current Limit



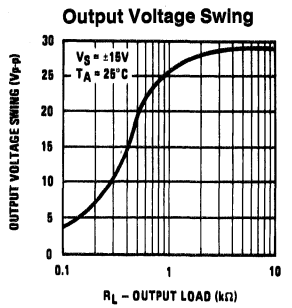
Negative Current Limit



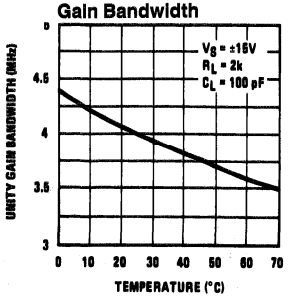
Voltage Swing



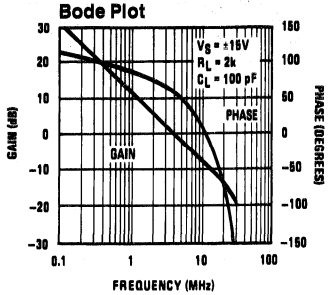
Output Voltage Swing



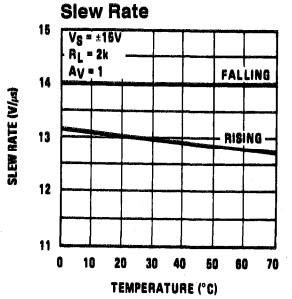
Gain Bandwidth



Bode Plot



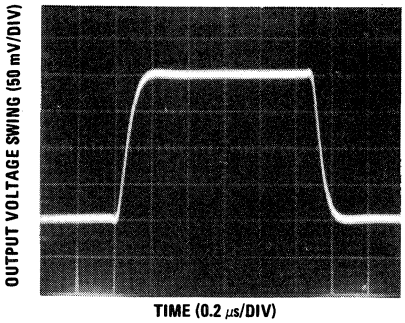
Slew Rate



TL/H/9660–4

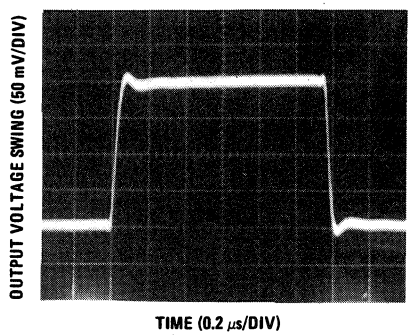
Pulse Response

Small Signal Inverting



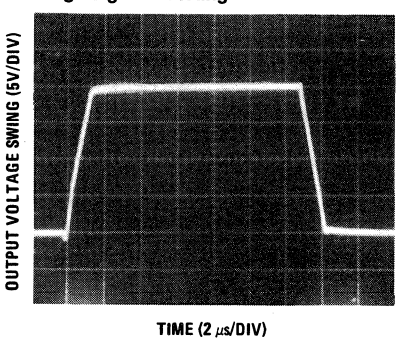
TL/H/9660–6

Small Signal Non-Inverting



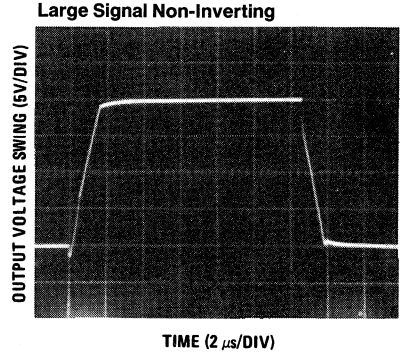
TL/H/9660–7

Large Signal Inverting



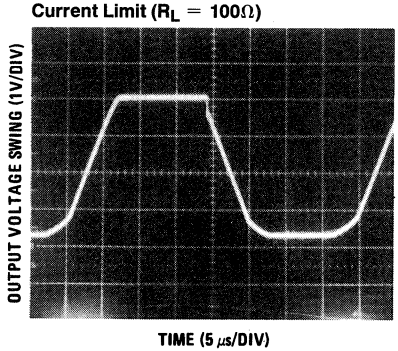
TL/H/9660–8

Large Signal Non-Inverting



TL/H/9660–9

Current Limit ($R_L = 100\Omega$)



TL/H/9660–10

Application Hints

The LF451CM is an op amp with an internally trimmed input offset voltage and JFET input devices (BI-FET II). These JFETs have large reverse breakdown voltages from gate to source and drain eliminating the need for clamps across the inputs. Therefore, large differential input voltages can easily be accommodated without a large increase in input current. The maximum differential input voltage is independent of the supply voltages. However, neither of the input voltages should be allowed to exceed the negative supply as this will cause large currents to flow which can result in a destroyed unit.

Exceeding the negative common-mode limit with the non-inverting input, or with both inputs, will force the output to a high state, potentially causing a reversal of phase to the output.

In neither case does a latch occur since raising the input back within the common-mode range again puts the input stage and thus the amplifier in a normal operating mode.

Application Hints (Continued)

Exceeding the positive common-mode limit on a single input will not change the phase of the output; however, if both inputs exceed the limit, the output of the amplifier will be forced to a high state.

The amplifier will operate with a common-mode input voltage equal to the positive supply; however, the gain bandwidth and slew rate may be decreased in this condition. When the negative common-mode voltage swings to within 3V of the negative supply, an increase in input offset voltage may occur.

The LF451 is biased by a zener reference which allows normal circuit operation on ±4V power supplies. Supply voltages less than these may result in lower gain bandwidth and slew rate.

The LF451 will drive a 2 kΩ load resistance to ±10V over the full temperature range of 0°C to +70°C. If the amplifier is forced to drive heavier load currents, however, an increase in input offset voltage may occur on the negative voltage swing and finally reach an active current limit on both positive and negative swings.

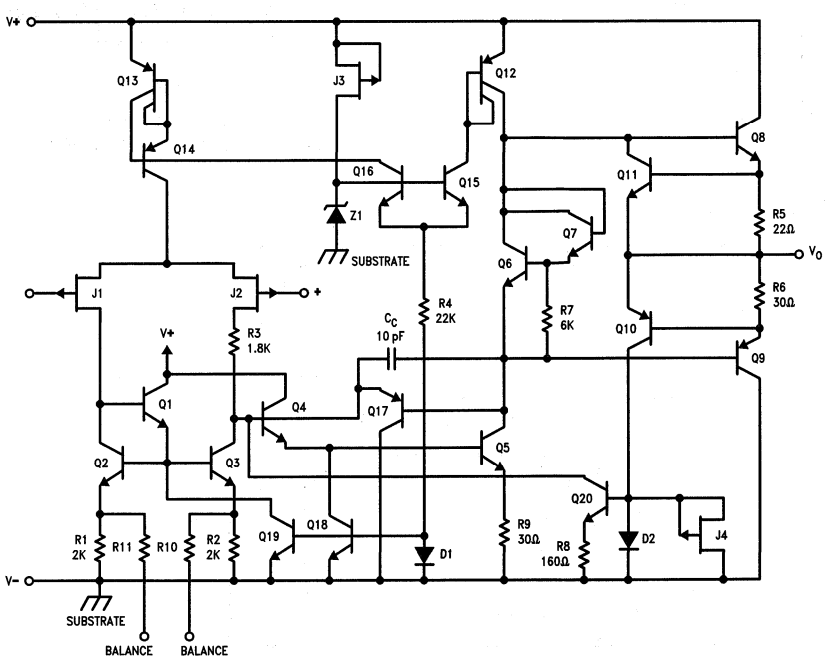
Precautions should be taken to ensure that the power supply for the integrated circuit never becomes reversed in polarity or that the unit is not inadvertently installed backwards in a socket as an unlimited current surge through the resulting forward diode within the IC could cause fusing of the internal conductors and result in a destroyed unit.

As with most amplifiers, care should be taken with lead dress, component placement and supply decoupling in order to ensure stability. For example, resistors from the output to an input should be placed with the body close to the input to minimize "pick-up" and maximize the frequency of the feedback pole by minimizing the capacitance from the input to ground.

A feedback pole is created when the feedback around any amplifier is resistive. The parallel resistance and capacitance from the input of the device (usually the inverting input) to AC ground set the frequency of the pole. In many instances the frequency of this pole is much greater than the expected 3 dB frequency of the closed loop gain and consequently there is negligible effect on stability margin. However, if the feedback pole is less than approximately 6 times the expected 3 dB frequency a lead capacitor should be placed from the output to the input of the op amp. The value of the added capacitor should be such that the RC time constant of this capacitor and the resistance it parallels is greater than or equal to the original feedback pole time constant.

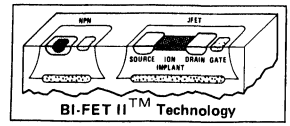
The benefit of the S.O. package results from its very small size. It follows, however, that the die inside the S.O. package is less protected from external physical forces than a die in a standard DIP would be, because there is so much less plastic in the S.O. Therefore, not following certain precautions when board mounting the LF451CM can put mechanical stress on the die, lead frame, and/or bond wires. This can cause shifts in the LF451CM's parameters, even causing them to exceed limits specified in the Electrical Characteristics. For recommended practices in LF451CM surface mounting refer to Application Note AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" and to Section 6 "Surface Mount" found in any Rev. 1 Linear Databook volume.

Detailed Schematic



TL/H/9660–11

National Semiconductor



LF453 Wide-Bandwidth Dual JFET-Input Operational Amplifiers

General Description

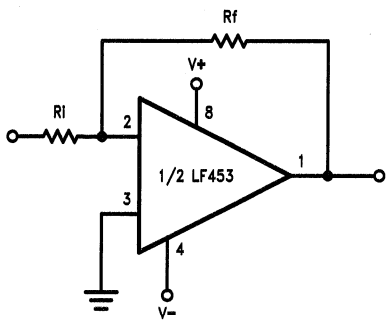
The LF453 is a low-cost, high-speed, dual JFET-input operational amplifier with an internally trimmed input offset voltage (BI-FET II technology). The device requires a low supply current and yet the amplifiers maintain a large gain bandwidth product and a fast slew rate. In addition, well matched high voltage JFET input devices provide very low input bias and offset currents. The LF453 is pin compatible with the standard LM1558, allowing designers to upgrade the overall performance of existing designs.

The LF453 may be used in such applications as high-speed integrators, fast D/A converters, sample-and-hold circuits and many other circuits requiring low input bias current, high input impedance, high slew rate and wide bandwidth.

Features

■ Internally trimmed offset voltage	5.0 mV (max)
■ Low input bias current	50 pA (typ)
■ Low input noise current	0.01 pA/$\sqrt{\text{Hz}}$ (typ)
■ Wide gain bandwidth	4 MHz (typ)
■ High slew rate	13 V/μs (typ)
■ Low supply current	6.5 mA (max)
■ High input impedance	$10^{12}\Omega$ (typ)
■ Low total harmonic distortion A_V = 10, R_L = 10k, V_O = 20 V_{p-p}, f = 20 Hz–20 kHz	<0.02% (typ)
■ Low 1/f noise corner	50 Hz (typ)
■ Fast settling time to 0.01%	2 μs (typ)

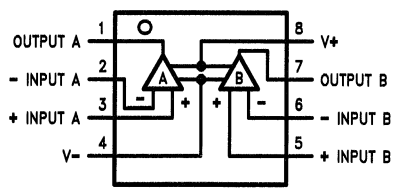
Typical Connection



TL/H/9710–1

Connection Diagram

SO Package

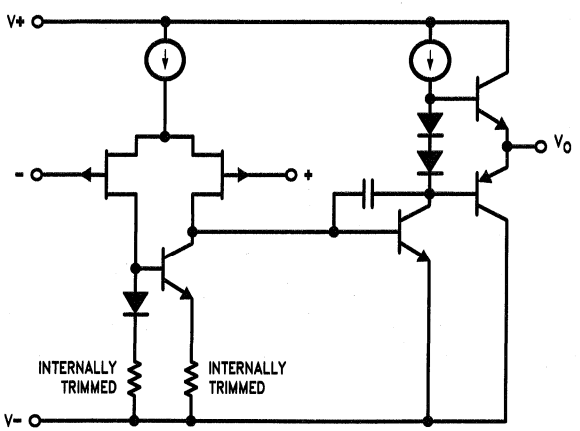


TL/H/9710–2

Top View

Order Number LF453CM
See NS Package Number M08A

Simplified Schematic



TL/H/9710–3

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage ($V^+ - V^-$)	36V
Input Voltage Range	$V^- \le V_{IN} \le V^+$
Differential Input Voltage (Note 2)	±30V
Junction Temperature (T_J MAX)	150°C
Output Short Circuit Duration	Continuous
Power Dissipation (Note 3)	500 mW
ESD Tolerance	TBD
Soldering Information (Note 4)	
SO Package: Vapor Phase (60 sec.)	215°C
Infrared (15 sec.)	220°C

Operating Ratings (Note 1)

Temperature Range	$T_{MIN} \le T_A \le T_{MAX}$
LF453CM	0°C ≤ T_A +70°C
Junction Temperature ($T_{J\,max}$)	125°C
Supply Voltage ($V^+ - V^-$)	10V to 32V

DC Electrical Characteristics

The following specifications apply for $V^+ = +15V$ and $V^- = -15V$. **Boldface limits apply for T_{MIN} to T_{MAX}**; all other limits $T_A = T_J = 25°C$.

Symbol	Parameter	Conditions	LF453CM			Units
			Typical (Note 5)	Tested Limit (Note 6)	Design Limit (Note 7)	
V_{OS}	Maximum Input Offset Voltage	$R_S = 10\,k\Omega$, (Note 9)		5		mV
I_{OS}	Maximum Input Offset Current	(Notes 8, 9) $T_J = 25°C$ $T_J = 70°C$	25	100	 **2**	pA nA
I_B	Maximum Input Bias Current	(Notes 8, 9) $T_J = 25°C$ $T_J = 70°C$	50	200	 **4**	pA nA
R_{IN}	Input Resistance	$T_J = 25°C$	10^{12}			Ω
AVOL	Minimum Large Signal Voltage Gain	$V_O = \pm 10V$, $R_L = 2\,k\Omega$ (Note 9)	200	50	**25**	V/mV
V_O	Minimum Output Voltage Swing	$R_L = 10k$	±13.5	±12	**±12**	V
V_{CM}	Minimum Input Common Mode Voltage Range		+14.5 −11.5	+11 −11	**+11** **−11**	V V
CMRR	Minimum Common-Mode Rejection Ratio	$R_S \le 10\,k\Omega$	100	80	**80**	dB
PSRR	Minimum Supply Voltage Rejection Ratio	(Note 10)	100	80	**80**	dB
I_S	Maximum Supply Current			6.5	**6.5**	mA

AC Electrical Characteristics

The following specifications apply for $V^+ = +15V$ and $V^- = -15V$. Limits apply for $T_A = T_J = 25°C$.

Symbol	Parameter	Conditions	LF453CM			Units
			Typical (Note 5)	Tested Limit (Note 6)	Design Limit (Note 7)	
SR	Slew Rate	$A_V = +1$	13	8		V/μs
GBW	Minimum Gain-Bandwidth Product	f = 100 kHz	4	2.7		MHz
e_n	Equivalent Input Noise Voltage	$R_S = 100\Omega$, f = 1 kHz	25			$nV/\sqrt{Hz}$
i_n	Equivalent Input Noise Current	$R_S = 100\Omega$, f = 1 kHz	0.01			$pA/\sqrt{Hz}$

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its specified operating ratings.

Note 2: When the input voltage exceeds the power supplies, the current should be limited to 1 mA.

Note 3: The maximum power dissipation must be derated at elevated temperatures and is dictated by T_J MAX, Θ_{JA} and the ambient temperature, T_A. The maximum allowable power dissipation at any temperature is $P_D = (T_J\,MAX - T_A)/\Theta_{JA}$ or the number given in the Absolute Maximum Ratings, whichever is lower. For guaranteed operation $T_{J\,max} = 125°C$. The typical thermal resistance (Θ_{JA}) of the LF453CM when board-mounted is 160°C/W.

Note 4: See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" (section titled "Surface Mount") for other methods of soldering surface mount devices.

Note 5: Typicals are at $T_J = 25°C$ and represent most likely parametric norm.

Note 6: Tested limits are guaranteed to National's AOQL (Average Outgoing Quality Level).

Note 7: Design limits are guaranteed to National's AOQL, but not 100% tested.

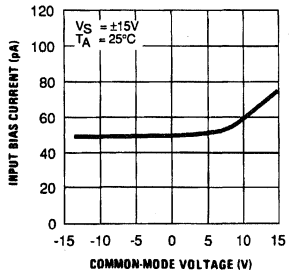
Note 8: The input bias currents are junction leakage currents which approximately double for every 10°C increase in the junction temperature T_J. Due to limited production test time, the input bias currents are correlated to junction temperature. In normal operation the junction temperature rises above the ambient temperature as a result of internal power dissipation, P_D. $T_J = T_A + \Theta_{JA} P_D$ where Θ_{JA} is the thermal resistance from junction to ambient.

Note 9: V_{OS}, I_B, AVOL and I_{OS} are measured at $V_{CM} = 0V$.

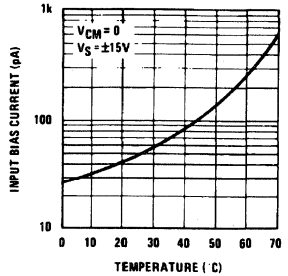
Note 10: Supply voltage rejection ratio is measured for both supply magnitudes increasing or decreasing simultaneously in accordance with common practice.

Typical Performance Characteristics

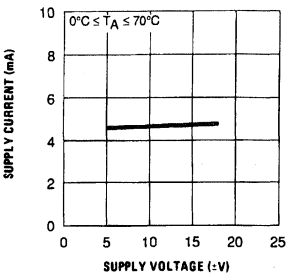
Input Bias Current



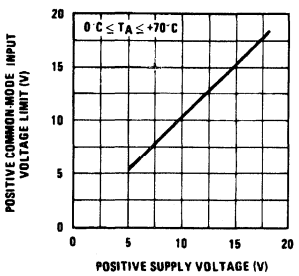
Input Bias Current



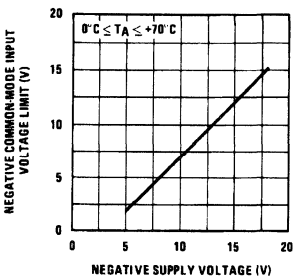
Supply Current



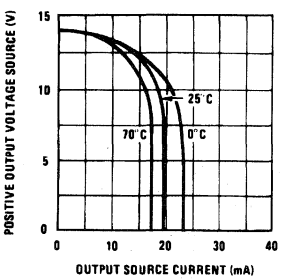
Positive Common-Mode Input Voltage Limit



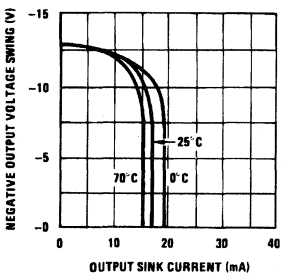
Negative Common-Mode Input Voltage Limit



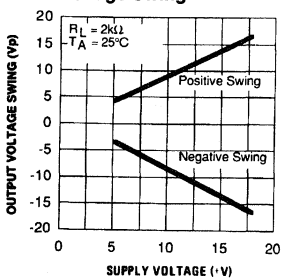
Positive Current Limit



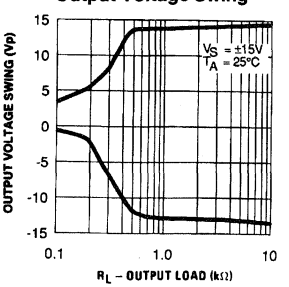
Negative Current Limit



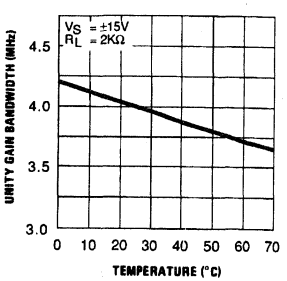
Voltage Swing



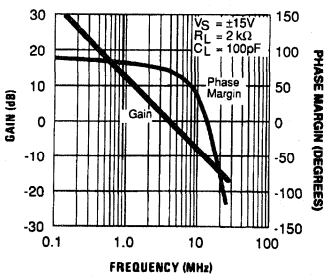
Output Voltage Swing



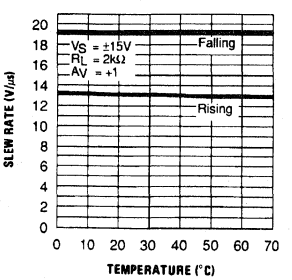
Gain Bandwidth



Bode Plot



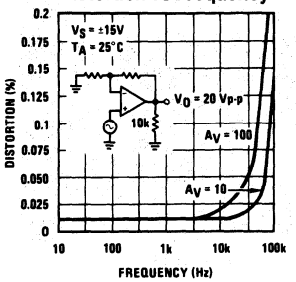
Slew Rate



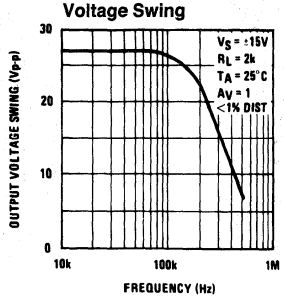
TL/H/9710–4

Typical Performance Characteristics (Continued)

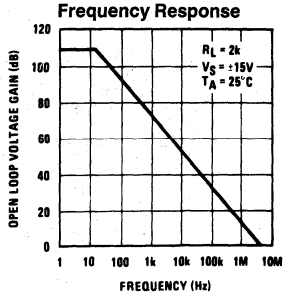
Distortion vs Frequency



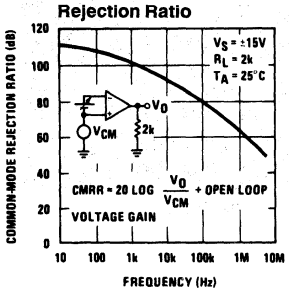
Undistorted Output Voltage Swing



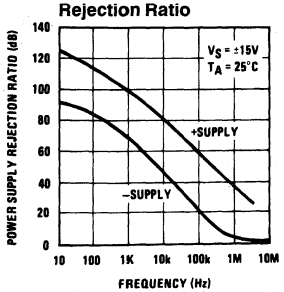
Open Loop Frequency Response



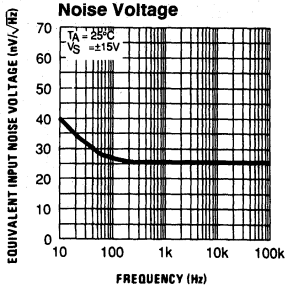
Common-Mode Rejection Ratio



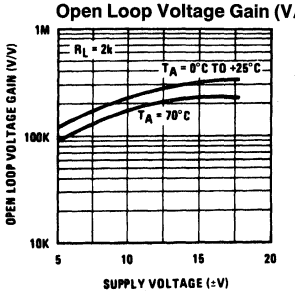
Power Supply Rejection Ratio



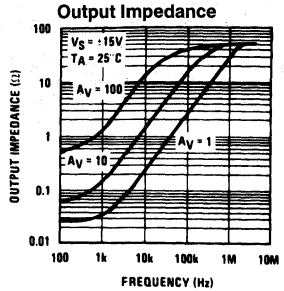
Equivalent Input Noise Voltage



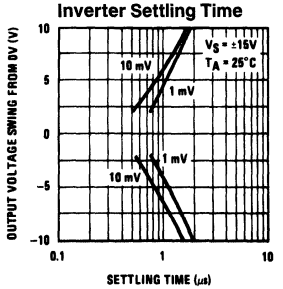
Open Loop Voltage Gain (V/V)



Output Impedance



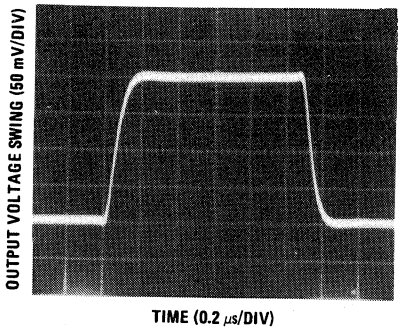
Inverter Settling Time



TL/H/9710–5

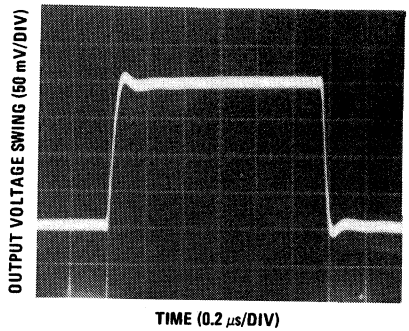
Pulse Response

Small Signal Inverting



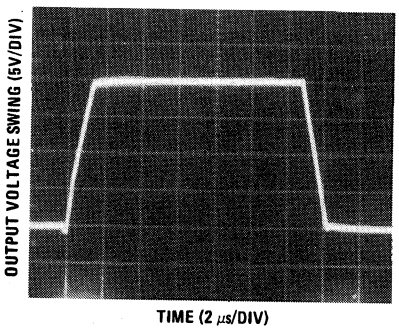
TL/H/9710–6

Small Signal Non-Inverting



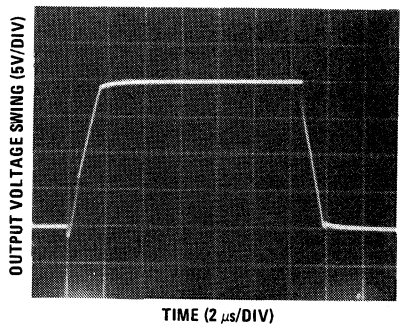
TL/H/9710–7

Large Signal Inverting



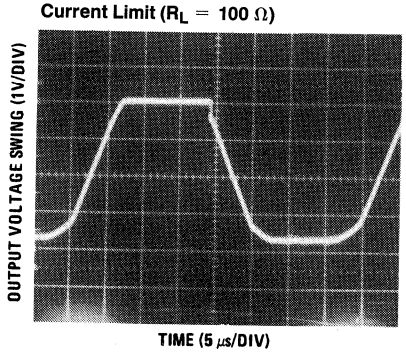
TL/H/9710–8

Large Signal Non-Inverting



TL/H/9710–9

Current Limit (R_L = 100 Ω)



TL/H/9710–10

Application Hints

These devices are op amps with an internally trimmed input offset voltage and JFET input devices (BI-FET II). These JFETs have large reverse breakdown voltages from gate to source and drain eliminating the need for clamps across the inputs. Therefore, large differential input voltages can easily be accommodated without a large increase in input current. The maximum differential input voltage is independent of the supply voltages. However, neither of the input voltages should be allowed to exceed the negative supply as this will cause large currents to flow which can result in a destroyed unit.

Exceeding the negative common-mode limit with the non-inverting input, or with both inputs, will force the output to a high state, potentially causing a reversal of phase to the output. In neither case does a latch occur since raising the input back within the common-mode range again puts the input stage and thus the amplifier in a normal operating mode.

Exceeding the positive common-mode limit on a single input will not change the phase of the output; however, if both inputs exceed the limit, the output of the amplifier will be forced to a high state.

The amplifiers will operate with a common-mode input voltage equal to the positive supply; however, the gain bandwidth and slew rate may be decreased in this condition. When the negative common-mode voltage swings to within 3V of the negative supply, an increase in input offset voltage may occur.

Each amplifier is individually biased by a zener reference which allows normal circuit operation on ± 5V power supplies. Supply voltages less than these may result in lower gain bandwidth and slew rate.

The amplifiers will drive a 2 kΩ load resistance to ± 10V over the full temperature range of 0°C to +70°C. If the amplifier is forced to drive heavier load currents, however, an increase in input offset voltage may occur on the negative voltage swing and finally reach an active current limit on both positive and negative swings.

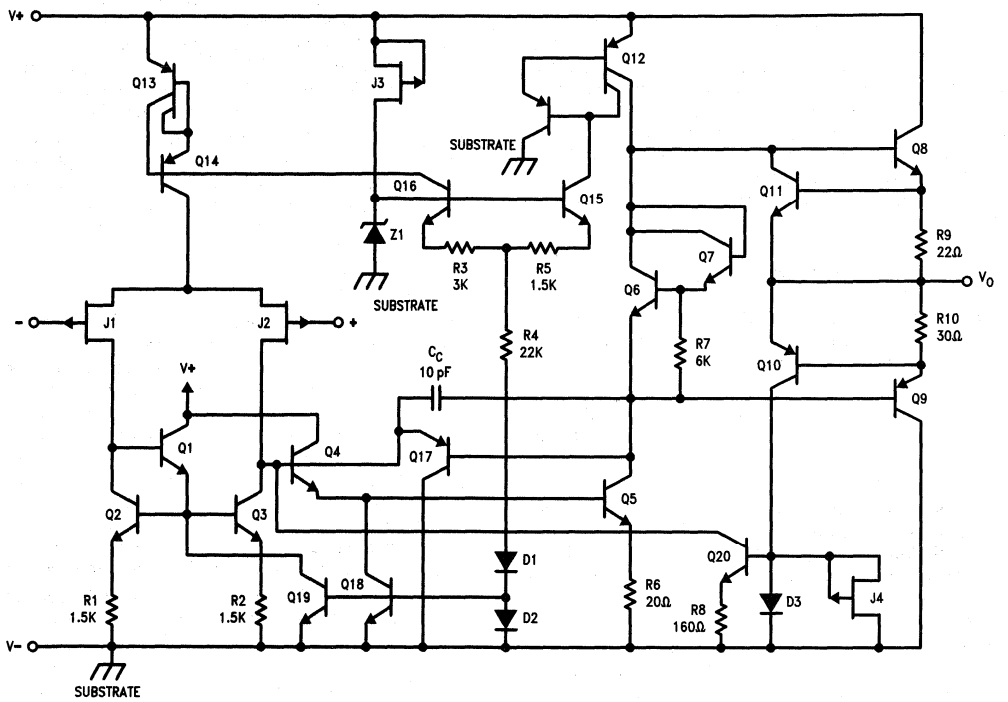
Precautions should be taken to ensure that the power supply for the integrated circuit never becomes reversed in polarity or that the unit is not inadvertently installed backwards in a socket as an unlimited current surge through the resulting forward diode within the IC could cause fusing of the internal conductors and result in a destroyed unit.

As with most amplifiers, care should be taken with lead dress, component placement and supply decoupling in order to ensure stability. For example, resistors from the output to an input should be placed with the body close to the input to minimize "pick-up" and maximize the frequency of the feedback pole by minimizing the capacitance from the input to ground.

A feedback pole is created when the feedback around any amplifier is resistive.The parallel resistance and capacitance from the input of the device (usually the inverting input) to AC ground set the frequency of the pole. In many instances the frequency of this pole is much greater than the expected 3 dB frequency of the closed loop gain and consequently there is negligible effect on stability margin. However, if the feedback pole is less than approximately 6 times the expected 3 dB frequency a lead capacitor should be placed from the output to the input of the op amp. The value of the added capacitor should be such that the RC time constant of this capacitor and the resistance it parallels is greater than or equal to the original feedback pole time constant.

The benefit of the SO package results from its very small size. It follows, however, that the die inside the SO package is less protected from external physical forces than a die in a standard DIP would be, because there is so much less plastic in the SO. Therefore, not following certain precautions when board mounting the LF453CM can put mechanical stress on the die, lead frame, and/or bond wires. This can cause shifts in the LF453CM's parameters, even causing them to exceed limits specified in the Electrical Characteristics. For recommended practices in LF453CM surface mounting refer to Application Note AN450 "Surface Mounting Methods and Their Effect on Product Reliability" and to the section titled "Surface Mount" found in any Rev 1. Linear Databook volume.

Detailed Schematic



TL/H/9710–11

National Semiconductor

PRELIMINARY

LH0003
Wide Bandwidth Operational Amplifier

General Description

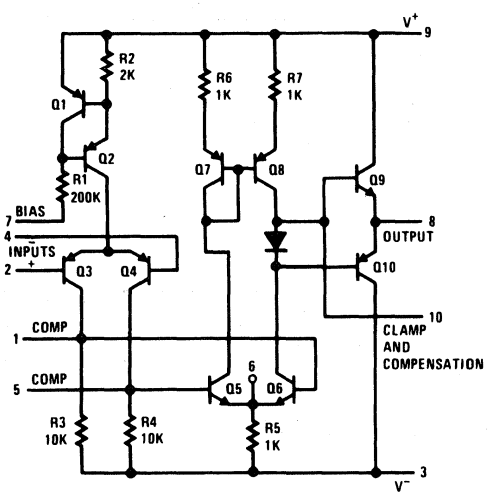
The LH0003/LH0003C is a general purpose operational amplifier which features: slewing rate up to 70 V/μs, a gain bandwidth of up to 30 MHz, and high output currents.

The LH0003 is specified for operation over the −55°C to +125°C military temperature range. The LH0003C is specified for operation over the 0°C to +85°C temperature range.

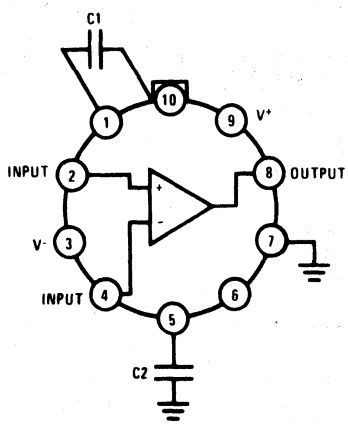
Features

■ Very low offset voltage	Typically 0.4 mV
■ Large output swing	> ±10V into 100Ω load
■ High CMRR	Typically >90 dB
■ Good large signal frequency response	50 kHz to 400 kHz depending on compensation

Schematic and Connection Diagrams



TL/H/5561–1



TL/H/5561–2

Top View

Order Number LH0003H or LH0003CH
See NS Package Number H10G

Typical Compensation

Circuit Gain	C_1 pF	C_2 pF	Slew Rate $R_L > 200\Omega$, V/μsec	Full Output Frequency $R_L > 200\Omega$ $V_{OUT} = \pm 10V$
≥40	0	0	70	400 kHz
≥10	5	30	30	350 kHz
≥ 5	15	30	15	250 kHz
≥ 2	50	50	5	100 kHz
≥ 1	90	90	2	50 kHz

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications. (Note 3)

Supply Voltage	±20V
Power Dissipation	See Curve
Differential Input Voltage	±7V
Input Voltage	Equal to Supply
Load Current	120 mA
Operating Temperature Range	
LH0003	−55°C to +125°C
LH0003C	0°C to +85°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec.)	260°C

ESD rating to be determined.

Electrical Characteristics (Notes 1 & 2)

Parameter	Conditions	Min	Typ	Max	Units
Input Offset Voltage	$R_S < 100\Omega$		0.4	3.0	mV
Input Offset Current			0.02	0.2	μA
Input Bias Current			0.4	2.0	μA
Supply Current	$V_S = \pm 20V$		1.2	3	mA
Voltage Gain	$R_L = 100k, V_S = \pm 15V, V_{OUT} = \pm 10V$	20	70		V/mV
	$R_L = 2k, V_S = \pm 15V, V_{OUT} = \pm 10V$	15	40		V/mV
Output Voltage Swing	$V_S = \pm 15V, R_L = 100\Omega$	±10	±12		V
Input Resistance			100		kΩ
Average Temperature Coefficient of Offset Voltage	$R_S \leq 100\Omega$		4		μV/°C
Average Temperature Coefficient of Bias Current			8		nA/°C
CMRR	$R_S < 100\Omega, V_S = \pm 15V, V_{IN} = \pm 10V$	70	90		dB
PSRR	$R_S < 100\Omega, V_S = \pm 15V, \Delta V = 5V$ to 20V	70	90		dB
Equivalent Input Noise Voltage	$R_S = 100\Omega$, f = 10 kHz to 100 kHz $V_S = \pm 15V$ dc		1.8		μVrms

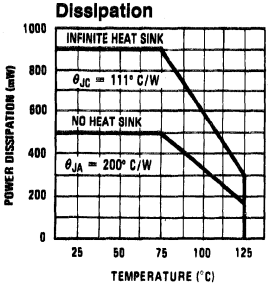
Note 1: These specifications apply for Pin 7 grounded, for $\pm 5V < V_S < \pm 20V$, with capacitor C_1 = 90 pF from Pin 1 to Pin 10 and C_2 = 90 pF from Pin 5 to ground, over the specified operating temperature range, unless otherwise specified.

Note 2: Typical values are for T_A = 25°C unless otherwise specified.

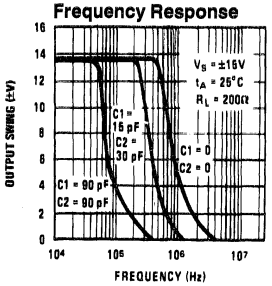
Note 3: Refer to RETS0003X for LH0003H military specifications.

Typical Performance Characteristics

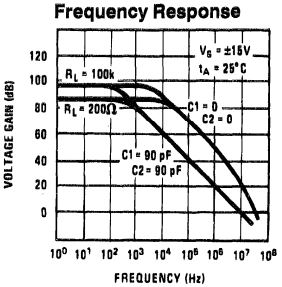
Maximum Power Dissipation



Large Signal Frequency Response



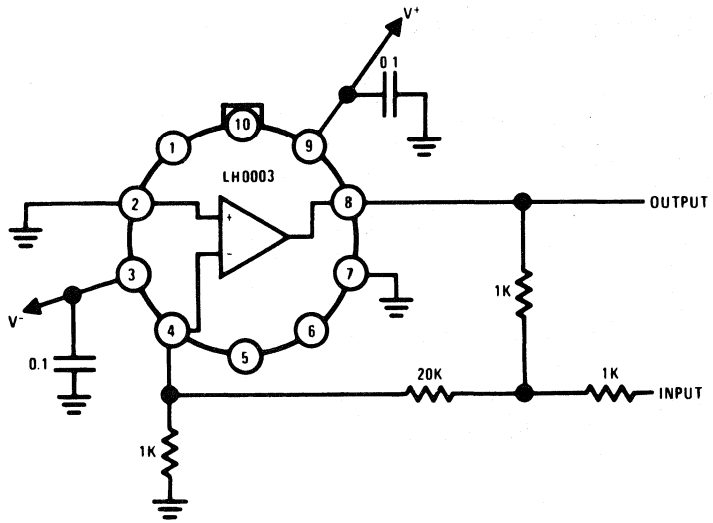
Open Loop Frequency Response



TL/H/5561–5

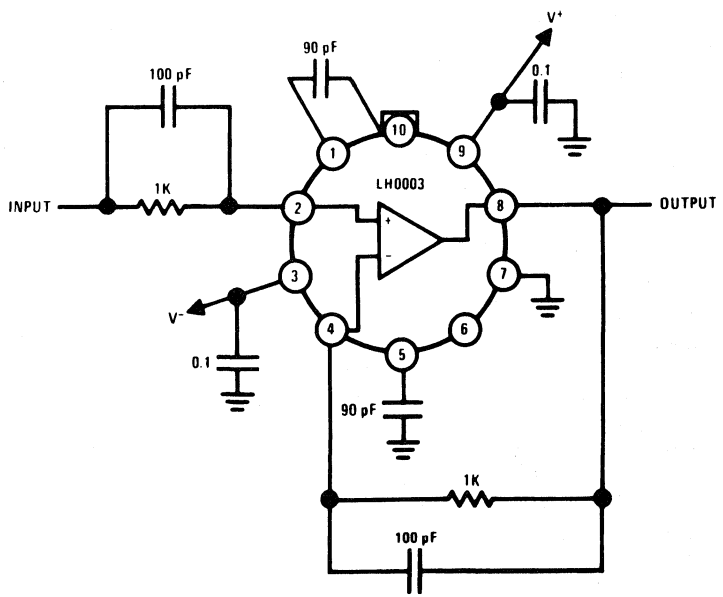
Typical Applications

High Slew Rate Unity Gain Inverting Amplifier



TL/H/5561–3

Unity Gain Follower



TL/H/5561–4

National Semiconductor

LH0004 High Voltage Operational Amplifier

General Description

The LH0004 is a general purpose operational amplifier designed to operate from supply voltages up to ±40V. The device dissipates extremely low quiescent power, typically 8 mW at 25°C and V_S = ±40V.

The LH0004's high gain and wide range of operating voltages make it ideal for applications requiring large output swing and low power dissipation.

The LH0004 is specified for operation over the −55°C to +125°C military temperature range. The LH0004C is specified for operation over the 0°C to +85°C temperature range.

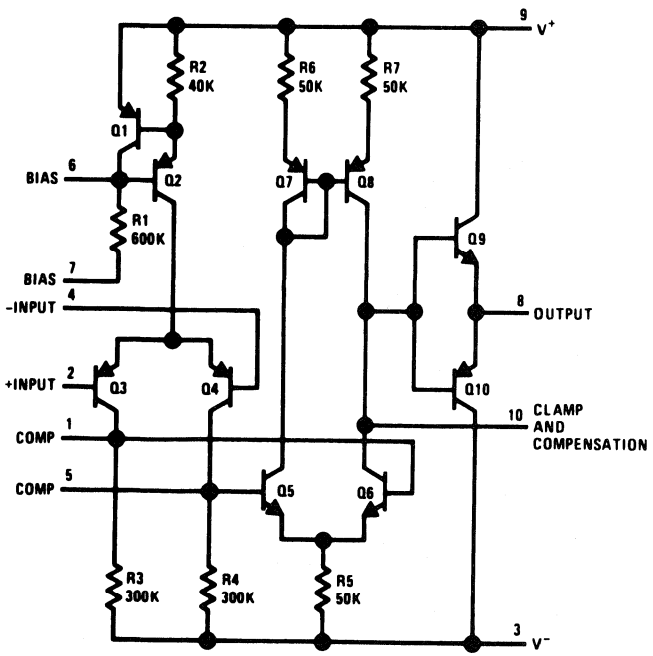
Features

- Capable of operation over the range of ±5V to ±40V
- Large output voltage typically ±35V for the LH0004 and ±33V for the LH0004C into a 2 kΩ load with ±40V supplies
- Low input offset voltage typically 0.3 mV
- Frequency compensation with 2 small capacitors
- Low power consumption 8 mW at ±40V

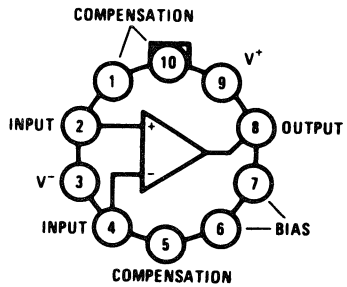
Applications

- High voltage power supply
- Resolver excitation
- Wideband high voltage amplifier
- Transducer power supply

Schematic and Connection Diagrams



TL/H/5559–1



TL/H/5559–2

Note: Pin 7 must be grounded or connected to a voltage at least 5V more negative than the positive supply (Pin 9). Pin 7 may be connected to the negative supply; however, the standby current will be increased. A resistor may be inserted in series with Pin 7 to Pin 9. The value of the resistor should be a maximum of 100 kΩ per volt of potential between Pin 3 and Pin 9.

Order Number LH0004H, LH0004H-MIL or LH0004CH
See NS Package Number H10G

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications. (Note 2)

Supply Voltage	±45V
Power Dissipation (see Curve)	400 mW
Differential Input Voltage	±7V
Input Voltage	Equal to Supply
Short Circuit Duration	3 sec
Operating Temperature Range	
LH0004	−55°C to +125°C
LH0004C	0°C to +85°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec.)	260°C

ESD rating to be determined.

Electrical Characteristics (Note 1)

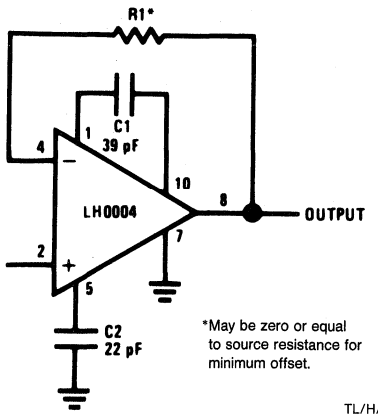
Parameter	Conditions	LH0004			LH0004C			Units
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	$R_S \leq 100\Omega$, $T_A = 25°C$ $R_S \leq 100\Omega$		0.3	1.0 2.0		0.3	1.5 3.0	mV
Input Bias Current	$T_A = 25°C$		20	100 300		30	120 300	nA
Input Offset Current	$T_A = 25°C$		3	20 100		10	45 150	nA
Positive Supply Current	$V_S = \pm 40V$, $T_A = 25°C$ $V_S = \pm 40V$		110	150 175		110	150 175	μA
Negative Supply Current	$V_S = \pm 40V$, $T_A = 25°C$ $V_S = \pm 40V$		80	100 135		80	100 135	μA
Voltage Gain	$V_S = \pm 40V$, $R_L = 100k$, $T_A = 25°C$ $V_{OUT} = \pm 30V$	30	60		30	60		V/mV
	$V_S = \pm 40V$, $R_L = 100k$ $V_{OUT} = \pm 30V$	10			10			V/mV
Output Voltage	$V_S = \pm 40V$, $R_L = 10k$		±35	±30		±33	±30	V
CMRR	$V_S = \pm 40V$, $R_S \leq 5k$ $V_{IN} = \pm 33V$	70	90		70	90		dB
PSRR	$V_S = \pm 40V$, $R_S \leq 5k$ $\Delta V = 20V$ to $40V$	70	90		70	90		dB
Average Temperature Coefficient Offset Voltage	$R_S \leq 100\Omega$		4.0			4.0		μV/°C
Average Temperature Coefficient of Offset Current			0.4			0.4		nA/°C
Equivalent Input Noise Voltage	$R_S = 100\Omega$, $V_S = \pm 40V$ $f = 500$ Hz to 5 kHz, $T_A = 25°C$		3.0			3.0		μVrms

Note 1: These specifications apply for $\pm 5V \leq V_S \leq \pm 40V$, Pin 7 grounded, with capacitors C1 = 39 pF between Pin 1 and Pin 10, C2 = 22 pF between Pin 5 and ground, −55°C to +125°C for the LH0004, and 0°C to +85°C for the LH0004C unless otherwise specified.

Note 2: Refer to RETS0004X for LH0004H military specifications.

Typical Applications

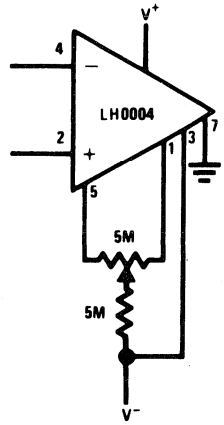
Voltage Follower



*May be zero or equal to source resistance for minimum offset.

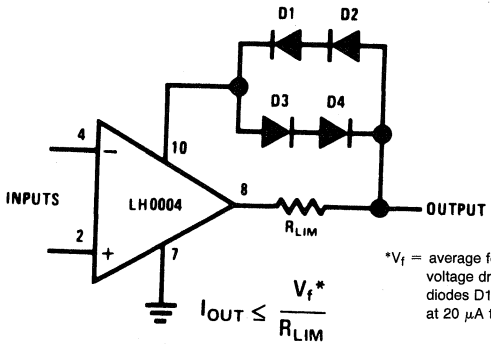
TL/H/5559-3

Input Offset Voltage Adjust



TL/H/5559-4

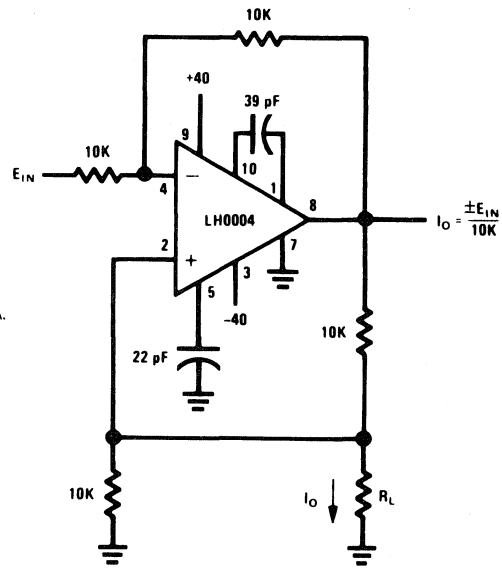
External Current Limiting Method



*V_f = average forward voltage drop of diodes D1 to D4 at 20 μA to 50 μA.

TL/H/5559-5

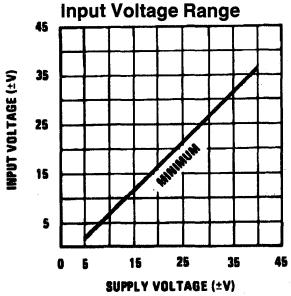
High Compliance Current Source



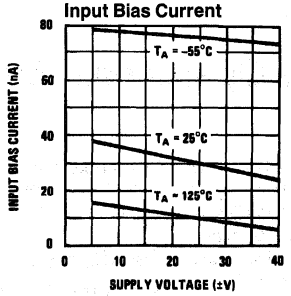
TL/H/5559-6

Typical Performance Characteristics

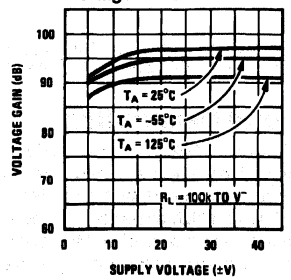
Input Voltage Range



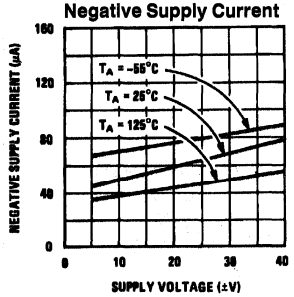
Input Bias Current



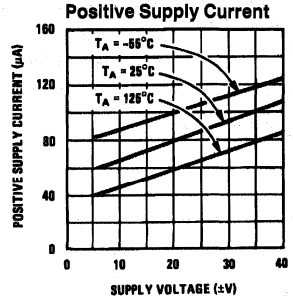
Voltage Gain



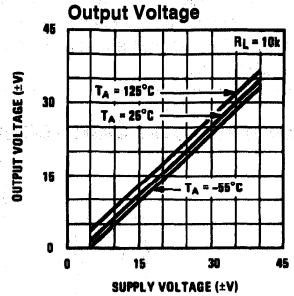
Negative Supply Current



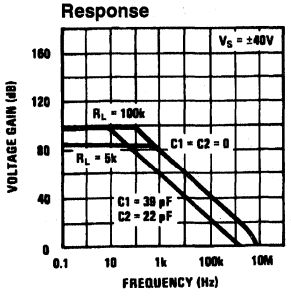
Positive Supply Current



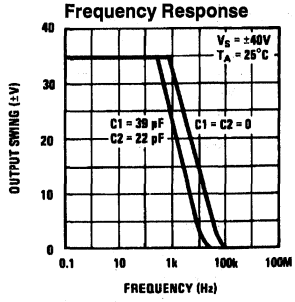
Output Voltage



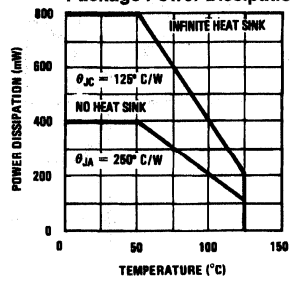
Open Loop Frequency Response



Large Signal Frequency Response



Package Power Dissipation



TL/H/5559–7

National Semiconductor

LH0024 High Slew Rate Operational Amplifier

General Description

The LH0024/LH0024C is a very wide bandwidth, high slew rate operational amplifier intended to fulfill a wide variety of high speed applications such as buffers to A to D and D to A converters and high speed comparators. The device exhibits useful gain in excess of 50 MHz making it possible to use in video applications requiring higher gain accuracy than is usually associated with such amplifiers.

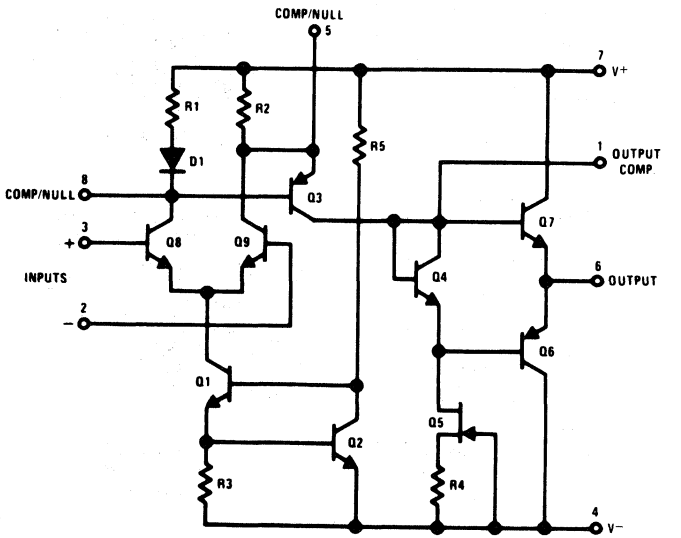
The LH0024/LH0024C's combination of wide bandwidth and high slew rate make it an ideal choice for a variety of high speed applications including active filters, oscillators, and comparators as well as many high speed general purpose applications.

The LH0024 is guaranteed over the temperature range −55°C to +125°C, whereas the LH0024C is guaranteed −25°C to +85°C.

Features

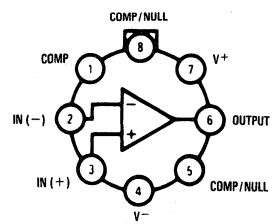
- Very high slew rate—500 V/μs at $A_V = +1$
- Wide small signal bandwidth—70 MHz
- Wide large signal bandwidth—15 MHz
- High output swing—±12V into 1k
- Low input offset—2 mV
- Pin compatible with standard IC op amps

Schematic and Connection Diagrams



TL/K/5552–1

Metal Can Package



TL/K/5552–2

Top View

Note: For heat sink use Thermalloy 2230-5 series.

Order Number LH0024H, LH0024H-MIL or LH0024CH
See NS Package Number H08B

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications. (Note 2)

Supply Voltage	±18V
Input Voltage	Equal to Supply
Differential Input Voltage	±5V
Power Dissipation	600 mW
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec.)	260°C

ESD rating to be determined.

Operating Temperature Range

LH0024	−55°C to +125°C
LH0024C	−25°C to +85°C

DC Electrical Characteristics (Note 1)

Parameter	Conditions	LH0024			LH0024C			Units
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	$R_S = 50\Omega$, $T_A = 25°C$ $R_S = 50\Omega$		2.0	4.0 6.0		5.0	8.0 10.0	mV mV
Average Temperature Coefficient of Input Offset Voltage	$V_S = \pm15V$, $R_S = 50\Omega$ −55°C to 125°C		−20			−25		µV/°C
Input Offset Current	$T_A = 25°C$		2.0	5.0 10.0		4.0	15.0 20.0	µA µA
Input Bias Current	$T_A = 25°C$		15	30 40		18	40 50	µA µA
Supply Current			12.5	15		12.5	15	mA
Large Signal Voltage Gain	$V_S = \pm15V$, $R_L = 1k$, $T_A = 25°C$ $V_S = \pm15V$, $R_L = 1k$	4 3	5		3 2.5	4		V/mV V/mV
Input Voltage Range	$V_S = \pm15V$	±12	±13		±12	±13		V
Output Voltage Swing	$V_S = \pm15V$, $R_L = 1k$, $T_A = 25°C$ $V_S = \pm15V$, $R_L = 1k$	±12 ±10	±13		±10 ±10	±13		V V
Slew Rate	$V_S = \pm15V$, $R_L = 1k$, $C_1 = C_2 = 30$ pF, $A_V = +1$, $T_A = 25°C$	400	500		250	400		V/µs
Common-Mode Rejection Ratio	$V_S = \pm15V$, $\Delta V_{IN} = \pm10V$, $R_S = 50\Omega$		60			60		dB
Power Supply Rejection Ratio	$\pm5V \leq V_S \leq \pm18V$, $R_S = 50\Omega$		60			60		dB

Note 1: These specifications apply for $V_S = \pm15V$ and −55°C to +125°C for the LH0024 and −25°C to +85°C for the LH0024C.

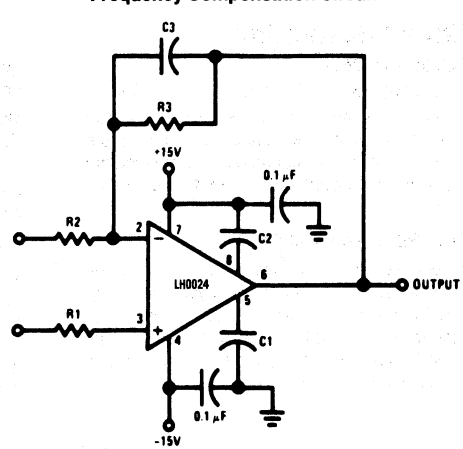
Note 2: Refer to RETS0024 for LH0024H military specifications.

Frequency Compensation

TABLE I

Closed Loop Gain	C_1	C_2	C_3
100	0	0	0
20	0	0	0
10	0	20 pF	1 pF
1	30 pF	30 pF	3 pF

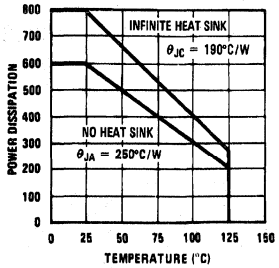
Frequency Compensation Circuit



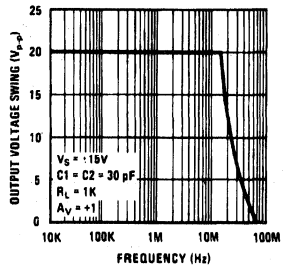
TL/K/5552–6

Typical Performance Characteristics

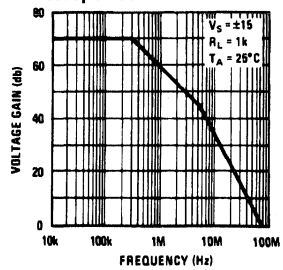
Maximum Power Dissipation



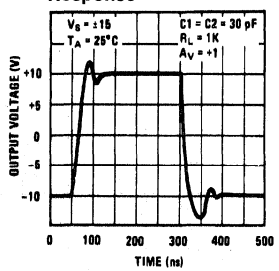
Large Signal Frequency Response



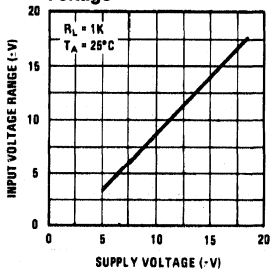
Open Loop Frequency Response



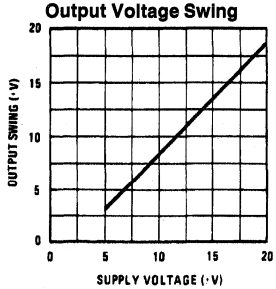
Voltage Follower Pulse Response



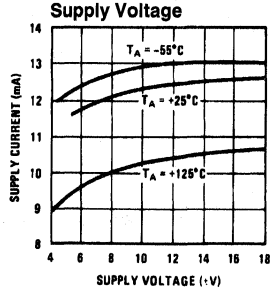
Input Voltage vs Supply Voltage



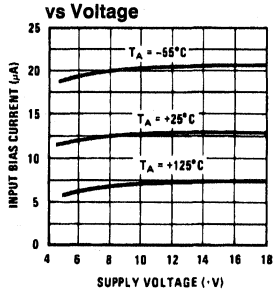
Output Voltage Swing



Supply Current vs Supply Voltage



Input Bias Current vs Voltage



TL/K/5552–7

Applications Information

LAYOUT CONSIDERATIONS

The LH0024/LH0024C, like most high speed circuitry, is sensitive to layout and stray capacitance. Power supplies should be by-passed as near the device as is practicable with at least 0.01 μF disc type capacitors. Compensating capacitors should also be placed as close to device as possible.

COMPENSATION RECOMMENDATIONS

Compensation schemes recommended in Table 1 work well under typical conditions. However, poor layout and long lead lengths can degrade the performance of the LH0024 or cause the device to oscillate. Slight adjustments in the values for C1, C2, and C3 may be necessary for a given layout. In particular, when operating at a gain of −1, C3 may require adjustment in order to perfectly cancel the input capacitance of the device.

When operating the LH0024/LH0024C at a gain of +1, the value of R1 should be at least 1 kΩ.

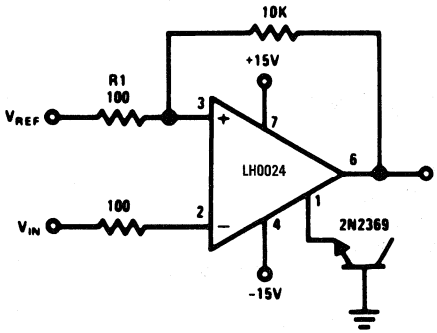
The case of the LH0024 is electrically isolated from the circuit; hence, it may be advantageous to drive the case in order to minimize stray capacitances.

HEAT SINKING

The LH0024/LH0024C is specified for operation without the use of an explicit heat sink. However, internal power dissipation does cause a significant temperature rise. Improved offset voltage drift can be obtained by limiting the temperature rise with a clip-on heat sink such as the Thermalloy 2228B or equivalent.

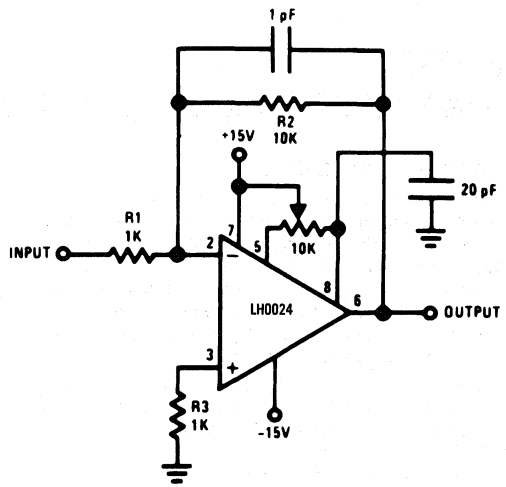
Typical Applications

TTL Compatible Comparator



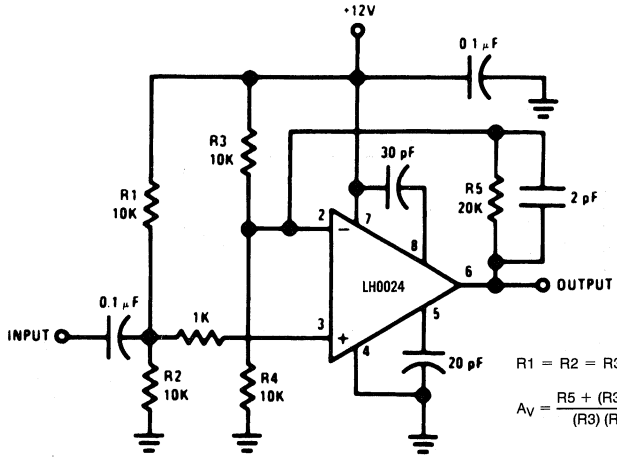
TL/K/5552–3

Offset Null



TL/K/5552–4

Video Amplifier



$R1 = R2 = R3 = R4$

$$A_V = \frac{R5 + (R3\,R4)}{(R3)\,(R4)} = 5$$

TL/K/5552–5

National Semiconductor

LH0032
Ultra Fast FET-Input Operational Amplifier

General Description

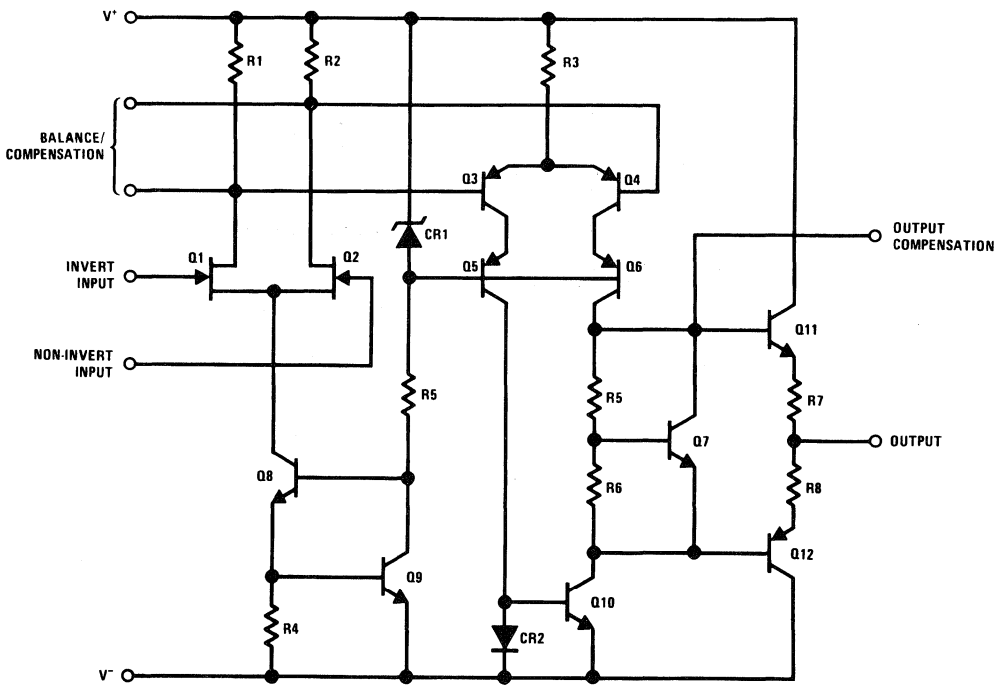
The LH0032 is a high slew rate, high input impedance differential operational amplifier suitable for diverse applications in fast signal handling. The high allowable differential input voltage, ease of output clamping, and high output drive capability particularly suit it for comparator applications. It may be used in applications normally reserved for video amplifiers allowing the use of operational gain setting and frequency response shaping into the megahertz region.

The LH0032's wide bandwidth, high input impedance and high output capacity make it an ideal choice for applications such as summing amplifiers in high speed D to A converters, buffers in data acquisition systems and sample and hold circuits. Additional applications include high speed integrators and video amplifiers. The LH0032 is guaranteed for operation over the temperature range −55°C to +125°C, the LH0032C is guaranteed for −25°C to +85°C.

Features

- 500 V/μs slew rate
- 70 MHz bandwidth
- $10^{12}\Omega$ input impedance
- As low as 2 mV max input offset voltage
- FET input
- Peak output current to 100 mA

Schematic



TL/K/5265–1

Absolute Maximum Ratings (Note 9)

Supply Voltage, V_S	±18V
Input Voltage, V_{IN}	±V_S
Differential Input Voltage	±30V or ±2V_S
Power Dissipation, P_D	(Note 10)
Steady State Output Current	±100 mA
Storage Temperature Range	−65°C to +150°C
Lead Temp. (Soldering, 10 seconds)	300°C

Operating Ratings

Temperature Range, T_A	
LH0032G	−55°C to +125°C
LH0032CG	−25°C to +85°C
Junction Temperature, T_J	
LH0032G	+175°C
Thermal Resistance (Note 8)	
θ_{JA} G Package	100°C/W
θ_{JC} G Package	70°C/W

DC Electrical Characteristics V_S = ±15V, $T_{MIN} \le T_A \le T_{MAX}$ unless otherwise noted (Note 2) ($T_A = T_J$)

Symbol	Parameter	Test Conditions		LH0032			LH0032C			Units
				Min	Typ	Max	Min	Typ	Max	
V_{OS}	Input Offset Voltage	V_{IN}=0	$T_A=T_J=25°C$ (Note 3)		2	5 10		2	15 20	mV
$\Delta V_{OS}/\Delta T$	Average Offset Voltage Drift		(Note 4)		15	50		15	50	µV/°C
I_{OS}	Input Offset Current		$T_J=25°C$ (Note 3) $T_A=25°C$ (Note 5)			25 250 25			50 500 5	pA pA nA
I_B	Input Bias Current		$T_J=25°C$ (Note 3) $T_A=25°C$ (Note 5)			100 1 50			500 5 15	pA nA nA
*V_{INCM}	Input Voltage Range			±10	±12		±10	±12		V
CMRR	Common Mode Rejection Ratio	ΔV_{IN} = ±10V		50	60		50	60		dB
A_{VOL}	Open-Loop Voltage Gain	V_O = ±10V, f=1 kHz R_L = 1 kΩ (Note 6)	$T_J=25°C$	60	70		60	70		dB
				57			57			
V_O	Output Voltage Swing	R_L = 1 kΩ		±10	±13.5		±10	±13		V
I_S	Power Supply Current	$T_A=25°C$, $I_O=0$ (Note 5)			18	20		20	22	mA
PSRR	Power Supply Rejection Ratio	ΔV_S=10V (±5 to ±15V)		50	60		50	60		dB

*Guaranteed by CMRR test condition.

AC Electrical Characteristics $V_S = \pm 15V$, $R_L = 1k\Omega$, $T_J = 25°C$ (Note 7)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
S_R	Slew Rate	$A_V = +1$		350	500		V/μs
t_s	Settling Time to 1% of Final Value	$A_V = -1$,	$\Delta V_{IN} = 20V$		100		ns
t_s	Settling Time to 0.1% of Final Value				300		ns
t_R	Small Signal Rise Time	$A_V = +1$, $\Delta V_{IN} = 1V$			8	20	
t_D	Small Signal Delay Time				10	25	

Note 1: In order to limit maximum junction temperature to +175°C, it may be necessary to operate with VS < ±15V when T_A or T_C exceeds specific values depending on the P_D within the device package. Total P_D is the sum of quiescent and load-related dissipation. See applications notes AN-277, "Applications of Wide-Band Buffer Amplifiers" and AN-253, "High-Speed Operational-Amplifier Applications" for a discussion of load-related power dissipation.

Note 2: LH0032G is 100% production tested as specified at 25°C, 125°C, and −55°C. LH0032CG is 100% production tested at 25°C only. Specifications at temperature extremes are verified by sample testing, but these limits are not used to calculate outgoing quality level.

Note 3: Specification is at 25°C junction temperature due to requirements of high-speed automatic testing. Actual values at operating temperature will exceed the value at T_J = 25 C. When supply voltages are ± 15V, no-load operating junction temperature may rise 40–60°C above ambient, and more under load conditions. Accordingly, V_{OS} may change one to several mV, and I_B and I_{OS} will change significantly during warm-up. Refer to I_B and I_{OS} vs. temperature graph for expected values.

Note 4: LH0032G is 100% production tested for this parameter. LH0032CG is sample tested only. Limits are not used to calculate outgoing quality levels. $\Delta V_{OS}/\Delta T$ is the average value calculated from measurements at 25°C and T_{MAX}.

Note 5: Measured in still air 7 minutes after application of power. Guaranteed thru correlated automatic pulse testing.

Note 6: Guaranteed thru correlated automatic pulse testing at $T_J = 25°C$.

Note 7: Not 100% production tested; verified by sample testing only. Limits are not used to calculate outgoing quality level.

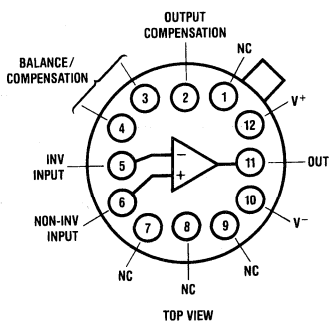
Note 8: For operating at elevated temperatures, the device must be derated based on the thermal resistance θ_{JA} and T_J max. $T_J = T_A + P_D\theta_{JA}$.

Note 9: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed.

Note 10: The maximum power dissipation is a function of maximum junction temperature T_J max, total thermal resistance θ_{JA}, and ambient temperature T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_J \text{ max} - T_A)/\theta_{JA}$.

Note 11: See RETS0032X for LH0032G military specifications.

Connection Diagram

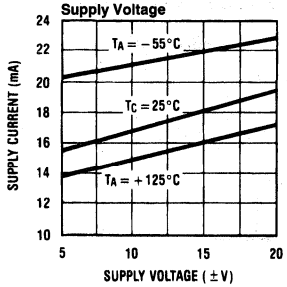


TL/K/5265–23

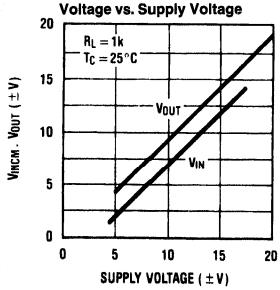
Order Number LH0032G, LH0032G/883 or LH0032CG
See NS Package Number G12B

Typical Performance Characteristics

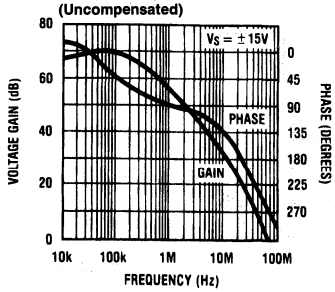
Supply Current vs. Supply Voltage



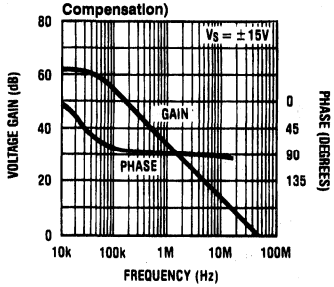
Input Voltage Range and Output Voltage vs. Supply Voltage



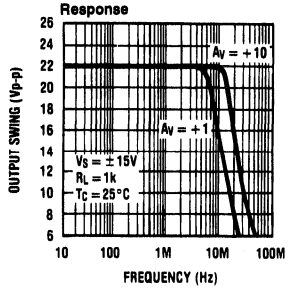
Bode Plot (Uncompensated)



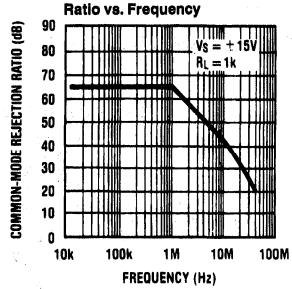
Bode Plot (Unity Gain Compensation)



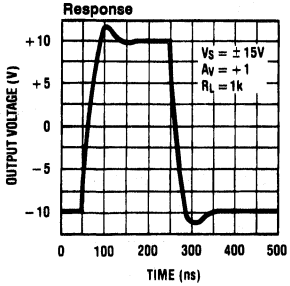
Large Signal Frequency Response



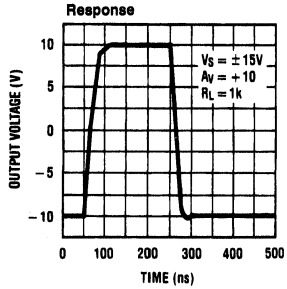
Common Mode Rejection Ratio vs. Frequency



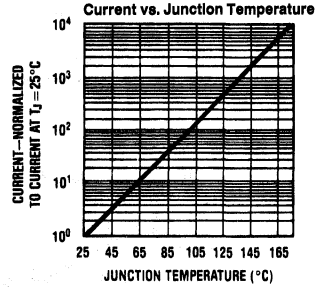
Large Signal Pulse Response



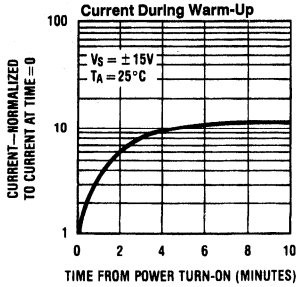
Large Signal Pulse Response



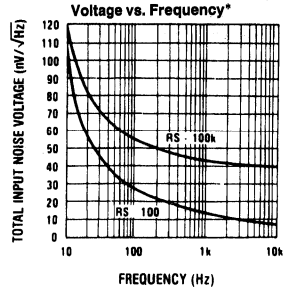
Normalized Input Bias and Offset Current vs. Junction Temperature



Normalized Input Bias Current During Warm-Up



Total Input Noise Voltage vs. Frequency*

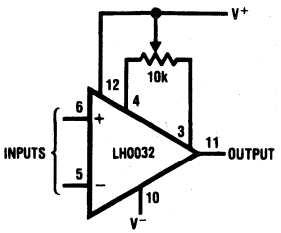


TL/K/5265–2

*Noise voltage includes contribution from source resistance.

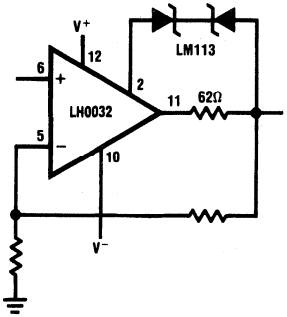
Auxiliary Circuits

Offset Null



TL/K/5265–15

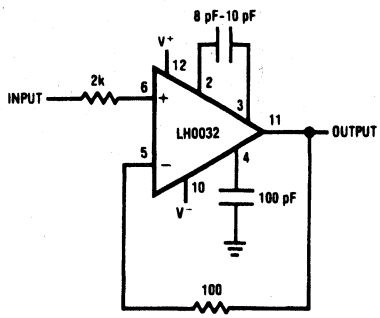
Output Short Circuit Protection



TL/K/5265–16

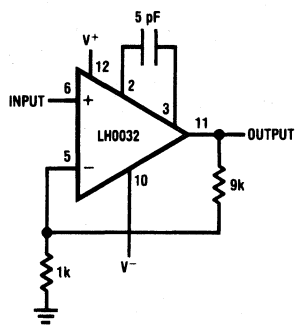
Typical Applications

Unity Gain Amplifier



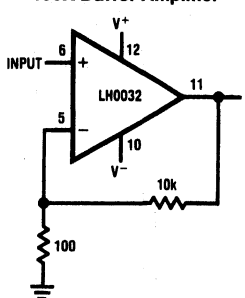
TL/K/5265–17

10X Buffer Amplifier



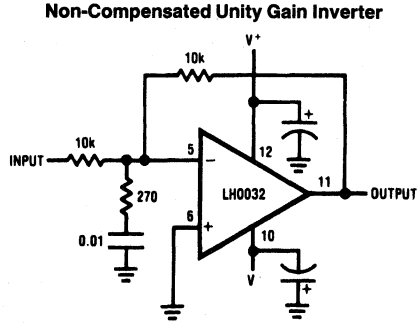
TL/K/5265–18

100X Buffer Amplifier



TL/K/5265–19

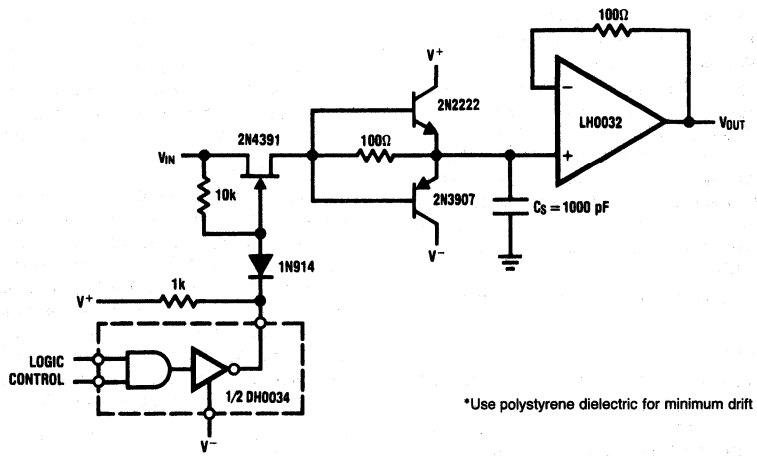
Non-Compensated Unity Gain Inverter



TL/K/5265–20

Typical Applications (Continued)

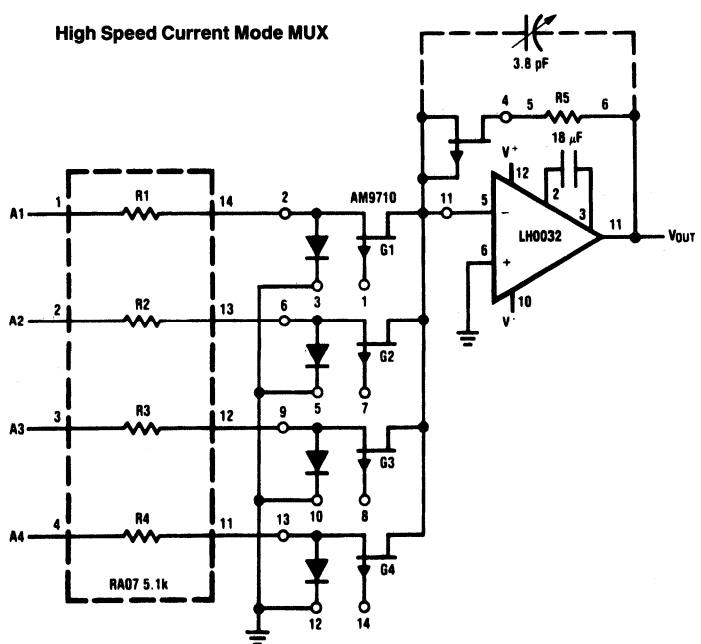
High Speed Sample and Hold



*Use polystyrene dielectric for minimum drift

TL/K/5265-21

High Speed Current Mode MUX



TL/K/5265-22

Applications Information

POWER SUPPLY DECOUPLING

The LH0032/LH0032A, like most high speed circuits, is sensitive to layout and stray capacitance. Power supplies should be by passed as near to pins 10 and 12 as practicable with low inductance capacitors such as 0.01 µF disc ceramics. Compensation components should also be located close to the appropriate pins to minimize stray reactances.

INPUT CURRENT

Because the input devices are FETs, the input bias current may be expected to double for each 11°C junction temperature rise. This characteristic is plotted in the typical performance characteristics graphs. The device will self-heat due to internal power dissipation after application of power thus raising the FET junction temperature 40–60°C above free-air ambient temperature when supplies are ±15V. The de-

Applications Information (Continued)

vice temperature will stabilize within 5–10 minutes after application of power, and the input bias currents measured at that time will be indicative of normal operating currents. An additional rise would occur as power is delivered to a load due to additional internal power dissipation.

There is an additional effect on input bias current as the input voltage is changed. The effect, common to all FETs, is an avalanche-like increase in gate current as the FET gate-to-drain voltage is increased above a critical value depending on FET geometry and doping levels. This effect will be noted as the input voltage of the LH0032 is taken below ground potential when the supplies are ±15V. All of the effects described here may be minimized by operating the device with $V_S \leq \pm 15V$.

These effects are indicated in the typical performance curves.

INPUT CAPACITANCE

The input capacitance to the LH0032/LH0032C is typically 5pF and thus may form a significant time constant with high value resistors. For optimum performance, the input capacitance to the inverting input should be compensated by a small capacitor across the feedback resistor. The value is strongly dependent on layout and closed loop gain, but will typically be in the neighborhood of several picofarads.

In the non-inverting configuration, it may be advantageous to bootstrap the case and/or a guard conductor to the inverting input. This serves both to divert leakage currents away from the non-inverting input and to reduce the effective input capacitance. A unity gain follower so treated will have an input capacitance under a picofarad.

HEAT SINKING

While the LH0032/LH0032A is specified for operation without any explicit heat sink, internal power dissipation does cause a significant temperature rise. Improved bias current performance can thus be obtained by limiting this temperature rise with a small heat sink such as the Thermalloy No. 2241 or equivalent. The case of the device has no internal connection, so it may be electrically connected to the sink if this is advantageous. Be aware, however, that this will affect the stray capacitances to all pins and may thus require adjustment of circuit compensation values.

For additional applications information request Application Note AN-253.

National Semiconductor

LH0041/LH0041C 0.2 Amp Power Operational Amplifier

General Description

The LH0041/LH0041C is a general purpose operational amplifier capable of delivering large output currents. The LH0041 delivers currents of 200 mA at voltage levels closely approaching the available power supplies. In addition, both the inputs and outputs are protected against overload.

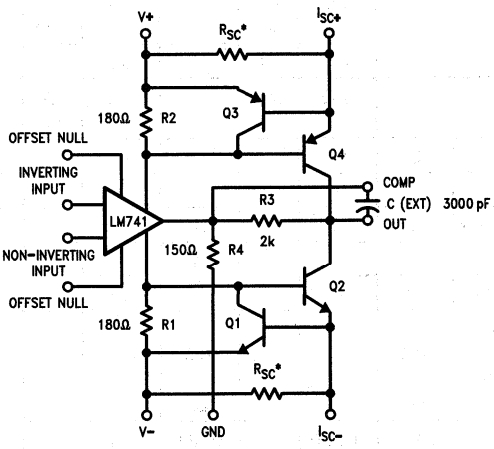
The LH0041 is suited for applications such as torque driver for inertial guidance systems, diddle yoke driver for alphanumeric CRT displays, cable drivers, and programmable power supplies for automatic test equipment.

The LH0041 is supplied in both 12-pin TO-8 (2.5 watts with clip on heatsink) and a power 8-pin ceramic DIP (2 watts with suitable heatsink). The LH0041 is guaranteed over the temperature range of −55°C to +125°C while the LH0041C is guaranteed from −25°C to +85°C.

Features

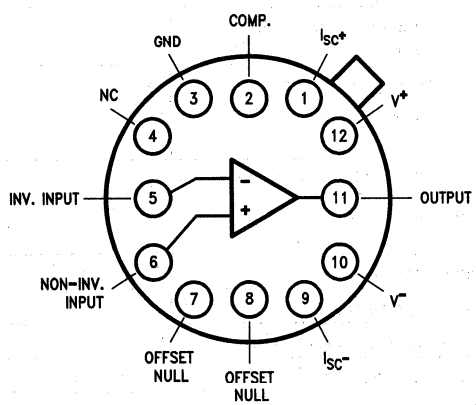
■ Output current	0.2 Amp (LH0041)
■ Output voltage swing	±14V into 100Ω (LH0041)
■ Low standby power	100 mW at ±15V
■ High open loop gain	100 dB

Schematic and Connection Diagrams



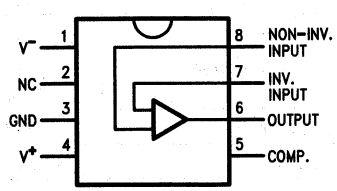
TL/K/10115–1

*R_{SC} external on "G" and "K" packages. R_{SC} internal on "J" package. Offset Null connections available only on "G" package.



TL/K/10115–3

Order Number LH0041G, LH0041G/883 or LH0041CG
See NS Package Number G12B



TL/K/10115–22

Top View

Order Number LH0041CJ
See NS Package Number HY08A

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	±18V
Power Dissipation	See curves
Differential Input Voltage	±30V
Input Voltage (Note 1)	±15V
Peak Output Current (Note 2) LH0041/LH0041C	0.5 Amps
Output Short Circuit Duration (Note 3)	Continuous
Operating Temperature Range LH0041	−55°C to +125°C
LH0041C	−25°C to +85°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec.)	300°C

DC Electrical Characteristics for LH0041/LH0041C (Note 4)

Parameter	Conditions	Limits						Units
		LH0041			LH0041C			
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	$R_S \leq 100\Omega$, $T_A = 25°C$ $R_S \leq 100\Omega$		1.0	3.0 5.0		3.0	6.0 7.5	mV mV
Voltage Drift with Temperature	$R_S \leq 100\Omega$		3			5		µV/°C
Offset Voltage Drift with Time			5			5		µV/week
Offset Voltage Change with Output Power			15			15		µV/watt
Offset Voltage Adjustment Range	(Note 5)		20			20		mV
Input Offset Current	$T_A = 25°C$		30	100 300		50	200 500	nA nA
Offset Current Drift with Temperature			0.1	1.0		0.2	1.0	nA/°C
Input Bias Current	$T_A = 25°C$		100	300 1.0		200	500 1.0	nA µA
Input Resistance	$T_A = 25°C$	0.3	1.0		0.3	1.0		MΩ
Input Capacitance			3			3		pF
Common Mode Rejection Ratio	$R_S \leq 100\Omega$, $\Delta V_{CM} = \pm 10V$	70	90		70	90		dB
Input Voltage Range	$V_S = \pm 15V$	±12			±12			V
Power Supply Rejection Ratio	$R_S \leq 100\Omega$, $\Delta V_S = \pm 10V$	80	96		70	90		dB
Voltage Gain	$V_S = \pm 15V$, $V_O = \pm 10V$ $R_L = 1\ k\Omega$, $T_A = 25°C$ $V_S = \pm 15V$, $V_O = \pm 10V$ $R_L = 100\Omega$	 100 25	 200 	 	 100 20	 200 	 	 V/mV V/mV
Output Voltage Swing	$V_S = \pm 15V$, $R_L = 100\Omega$	±13.0	±14.0		±13.0	±14.0		V
Output Short Circuit Current	$V_S = \pm 15V$, $T_A = 25°C$ (Note 6)		200	300		200	300	mA
Power Supply Current	$V_S = \pm 15V$, $V_{OUT} = 0$		2.5	3.5		3.0	4.0	mA
Power Consumption	$V_S = \pm 15V$, $V_{OUT} = 0$		75	105		90	120	mW

AC Electrical Characteristics for LH0041/LH0041C (T_A = 25°C, V_S = ±15V, C_C = 3000 pF)

Slew Rate	A_V = +1, R_L = 100Ω	1.5	3.0		1.0	3.0		V/μs
Power Bandwidth	R_L = 100Ω		20			20		kHz
Small Signal Overshoot			5	20		10	30	%
Settling Time (0.1%)	ΔV_{IN} = 10V, A_V = +1		4			4		μs
Overload Recovery Time			3			3		μs
Harmonic Distortion	f = 1 kHz, P_O = 0.5W		0.2			0.2		%
Input Noise Voltage	R_S = 50Ω, B.W. = 10 Hz to 10 kHz		5			5		μV rms
Input Noise Current	B.W. = 10 Hz to 10 kHz		0.05			0.05		nA rms

Note 1: Rating applies for supply voltages above ±15V. For supplies less than ±15V, rating is equal to supply voltage.

Note 2: Rating applies for LH0041G with R_{SC} = 0Ω.

Note 3: Rating applies as long as package power rating is not exceeded.

Note 4: Specifications apply for V_S = ±5V to ±18V, and −55°C ≤ T_C ≤ +125°C for LH0041G, and −25°C ≤ T_C ≤ +85°C for LH0041CG and LH0041CJ unless otherwise specified. Typical values are for 25°C only.

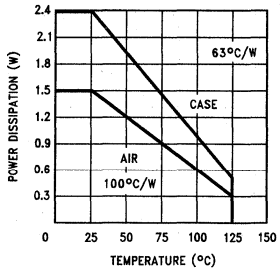
Note 5: TO-8 "G" packages only.

Note 6: Rating applies for "J" DIP package and for TO-8 "G"package with R_{SC} = 3.3Ω.

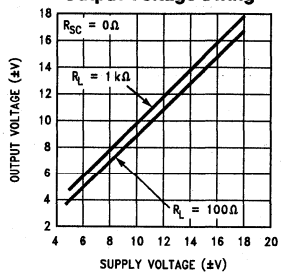
Note 7: See RETS0041X for LH0041G military specifications.

Typical Performance Characteristics

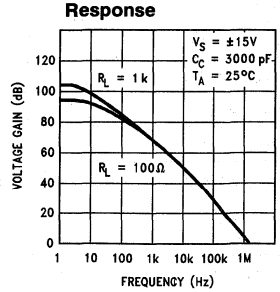
Power Dissipation LH0041/LH0041C



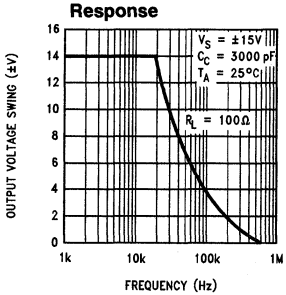
Output Voltage Swing



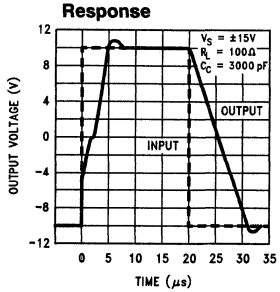
Open Loop Frequency Response



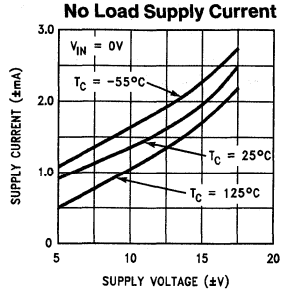
Large Signal Frequency Response



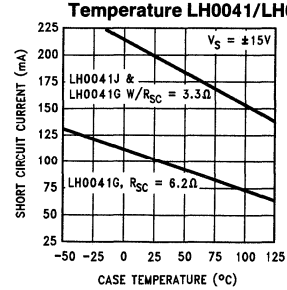
Voltage Follower Pulse Response



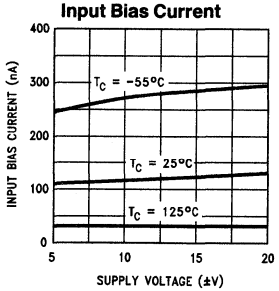
No Load Supply Current



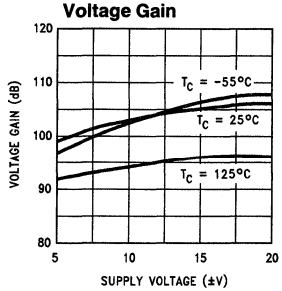
Short Circuit vs Temperature LH0041/LH0041C



Input Bias Current



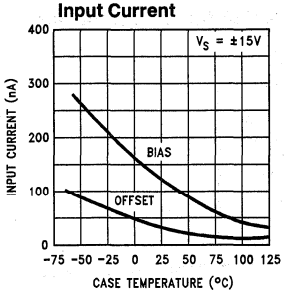
Voltage Gain



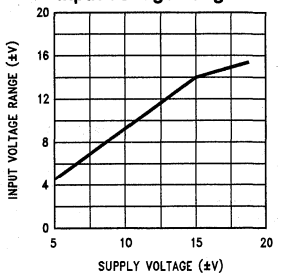
TL/K/10115–4

Typical Performance Characteristics (Continued)

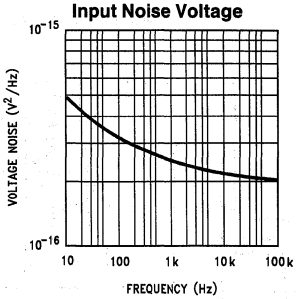
Input Current



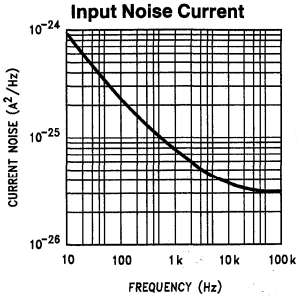
Input Voltage Range



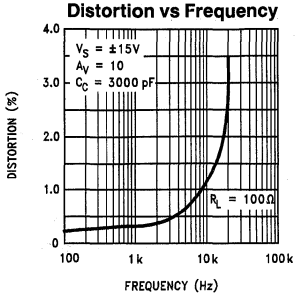
Input Noise Voltage



Input Noise Current



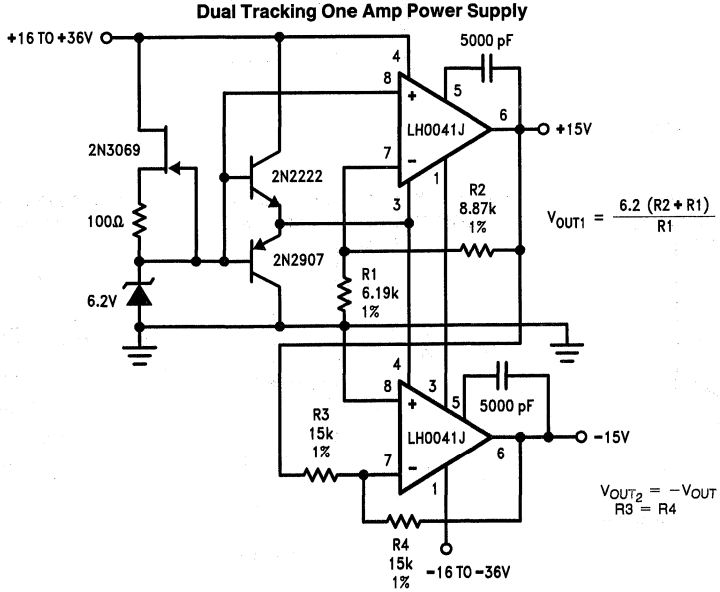
Distortion vs Frequency



TL/K/10115–5

Typical Applications

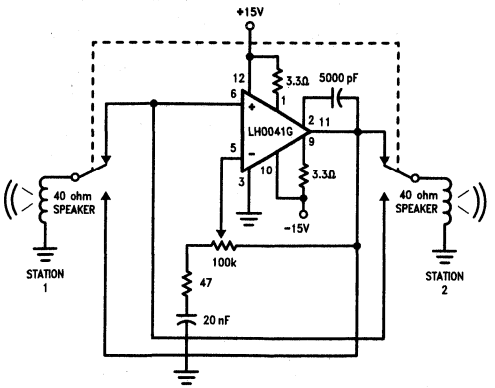
Dual Tracking One Amp Power Supply



TL/K/10115–8

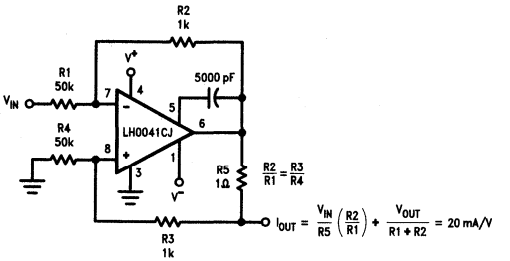
Typical Applications (Continued)

Two Way Intercom



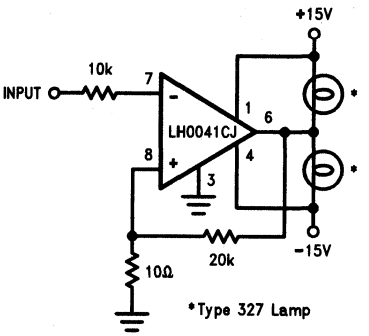
TL/K/10115–10

Programmable High Current Source/Sink



TL/K/10115–11

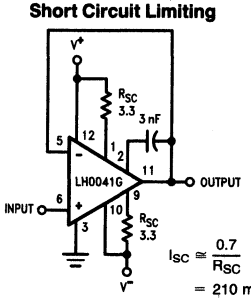
Power Comparator



TL/K/10115–12

Auxiliary Circuits

LH0041G Unity Gain with Short Circuit Limiting

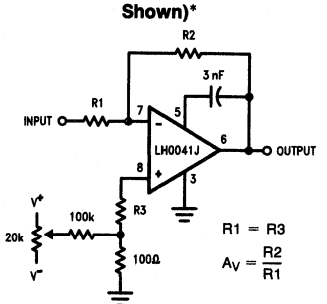


$I_{SC} \cong \frac{0.7}{R_{SC}}$

= 210 mA

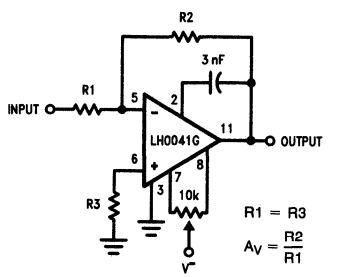
TL/K/10115–15

LH0041 Offset Voltage Null Circuit (LH0041CJ Pin Connections Shown)*



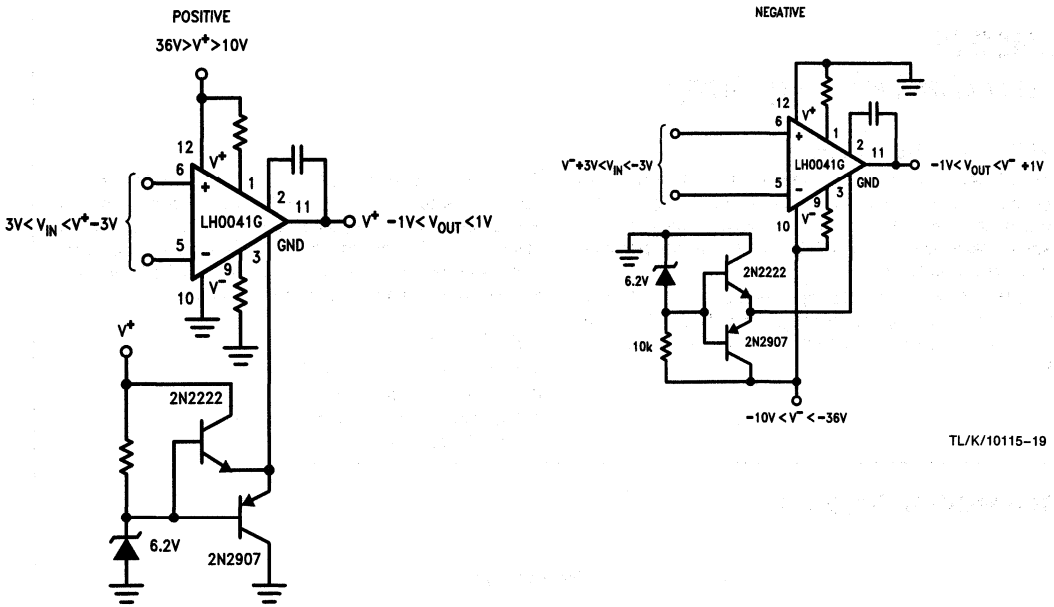
TL/K/10115–16

LH0041G Offset Voltage Null Circuit*



TL/K/10115–17

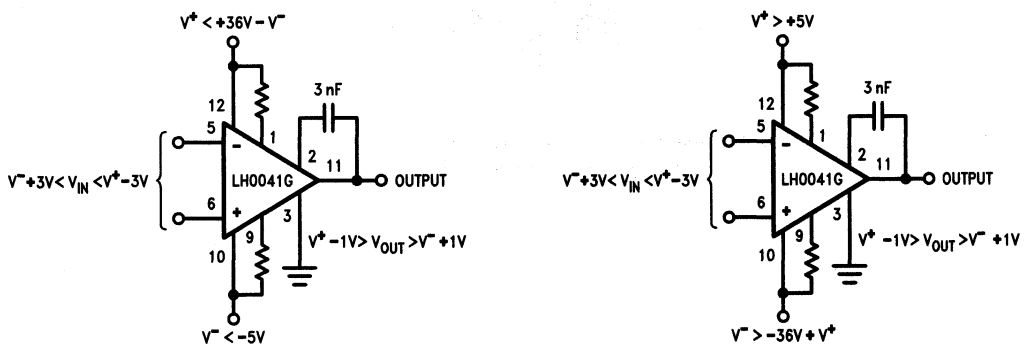
Auxiliary Circuits (Continued)



TL/K/10115–19

TL/K/10115–18

Operation from Single Supplies



TL/K/10115–20

TL/K/10115–21

Operation from Non-Symmetrical Supplies

*For additional offset null circuit techniques see National Linear Applications Handbook.

National Semiconductor

LH0042
Low Cost FET Op Amp

General Description

The LH0042 is a FET input operational amplifier with very high input impedance and low input currents with no compromise in noise, common mode rejection ratio, open loop gain, or slew rate. The LH0042 is internally compensated and is free of latch-up.

The LH0042 is specified for operation over the −55°C to +125°C military temperature range. The LH0042C is specified for operation over the −25°C to +85°C temperature range.

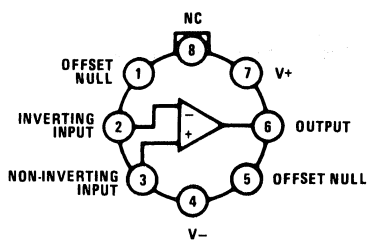
The LH0042 op amp is intended to fulfill a wide variety of applications for process control, medical instrumentation, and other systems requiring very low input currents. The LH0042 provides low cost high performance for such applications as electrometer and photocell amplification, picoammeters, and high input impedance buffers.

Features

- High open loop gain—100 dB typ
- Internal compensation
- Pin compatible with standard IC op amps (TO-99 package)

Connection Diagram

Metal Can Package



TL/K/5557–3

Top View

Order Number LH0042H-MIL, LH0042H or LH0042CH
See NS Package Number H08D

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	±22V
Power Dissipation (see Graph)	500 mW
Input Voltage (Note 1)	±15V
Differential Input Voltage (Note 2)	±30V
Voltage Between Offset Null and V^-	±0.5V
Short Circuit Duration	Continuous
Operating Temperature Range	
LH0022, LH0042, LH0052	−55°C to +125°C
LH0022C, LH0042C, LH0052C	−25°C to +85°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec.)	300°C

DC Electrical Characteristics for LH0022/LH0022C (Note 3) $T_A = T_J(Max)$

Parameter	Conditions	Limits						Units
		LH0022			LH0022C			
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	$R_S \leq 100\ k\Omega$, $T_A = 25°C$ $V_S = \pm 15V$		2.0	4.0		3.5	6.0	mV
	$R_S \leq 100\ k\Omega$, $V_S = \pm 15V$			5.0			7.0	mV
Temperature Coefficient of Input Offset Voltage	$R_S \leq 100\ k\Omega$		10			15		µV/°C
Offset Voltage Drift with Time			3			4		µV/week
Input Offset Current	$T_A = 25°C$ (Note 4)		0.2	2.0		1.0	5.0	pA
				2.0			0.5	nA
Temperature Coefficient of Input Offset Current		Doubles Every 10°C			Doubles Every 10°C			
Offset Current Drift with Time			0.1			0.1		pA/week
Input Bias Current	$T_A = 25°C$ (Note 4)		5	10		10	25	pA
				10			2.5	nA
Temperature Coefficient of Input Bias Current		Doubles Every 10°C			Doubles Every 10°C			
Differential Input Resistance			10^{12}			10^{12}		Ω
Common Mode Input Resistance			10^{12}			10^{12}		Ω
Input Capacitance			4.0			4.0		pF
Input Voltage Range	$V_S = \pm 15V$	±12	±13.5		±12	±13.5		V
Common Mode Rejection Ratio	$R_S \leq 10\ k\Omega$, $V_{IN} = \pm 10V$	74	90		70	90		dB
Supply Voltage Rejection Ratio	$R_S \leq 10\ k\Omega$, $\pm 5V \leq V_S \leq \pm 15V$	74	90		70	90		dB
Large Signal Voltage Gain	$R_L = 2\ k\Omega$, $V_{OUT} = \pm 10V$ $T_A = 25°C$, $V_S = \pm 15V$	75	100		75	100		V/mV
	$R_L = 2\ k\Omega$, $V_{OUT} = \pm 10V$ $V_S = \pm 15V$	30			30			V/mV
Output Voltage Swing	$R_L = 1\ k\Omega$, $T_A = 25°C$ $V_S = \pm 15V$	±10	±12.5		±10	±12		V
	$R_L = 2\ k\Omega$, $V_S = \pm 15V$	±10			±10			V
Output Current Swing	$V_{OUT} = \pm 10V$, $T_A = 25°C$	±10	±15		±10	±15		mA
Output Resistance			75			75		Ω
Output Short Circuit Current			25			25		mA
Supply Current	$V_S = \pm 15V$		2.0	2.5		2.4	2.8	mA
Power Consumption	$V_S = \pm 15V$			75			85	mW

DC Electrical Characteristics for LH0042/LH0042C (Note 3)

Parameter	Conditions	Limits						Units
		LH0042			LH0042C			
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	$R_S \leq 100\ k\Omega$		5.0	20		6.0	20	mV
Temperature Coefficient of Input Offset Voltage	$R_S \leq 100\ k\Omega$		10			15		$\mu V/°C$
Offset Voltage Drift with Time			7.0			10		μV/week
Input Offset Current	$T_A = 25°C$ (Note 4)		1.0	5.0		2.0	10	pA
Input Bias Current	$T_A = 25°C$ (Note 4)		10	25		15	50	pA
Temperature Coefficient of Input Bias Current		Doubles Every 10°C			Doubles Every 10°C			
Differential Input Resistance			10^{12}			10^{12}		Ω
Common Mode Input Resistance			10^{12}			10^{12}		Ω
Input Capacitance			4.0			4.0		pF
Input Voltage Range		±12	±13.5		±12	±13.5		V
Common Mode Rejection Ratio	$R_S \leq 10\ k\Omega$, $V_{IN} = \pm 10V$	70	86		70	80		dB
Supply Voltage Rejection Ratio	$R_S \leq 10\ k\Omega$, $\pm 5V \leq V_S \leq \pm 15V$	70	86		70	86		dB
Large Signal Voltage Gain	$R_S \leq 2\ k\Omega$, $V_{OUT} = \pm 10V$, $T_A = 25°C$	50	100		25	100		V/mV
	$R_S \leq 2\ k\Omega$, $V_{OUT} = \pm 10V$	30			25			V/mV
Output Voltage Swing	$R_L = 1\ k\Omega$, $T_A = 25°C$	±10	±12.5		±10	±12		V
	$R_L = 2\ k\Omega$	±10			±10			V
Output Current Swing	$V_{OUT} = \pm 10V$	±10	±15		±10	±15		mA
Output Resistance			75			75		Ω
Output Short Circuit Current			20			20		mA
Supply Current	$V_S = \pm 15V$		2.5	3.5		2.8	4.0	mA
Power Consumption	$V_S = \pm 15V$			105			120	mW

DC Electrical Characteristics for LH0052/LH0052C (Note 3) (Continued)

Parameter	Conditions	Limits						Units
		LH0052			LH0052C			
		Min	Typ	Max	Min	Typ	Max	
Input Bias Current	T_A = 25°C (Note 4)		0.5	2.5		1.0	5.0	pA
				2.5			0.5	nA
Temperature Coefficient of Input Bias Current		Doubles Every 10°C			Doubles Every 10°C			
Differential Input Resistance			10^{12}			10^{12}		Ω
Common Mode Input Resistance			10^{12}			10^{12}		Ω
Input Capacitance			4.0			4.0		pF
Input Voltage Range	V_S = ±15V	±12	±13.5		±12	±13.5		V
Common Mode Rejection Ratio	$R_S \leq 10\ k\Omega$, V_{IN} = ±10V	74	90		70	90		dB
Supply Voltage Rejection Ratio	$R_S \leq 10\ k\Omega$, ±5V ≤ V_S ≤ ±15V	74	90		70	90		dB
Large Signal Voltage Gain	R_L = 2 kΩ, V_{OUT} = ±10V V_S = ±15V, T_A = 25°C	75	100		75	100		V/mV
	R_L = 2 kΩ, V_{OUT} = ±10V V_S = ±15V	30			30			V/mV
Output Voltage Swing	R_L = 1 kΩ, T_A = 25°C V_S = ±15V	±10	±12.5		±10	±12		V
	R_L = 2 kΩ, V_S = ±15V	±10			±10			V
Output Current Swing	V_{OUT} = ±10V, T_A = 25°C	±10	±15		±10	±15		mA
Output Resistance			75			75		Ω
Output Short Circuit Current			25			25		mA
Supply Current	V_S = ±15V		3.0	3.5		3.0	3.8	mA
Power Consumption	V_S = ±15V			105			114	mW

AC Electrical Characteristics for all amplifiers (T_A = 25°C, V_S = ±15V)

Parameter	Conditions	Limits						Units
		LH0022/42/52			LH0022C/42C/52C			
		Min	Typ	Max	Min	Typ	Max	
Slew Rate	Voltage Follower	1.5	3.0		1.0	3.0		V/μs
Large Signal Bandwidth	Voltage Follower		40			40		kHz
Small Signal Bandwidth			1.0			1.0		MHz
Rise Time			0.3	1.5		0.3	1.5	μs
Overshoot			10	30		15	40	%
Settling Time (0.1%)	ΔV_{IN} = 10V		4.5			4.5		μs
Overload Recovery			4.0			4.0		μs

AC Electrical Characteristics for all amplifiers (T_A = 25°C, V_S = ±15V) (Continued)

Parameter	Conditions	Limits						Units
		LH0042			LH0042C			
		Min	Typ	Max	Min	Typ	Max	
Input Noise Voltage	R_S = 10 kΩ, f_o = 10 Hz		150			150		nV/√Hz
	R_S = 10 kΩ, f_o = 100 Hz		55			55		nV/√Hz
	R_S = 10 kΩ, f_o = 1 kHz		35			35		nV/√Hz
	R_S = 10 kΩ, f_o = 10 kHz		30			30		nV/√Hz
	BW = 10 Hz to 10kHz, R_S = 10 kΩ		12			12		μVrms

Note 1: For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

Note 2: Rating applies for minimum source resistance of 10 kΩ, for source resistances less than 10 kΩ, maximum differential input voltage is ±5V.

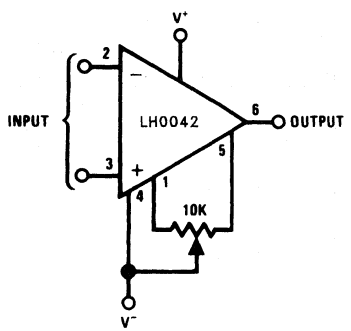
Note 3: Unless otherwise specified, these specifications apply for ±5V ≤ V_S ≤ ±20V and −55°C ≤ T_A ≤ +125°C for the LH0042 and −25°C ≤ T_A ≤ +85°C for the LH0042C. Typical values are given for T_A = 25°C.

Note 4: Input currents are a strong function of temperature. Due to high speed testing they are specified at a junction temperature T_j = 25°C. Self heating will cause an increase in current in manual tests. 25°C spec is guaranteed by testing at 125°C.

Note 5: See RETS0042X for the LH0042H military specifications.

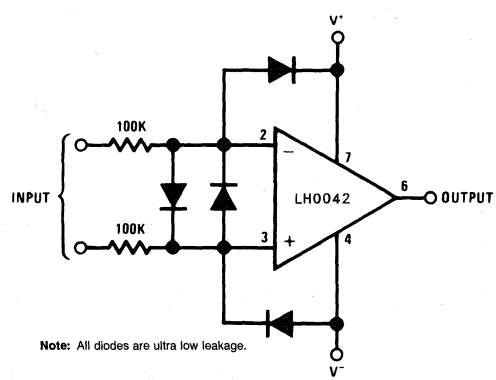
Auxiliary Circuits (Shown for TO-99 pin out)

Offset Null



TL/K/5557–5

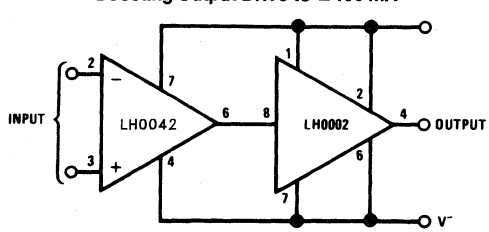
Protecting Inputs from ±150V Transients



Note: All diodes are ultra low leakage.

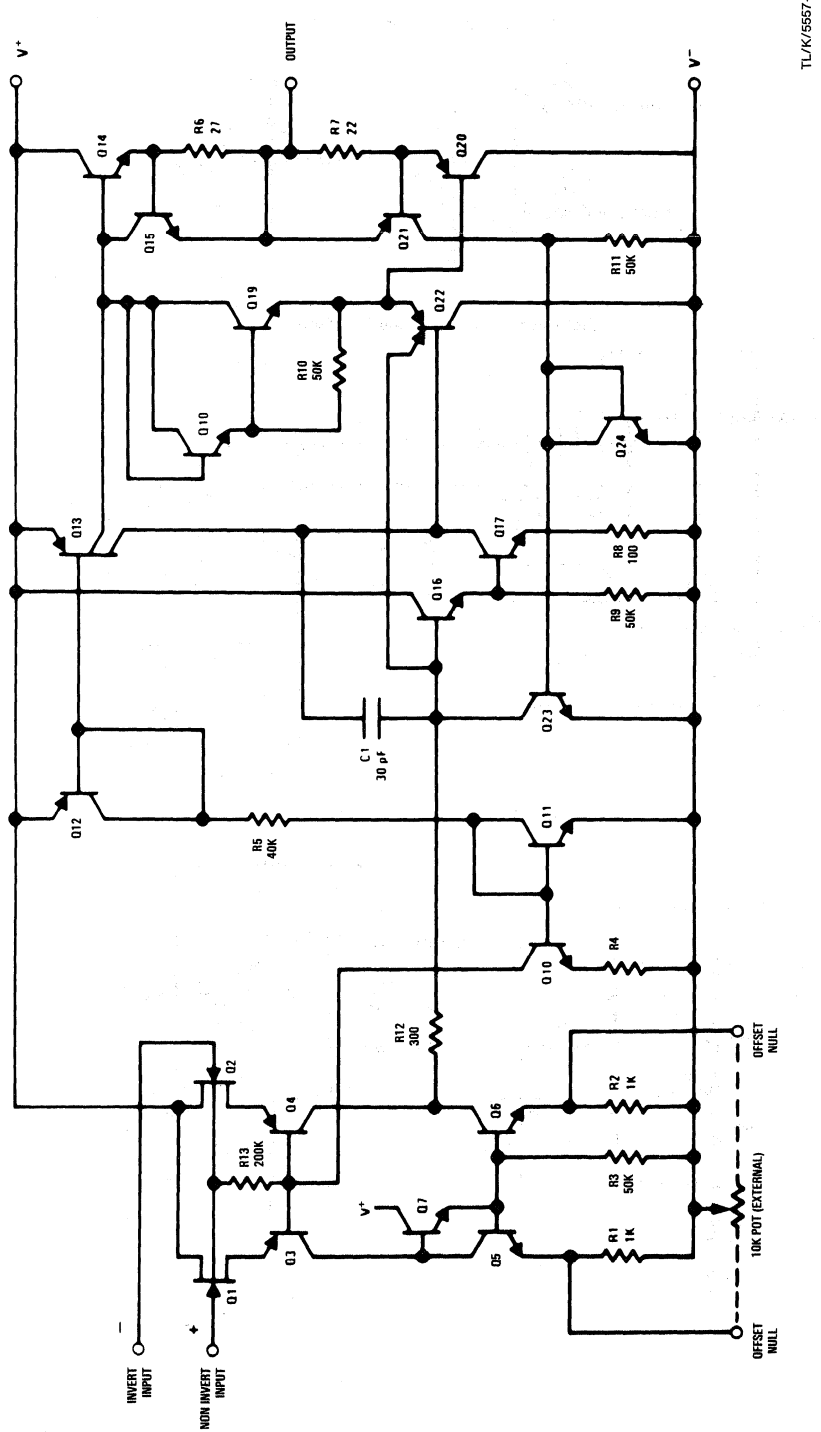
TL/K/5557–6

Boosting Output Drive to ±100 mA



TL/K/5557–7

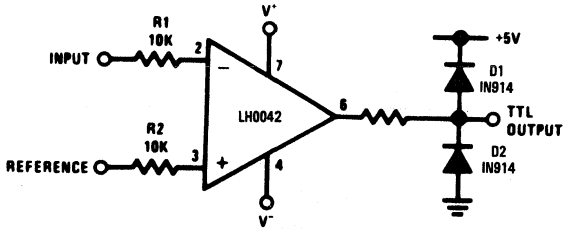
Schematic Diagram



TL/K/5557–1

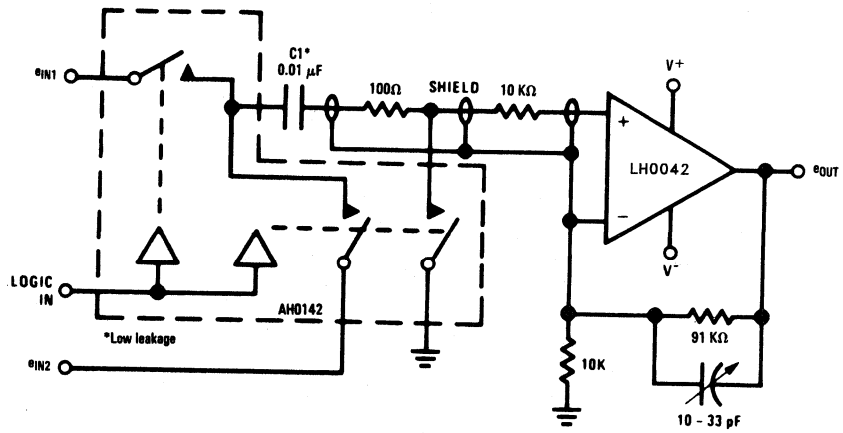
Typical Applications

Precision Voltage Comparator



TL/K/5557–9

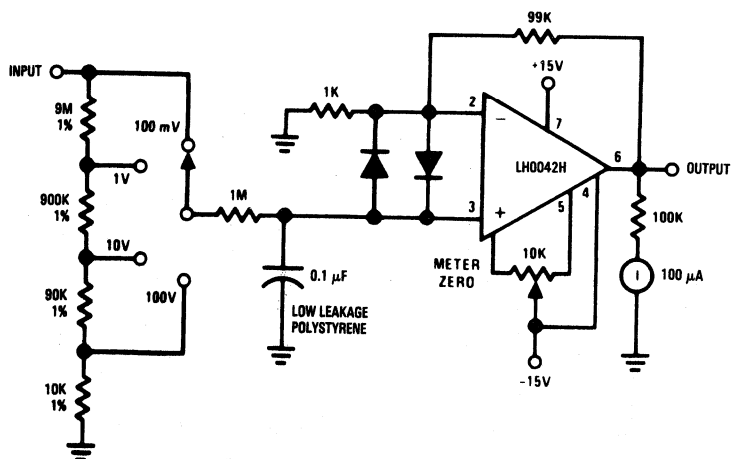
Subtractor for Automatic Test Gear



TL/K/5557–11

$e_{OUT} = 10 \times (e_{IN1} - e_{IN2})$

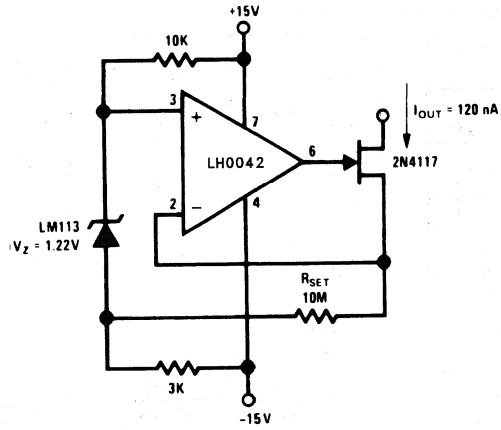
Sensitive Low Cost "VTVM"



TL/K/5777–12

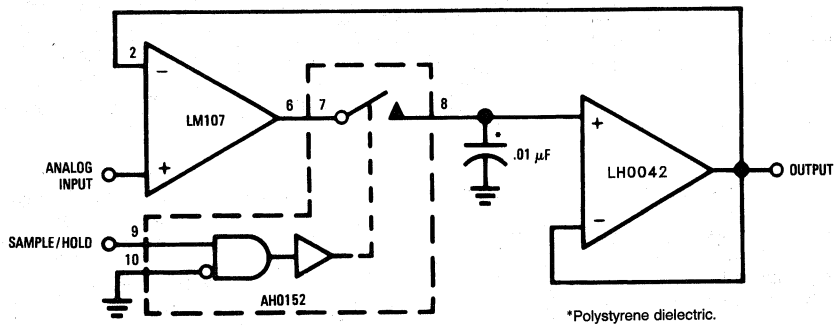
Typical Applications (Continued)

Ultra Low Level Current Source



TL/K/5777–13

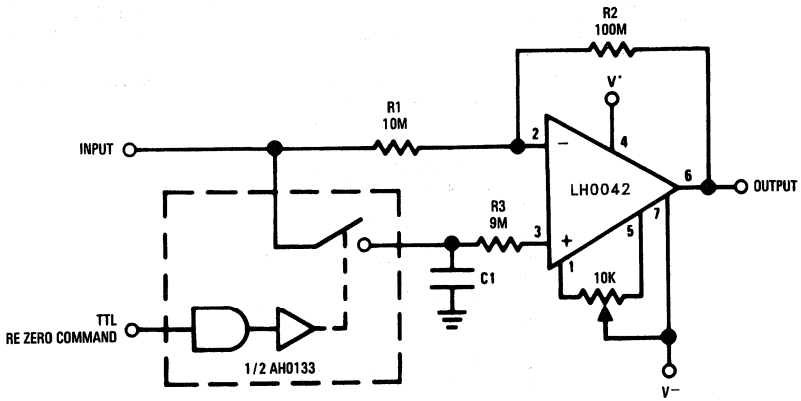
Sample and Hold



*Polystyrene dielectric.

TL/K/5557–16

Re-Zeroing Amplifier

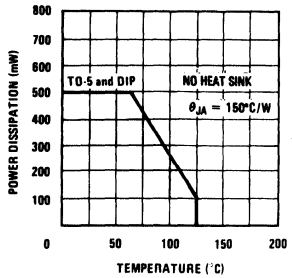


C1—0.01 μF polystyrene.

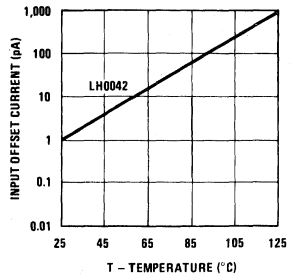
TL/K/5557–17

Typical Performance Characteristics

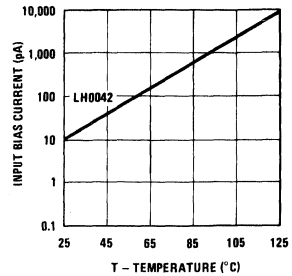
Maximum Power Dissipation



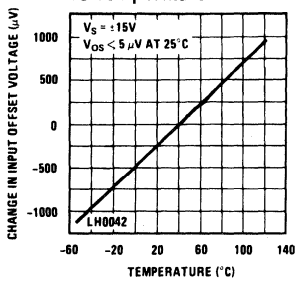
Input Offset Current vs Temperature



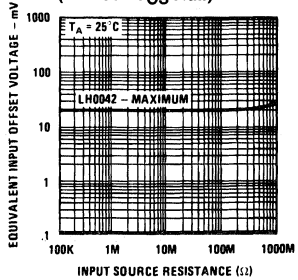
Input Bias Current vs Temperature



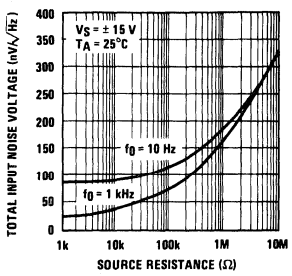
Input Offset Voltage vs Temperature



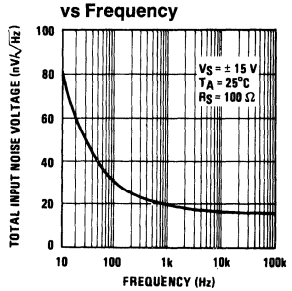
Offset Error (without V_{OS} Null)



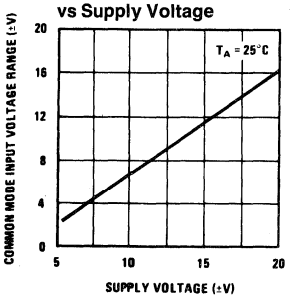
Total Input Noise Voltage* vs Source Resistance



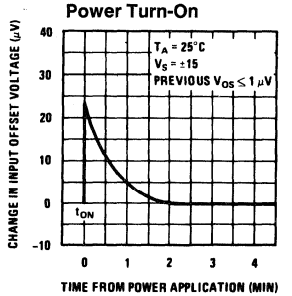
Total Input Noise Voltage* vs Frequency



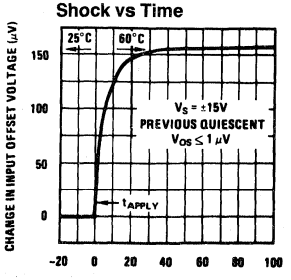
Common Mode Input Voltage vs Supply Voltage



Stabilization Time of Input Offset Voltage from Power Turn-On



Change in Input Offset Voltage Due to Thermal Shock vs Time



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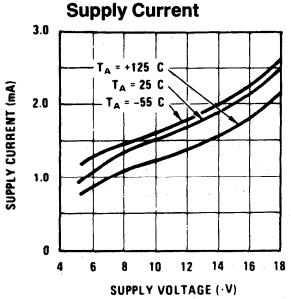
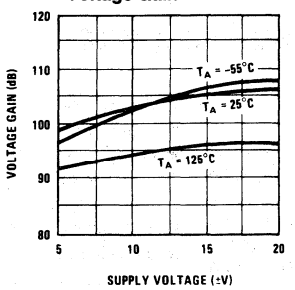
*Noise voltage includes contribution from source resistance.

Typical Performance Characteristics (Continued)

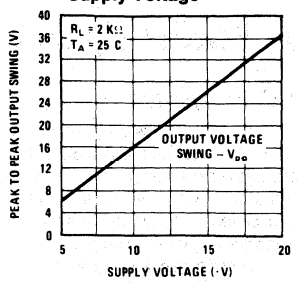
Supply Voltage vs Supply Current



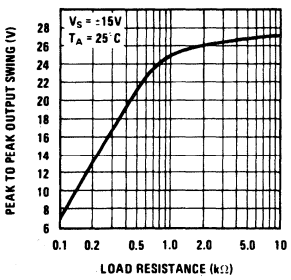
Voltage Gain



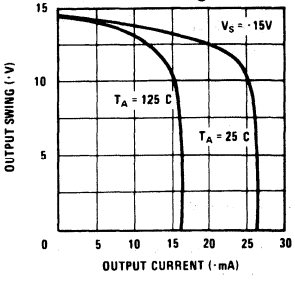
Output Swing vs Supply Voltage



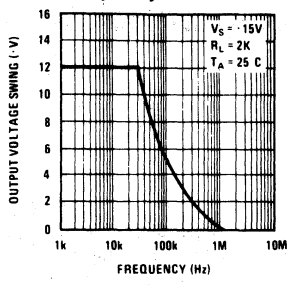
Output Voltage Swing vs Load Resistance



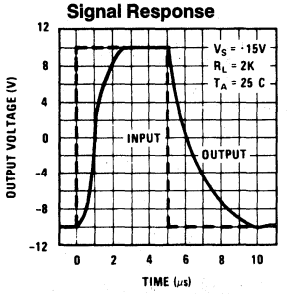
Current Limiting



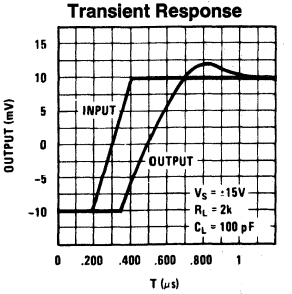
Output Voltage Swing vs Frequency



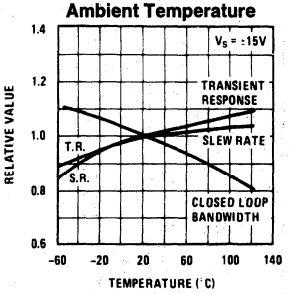
Voltage Follower Large Signal Response



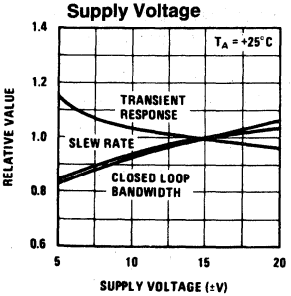
Transient Response



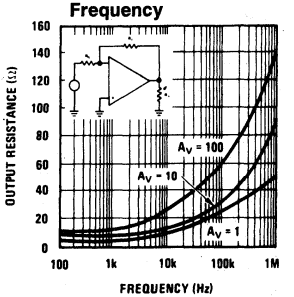
Frequency Characteristics vs Ambient Temperature



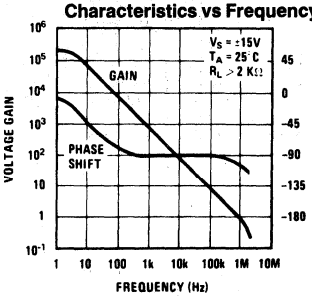
Frequency Characteristics vs Supply Voltage



Output Resistance vs Frequency



Open Loop Transfer Characteristics vs Frequency



TL/K/5557–19

National Semiconductor

LH0101 Power Operational Amplifier

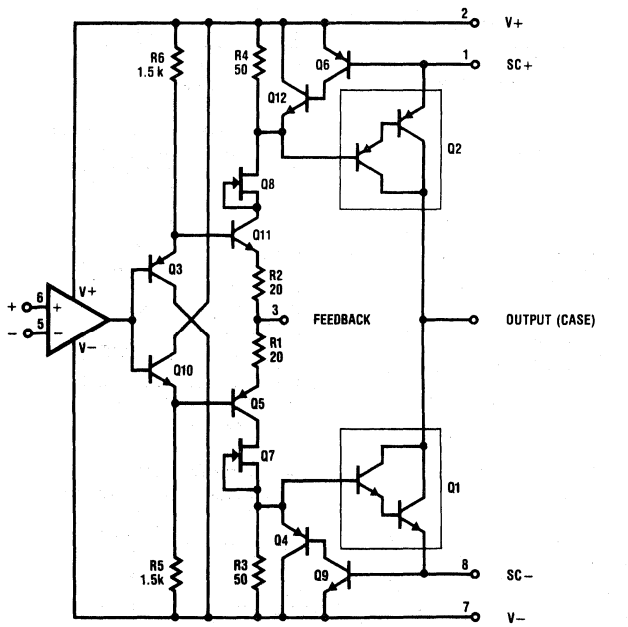
General Description

The LH0101 is a wideband power operational amplifier featuring FET inputs, internal compensation, virtually no crossover distortion, and rapid settling time. These features make the LH0101 an ideal choice for DC or AC servo amplifiers, deflection yoke drives, programmable power supplies, and disk head positioner amplifiers. The LH0101 is packaged in an 8 pin TO-3 hermetic package, rated at 60 watts with a suitable heat sink.

Features

- 5 Amp peak, 2 Amp continuous output current
- 300 kHz power bandwidth
- 850 mW standby power (±15V supplies)
- 300 pA input bias current
- 10 V/μs slew rate
- Virtually no crossover distortion
- 2 μs settling time to 0.01%
- 5 MHz gain bandwidth

Schematic and Connection Diagrams



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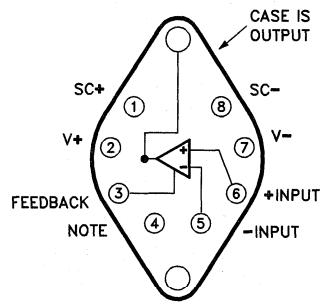

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Top View

Order Numbers LH0101K, LH0101K-MIL, LH0101CK, LH0101AK, LH0101AK-MIL or LH0101ACK
See NS Package Number K08A

Note: Electrically connected internally, no connection should be made to pin.

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications. (Note 5)

Supply Voltage, V_S ±22V

Power Dissipation at $T_A = 25°C$, P_D 5W
Derate linearly at 25°C/W to zero at 150°C,

Power Dissipation at $T_C = 25°C$ 62W
Derate linearly at 2°C/W to zero at 150°C

Differential Input Voltage, V_{IN} ±40V but < $\pm V_S$

Input Voltage Range, V_{CM} ±20V but < $\pm V_S$

Thermal Resistance—
See Typical Performance Characteristics

Peak Output Current (50 ms pulse), $I_{O(PK)}$ 5A

Output Short Circuit Duration
(within rated power dissipation,
$R_{SC} = 0.35\Omega$, $T_A = 25°C$) Continuous

Operating Temperature Range, T_A
LH0101AC, LH0101C −25°C to +85°C
LH0101A, LH0101 −55°C to +125°C

Storage Temperature Range, T_{STG} −65°C to +150°C

Maximum Junction Temperature, T_J 150°C

Lead Temperature (Soldering <10 sec.) 260°C

ESD rating to be determined.

DC Electrical Characteristics (Note 1) $V_S = \pm 15V$, $T_A = 25°C$ unless otherwise noted

Symbol	Parameter	Conditions			LH0101AC LH0101A			LH0101C LH0101			Units
					Min	Typ	Max	Min	Typ	Max	
V_{OS}	Input Offset Voltage					1	3		5	10	mV
		$T_{MIN} \le T_A \le T_{MAX}$					7			15	
$\Delta V_{OS}/\Delta P_D$	Change in Input Offset Voltage with Dissipated Power	(Note 2)				150			300		µV/W
$\Delta V_{OS}/\Delta T$	Change in Input Offset Voltage with Temperature	$V_{CM} = 0$				10			10		µV/°C
I_B	Input Bias Current						300			1000	pA
			$T_A \le T_{MAX}$	LH0101C/AC			60			60	nA
				LH0101/A			300			1000	
I_{OS}	Input Offset Current						75			250	pA
			$T_A \le T_{MAX}$	LH0101C/AC			15			15	nA
				LH0101/A			75			250	
A_{VOL}	Large Signal Voltage Gain	$V_O = \pm 10V$ $R_L = 10\Omega$			50	200		50	200		V/mV
V_O	Output Voltage Swing	$R_{SC} = 0$	$R_L = 100\Omega$		±12	±12.5		±12	±12.5		V
		$A_V = +1$	$R_L = 10\Omega$		±11.25	±11.6		±11.25	±11.6		
		Note 3	$R_L = 5\Omega$		±10.5	±11		±10.5	±11		
CMRR	Common Mode Rejection Ratio	$\Delta V_{IN} = \pm 10V$			85	100		85	100		dB
PSRR	Power Supply Rejection Ratio	$\Delta V_S = \pm 5V$ to $\pm 15V$			85	100		85	100		
I_S	Quiescent Supply Current					28	35		28	35	mA

AC Electrical Characteristics (Note 1), $V_S = \pm 15V$, $T_A = 25°C$

Symbol	Parameter	Conditions		LH0101 LH0101A			LH0101C LH0101AC			Units
				Min	Typ	Max	Min	Typ	Max	
e_n	Equivalent Input Noise Voltage	f = 1 kHz			25			25		$nV\sqrt{Hz}$
C_{IN}	Input Capacitance	f = 1 MHz			3.0			3.0		pF
	Power Bandwidth, −3 dB	$R_L = 10\Omega$	$A_V = +1$		300			300		kHz
SR	Slew Rate			7.5 (Note 4)	10			10		V/μs
t_r, t_f	Small Signal Rise or Fall Time				200			200		ns
	Small Signal Overshoot				10			10		%
GBW	Gain-Bandwidth Product	$R_L = \infty$		4.0 (Note 4)	5.0			5.0		MHz
t_s	Large Signal Settling Time to 0.01%				2.0			2.0		μs
THD	Total Harmonic Distortion	$P_o = 10W$, f = 1 kHz, $R_L = 10\Omega$			0.008			0.008		%

Note 1: Specification is at $T_A = 25°C$. Actual values at operating temperature may differ from the $T_A = 25°C$ value. When supply voltages are ±15V, quiescent operating junction temperature will rise approximately 20°C without heat sinking. Accordingly, V_{OS} may change 0.5 mV and I_B and I_{OS} will change significantly during warm-ups. Refer to the I_B vs. temperature and power dissipation graphs for expected values. Power supply voltage is ±15V. Temperature tests are made only at extremes.

Note 2: Change in offset voltage with dissipated power is due entirely to average device temperature rise and not to differential thermal feedback effects. Test is performed without any heat sink.

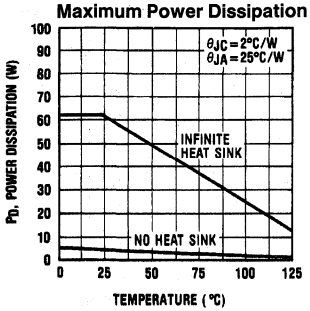
Note 3: At light loads, the output swing may be limited by the second stage rather than the output stage. See the application section under "Output swing enhancement" for hints on how to obtain extended operation.

Note 4: These parameters are sample tested to 10% LTPD.

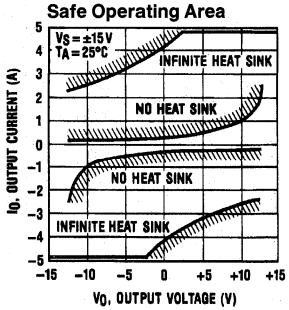
Note 5: Refer to RETS0101AK for the LH0101AK military specifications and RETS0101K for the LH0101K military specifications.

Typical Performance Characteristics

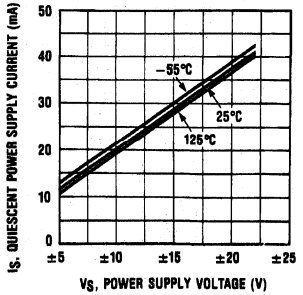
Maximum Power Dissipation



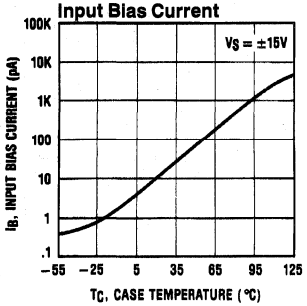
Safe Operating Area



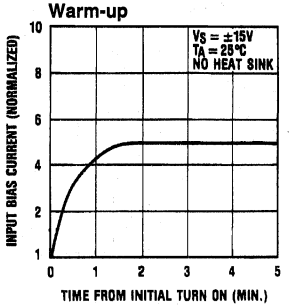
Quiescent Power Supply Current



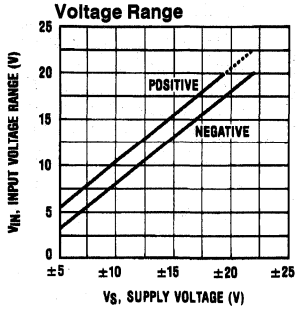
Input Bias Current



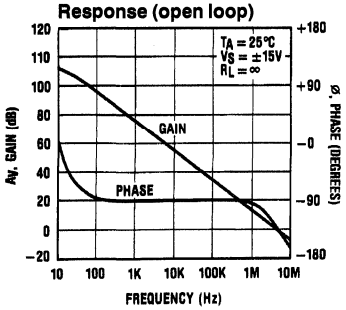
Input Bias Current after Warm-up



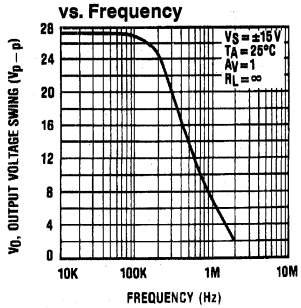
Input Common-Mode Voltage Range



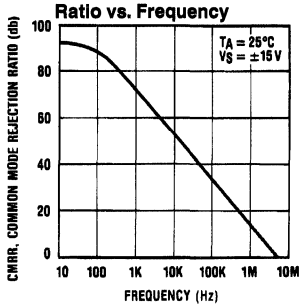
Small Signal Frequency Response (open loop)



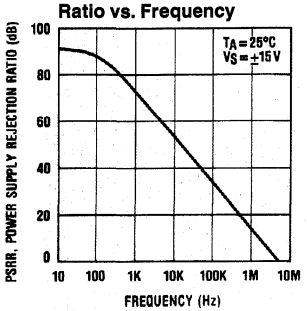
Output Voltage Swing vs. Frequency



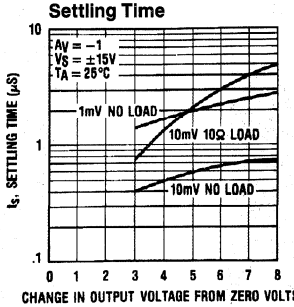
Common-Mode Rejection Ratio vs. Frequency



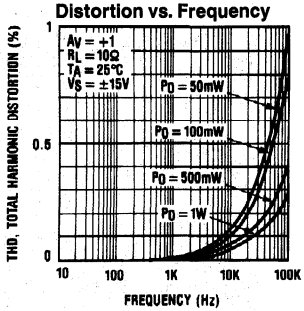
Power Supply Rejection Ratio vs. Frequency



Settling Time



Total Harmonic Distortion vs. Frequency



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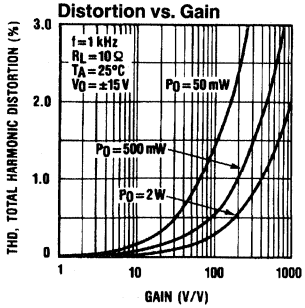
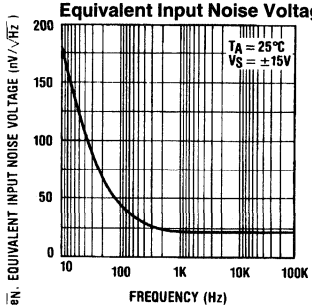
Typical Performance Characteristics (Continued)

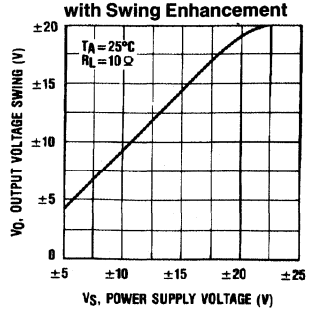
Total Harmonic Distortion vs. Gain



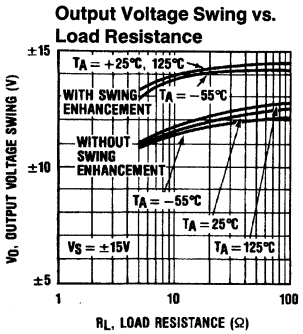
Equivalent Input Noise Voltage



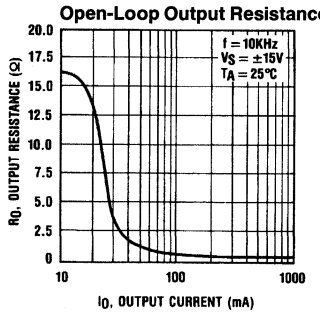
Output Voltage Swing with Swing Enhancement



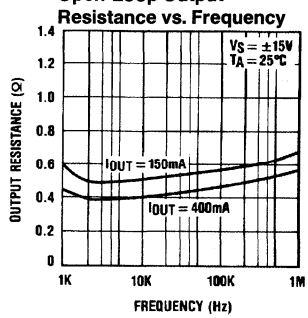
Output Voltage Swing vs. Load Resistance



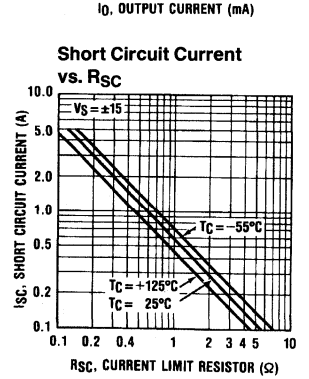
Open-Loop Output Resistance



Open-Loop Output Resistance vs. Frequency

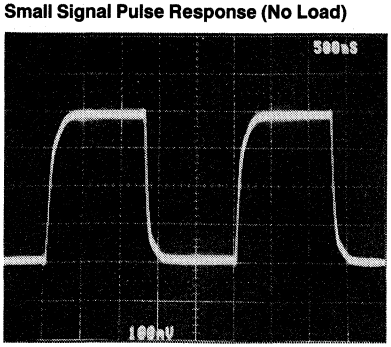


Short Circuit Current vs. R_{SC}



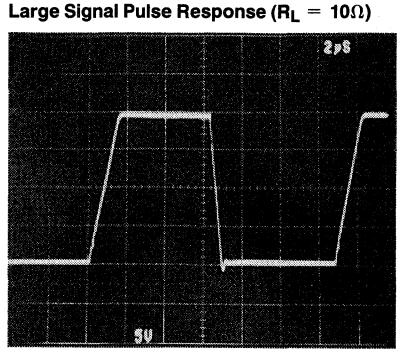
TL/K/5558–4

Small Signal Pulse Response (No Load)



TL/K/5558–5

Large Signal Pulse Response (R_L = 10Ω)



TL/K/5558–6

Application Hints

Input Voltages

The LH0101 operational amplifier contains JFET input devices which exhibit high reverse breakdown voltages from gate to source or drain. This eliminates the need for input clamp diodes, so that high differential input voltages may be applied without a large increase in input current. However, neither input voltage should be allowed to exceed the negative supply as the resultant high current flow may destroy the unit.

Exceeding the negative common-mode limit on either input will cause a reversal of the phase to the output and force the amplifier output to the corresponding high or low state. Exceeding the negative common-mode limit on both inputs will force the amplifier output to a high state. In neither case does a latch occur since raising the input back within the common-mode range again puts the input stage and thus the amplifier in a normal operating mode.

Exceeding the positive common-mode limit on a single input will not change the phase of the output however, if both inputs exceed the limit, the output of the amplifier will be forced to a high state.

These amplifiers will operate with the common-mode input voltage equal to the positive supply. In fact, the common-mode voltage may exceed the positive supply by approximately 100 mV, independent of supply voltage and over the full operating temperature range. The positive supply may therefore be used as a reference on an input as, for example, in a supply current monitor and/or limiter.

With the LH0101 there is a temptation to remove the bias current compensation resistor normally used on the non-inverting input of a summing amplifier. Direct connection of the inputs to ground or a low-impedance voltage source is not recommended with supply voltages greater than 3V. The potential problem involves loss of one supply which can cause excessive current in the second supply. Destruction of the IC could result if the current to the inputs of the device is not limited to less than 100 mA or if there is much more than 1 μF bypass on the supply buss.

Although difficulties can be largely avoided by installing clamp diodes across the supply lines on every PC board, a conservative design would include enough resistance in the input lead to limit current to 10 mA if the input lead is pulled to either supply by internal currents. This precaution is by no means limited to the LH0101.

Layout Considerations

When working with circuitry capable of resolving pico-ampere level signals, leakage currents in circuitry external to the op amp can significantly degrade performance. High quality insulation is a must (Kel-F and Teflon rate high). Proper cleaning of all insulating surfaces to remove fluxes and other residues is also required. This includes the IC package as well as sockets and printed circuit boards. When operating in high humidity environments or near 0°C, some form of surface coating may be necessary to provide a moisture barrier.

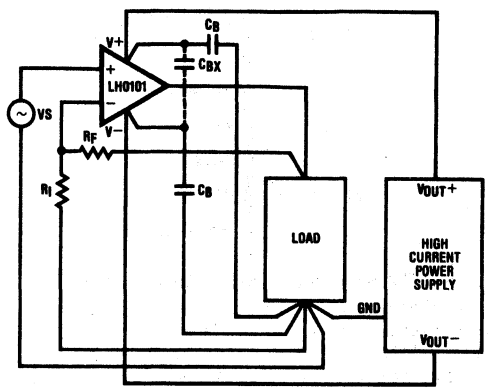
The effects of board leakage can be minimized by encircling the input circuitry with a conductive guard ring operated at a potential close to that of the inputs.

Electrostatic shielding of high impedance circuitry is advisable.

Error voltages can also be generated in the external circuitry. Thermocouples formed between dissimilar metals can cause hundreds of microvolts of error in the presence of temperature gradients.

Since the LH0101 can deliver large output currents, careful attention should be paid to power supply, power supply bypassing and load currents. Incorrect grounding of signal inputs and load can cause significant errors.

Every attempt should be made to achieve a single point ground system as shown in the figure below.



TL/K/5558–7

FIGURE 1. Single-Point Grounding

Bypass capacitor C_{BX} should be used if the lead lengths of bypass capacitors C_B are long. If a single point ground system is not possible, keep signal, load, and power supply from intermingling as much as possible. For further information on proper grounding techniques refer to "Grounding and Shielding Techniques in Instrumentation" by Morrison, and "Noise Reduction Techniques in Electronic Systems" by Ott (both published by John Wiley and Sons).

Leads or PC board traces to the supply pins, short-circuit current limit pins, and the output pin must be substantial enough to handle the high currents that the LH0101 is capable of producing.

Short Circuit Current Limiting

Should current limiting of the output not be necessary, SC+ should be shorted to V+ and SC− should be shorted to V−. Remember that the short circuit current limit is dependent upon the total resistance seen between the supply and current limit pins. This total resistance includes the desired resistor plus leads, PC Board traces, and solder joints.* Assuming a zero TCR current limit resistor, typical temperature coefficient of the short circuit current will be approximately .3%/°C.

*Short circuit current will be limited to approximately $\frac{0.6}{RSC}$.

Application Hints (Continued)

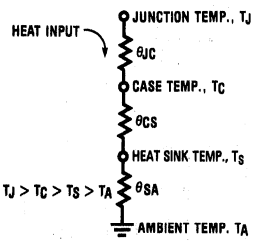
Thermal Resistance

The thermal resistance between two points of a conductive system is expressed as:

$$\theta_{12} = \frac{T_1 - T_2}{P_D} °C/W$$

where subscript order indicates the direction of heat flow. A simplified heat transfer circuit for a cased semiconductor and heat sink system is shown in the figure below.

The circuit is valid only if the system is in thermal equilibrium (constant heat flow) and there are, indeed, single specific temperatures T_J, T_C and T_S (no temperature distribution in junction, case, or heat sink). Nevertheless, this is a reasonable approximation of actual performance.



TL/K/5558-8

FIGURE 2. Semiconductor-Heat Sink Thermal Circuit

The junction-to-case thermal resistance θ_{JC} specified in the data sheet depends upon the material and size of the package, die size and thickness, and quality of the die bond to the case or lead frame. The case-to-heat sink thermal resistance θ_{CS} depends on the mounting of the device to the heat sink and upon the area and quality of the contact surface. Typical θ_{CS} for a TO-3 package is 0.5 to 0.7°C/W, and 0.3 to 0.5°C/W using silicone grease.

The heat sink to ambient thermal resistance θ_{SA} depends on the quality of the heat sink and the ambient conditions.

Cooling is normally required to maintain the worst case operating junction temperature T_J of the device below the specified maximum value $T_{J(MAX)}$. T_J can be calculated from known operating conditions. Rewriting the above equation, we find:

$$\theta_{JA} = \frac{T_J - T_A}{P_D} °C/W$$

$$T_J = T_A + P_D\theta_{JA} °C$$

Where: P_D $(V_S - V_{OUT})I_{OUT} + |V+ - (V-)|I_Q$ for a DC Signal

$\theta_{JA} = \theta_{JC} + \theta_{CS} + \theta_{SA}$ and V_S = Supply Voltage

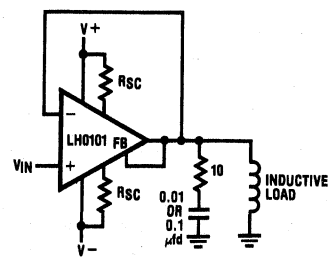
θ_{JC} for the LH0101 is about 2°C/W.

Stability and Compensation

As with most amplifiers, care should be taken with lead dress, component placement and supply decoupling in order to ensure stability. For example, resistors from the output to an input should be placed with the body close to the input to minimize "pickup" and maximize the frequency of the feedback pole by minimizing the capacitance from the input to ground.

A feedback pole is created when the feedback around any amplifier is resistive. The parallel resistance and capacitance from the input device (usually the inverting input) to ac ground set the frequency of the pole. In many instances the frequency of this pole is much greater than the expected 3 dB frequency of the closed loop gain and consequently there is negligible effect on stability margin. However, if the feedback pole is less than approximately six times the expected 3 dB frequency a lead capacitor should be placed from the output to the input of the op amp. The value of the added capacitor should be such that the RC time consistant of this capacitor and the resistance it parallels is greater than or equal to the original feedback pole time constant.

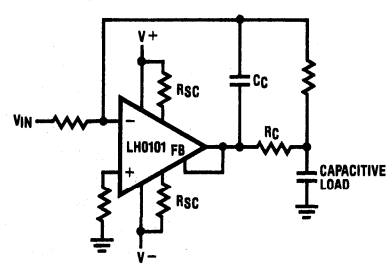
Some inductive loads may cause output stage oscillation. A .01 μF ceramic capacitor in series with a 10Ω resistor from the output to ground will usually remedy this situation.



TL/K/5558-9

FIGURE 3. Driving Inductive Loads

Capacitive loads may be compensated for by traditional techniques. (See "Operational Amplifiers: Theory and Practice" by Roberge, published by Wiley):



TL/K/5558-10

FIGURE 4. R_C and C_C Selected to Compensate for Capacitive Load

A similar but alternative technique may be used for the LH0101:

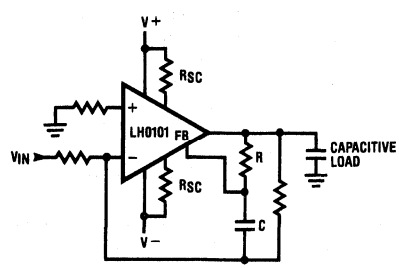


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FIGURE 5. Alternate Compensation for Capacitive Load

Application Hints (Continued)

Output Swing Enhancement

When the feedback pin is connected directly to the output, the output voltage swing is limited by the driver stage and not by output saturation. Output swing can be increased as shown by taking gain in the output stage as shown in High Power Voltage Follower with Swing Enhancement below. Whenever gain is taken in the output stage, as in swing enhancement, either the output stage, or the entire op amp must be appropriately compensated to account for the additional loop gain.

Output Resistance

The open loop output resistance of the LH0101 is a function of the load current. No load output resistance is approximately 10Ω. This decreases to under 1Ω for load currents exceeding 100 mA.

Typical Applications

See AN261 for more information.

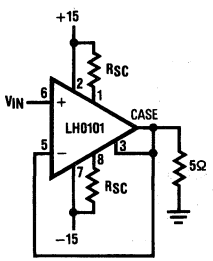

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FIGURE 6. High Power Voltage Follower

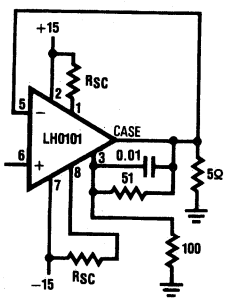

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FIGURE 7. High Power Voltage Follower with Swing Enhancement

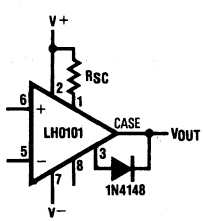

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FIGURE 8. Restricting Outputs to Positive Voltages Only

Following is a partial list of sockets and heat dissipators for use with the LH0101. National assumes no responsibility for their quality or availability.

8-Lead TO-3 Hardware

SOCKETS

Keystone 4626 or 4627
Robinson Nugent 0002011
Azimuth 6028 (test socket)

HEAT SINKS

Thermalloy 2266B (35°C/W)
IERC LAIC3B4CB
IERC HP1-TO3-33CB (7°C/W)
AAVID 5791B

MICA WASHERS

Keystone 4658

AAVID Engineering
30 Cook Court
Laconia, New Hampshire 03246

Azimuth Electronics
2377 S. El Camino Real
San Clemente, CA 92572

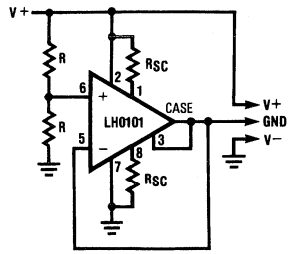
IERC
135 W. Magnolia Blvd.
Burbank, CA 91502

Keystone Electronics Corp.
49 Bleecker St.
New York, NY 10012

Robinson Nugent Inc.
800 E. 8th St.
New Albany, IN 47150

Thermalloy
P.O. Box 34829
Dallas, TX 75234

Typical Applications (Continued)



TL/K/5558–15

FIGURE 9. Generating a Split Supply from a Single Voltage Supply

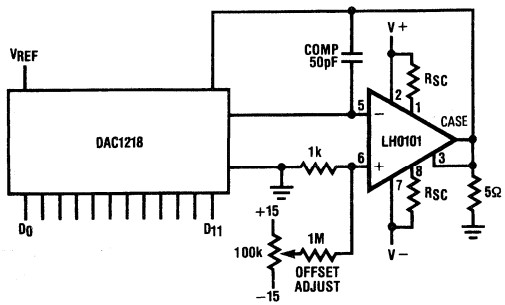


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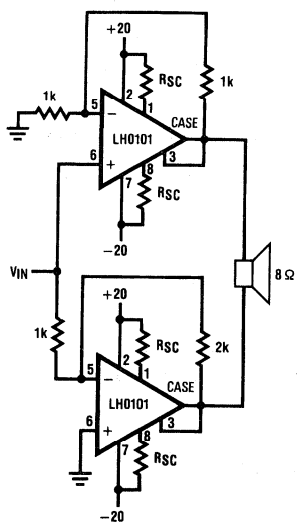
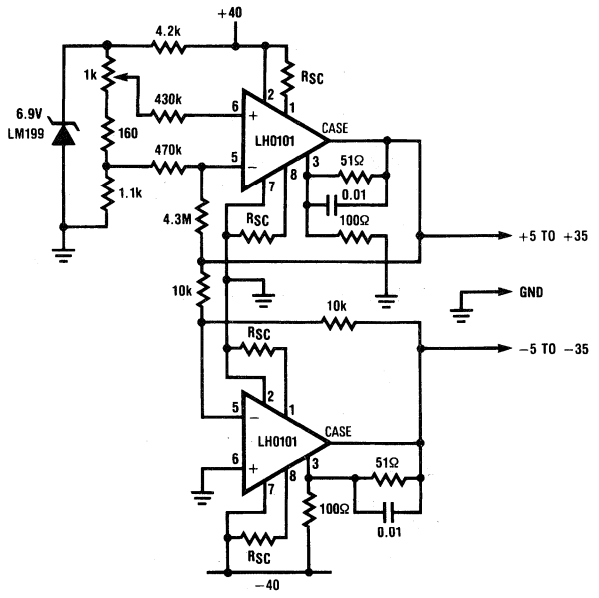
FIGURE 10. Power DAC



TL/K/5558–17

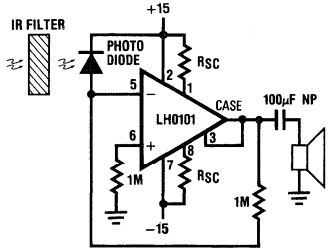
FIGURE 11. Bridge Audio Amplifier

Typical Applications (Continued)



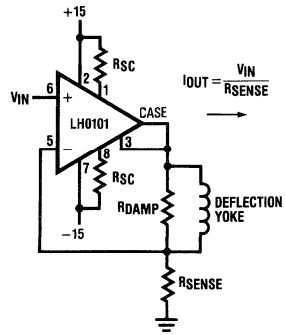
TL/K/5558–18

FIGURE 12. ±5 to ±35 Power Source or Sink



TL/K/5558–19

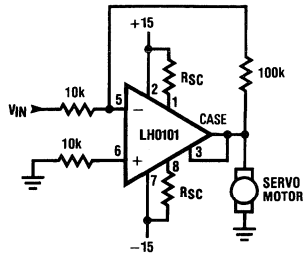
FIGURE 13. Remote Loudspeaker via Infrared Link



TL/K/5558–20

FIGURE 14. CRT Deflection Yoke Driver

Typical Applications (Continued)



TL/K/5558–21

FIGURE 15. DC Servo Amplifier

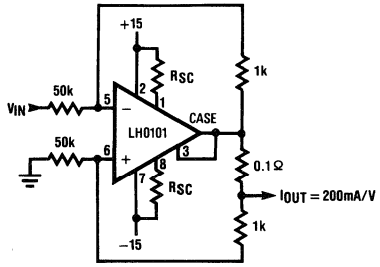


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FIGURE 16. High Current Source/Sink

National Semiconductor

LH4104G-MIL Fast Settling High Current Operational Amplifier

General Description

The LH4104 is a fast settling high current Bi-Fet op amp designed for applications that require a fast settling time of 500 ns to 0.01% and 100 mA continuous output current. The high output current eliminates the need for a buffer to provide the additional current drive not available in most operational amplifiers. The operational amplifier also features a gain bandwidth product of 18 MHz and a slew rate of 40V/μs.

Designed for use with minimum external circuitry, the LH4104 provides internal compensation for unity gain stability as well as internal supply bypass capacitors. These features minimize the circuit's sensitivity to external layout conditions.

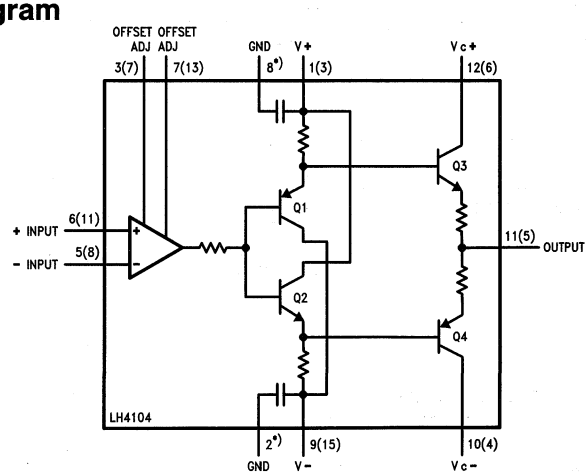
Features

- 500 ns settling time to 0.01% for a 10V step
- 100 mA continuous output current
- 18 MHz gain bandwidth product
- Internal supply bypassing
- Unity gain stable

Applications

- Cable Drivers
- High Speed Ramp Generators
- DAC Output Amplifiers
- Fast Buffers
- Sample and Holds
- Fast Integrators

Schematic Diagram



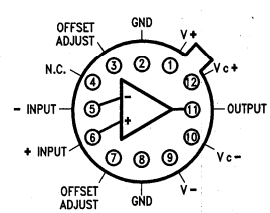
TL/K/8840-1

Pinout shown for metal can package (for molded package in parenthesis)

*On metal can package (G) pins #2 and #8 are internally connected. The case is electrically isolated. The molded package (N) does not have ground connections or bypass capacitors.

Connection Diagrams

Metal Can Package



TL/K/8840-2

Top View

Order Number LH4104G-MIL
See NS Package Number H12B

Absolute Maximum Ratings

Supply Voltage, V_S ±18V

Steady State Output Current, I_o 100 mA

Power Dissipation (See Curves)

T_A = 25°C, LH4104G-MIL 1.5W

T_C = 25°C, LH4104G-MIL 2.5W

Differential Input Voltage, V_{IN} ±30V but ≤ $\pm 2V_s$

Input Voltage Range, V_{CM} ±18V but ≤ $\pm V_s$

Operating Temperature Range, T_A

LH4104 −55°C to +125°C

Storage Temperature Range, T_{STG} −65°C to +150°C

Maximum Junction Temperature, T_j 150°C

Lead Temperature (Soldering < 10 sec.) 300°C

ESD rating is to be determined.

DC Electrical Characteristics V_{CC} = ±15V, T_A = 25°C unless otherwise noted (Notes 1 and 6)

Symbol	Parameter	Conditions	LH4104G-MIL		(Max Unless Otherwise Stated)
			Typ	Tested Limit (Note 2)	
V_{OS}	Input Offset Voltage	R_S = 50Ω	2	**10**	mV
$V_{OS}/\Delta T$	Offset Voltage Drift	R_S = 50Ω	20		µV/°C
I_B	Input Bias Current	T_j = 25°C, (Note 4) V_{CM} = 0V	200	600	pA
				350	nA
I_{OS}	Input Offset Current	T_j = 25°C, V_{CM} = 0V	20	400	pA
				250	nA
R_{IN}	Input Resistance	T_j = 25°C	10^{11}		Ω
A_{VOL}	Large Signal Voltage Gain	R_L = 100Ω	106	87	dB (Min)
		R_L = 1 kΩ	106	87	
				80	
V_O	Output Voltage Swing	R_L = 100Ω (Note 5)		±10	V (Min)
		R_L = 1 kΩ	±13	**±10**	
CMRR	Common Mode Rejection Ratio	V_{IN} −11V to +11V	100	80	dB (Min)
				70	
PSRR	Power Supply Rejection Ratio	V_{CC} = ±10V to ±15V	100	80	dB (Min)
				70	
I_S	Supply Current		20	25	mA

AC Electrical Characteristics V_{CC} = ±15V, T_A = 25°C unless otherwise noted

Symbol	Parameter	Conditions	LH4104G-MIL			Units (Max Unless Otherwise Stated)
			Typ	Tested Limit (Note 2)	Design Limit (Note 3)	
t_S	Settling Time to 0.01%	A_V = −1, V_{IN} = −5V to +5V, R_L = 100Ω	500	800		ns
S_R	Slew Rate	V_{IN} = −10V to +10V, R_L = 100Ω	40		32	V/µs(min)
GBW	Gain Bandwidth Product		18			MHz
t_r	Small Signal Rise Time	A_V = 1, R_L = 100Ω	10		20	ns

Note 1: Boldface limits are guaranteed over full temperature range. Operating ambient temperature range of LH4104 is −55°C to +125°C.

Note 2: Tested limits are guaranteed and 100% production tested.

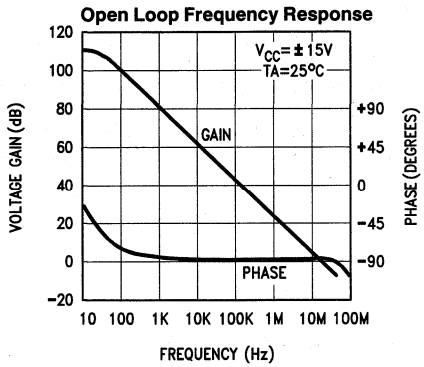
Note 3: Design limits are guaranteed (but not production tested).

Note 4: Specifications is at 25°C junction temperature due to requirements of high speed automatic testing. Actual values at operating temperature will exceed value at T_j = 25°C.

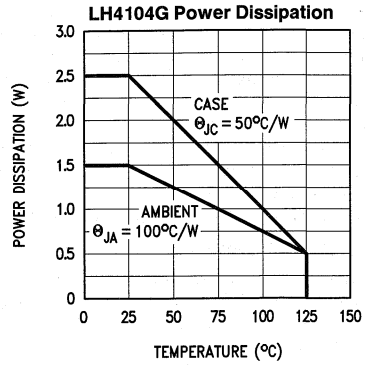
Note 5: The output swing is limited by the maximum output current of ±100 mA when R_L = 100Ω.

Note 6: When the LH4104 is operated at elevated temperture (such as 125°C), some form of heat sinking or forced air cooling is required. The quiescent power with V_{CC} of ±15V is 750 mW, whereas the package can only handle 500 mW without a heatsink at 125°C.

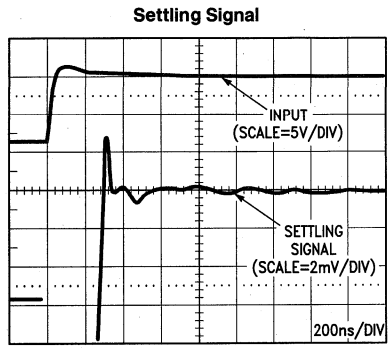
Typical Performance Characteristics



TL/K/8840–4



TL/K/8840–5



TL/K/8840–3

Applications Information

POWER SUPPLY BYPASSING

The LH4104 will perform well in most circuit boards even without external supply bypassing; however it is recommended that some bulk bypassing be provided to maintain optimum settling time. A 0.1 μF disc ceramic capacitor and 1 μF tantalum capacitor on each supply is recommended. Place the bypass capacitors close to the amplifiers supply pins.

COMPENSATION

To minimize the effects of input capacitance at the LH4104's inverting input and any additional layout capacitance, an external compensation capacitor must be used. The compensation capacitor (C1) used in *Figure 2* (Test Circuit Section) is typically 66 pF. The optimum value for the compensation capacitor depends on the application circuit and the board layout.

INPUT BIAS CURRENT

The input devices are JFETs, and will normally have input bias (I_B) currents in the tens of picoamps. However, these currents vary with temperature and input voltage range. I_B will normally double with each 11°C rise in junction temperature.

LAYOUT PRECAUTIONS

Grounding and circuit layout are extremely important in preserving the settling time of the LH4104. It is important to use single point ground returns for inputs, loads, and feedback components and to keep the returns short. Compensation components should be located close to the appropriate pins to minimize stray reactances. Keep the system's digital signals (or any other signals with fast rise times) separated from the amplifier. If such signals are too close to the amplifier, they can couple capacitively to the amplifier's inputs, resulting in undesirable signals at the output.

PRESERVING AND VERIFYING THE LH4104'S FAST SETTLING TIME

To realize optimum settling performance in circuits using the LH4104, both the design and layout must be meticulous. Application note AN-428, "Preserving and Verifying the

Applications Information (Continued)

LF400's Fast Settling Time", explains the required design and measurement techniques. Although this application note was written for the LF400, it suggests good guidelines and is directly applicable to the LH4104. Only the sections covering supply bypassing and output load limitations should be ignored. This is because the LH4104 has internal bypassing capacitors and substantially greater output drive current than the LF400. The suggested circuits require only small and straightforward modifications; even the printed circuit board layout can be easily modified to accept the footprint of the LH4104 without impacting setting time.

PROTECTION SCHEMES FOR THE LH4104

The LH4104 has similar input characteristics of National Semiconductor's BI-FET™ family of operational amplifiers. As such, designing with this part requires that several precautions are observed which are uncharacteristic of other op amps. Application Note AN-447 covers these caveats in greater detail for the whole product family. (The LH4104's input stage shares its topology with the LF400.)

NEVER LEAVE AN INPUT UNATTENDED!

If an input to the LH4104 is left open circuited (or connected to an analog multiplexer in a high impedance state), the input bias current will be drawn from the very small parasitic input capacitance (<10 pF). This capacitor will rapidly charge up to the power supply rail at a rate of $dv/dt = I_{BIAS}/C_{IN}$. Since the LH4104 is capable of large output currents and has no internal current limiting, it will easily be destroyed by excessive power dissipation if such an input condition exists while driving a low impedance load (e.g. 50Ω).

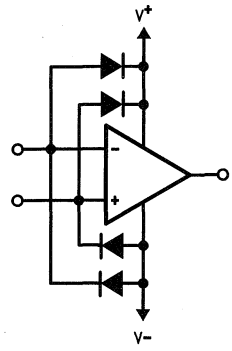
To avoid this condition in circuits where the LH4104 is buffering the FET switch of an analog multiplexer, one must connect a resistor between the input and ground to provide a bias current path. This will invariably degrade the effective input impedance of the device, so a large resistor is desirable.

For example, selecting a 1 MΩ resistor will result in a harmless 25 mV output signal during the "deselected" state (for the worst case bias current of 25 nA). Increasing this resistor will increase the output signal for the deselected" state; decreasing it will reduce this signal while degrading the input impedance. Depending on the user's circuit specifications, a compromise must be selected. This resistor will not introduce an increase in the effective offset voltage during the "selected" state because the input is driven by a low impedance source.

POWER SUPPLY SEQUENCING

Adding the clamp diodes shown in *Figure 1* not only protects the inputs from transients when the circuit is operating, but protects them as power is being applied to the circuit. Because the parasitic transistor apears when the input voltage is less than the negative supply, applying the positive supply or input voltage before the negative supply is applied can cause this problem. For this reason, it is always recommended that the negative supply be turned on **first,** if the supplies can be turned on independently.

Also, even if the input stage is well protected with clamp diodes and current limiting, the inputs should not be allowed to be heavily unbalanced (for example, one input at ground and the other at the rail) for extended periods of time (for example, many hours). The long-term effects of an unbalanced differential pair are increased offset voltage and offset current.



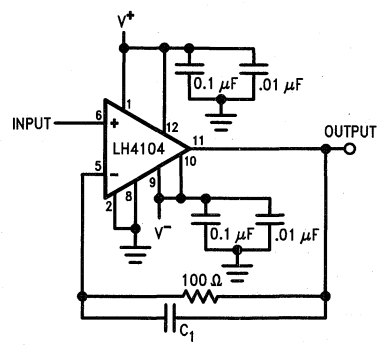
TL/K/8840–13

FIGURE 1. Clamping Inputs of Op Amp

V_{OS} ADJUSTMENT

Offset voltage can be nulled using a 56K resistor and a 25K potentiometer connected to pins 3 and 7 as shown in *Figure 3.* Bypassing the V_{OS} adjust pins with 0.1 μF capacitors will help to avoid noise pickup. When not used for offset adjustment, pins 3 and 7 can often be left open, but to minimize the possibility of noise pickup the unused V_{OS} trim pins should be connected to ground or V^-.

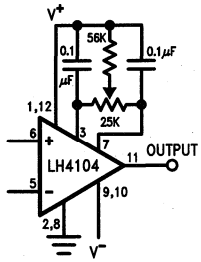
Test Circuit for Pulse Response



TL/K/8840–6

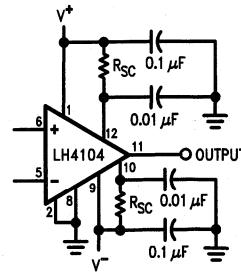
FIGURE 2

Typical Applications



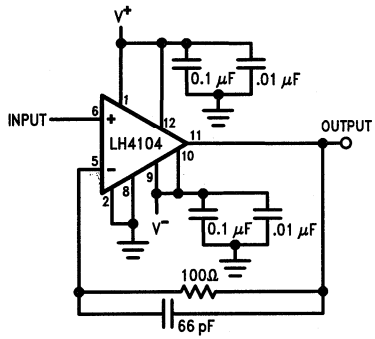
TL/K/8840–8

FIGURE 3. Offset Null



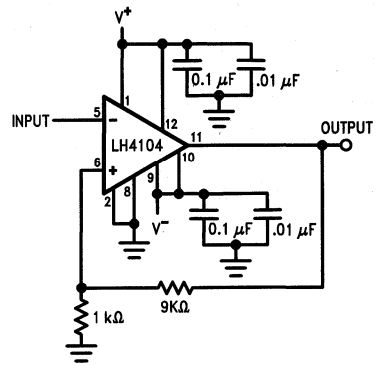
TL/K/8840–9

FIGURE 4. Using Resistor Current Limiting



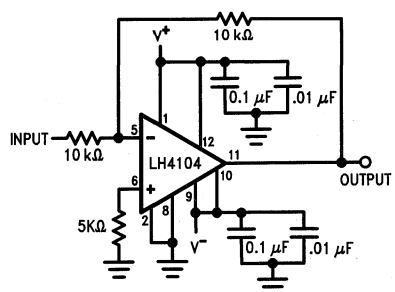
TL/K/8840–10

FIGURE 5. Unity Gain Follower



TL/K/8840–11

FIGURE 6. 10X Buffer Amplifier



TL/K/8840–12

FIGURE 7. Unity Gain Inverter

National Semiconductor

LH4118G-MIL
Current Feedback Wide Band RF Amplifier

General Description

The LH4118 is a wideband amplifier optimized for high speed, low gain applications. It is an ideal alternative to low precision amplifiers. It features a closed loop −3 dB unity gain bandwidth in excess of 200 MHz. Unlike conventional op-amps, the bandwidth is relatively independent of closed loop gain between 1 and 5. A high current output stage is also incorporated, allowing the LH4118 to drive 50Ω terminated lines directly. It is an ideal choice for video distribution, flash converter input buffering and ATE pin driver.

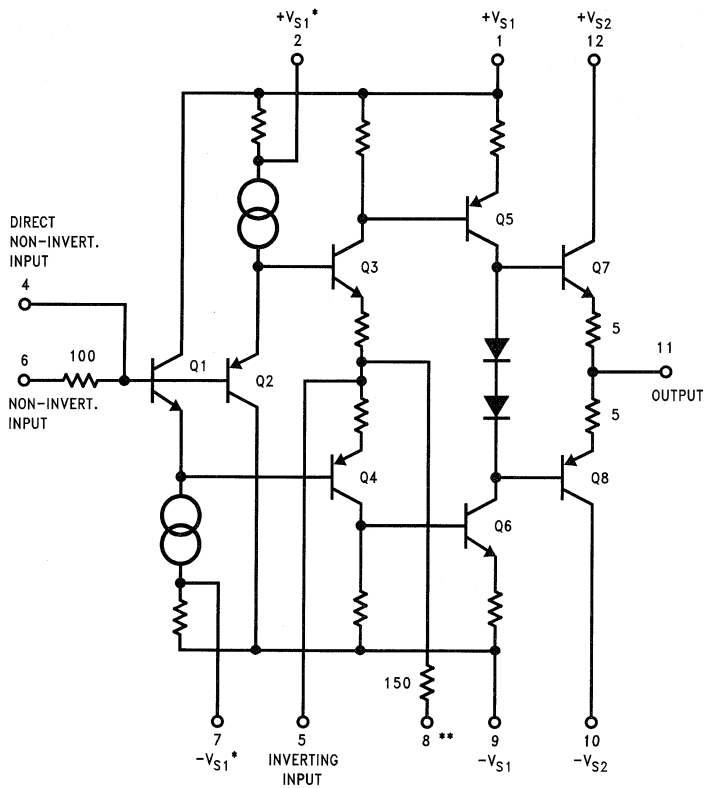
Features

- 250 MHz bandwidth
- 15 ns settling time to 0.1%
- 2.5 ns rise and fall times
- Output current to 100 mA
- 2 mV offset voltage
- 2500 V/μs slew rate (100Ω load)
- ±0.5 dB gain flatness (AV = 5)

Applications

- Unity gain buffers
- Low gain op amp
- High speed peak detectors
- Video amplifier
- Flash converter driver

Simplified Schematic



TL/K/9768–1

*Pins 2 and 7 can also be left disconnected (floating)

**The built-in 150Ω can be used as feedback resistor for A_V = 1. For details see applications section.

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

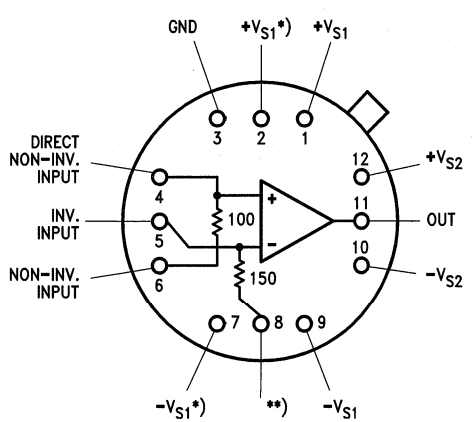
Supply Voltage, V_S	±18V
Power Dissipation, P_D (See Graph)	1.65W
Output Current	125 mA
Non-Inverting Input Voltage Range, V_{CM} (For $V_S \leq +15V$) (Note 1)	$\pm V_S$
Operating Temperature Range, T_A	−55°C to +125°C
Storage Temperature Range, T_{STG}	−65°C to +150°C
Maximum Junction Temperature, T_J	175°C
Lead Temperature (Soldering, < 10 sec.)	300°C
ESD Tolerance (Note 2)	650V

DC Electrical Characteristics

Unless otherwise noted, $R_S = 50\Omega$, $T_A = T_C = 25°C$, $V_S = \pm 15V$ (Notes 3, 4)

Symbol	Parameter	Conditions	LH4118G-MIL		Units (Max Unless Otherwise Noted)
			Typical	Tested Limit (Note 5)	
V_{OS}	Non-Inverting Input Offset Voltage	$V_{IN} = 0V$	±2	**±5**	mV
$\frac{\Delta V_{OS}}{\Delta T}$	Offset Voltage Drift		10		μV/°C
I_B	Non-Inverting Input Bias Current		±5	±25 **±30**	μA
V_O	Output Voltage Swing	$R_L = 500\Omega$	±13	±11 **±10.5**	V (Min)
V_O	Output Voltage Swing	$R_L = \infty$	±14	±12 **±11.5**	V (Min)
I_O	Output Current Swing	$R_L = 50\Omega$ (Note 6)		**±100**	mA (Min)
CMRR	Common Mode Rejection Ratio	$V_{IN} = -11V$ to $+11V$, $V_S = \pm 18V$	54	**50**	dB (Min)
PSRR	Power Supply Rejection Ratio	$\pm V_S = 9V$ to $15V$ $\Delta V = 6V$	72	**50**	dB (Min)
I_S	Quiescent Supply Current	$V_{IN} = 0V$	20		
P_D	Quiescent Power Dissipation	(Note 6)	600		
C_{IN}	Input Capacitance		1.5		pF

Connection Diagram



TL/K/9768–2

Top View

*Pins 2 and 7 can also be left disconnected (floating)

**The built-in 150Ω can be used as feedback resistor for $A_V = 1$. For details see applications section.

Order Number LH4118G-MIL
See NS Package Number H12B

AC Electrical Characteristics

Unless otherwise noted, Av = +2, R_S = 50Ω, R_L = 100Ω, V_S = ±15V, T_A = 25°C

Symbol	Parameter	Conditions		LH4118G-MIL		Units (Max Unless Otherwise Noted)
				Typical	Tested Limit	
SSBW −3 dB	Small Signal Bandwidth	V_{OUT} = 0.2 V_{P-P}		250	200	MHz (Min)
PBW −3 dB	Power Bandwidth	V_{OUT} = 10 V_{P-P}		68	55	MHz (Min)
GF	Gain Flatness	V_{OUT} = 0.2 V_{P-P}	0.5 MHz, −50 MHz	±0.3		dB (Max)
			0.5 MHz, −100 MHz	−1.0		
SR	Slew Rate	20%–80%			2000	V/μs (Min)
t_r	Rise Time	V_{OUT} = 10 V_{P-P} 10%–90%		2.5		ns
V_{GC}	−1 dB Gain Compression	f = 50 MHz		23.5		dBm
e_n	Input Noise Voltage	A_V = 5, R_S = 50Ω, f = 10 MHz		1.3		nV/√Hz
HD_2	Second Harmonic Distortion	V_{OC} = 1.27 V_{P-P} F_C = 14 MHz		−58		dBc
HD_3	Third Harmonic Distortion	V_{OC} = 1.27 V_{P-P} F_C = 14 MHz		−40		dBc
t_s	Settling Time	A_V = −1 V_{IN} = +5 V_{P-P} to 0.1%		15		ns
LVBW −3 dB	Low Supply Voltage Bandwidth	V_{OUT} = 0.2 V_{P-P} V_S = ±5V		230		MHz
LVSR	Low Supply Voltage Slew Rate	V_S = ±5V, V_{OUT} = 5 V_{P-P} 20%–80%		1400		V/μs
DG	Differential Gain	V_{IN} = ±4 V_{DC} 0.4 V_{P-P} AC f = 4 MHz		<0.01		dB
PL	Phase Linearity	V_{IN} = ±4 V_{DC} 0.4 V_{P-P} AC, f = 4 MHz		<0.1		DEG

Note 1: The input signal should be within the supply rails. Also, the input signal as well as the output signal should not be more than 30V from any supply voltage.

Note 2: The average voltage that the weakest pin combinations can withstand and still conform to the datasheet limits. The test circuit used consists of the human body model of 100 pF in series with 1500Ω.

Note 3: Boldface limits are guaranteed over full temperature range. Operating ambient temperature range of LH4118G-MIL is −55°C to +125°C.

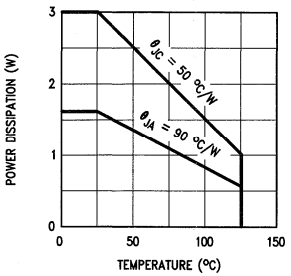
Note 4: Specifications are at 25°C junction temperature due to requirements of high speed automatic testing. Actual values at operating temperature will exceed value at T_J = 25°C.

Note 5: Tested limits are guaranteed and 100% production tested.

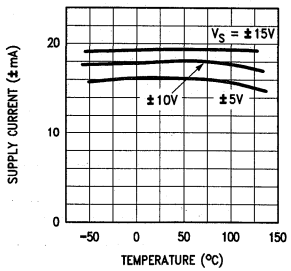
Note 6: When the LH4118 is operated at elevated temperature (such as 125°C), some form of heat sinking or forced air cooling is required. The quiescent power with V_S = ±15V is 750 mW, whereas the package can only handle 550 mW without a heatsink at 125°C.

Typical Performance Characteristics

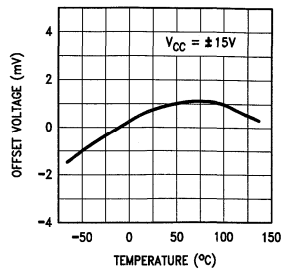
Power Dissipation



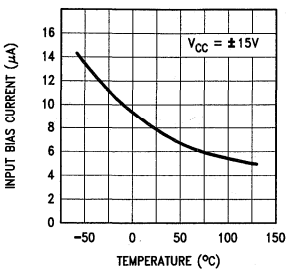
Supply Current vs Temperature



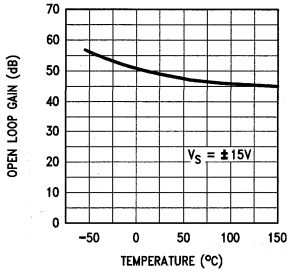
Offset Voltage vs Temperature



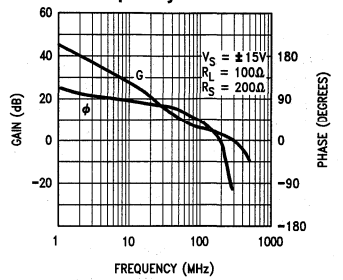
Input Bias Current vs Temperature



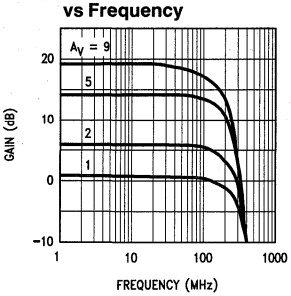
Open Loop Gain vs Temperature



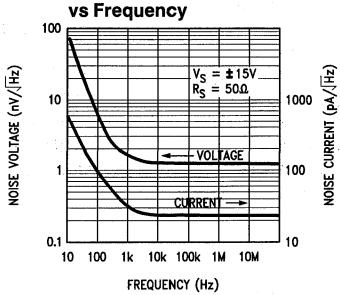
Inverting Open Loop Gain and Phase vs Frequency



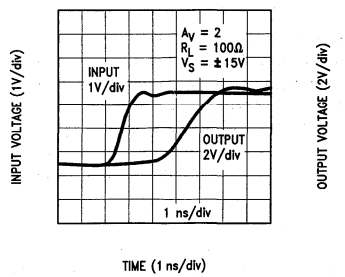
Non-Inverting Closed Loop Gain vs Frequency



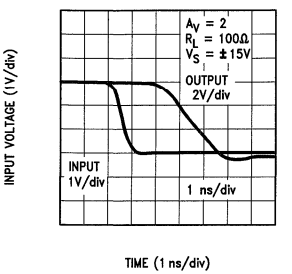
Input Noise vs Frequency



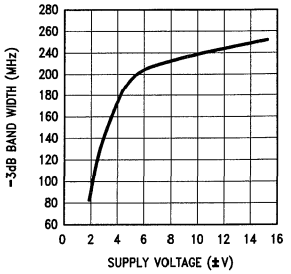
Rise Time



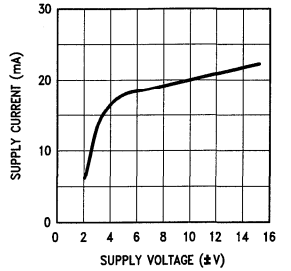
Fall Time



Bandwidth vs Supply Voltage



Supply Current vs Supply Voltage



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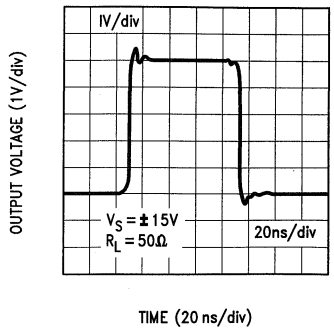
Typical Performance Characteristics (Continued)

Pulse Response



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Applications Information

LAYOUT

Breadboards should have a solid ground plane and short point-to-point wiring. Do not use wirewrap boards or techniques. PC boards should have short connections and as much ground plane as possible.

The inputs (Pins 4, 5 & 6) should have low capacitance and, therefore, the ground plane should be taken out around these pins. The body of RG should be close to Pin 5 for the same reason.

It is best to have a layout without sockets, but sockets with short pins and receptacles do not degrade the performance much.

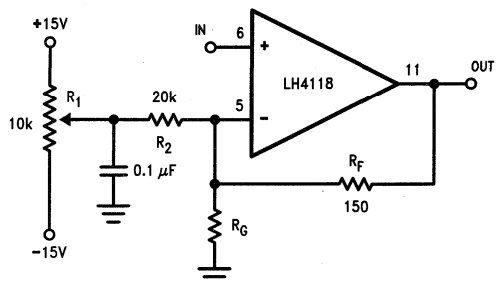
Input and output should be led by coax or microstrip if the distances are more than a few inches to avoid impedance shifts and resulting reflections.

Power supplies need to be bypassed with 0.01 μF to 0.1 μF as close as 0.15″ to the pins and additional 1 μF tantalum a maximum 1″ distant. Please make sure that the return current from the ground end of R_L does not flow across the input: the grounding point of R_L should be close to the grounding points of the power supply bypass capacitors. On the LH4118, this comes almost natural because of the layout of the pins.

The direct non-inverting input on pin 4, if used, should not see impedances of less than 100Ω.

The built-in feedback resistor (pin 8) is limited to a maximum dissipation of 150 mW. It can be used for unity gain and for higher gains at lower amplitudes.

Output Offset Zero Adjust

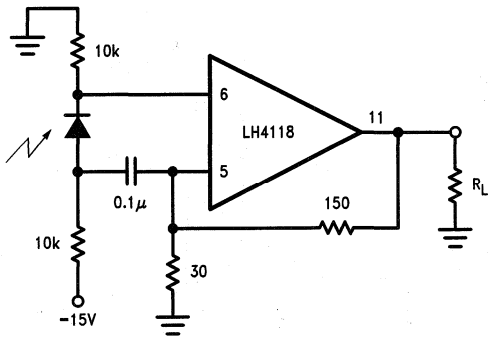


TL/K/9768–5

This circuit lets the V_{OS} between non-inverting input (pin 6) and output (pin 11) be adjusted. For $R_G = 15\Omega$ the range of adjustment is ± 11 mV, for higher R_G proportionately more. For higher R_G it is recommended to increase R_2 to decrease the range and make trimming less sensitive.

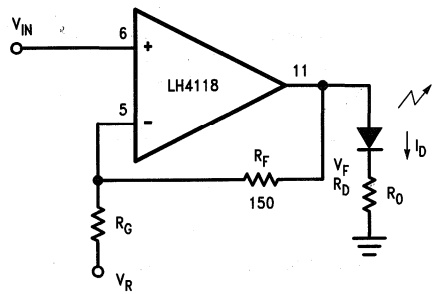
There is also an offset between inverting and non-inverting input which cannot be trimmed out.

Typical Applications



TL/K/9768–6

FIGURE 1. Bootstrapped Fiber Optic Receiver



$$I_D = I_{BIAS} + I_{Signal}$$

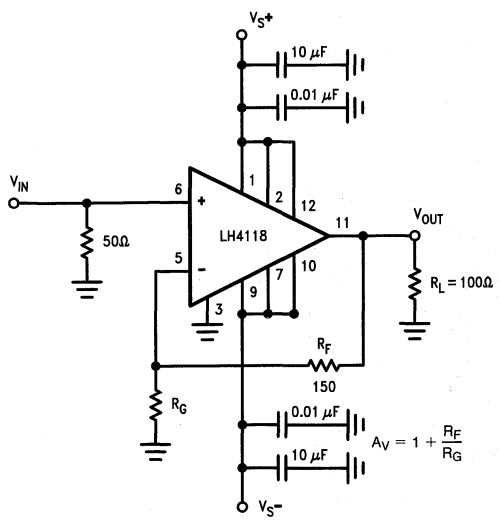
$$I_{BIAS} = \frac{V_R(-R_F/R_G) - V_F}{R_O}$$

$$I_{Signal} = \frac{V_{IN}(1 + R_F/R_G}{R_O + R_D}$$

$$R_D \approx 26\ mV/I_{BIAS}$$

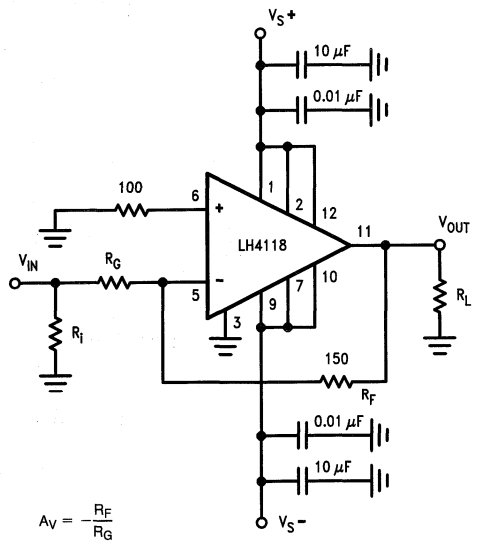
TL/K/9768–7

FIGURE 2. Fiber Optic Transmitter



TL/K/9768–8

FIGURE 3. Non-Inverting Circuit

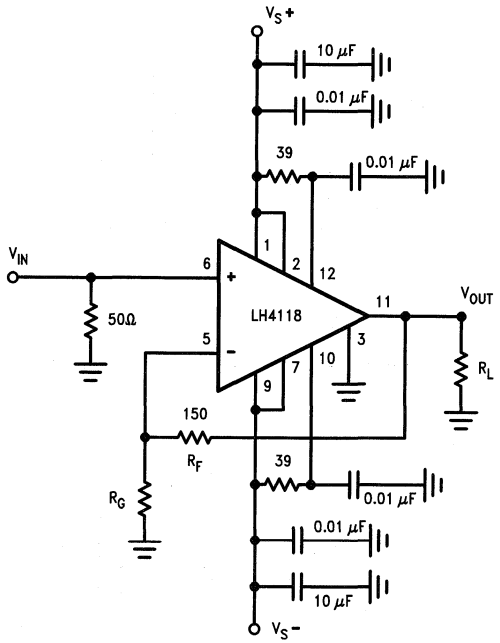


TL/K/9768–9

R_i is selected so that $R_i \,||\, R_G$ matches the line impedance (e.g., 50Ω)

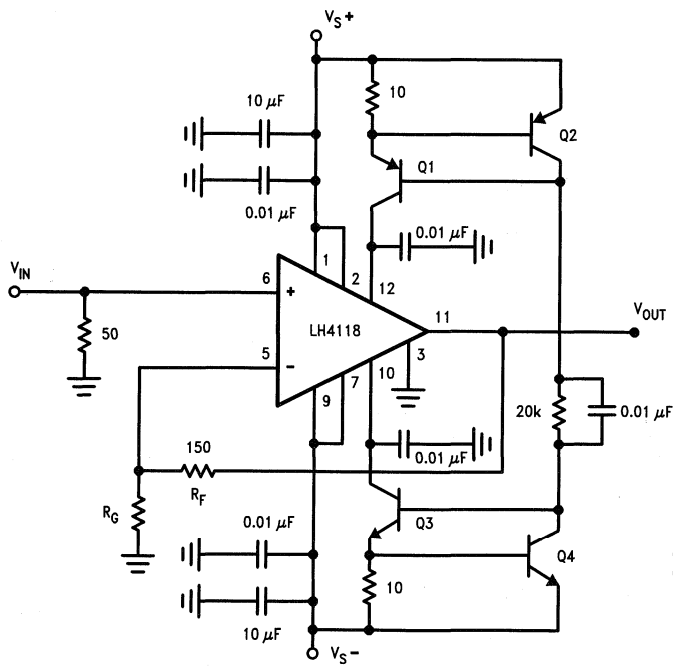
FIGURE 4. Inverting Circuit

Typical Applications (Continued)



TL/K/9768–10

FIGURE 5. Current Limiting Using Resistor



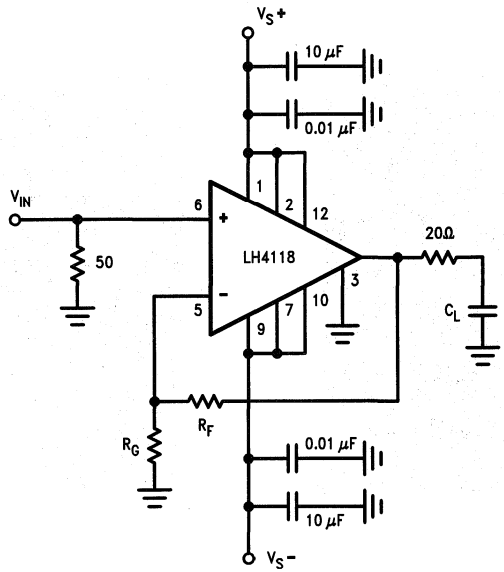
Q1 = Q2 = 2N2905
Q3 = Q4 = 2N2219

TL/K/9768–11

The current cutoff is set to $I = \frac{VBE}{R} = \frac{600\ mV}{10\Omega} = 60$ mA. Higher current peaks are sustained by the 0.01 µF Capacitors.

FIGURE 6. Current Limiting Using Transistor Current Source

Typical Applications (Continued)

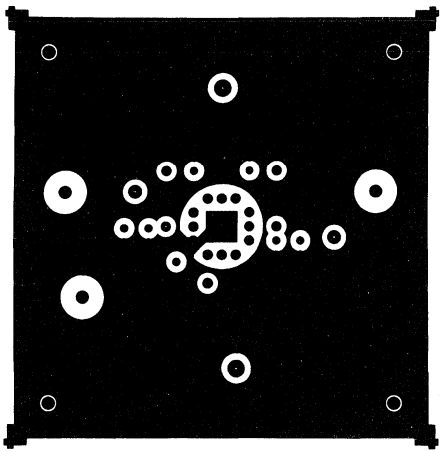


TL/K/9768–12

A series resistor between 5Ω and 50Ω helps to stabilize capacitive loads. There is, however, a corresponding drop in bandwidth.

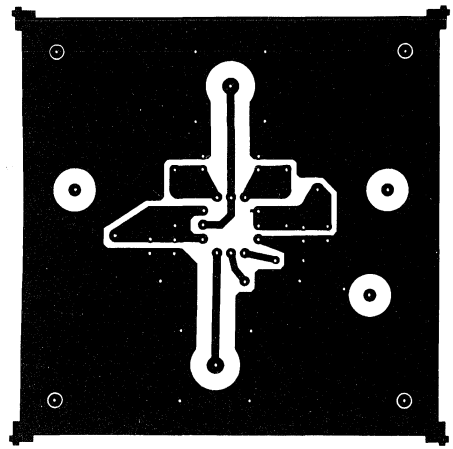
Evaluation Board

(3″ x 3″, not to scale)



TL/K/9768–13

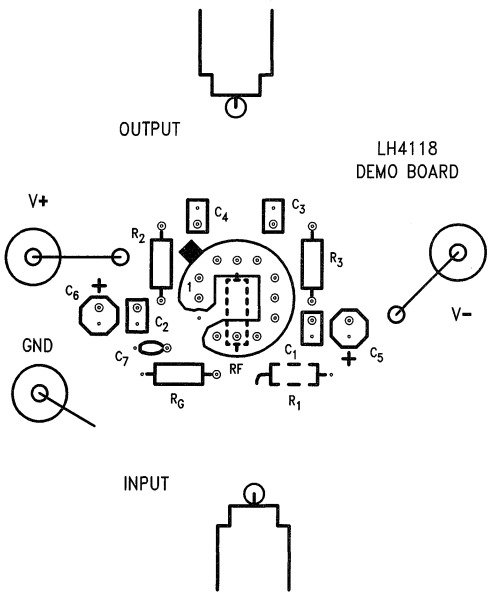
Top



TL/K/9768–14

Bottom

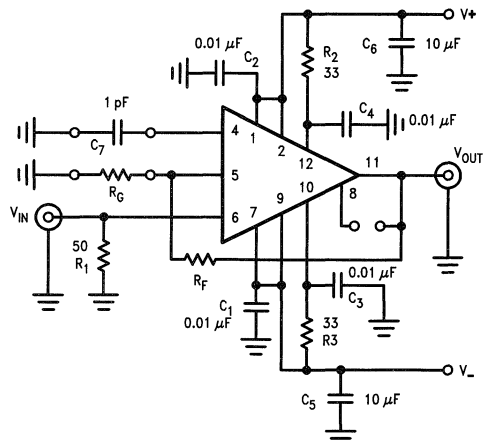
Components



TL/K/9768–15

Top View

Schematic Diagram



TL/K/9768–16

Input and output connections are made through BNC connectors. When the indicated cut-outs are made, the connectors can be placed in-line. As an alternative, Amphenol No. 31-4758 connectors can be used soldered upright into the board.

R1 is the termination resistor of the input line. It is mounted on the bottom of the board, with one side soldered flat to the center of the input strip-line.

The LH4118 can be soldered directly into the board or Hole-tight pins can be used (Augat part No. 8134-HC-5P2). These pins need plated through holes with a finished inner diameter of 41 ±2 Mil. For $A_V = 1$ the built-in R_F (150Ω) can be utilized by bridging the trace between pins 8 and 11. In this case no external R_F should be used.

National Semiconductor

LM10 Operational Amplifier and Voltage Reference

General Description

The LM10 series are monolithic linear ICs consisting of a precision reference, an adjustable reference buffer and an independent, high quality op amp.

The unit can operate from a total supply voltage as low as 1.1V or as high as 40V, drawing only 270μA. A complementary output stage swings within 15 mV of the supply terminals or will deliver ±20 mA output current with ±0.4V saturation. Reference output can be as low as 200 mV. Some other characteristics of the LM10 are

- input offset voltage 2.0 mV (max)
- input offset current 0.7 nA (max)
- input bias current 20 nA (max)
- reference regulation 0.1% (max)
- offset voltage drift 2μV/°C
- reference drift 0.002%/°C

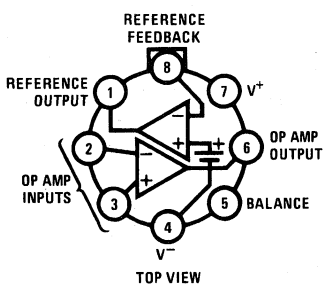
The circuit is recommended for portable equipment and is completely specified for operation from a single power cell. In contrast, high output-drive capability, both voltage and current, along with thermal overload protection, suggest it in demanding general-purpose applications.

The device is capable of operating in a floating mode, independent of fixed supplies. It can function as a remote comparator, signal conditioner, SCR controller or transmitter for analog signals, delivering the processed signal on the same line used to supply power. It is also suited for operation in a wide range of voltage- and current-regulator applications, from low voltages to several hundred volts, providing greater precision than existing ICs.

This series is available in the three standard temperature ranges, with the commercial part having relaxed limits. In addition, a low-voltage specification (suffix "L") is available in the limited temperature ranges at a cost savings.

Connection and Functional Diagrams

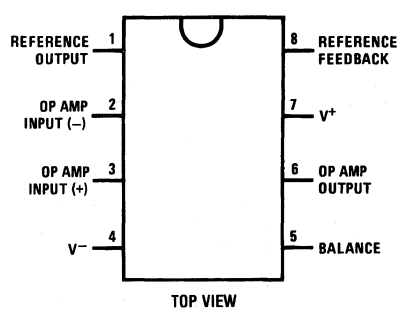
Metal Can Package (H)



TL/H/5652–1

Order Number LM10H, LM10BH, LM10CH, LM10BLH, LM10CLH or LM10H/883 available per SMA# 5962-8760401
See NS Package Number H08A

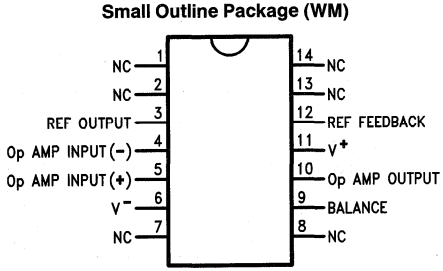
Dual-In-Line Package (N)



TL/H/5652–15

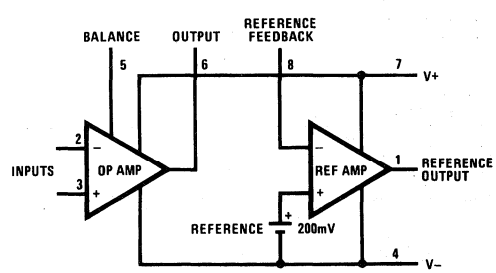
Order Number LM10CN or LM10CLN
See NS Package Number N08E

Small Outline Package (WM)



TL/H/5652–17

Order Number LM10CWM or LM10CLWM
See NS Package Number M14B



TL/H/5652–16

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications. (Note 7)

	LM10/LM10B/ LM10C	LM10BL/ LM10CL
Total Supply Voltage	45V	7V
Differential Input Voltage (note 1)	±40V	±7V
Power Dissipation (note 2)	internally limited	
Output Short-circuit Duration (note 3)	continuous	
Storage-Temp. Range	−55°C to +150°C	
Lead Temp. (Soldering, 10 seconds)		
Metal Can	300°C	
Lead Temp. (Soldering, 10 seconds) DIP	260°C	
Vapor Phase (60 seconds)	215°C	
Infrared (15 seconds)	220°C	

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

ESD rating is to be determined.

Maximum Junction Temperature

LM10	150°C
LM10B	100°C
LM10C	85°C

Operating Ratings

Package Thermal Resistance

θ_{JA}	
H Package	150°C/W
N Package	87°C/W
WM Package	90°C/W
θ_{JC}	
H Package	45°C/W

Electrical Characteristics

$T_J = 25°C$, $T_{MIN} \le T_J \le T_{MAX}$ (note 4) **(Boldface type refers to limits over temperature range)**

Parameter	Conditions	LM10/LM10B			LM10C			Units
		Min	Typ	Max	Min	Typ	Max	
Input offset voltage			0.3	2.0 **3.0**		0.5	4.0 **5.0**	mV mV
Input offset current (note 5)			0.25	0.7 **1.5**		0.4	2.0 **3.0**	nA nA
Input bias current			10	20 **30**		12	30 **40**	nA nA
Input resistance		250 **150**	500		150 **115**	400		kΩ kΩ
Large signal voltage gain	$V_S = \pm 20V$, $I_{OUT} = 0$ $V_{OUT} = \pm 19.95V$ $V_S = \pm 20V$, $V_{OUT} = \pm 19.4V$ $I_{OUT} = \pm 20$ mA **(± 15 mA)** $V_S = \pm 0.6V$ **(0.65V)**, $I_{OUT} = \pm 2$ mA $V_{OUT} = \pm 0.4V$ **(± 0.3V)**, $V_{CM} = -0.4V$	120 **80** 50 **20** 1.5 **0.5**	400 130 3.0 		80 **50** 25 **15** 1.0 **0.75**	400 130 3.0 		V/mV V/mV V/mV V/mV V/mV V/mV
Shunt gain (note 6)	1.2V **(1.3V)** ≤ V_{OUT} ≤ 40V, $R_L = 1.1$ kΩ 0.1 mA ≤ I_{OUT} ≤ 5 mA 1.5V ≤ V^+ ≤ 40V, $R_L = 250\Omega$ 0.1 mA ≤ I_{OUT} ≤ 20 mA	14 **6** 8 **4**	33 25 		10 **6** 6 **4**	33 25 		V/mV V/mV V/mV V/mV
Common-mode rejection	−20V ≤ V_{CM} ≤ 19.15V **(19V)** $V_S = \pm 20V$	93 **87**	102		90 **87**	102		dB dB
Supply-voltage rejection	−0.2V ≥ V^- ≥ −39V $V^+ = 1.0V$ **(1.1V)** 1.0V **(1.1V)** ≤ V^+ ≤ 39.8V $V^- = -0.2V$	90 **84** 96 **90**	96 106 		87 **84** 93 **90**	96 106 		dB dB dB dB
Offset voltage drift			2.0			5.0		μV/°C
Offset current drift			2.0			5.0		pA/°C
Bias current drift	$T_C < 100°C$		60			90		pA/°C
Line regulation	1.2V **(1.3V)** ≤ V_S ≤ 40V 0 ≤ I_{REF} ≤ 1.0 mA, $V_{REF} = 200$ mV		0.001	0.003 **0.006**		0.001	0.008 **0.01**	%/V %/V
Load regulation	0 ≤ I_{REF} ≤ 1.0 mA $V^+ - V_{REF} \ge 1.0V$ **(1.1V)**		0.01	0.1 **0.15**		0.01	0.15 **0.2**	% %

Electrical Characteristics

$T_J = 25°C$, $T_{MIN} \leq T_J \leq T_{MAX}$, (note 4) **(Boldface type refers to limits over temperature range)** (Continued)

Parameter	Conditions	LM10/LM10B			LM10C			Units
		Min	Typ	Max	Min	Typ	Max	
Amplifier gain	$0.2V \leq V_{REF} \leq 35V$	50 **23**	75		25 **15**	70		V/mV V/mV
Feedback sense voltage		195 **194**	200	205 **206**	190 **189**	200	210 **211**	mV mV
Feedback current			20	50 **65**		22	75 **90**	nA nA
Reference drift			0.002			0.003		%/°C
Supply current			270	400 **500**		300	500 **570**	μA μA
Supply current change	$1.2V$ **(1.3V)** $\leq V_S \leq 40V$		15	**75**		15	**75**	μA

Parameter	Conditions	LM10BL			LM10CL			Units
		Min	Typ	Max	Min	Typ	Max	
Input offset voltage			0.3	2.0 **3.0**		0.5	4.0 **5.0**	mV mV
Input offset current (note 5)			0.1	0.7 **1.5**		0.2	2.0 **3.0**	nA nA
Input bias current			10	20 **30**		12	30 **40**	nA nA
Input resistance		250 **150**	500		150 **115**	400		kΩ kΩ
Large signal voltage gain	$V_S = \pm 3.25V$, $I_{OUT} = 0$ $V_{OUT} = \pm 3.2V$ $V_S = \pm 3.25V$, $I_{OUT} = 10$ mA $V_{OUT} = \pm 2.75$ V $V_S = \pm 0.6V$ **(0.65V)**, $I_{OUT} = \pm 2$ mA $V_{OUT} = \pm 0.4V$ **(±0.3V)**, $V_{CM} = -0.4V$	60 **40** 10 **4** 1.5 **0.5**	300 25 3.0 		40 **25** 5 **3** 1.0 **0.75**	300 25 3.0 		V/mV V/mV V/mV V/mV V/mV V/mV
Shunt gain (note 6)	$1.5V \leq V^+ \leq 6.5V$, $R_L = 500\Omega$ $0.1\ mA \leq I_{OUT} \leq 10$ mA	8 **4**	30		6 **4**	30		V/mV V/mV
Common-mode rejection	$-3.25V \leq V_{CM} \leq 2.4V$ **(2.25V)** $V_S = \pm 3.25V$	89 **83**	102		80 **74**	102		dB dB
Supply-voltage rejection	$-0.2V \geq V^- \geq -5.4V$ $V^+ = 1.0V$ **(1.2V)** $1.0V$ **(1.1V)** $\leq V^+ \leq 6.3V$ $V^- = 0.2V$	86 **80** 94 **88**	96 106 		80 **74** 80 **74**	96 106 		dB dB dB dB
Offset voltage drift			2.0			5.0		μV/°C
Offset current drift			2.0			5.0		pA/°C
Bias current drift			60			90		pA/°C
Line regulation	$1.2V$ **(1.3V)** $\leq V_S \leq 6.5V$ $0 \leq I_{REF} \leq 0.5$ mA, $V_{REF} = 200$ mV		0.001	0.01 **0.02**		0.001	0.02 **0.03**	%/V %/V
Load regulation	$0 \leq I_{REF} \leq 0.5$ mA $V^+ - V_{REF} \geq 1.0V$ **(1.1V)**		0.01	0.1 **0.15**		0.01	0.15 **0.2**	% %
Amplifier gain	$0.2V \leq V_{REF} \leq 5.5V$	30 **20**	70		20 **15**	70		V/mV V/mV

Electrical Characteristics

$T_J = 25°C$, $\mathbf{T_{MIN} \leq T_J \leq T_{MAX}}$, (note 4) **(Boldface type refers to limits over temperature range)** (Continued)

Parameter	Conditions	LM10BL			LM10CL			Units
		Min	Typ	Max	Min	Typ	Max	
Feedback sense voltage		195 **194**	200	205 **206**	190 **189**	200	210 **211**	mV mV
Feedback current			20	50 **65**		22	75 **90**	nA nA
Reference drift			0.002			0.003		%/°C
Supply current			260	400 **500**		280	500 **570**	μA μA

Note 1: The Input voltage can exceed the supply voltages provided that the voltage from the input to any other terminal does not exceed the maximum differential input voltage and excess dissipation is accounted for when $V_{IN} < V^-$.

Note 2: The maximum, operating-junction temperature is 150°C for the LM10, 100°C for the LM10B(L) and 85°C for the LM10C(L). At elevated temperatures, devices must be derated based on package thermal resistance.

Note 3: Internal thermal limiting prevents excessive heating that could result in sudden failure, but the IC can be subjected to accelerated stress with a shorted output and worst-case conditions.

Note 4: These specifications apply for $V^- \leq V_{CM} \leq V^+ - 0.85V$ **(1.0V)**, 1.2V **(1.3V)** $< V_S \leq V_{MAX}$, $V_{REF} = 0.2V$ and $0 \leq I_{REF} \leq 1.0$ mA, unless otherwise specified: $V_{MAX} = 40V$ for the standard part and 6.5V for the low voltage part. Normal typeface indicates 25°C limits. **Boldface type indicates limits and altered test conditions for full-temperature-range operation;** this is −55°C to 125°C for the LM10, −25°C to 85°C for the LM10B(L) and 0°C to 70°C for the LM10C(L). The specifications do not include the effects of thermal gradients ($\tau_1 \cong 20$ ms), die heating ($\tau_2 \cong 0.2$s) or package heating. Gradient effects are small and tend to offset the electrical error (see curves).

Note 5: For $T_J > 90°C$, I_{OS} may exceed 1.5 nA for $V_{CM} = V^-$. With $T_J = 125°C$ and $V^- \leq V_{CM} \leq V^- + 0.1V$, $I_{OS} \leq 5$ nA.

Note 6: This defines operation in floating applications such as the bootstrapped regulator or two-wire transmitter. Output is connected to the V^+ terminal of the IC and input common mode is referred to V^- (see typical applications). Effect of larger output-voltage swings with higher load resistance can be accounted for by adding the positive-supply rejection error.

Note 7: Refer to RETS10X for LM10H military specifications.

Definition of Terms

Input offset voltage: That voltage which must be applied between the input terminals to bias the unloaded output in the linear region.

Input offset current: The difference in the currents at the input terminals when the unloaded output is in the linear region.

Input bias current: The absolute value of the average of the two input currents.

Input resistance: The ratio of the change in input voltage to the change in input current on either input with the other grounded.

Large signal voltage gain: The ratio of the specified output voltage swing to the change in differential input voltage required to produce it.

Shunt gain: The ratio of the specified output voltage swing to the change in differential input voltage required to produce it with the output tied to the V^+ terminal of the IC. The load and power source are connected between the V^+ and V^- terminals, and input common-mode is referred to the V^- terminal.

Common-mode rejection: The ratio of the input voltage range to the change in offset voltage between the extremes.

Supply-voltage rejection: The ratio of the specified supply-voltage change to the change in offset voltage between the extremes.

Line regulation: The average change in reference output voltage over the specified supply voltage range.

Load regulation: The change in reference output voltage from no load to that load specified.

Feedback sense voltage: The voltage, referred to V^-, on the reference feedback terminal while operating in regulation.

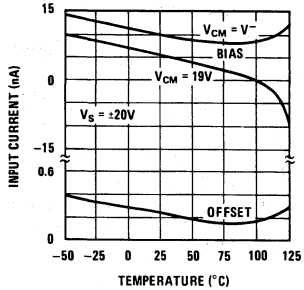
Reference amplifier gain: The ratio of the specified reference output change to the change in feedback sense voltage required to produce it.

Feedback current: The absolute value of the current at the feedback terminal when operating in regulation.

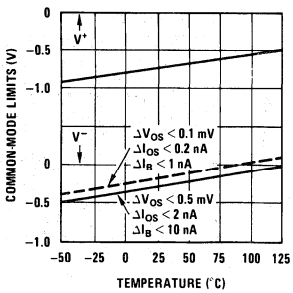
Supply current: The current required from the power source to operate the amplifier and reference with their outputs unloaded and operating in the linear range.

Typical Performance Characteristics (Op Amp)

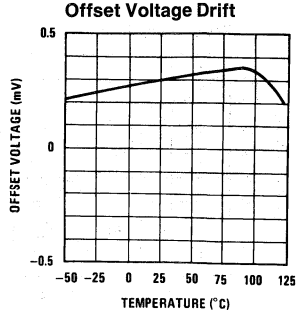
Input Current



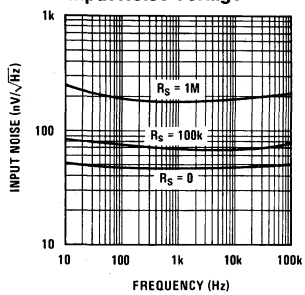
Common Mode Limits



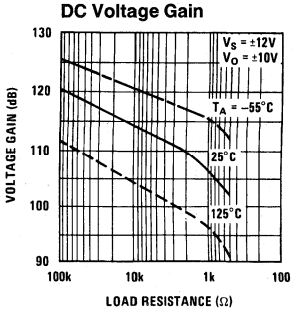
Offset Voltage Drift



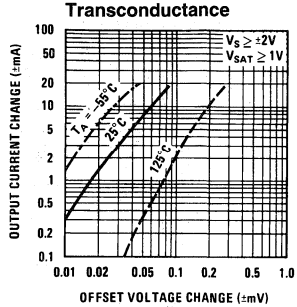
Input Noise Voltage



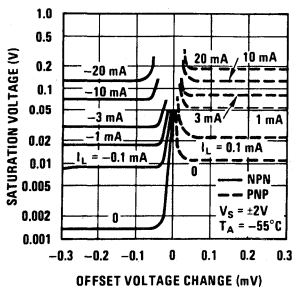
DC Voltage Gain



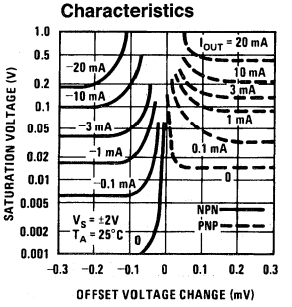
Transconductance



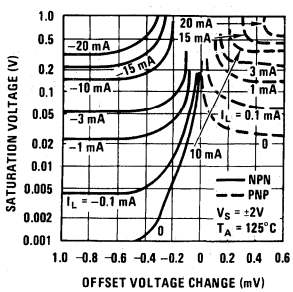
Output Saturation Characteristics



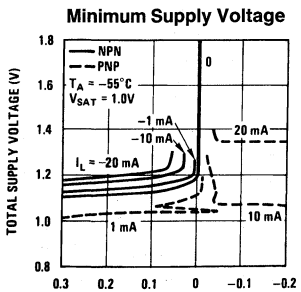
Output Saturation Characteristics



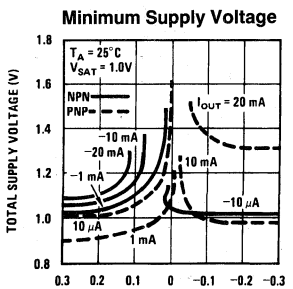
Output Saturation Characteristics



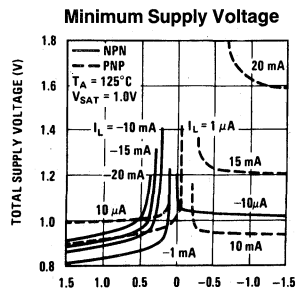
Minimum Supply Voltage



Minimum Supply Voltage



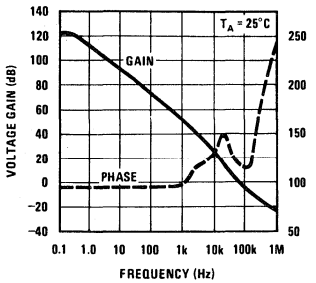
Minimum Supply Voltage



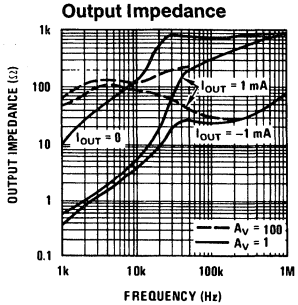
TL/H/5652–2

Typical Performance Characteristics (Op Amp) (Continued)

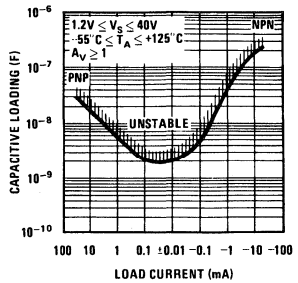
Frequency Response



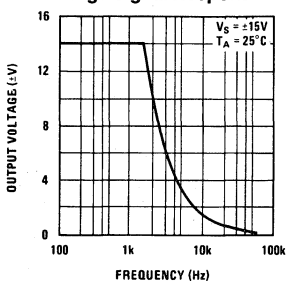
Output Impedance



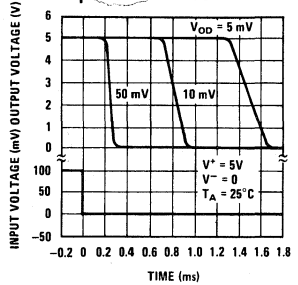
Typical Stability Range



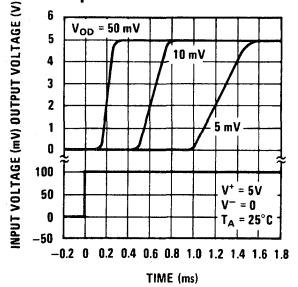
Large Signal Response



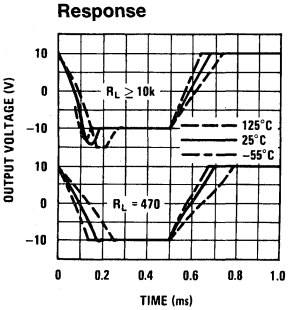
Comparator Response Time For Various Input Overdrives



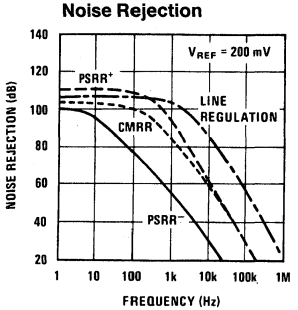
Comparator Response Time For Various Input Overdrives



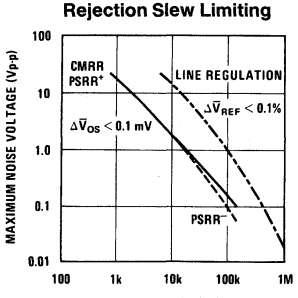
Follower Pulse Response



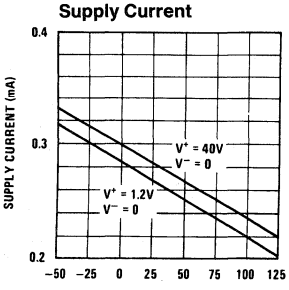
Noise Rejection



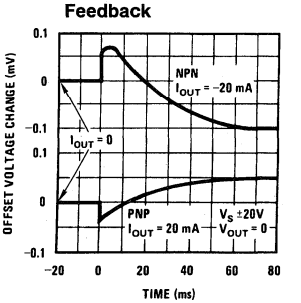
Rejection Slew Limiting



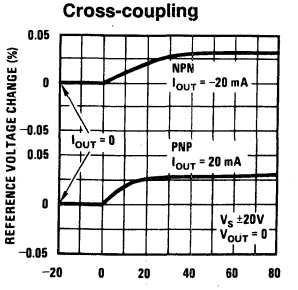
Supply Current



Thermal Gradient Feedback



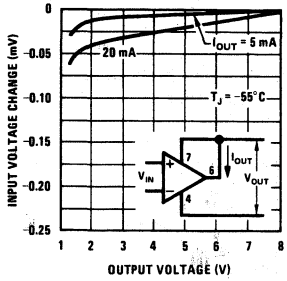
Thermal Gradient Cross-coupling



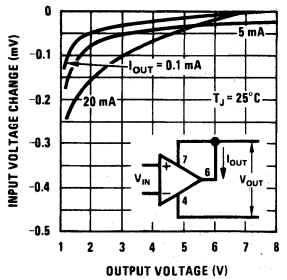
TL/H/5652–3

Typical Performance Characteristics (Op Amp) (Continued)

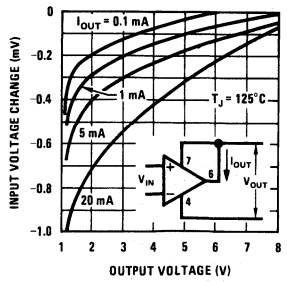
Shunt Gain



Shunt Gain



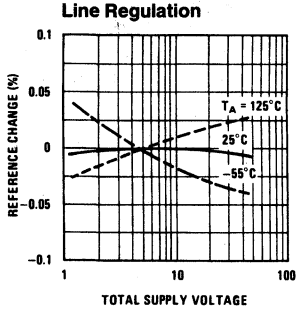
Shunt Gain



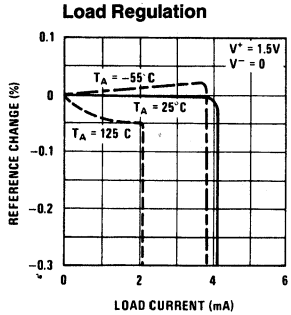
TL/H/5652–4

Typical Performance Characteristics (Reference)

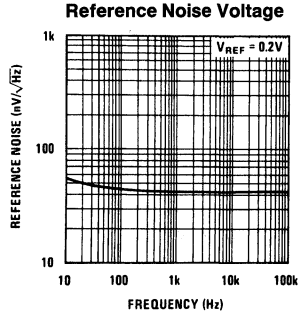
Line Regulation



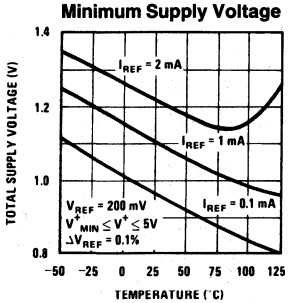
Load Regulation



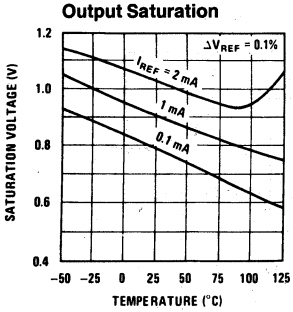
Reference Noise Voltage



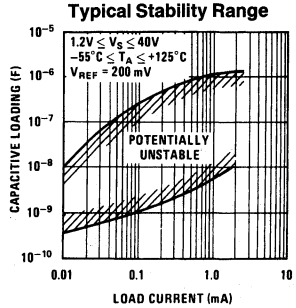
Minimum Supply Voltage



Output Saturation



Typical Stability Range

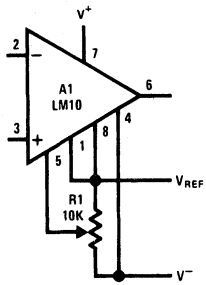


TL/H/5652–5

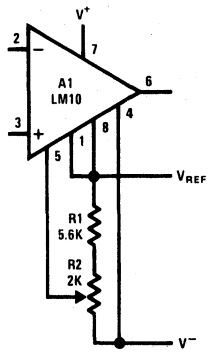
Typical Applications†† (Pin numbers are for devices in 8-pin packages)

Op Amp Offset Adjustment

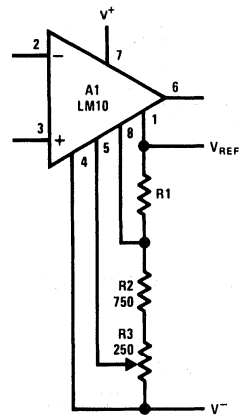
Standard



Limited Range

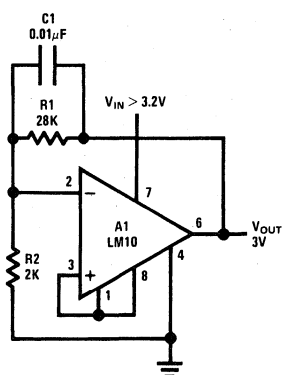


Limited Range With Boosted Reference

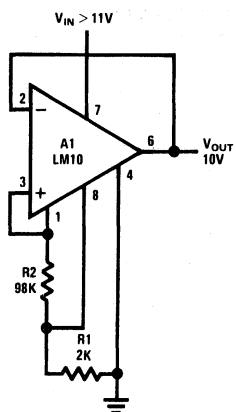


Positive Regulators†

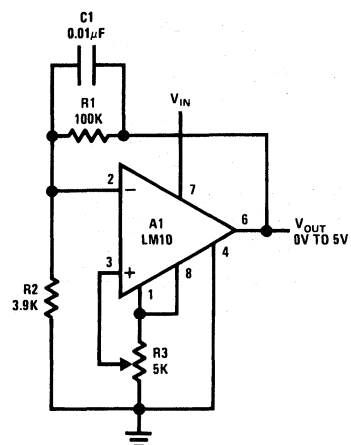
Low Voltage



Best Regulation



Zero Output



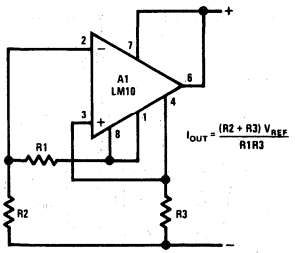
TL/H/5652–6

†Use only electrolytic output capacitors.

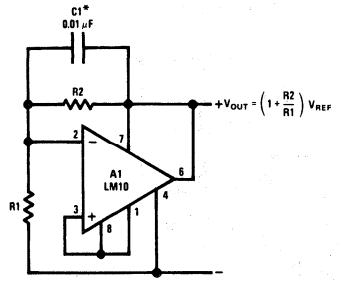
††Circuit descriptions available in application note AN-211.

Typical Applications†† (Pin numbers are for devices in 8-pin packages) (Continued)

Current Regulator

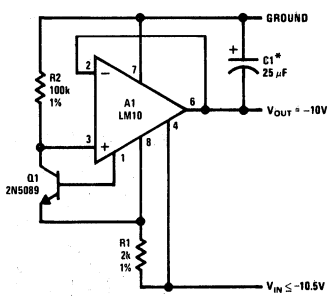


Shunt Regulator



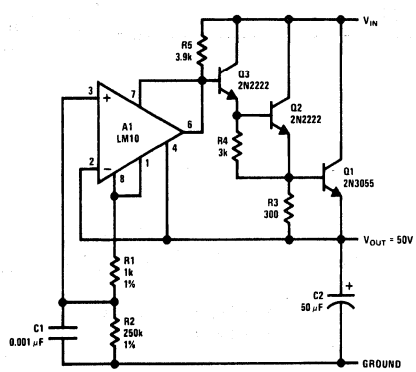
*Required For Capacitive Loading

Negative Regulator

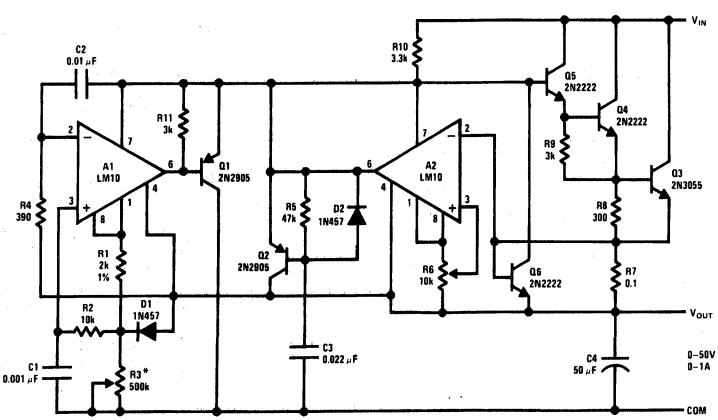


*Electrolytic

Precision Regulator



Laboratory Power Supply



TL/H/5652–7

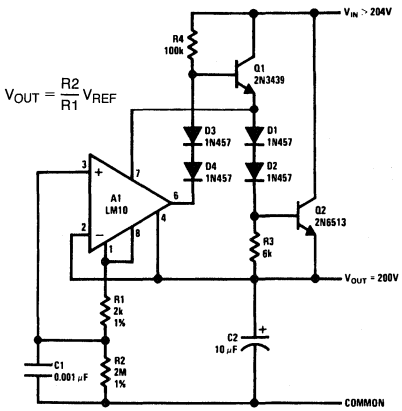
*$V_{OUT} = 10^{-4}$ R3

††Circuit descriptions available in application note AN-211.

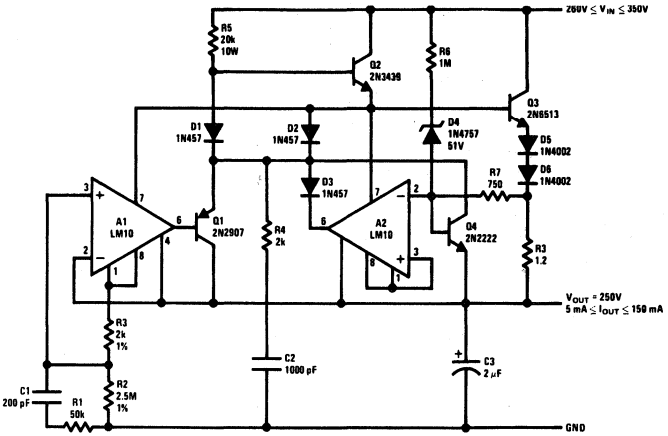
Typical Applications†† (Pin numbers are for devices in 8-pin packages) (Continued)

HV Regulator

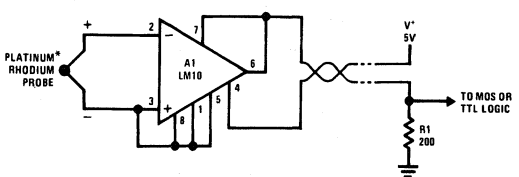
$V_{OUT} = \frac{R2}{R1} V_{REF}$



Protected HV Regulator

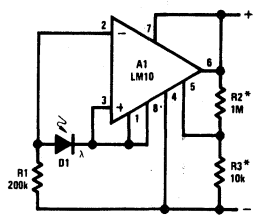


Flame Detector



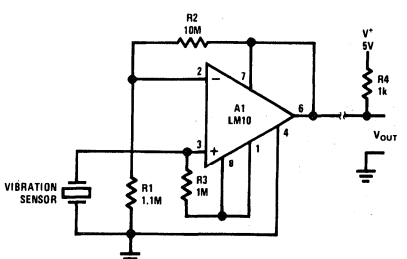
*800°C Threshold Is Established By Connecting Balance To V_{REF}.

Light Level Sensor

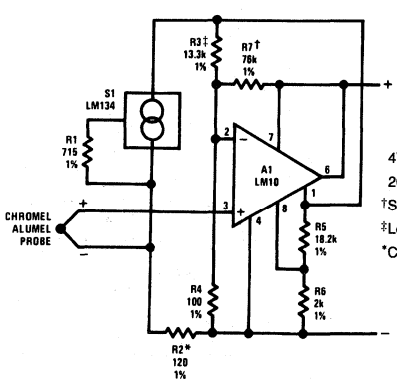


*Provides Hysteresis

Remote Amplifier



Remote Thermocouple Amplifier



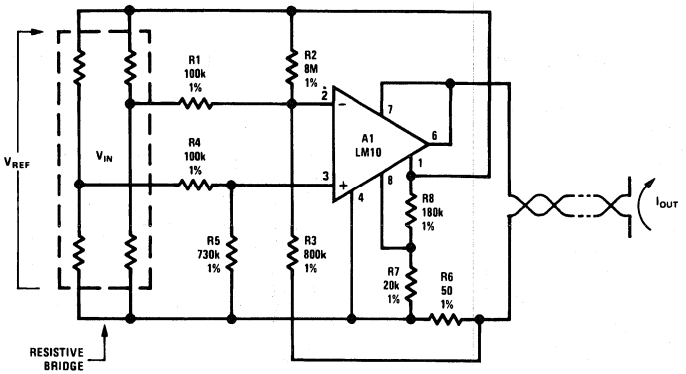
$4V \leq V_{OUT} \leq 20V$
$200°C \leq T_P \leq 700°C$
†Span Trim
‡Level-shift Trim
*Cold-junction Trim

TL/H/5652–8

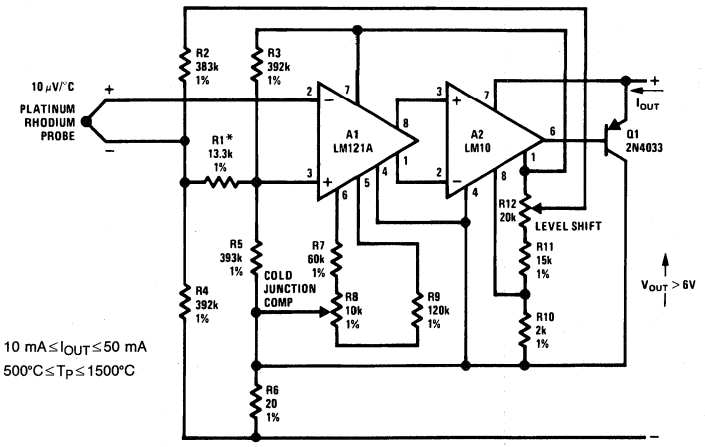
††Circuit descriptions available in application note AN-211.

Typical Applications †† (Pin numbers are for devices in 8-pin packages) (Continued)

Transmitter for Bridge Sensor

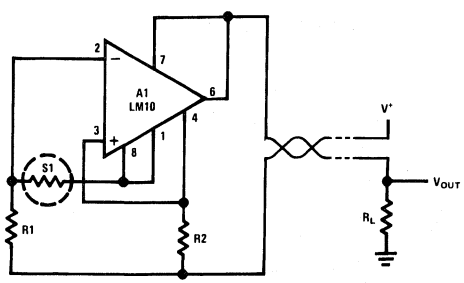


Precision Thermocouple Transmitter

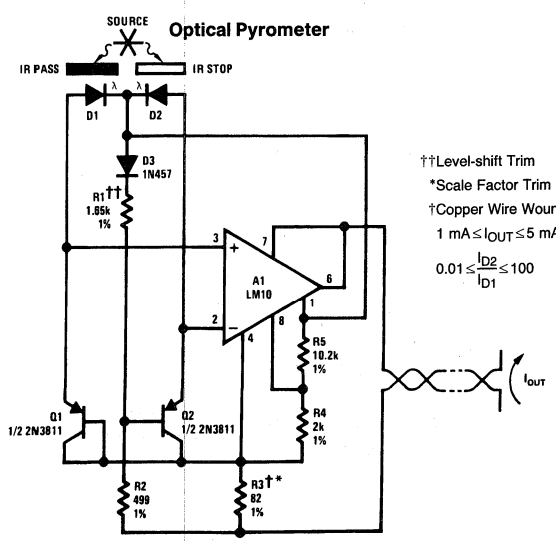


*Gain Trim

Resistance Thermometer Transmitter



Optical Pyrometer



††Level-shift Trim
*Scale Factor Trim
†Copper Wire Wound
1 mA ≤ I_{OUT} ≤ 5 mA
$0.01 \leq \frac{I_{D2}}{I_{D1}} \leq 100$

††Circuit descriptions available in application note AN-211.

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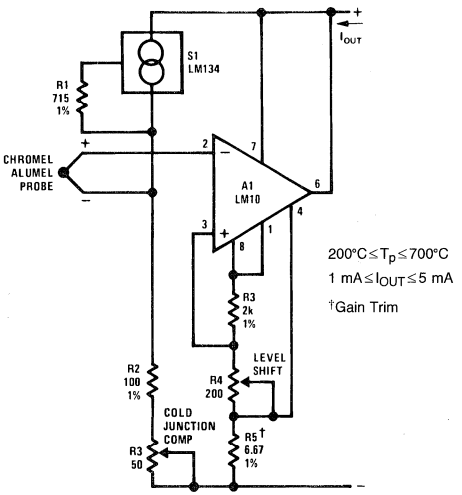
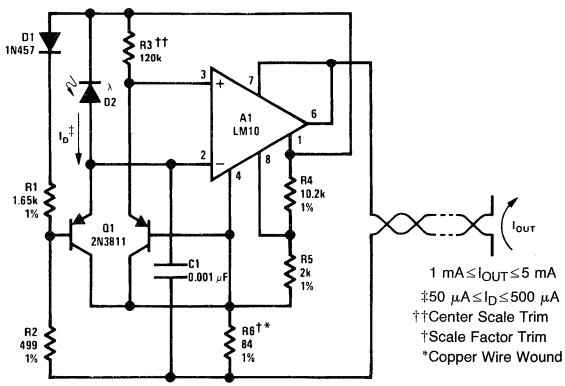
Typical Applications †† (Pin numbers are for devices in 8-pin packages) (Continued)

Thermocouple Transmitter



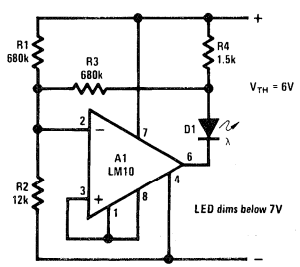
200°C ≤ T_P ≤ 700°C
1 mA ≤ I_{OUT} ≤ 5 mA
†Gain Trim

Logarithmic Light Sensor

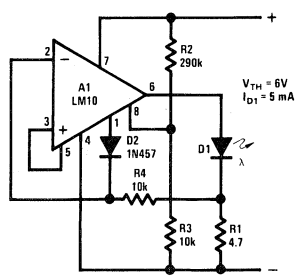


1 mA ≤ I_{OUT} ≤ 5 mA
‡50 μA ≤ I_D ≤ 500 μA
††Center Scale Trim
†Scale Factor Trim
*Copper Wire Wound

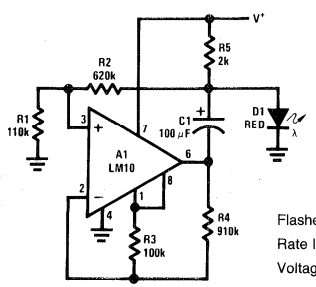
Battery-level Indicator



Battery-threshold Indicator

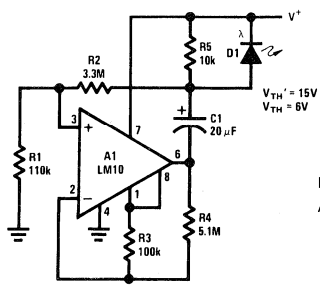


Single-cell Voltage Monitor



Flashes Above 1.2V
Rate Increases With
Voltage

Double-ended Voltage Monitor



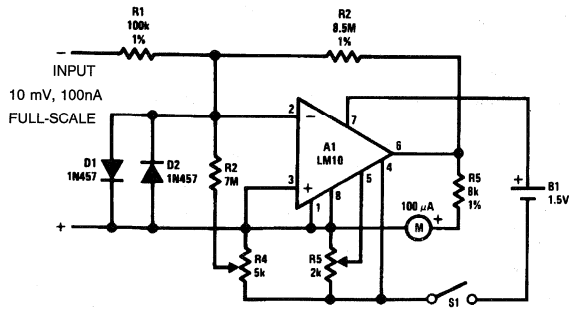
Flash Rate Increases
Above 6V and Below 15V

TL/H/5652–10

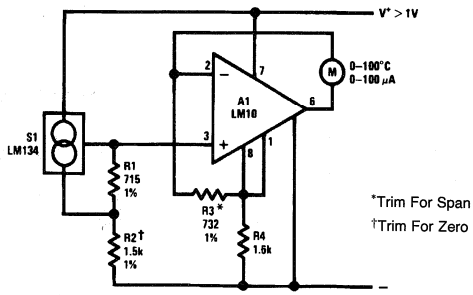
††Circuit descriptions available in application note AN-211.

Typical Applications †† (Pin numbers are for devices in 8-pin packages) (Continued)

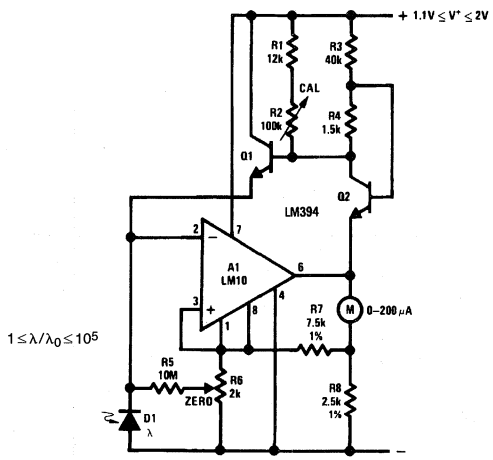
Meter Amplifier



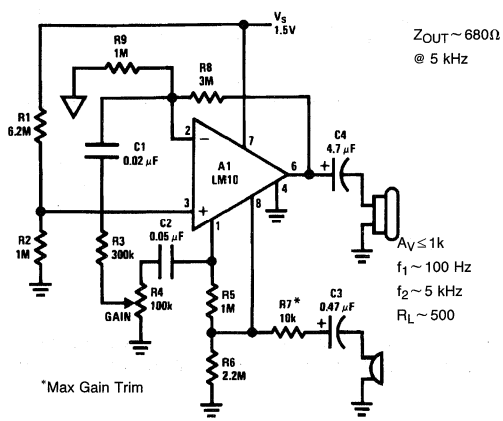
Thermometer



Light Meter



Microphone Amplifier

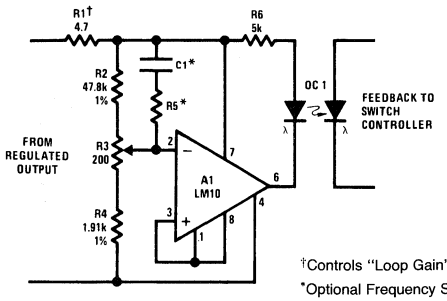


TL/H/5652–11

††Circuit descriptions available in application note AN-211.

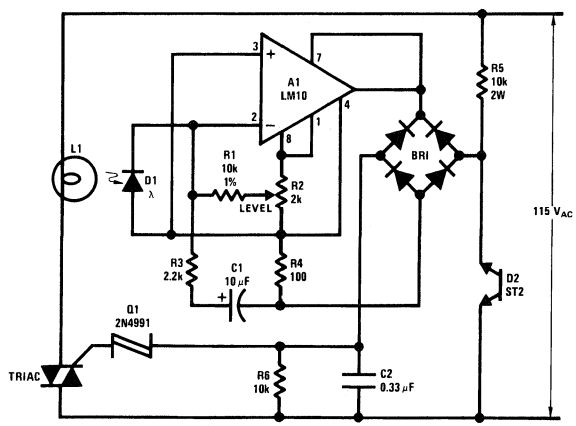
Typical Applications †† (Pin numbers are for devices in 8-pin packages) (Continued)

Isolated Voltage Sensor



†Controls "Loop Gain"
*Optional Frequency Shaping

Light-level Controller



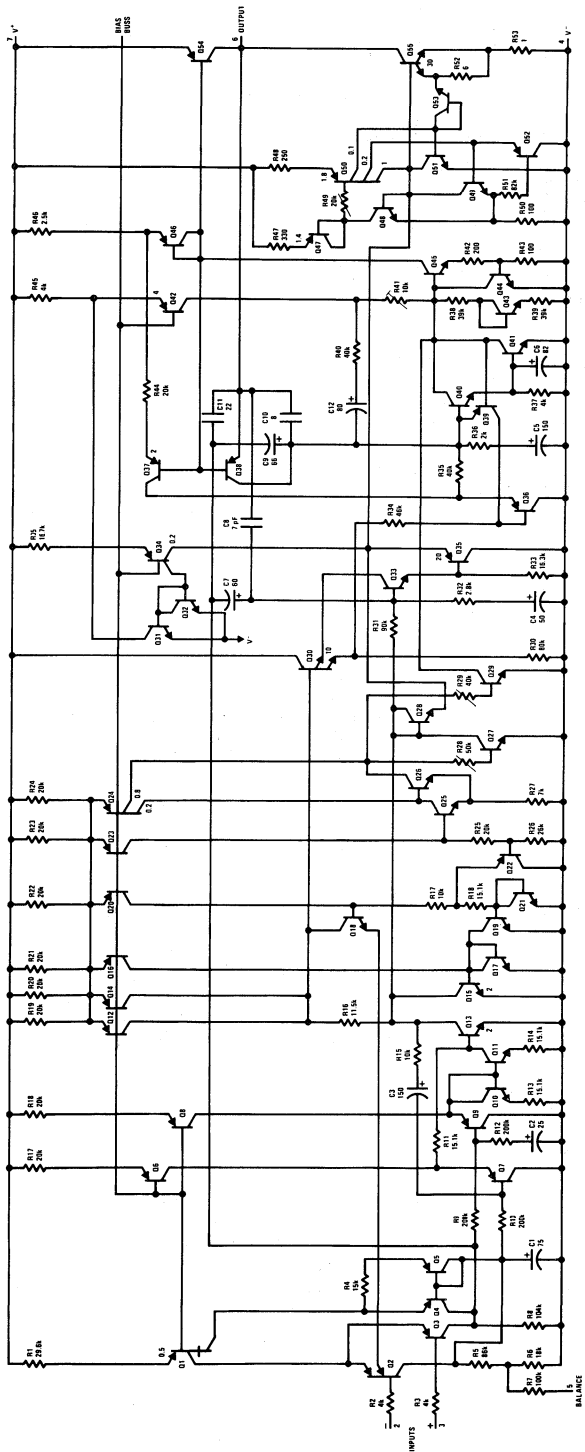
TL/H/5652–12

††Circuit descriptions available in application note AN-211.

Application Hints

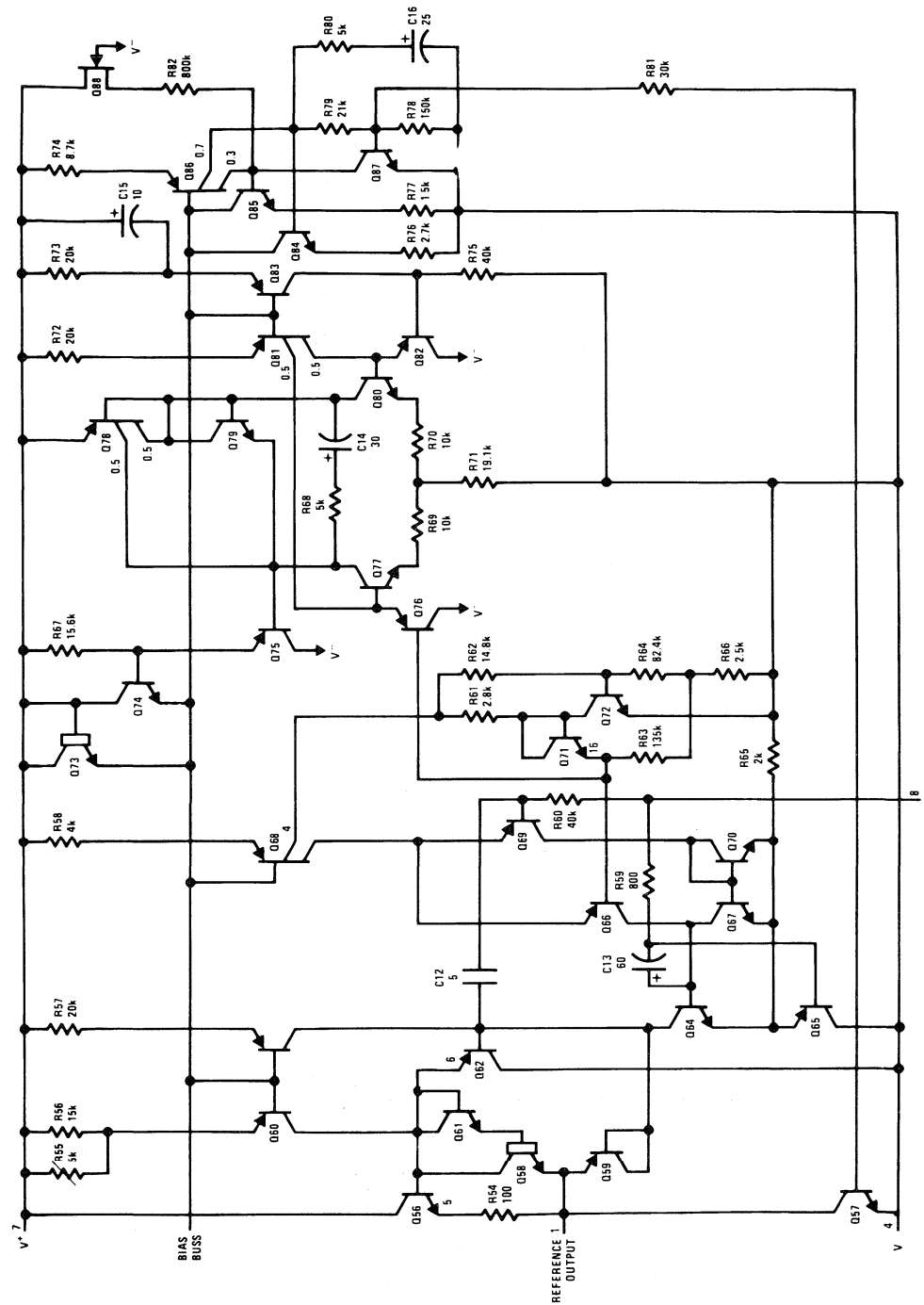
With heavy amplifier loading to V^-, resistance drops in the V^- lead can adversely affect reference regulation. Lead resistance can approach 1Ω. Therefore, the common to the reference circuitry should be connected as close as possible to the package.

Operational Amplifier Schematic (Pin numbers are for 8-pin packages)



TL/H/5662–13

Reference and Internal Regulator (Pin numbers are for 8-pin packages)



National Semiconductor

LM11 Operational Amplifiers

General Description

The LM11 is a precision dc amplifier combining the best features of existing bipolar and FET op amps. It is similar to the LM108A, except that input currents have been reduced by more than a factor of ten. Offset voltage and drift have also been approved.

Compared to FETs, the device provides inherently lower offset voltage and offset voltage drift, along with at least an order of magnitude better long-term stability. Low frequency noise is also somewhat reduced. Bias current is significantly lower even under laboratory conditions, and its low drift makes compensation practical. Offset current is almost unmeasureable. Although not as fast as FETs, it does have a much lower power drain. This low dissipation has the added advantage of eliminating warm up time in critical applications.

Typical characteristics for 25°C (−**55°C** to **125°C**) are:

- offset voltage: 100 μV (**200 μV**)
- bias current: 25 pA (**65 pA**)
- offset current: 0.5 pA (**3 pA**)
- temperature drift: **1 μV/°C**
- long-term stability: 10 μV/year

The LM11 is internally compensated, but external compensation can be added for improved frequency stability, particularly with capacitive loads. Offset voltage balancing is also provided, with the balance range determined by a low-resistance potentiometer.

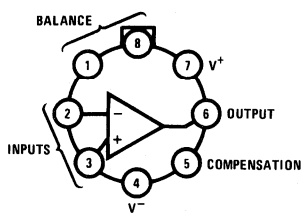
Otherwise, the device is the electrical equivalent of the LM108, except that the negative common-mode limit is 0.6V less, performance is specified down to ±2.5V and the guaranteed output drive has been increased to ±2 mA. The input noise is somewhat higher, but amplifier noise is obscured by resistor noise with higher source resistances.

This monolithic IC has obviously applications as electrometer amplifiers, charge integrators, analog memories, low frequency active filters or for frequency shaping in slow servo loops. It can be substituted for existing circuits to provide improved performance or eliminate trimming operations. The greater precision can also be used to extend the dynamic range of logarithmic amplifiers, light meters and solid-state particle detectors.

The LM11 is manufactured with standard bipolar processing using super-gain transistors.

Connection Diagrams

Metal Can*



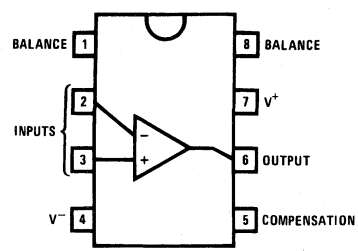
TL/H/5653–1

Top View

Order Number LM11H, LM11CH or LM11CLH
See NS Package H08C

*Case connected to V−

Mini-DIP



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Top View

Order Number LM11CN or LM11CLN
See NS Package N08E

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications. (Note 5)

Total Supply Voltage	40V
Input Current (Note 1)	±10 mA
Power Dissipation (Note 2)	500 mW
Output Short-Circuit Duration (Note 3)	Indefinite
Storage Temperature Range	−65°C to +150°C
Lead Temp. (Soldering, 10 seconds)	
(DIP)	260°C
(Metal Can)	300°C
ESD Tolerance (R_{ZAP} = 1.5k, C_{ZAP} = 100 pF)	1500V

Electrical Characteristics $T_J = 25°C$, $T_{MIN} \le T_J \le T_{MAX}$ (Note 4)

(Boldface type refers to limits over temperature range.)

Parameter	Conditions	LM11		LM11C		LM11CL		Units
		Typ	Lim	Typ	Lim	Typ	Lim	
Input Offset Voltage	(Note 4)	0.1	0.3 **0.6**	0.2	0.6 **0.8**	0.5	5 **6**	mV mV
Input Offset Current	(Note 4)	0.5	10 **30**	1	10 **20**	4	25 **50**	pA pA
Input Bias Current	(Note 4)	25	50 **150**	40	100 **150**	70	200 **300**	pA pA
Input Resistance	(Note 4)	10^{11}		10^{11}		10^{11}		Ω
Offset Voltage Drift	(Note 4)	1	**3**	2	**5**	3		μV/°C
Offset Current Drift	(Note 4)	20		10		50		fA/°C
Bias Current Drift	(Note 4)	0.5	**1.5**	0.8	**3**	1.4		pA/°C
Large Signal Voltage Gain	V_S ±15V, I_{OUT} = ±2 mA V_{OUT} = ±12V(±**11.5V**) V_S = ±15V, I_{OUT} = ±0.5 mA V_{OUT} ±12V	300 1200	100 **50** 250 **100**	300 1200	100 **50** 250 **100**	300 800	25 **15** 50 **30**	V/mV V/mV V/mV V/mV
Common-Mode Rejection	−13V (−**12.5V**)≤V_{CM}≤14V V_S = ±15V	130	110 **100**	130	110 **100**	110	96 **90**	dB dB
Power Supply Rejection Ratio	±2.5V≤V_S≤±20V	118	100 **96**	118	100 **96**	100	84 **80**	dB dB
Supply Current	(Note 4)	0.3	0.6 **0.8**	0.3	0.8 **1**	0.3	0.8 **1**	mA mA
Output Short-Circuit Current	T_J = 150°C		±15					mA

Note 1: The inputs are shunted with back-to-back diodes for overvoltage protection. Therefore, excessive current will flow if a differential input voltage in excess of 1V is applied between the inputs unless some limiting resistance is used. In addition, a 2 kΩ minimum resistance in each input is advised to avoid possible latch up initiated by supply reversals.

Note 2: The maximum operating-junction temperature is 150°C for the LM11 and 85°C for the LM11C(L). Devices must be derated at 150°C/W for the metal can and 155°C/W for the plastic DIP. The metal can has a thermal resistance of 45°C/W for the junction to case if a heat sink is used.

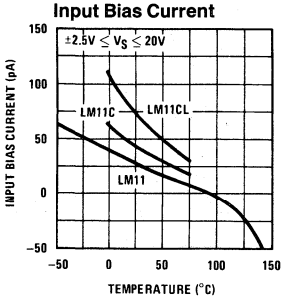
Note 3: Current limiting protects the output when it is shorted to ground or any voltage less than the supplies. With continuous overloads, package dissipation must be taken into account and heat sinking provided when necessary.

Note 4: These specifications apply for V^- + 2V (**2.5V**) ≤ V_{CM} ≤ V^+ − 1V and ±2.5V ≤ V_S ≤ ±20V, unless otherwise specified. Normal typeface indicates 25°C limits. **Boldface type indicates limits for full-temperature range operation.** This is −55°C ≤ T_J ≤ 125°C for the LM11 and 0°C ≤ T_J ≤ 70°C for the LM11C(L).

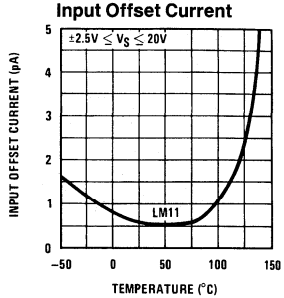
Note 5: Refer to RETS11X for LM11 military specifications.

Typical Characteristics

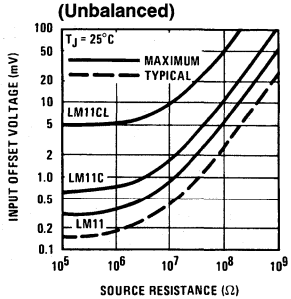
Input Bias Current



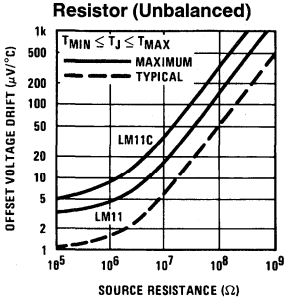
Input Offset Current



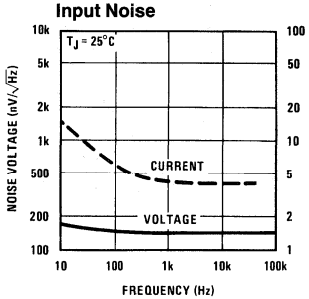
Offset: Single Source Resistor (Unbalanced)



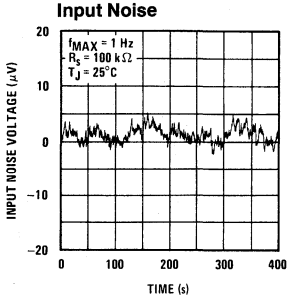
Drift: Single Source Resistor (Unbalanced)



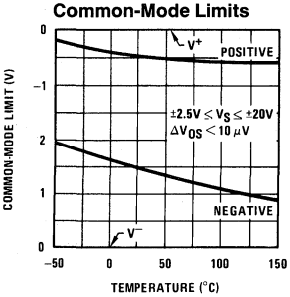
Input Noise



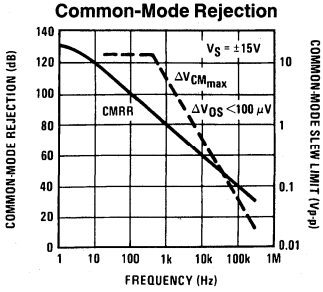
Input Noise



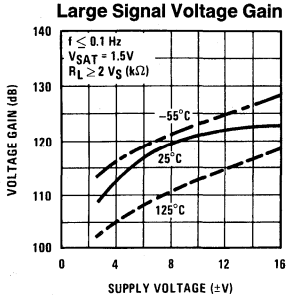
Common-Mode Limits



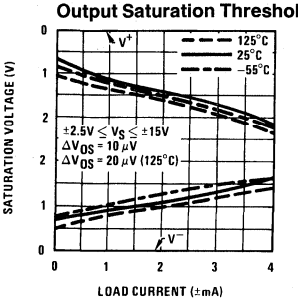
Common-Mode Rejection



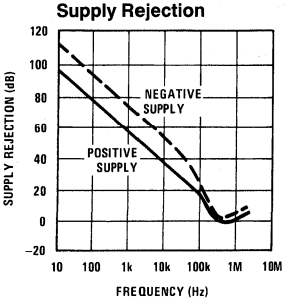
Large Signal Voltage Gain



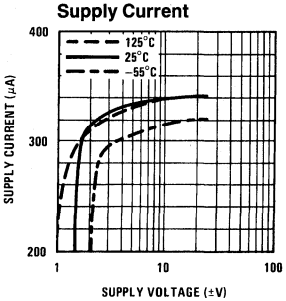
Output Saturation Threshold



Supply Rejection



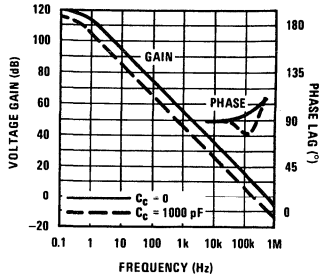
Supply Current



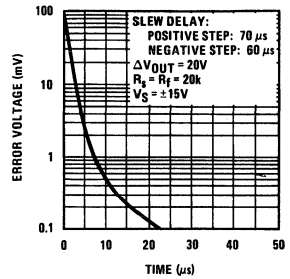
TL/H/5653–2

Typical Characteristics (Continued)

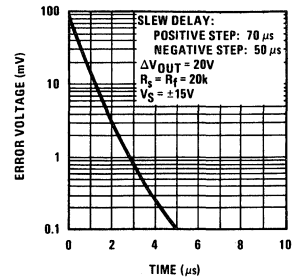
Open Loop Response



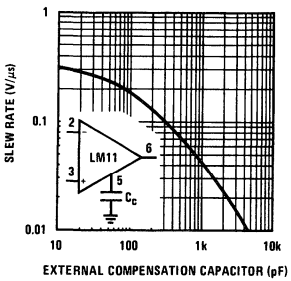
Follower Final Settling Time



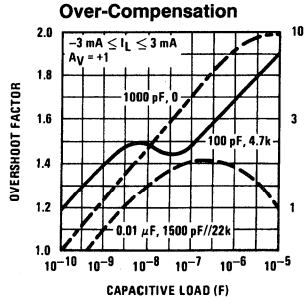
Inverter Final Settling Time



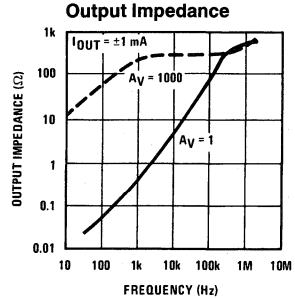
Slew Rate



Stability With Over-Compensation



Closed Loop Output Impedance



TL/H/5653–3

Application Hints

When working with circuitry capable of resolving picoampere level signals, leakage currents in circuitry external to the op amp can significantly degrade performance. High quality insulation is a must (Kel-F and Teflon rate high). Proper cleaning of all insulating surfaces to remove fluxes and other residues is also required. This includes the IC package as well as sockets and printed circuit boards. When operating in high humidity environments or near 0°C, some form of surface coating may be necessary to provide a moisture barrier.

The effects of board leakage can be minimized by encircling the input circuitry with a conductive guard ring operated at a potential close to that of the inputs. For critical applications, dual-in-line packages are available that include input guard pins.

Electrostatic shielding of high impedance circuitry is advisable.

Error voltages can also be generated in the external circuitry. Thermocouples formed between dissimilar metals can cause hundreds of microvolts of error in the presence of temperature gradients. The most troublesome thermocouples are the junction of the IC package and the printed circuit board (35 µV/°C for copper-kovar) and internal resistor connections. Problems can be avoided by keeping low level circuitry away from heat generating elements. Mounting the IC directly to the PC board while keeping package leads short and the input leads close together can also help.

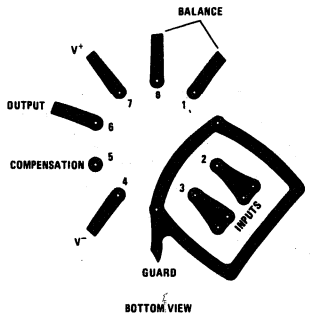
With the LM11 there is a temptation to remove the bias-current-compensation resistor normally used on the noninverting input of a summing amplifier. Direct connection of the inputs to ground or a low-impedance voltage source is not recommended with supply voltages greater than about 3V. The potential problem involves reversal of one supply which can cause excessive current in the second supply. Destruction of the IC could result if the output current of the second supply is not limited to about 100 mA or if there is much more than 1 µF bypass on the supply buss.

Just disconnecting one supply will generally involve reversal because of loading to the other supply both within the IC and in external circuitry. Although difficulties can be largely avoided by installing clamp diodes across the supply lines on every PC board, a conservative design would include enough resistance in the input lead to limit current to 10 mA if the input lead is pulled to either supply by internal currents. This precaution is by no means limited to the LM11.

Application Hints (Continued)

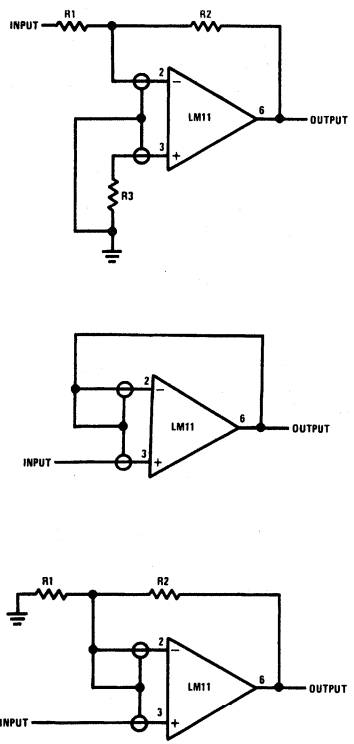
Input Guarding

Input guarding can drastically reduce surface leakage. Layout for metal can is shown here. Guarding both sides of board is required. Bulk leakage reduction is less and depends on guard ring width.



TL/H/5653–4

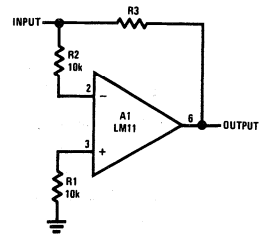
Guard ring is connected to low impedance point at same potential as sensitive input leads. Connections for various op amp configurations are here.



TL/H/5653–7

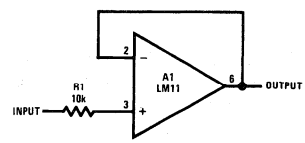
Input Protection

Current is limited by R2 even when input is connected to voltage source outside common mode range. If one supply reverses, current is controlled by R1. These resistors do not affect normal operation.



TL/H/5653–5

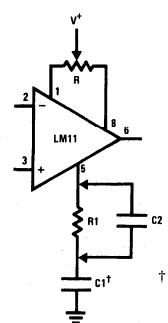
Input resistor controls current when input exceeds supply voltages, when power for op amp is turned off or when output is shorted.



TL/H/5653–6

Balancing And Over-Compensation

Over-compensation will improve stability with capacitive loading (see curves). Offset voltage adjustment range is determined by balance potentiometer resistance as indicated in the table.



† See stability with over-compensation curve

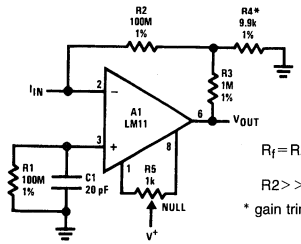
TL/H/5653–8

min. adj range	R
±4 mV	100 kΩ
±2	10k
±0.8	3k
±0.4	1k

Application Hints (Continued)

Resistance Multiplication

Equivalent feedback resistance is 10 GΩ, but only standard resistors are used. Even though the offset voltage is multiplied by 100, output offset is actually reduced because error is dependent on offset current rather than bias current. Voltage on summing junction is less than 5 mV.



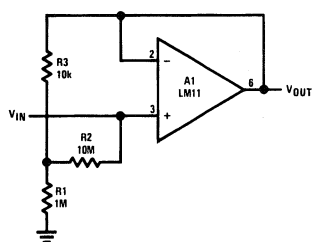
$$R_f = R2\left(1+\frac{R3}{R4}\right)$$

$R2 >> R3 \| R4$

* gain trim

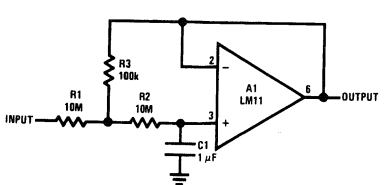
TL/H/5653–9

Follower input resistance is 1 GΩ. With the input open, offset voltage is multiplied by 100, but the added error is not great because the op amp offset is low.



TL/H/5653–11

This circuit multiplies RC time constant to 1000 seconds and provides low output impedance.

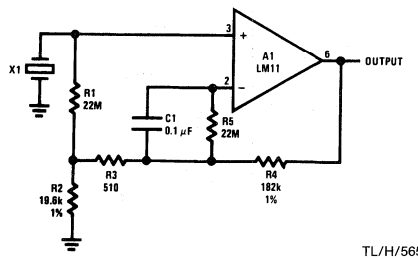


TL/H/5653–13

$$\tau = \frac{R1C}{R3}(R2+R3)$$

$$\Delta V_{OUT} = \frac{R1+R3}{R3}(I_B R2 + V_{OS})$$

A high-input-impedance ac amplifier for a piezoelectric transducer. Input resistance of 880 MΩ and gain of 10 is obtained.

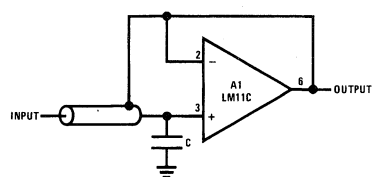


TL/H/5653–10

$$R_{IN} = R1\left(1+\frac{R2}{R3}\right) \quad A_V = \frac{R2+R3+R4}{R2+R3}$$

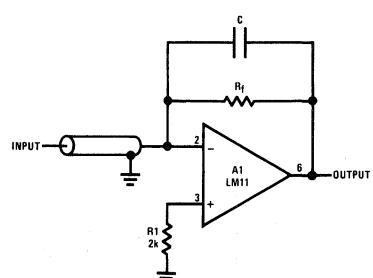
Cable Bootstrapping

Bootstrapping input shield for a follower reduces cable capacitance, leakage and spurious voltages from cable flexing. Instability can be avoided with small capacitor on input.



TL/H/5653–12

With summing amplifier, summing node is at virtual ground so input shield is best grounded. Small feedback capacitor insures stability.



TL/H/5653–14

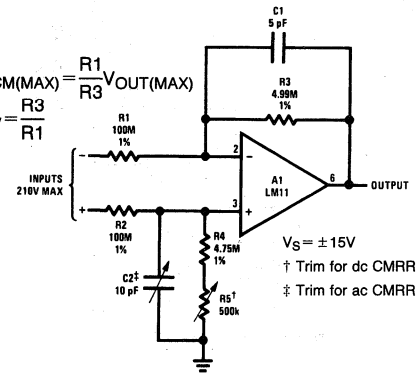
Application Hints (Continued)

Differential Amplifiers

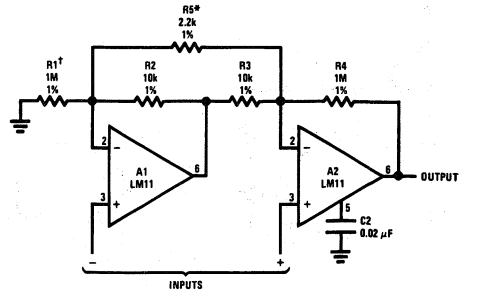
This differential amplifier handles high input voltages. Resistor mismatches and stray capacitors should be balanced out for best common-mode rejection.

$$V_{CM(MAX)} = \frac{R1}{R3} V_{OUT(MAX)}$$

$$A_V = \frac{R3}{R1}$$

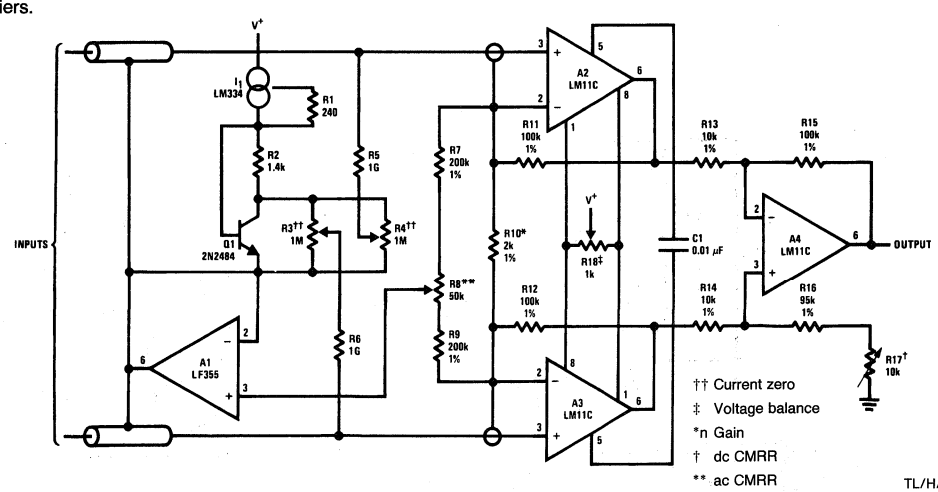


Two op-amp instrumentation amplifier has poor ac common mode rejection. This can be improved at the expense of differential bandwidth with C2.



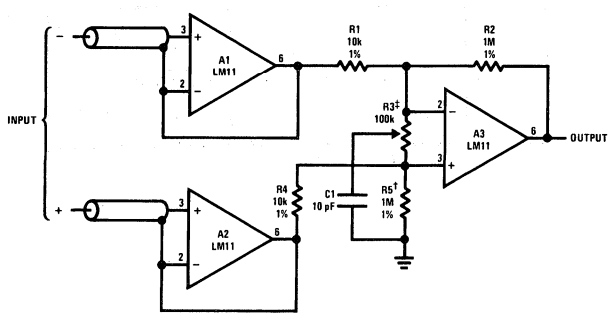
TL/H/5653–15

High gain differential instrumentation amplifier includes input guarding, cable bootstrapping and bias current compensation. Differential bandwidth is reduced by C1 which also makes common-mode rejection less dependent on matching of input amplifiers.



TL/H/5653–16

For moderate-gain instrumentation amplifiers, input amplifiers can be connected as followers. This simplifies circuitry, but A3 must also have low drift.



R1 = R3; R2 = R4

$$A_V = \frac{R2}{R1}$$

†Trim for dc CMRR

‡Set for ac CMRR

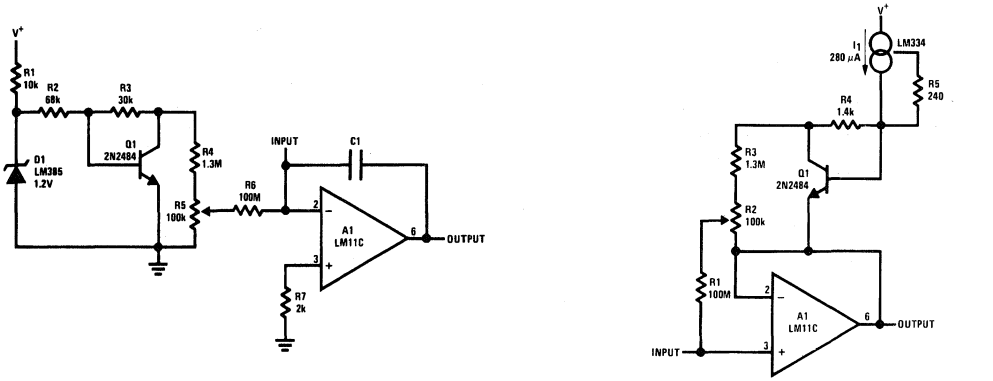
TL/H/5653–17

Application Hints (Continued)

Bias Current Compensation

Precise bias current compensation for use with unregulated supplies. Reference voltage is available for other circuitry.

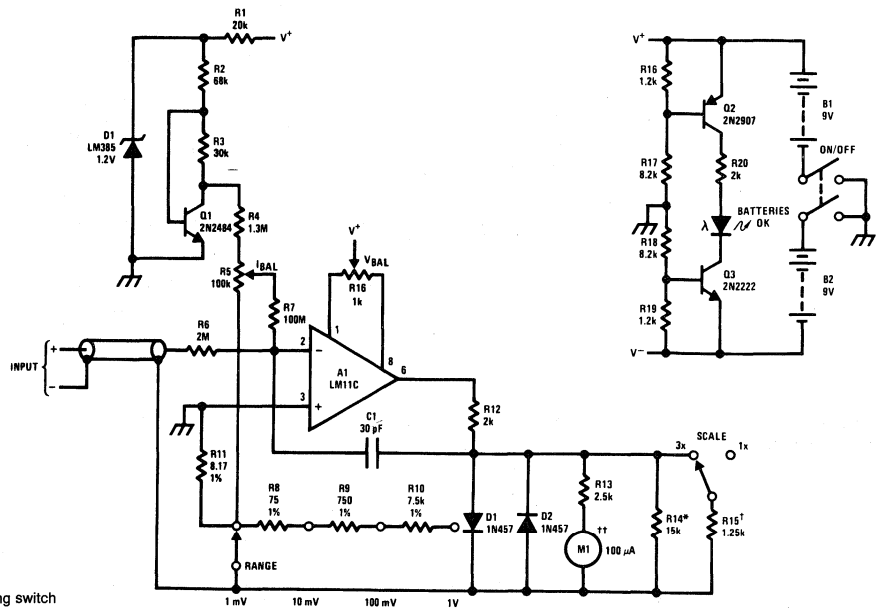
This circuit shows how bias current compensation can be used on a voltage follower.



TL/H/5653–18

Voltmeter

High input impedance millivoltmeter. Input current is proportional to input voltage, about 10 pA at full scale. Reference could be used to make direct reading linear ohmmeter.



* 1×scale calibrate

† 3×scale calibrate

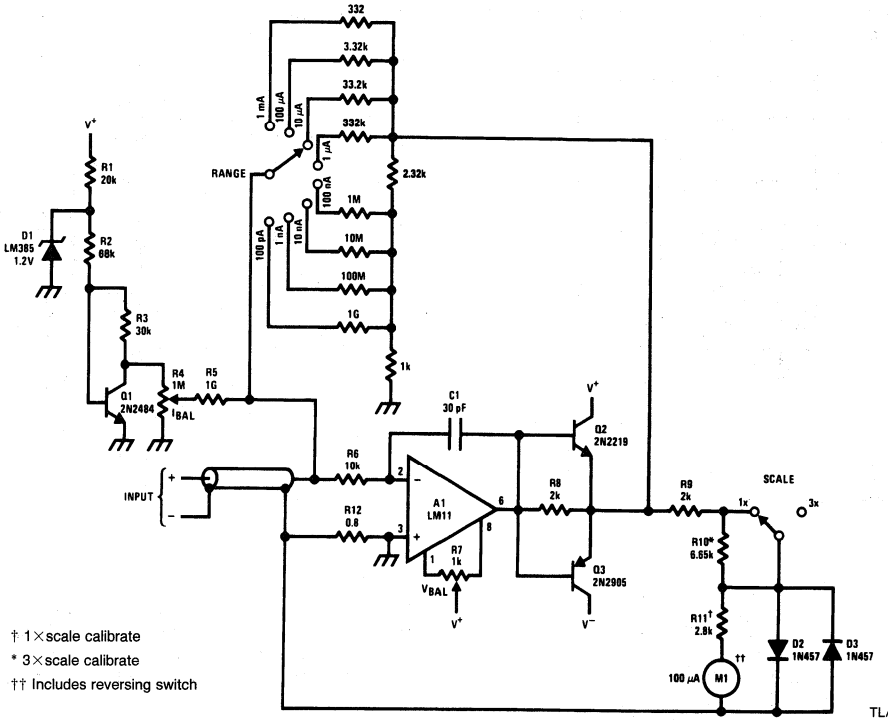
†† Includes reversing switch

TL/H/5653–19

Application Hints (Continued)

Ammeter

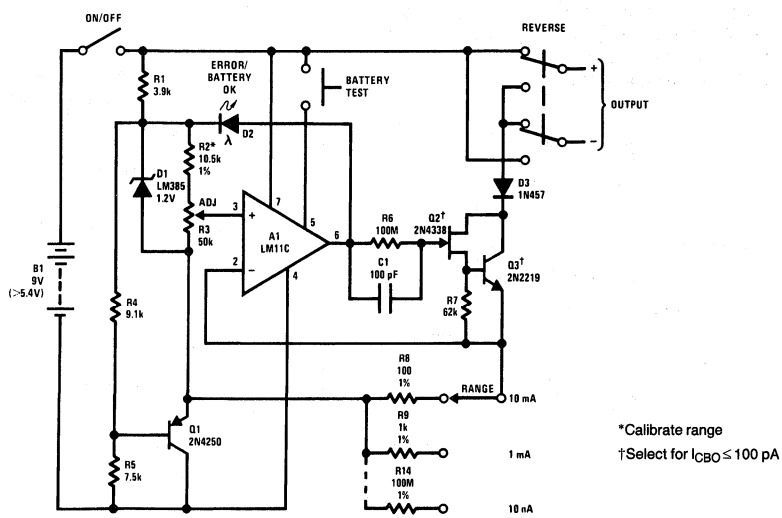
Current meter ranges from 100 pA to 3 mA full scale. Voltage across input is 100 μV at lower ranges rising to 3 mV at 3 mA. Buffers on op amp are to remove ambiguity with high-current overload. Output can also drive DVM or DPM.



TL/H/5653–20

Current Source

Precision current source has 10 μA to 10 mA ranges with output compliance of 30V to −5V. Output current is fully adjustable on each range with a calibrated, ten-turn potentiometer. Error light indicates saturation.

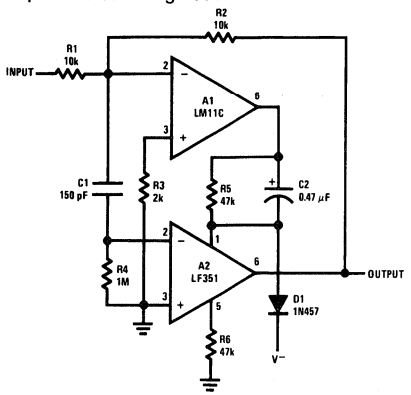


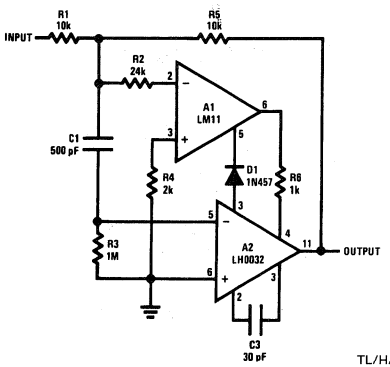
TL/H/5653–21

Application Hints (Continued)

Fast Amplifiers

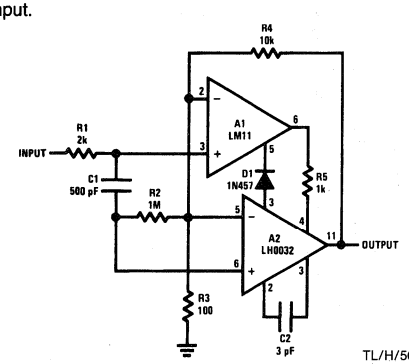
These inverters have bias current and offset voltage of LM11 along with speed of the FET op amps. Open loop gain is about 140 dB and settling time to 1 mV about 8 μS. Overload-recovery delay can be eliminated by direct coupling the FET amplifier to summing node.





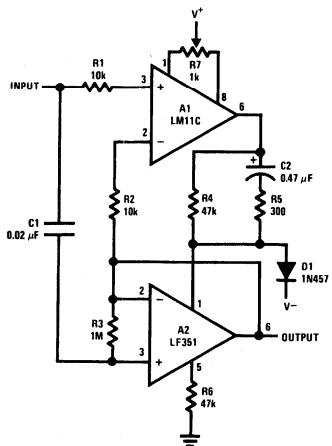
TL/H/5653–22

This 100× amplifier has small and large signal bandwidth of 1 MHz. The LM11 greatly reduces offset voltage, bias current and gain error. Eliminating long recovery delay for greater than 100% overload requires direct coupling of A2 to input.



TL/H/5653–24

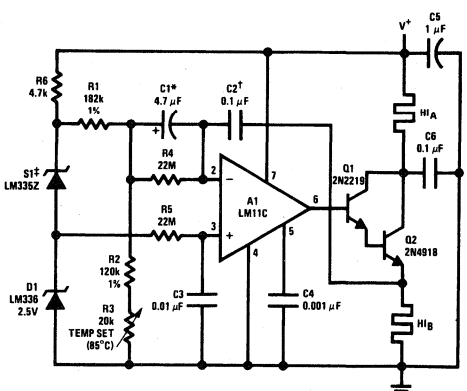
Follower has 10 μS setting to 1 mV, but signal repetition frequency should not exceed 10 kHz if the FET amplifier is ac coupled to input. The circuit does not behave well if common-mode range is exceeded.



TL/H/5653–23

Heater Control

Proportional control crystal oven heater uses lead/lag compensation for fast settling. Time constant is changed with R4 and compensating resistor R5. If Q2 is inside oven, a regulated supply is recommended for 0.1°C control.



TL/H/5653–25

* Solid tantalum

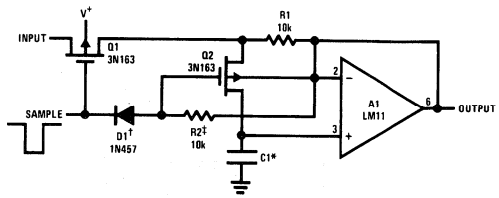
† Mylar

‡ Close thermal coupling between sensor and oven shell is recommended.

Application Hints (Continued)

Leakage Isolation

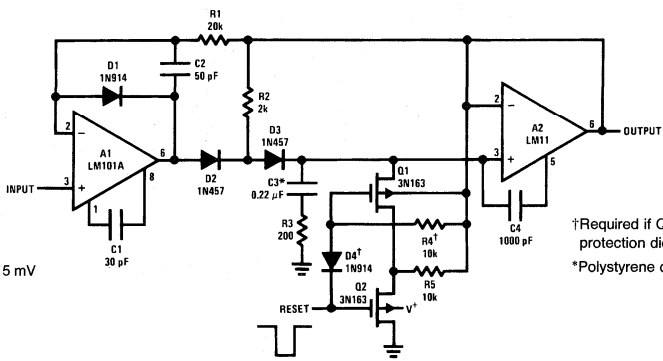
Switch leakage in this sample and hold does not reach storage capacitor.



*Polystyrene or Teflon
†Required if protected-gate switch is used

TL/H/5653–26

A peak detector designed for extended hold. Leakage currents of peak-detecting diodes and reset switch are absorbed before reaching storage capacitor.

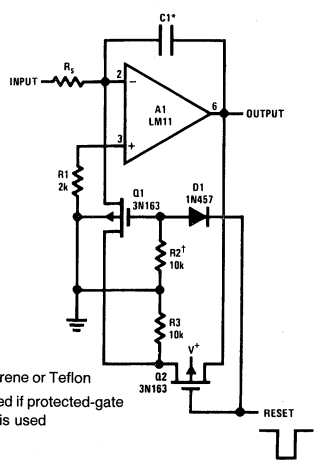


300 µS min single pulse
200 µS min repetitive pulse
300 Hz max sine wave error < 5 mV

†Required if Q1 has gate-protection diode
*Polystyrene or Teflon

TL/H/5653–27

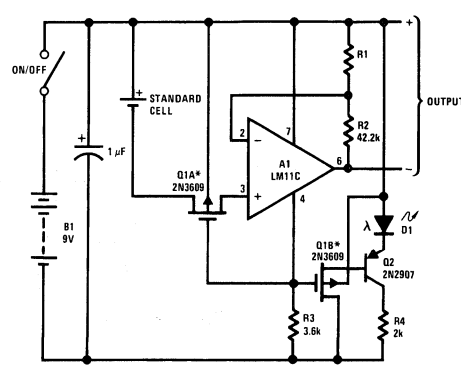
Reset is provided for this integrater and switch leakage is isolated from the summing junction. Greater precision can be provided if bias-current compensation is included.



*Polystyrene or Teflon
†Required if protected-gate switch is used

Standard-Cell Buffer

Battery powered buffer amplifier for standard cell has negligible loading and disconnects cell for low supply voltage or overload on output. Indicator diode extinguishes as disconnect circuitry is activated.



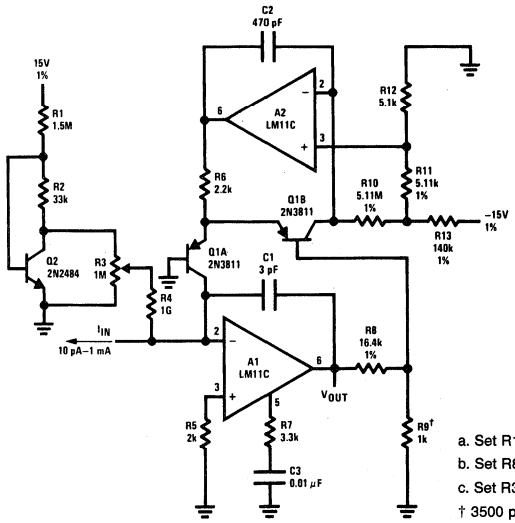
TL/H/5653–28

*Cannot have gate protection diode; $V_{TH} > V_{OUT}$

Application Hints (Continued)

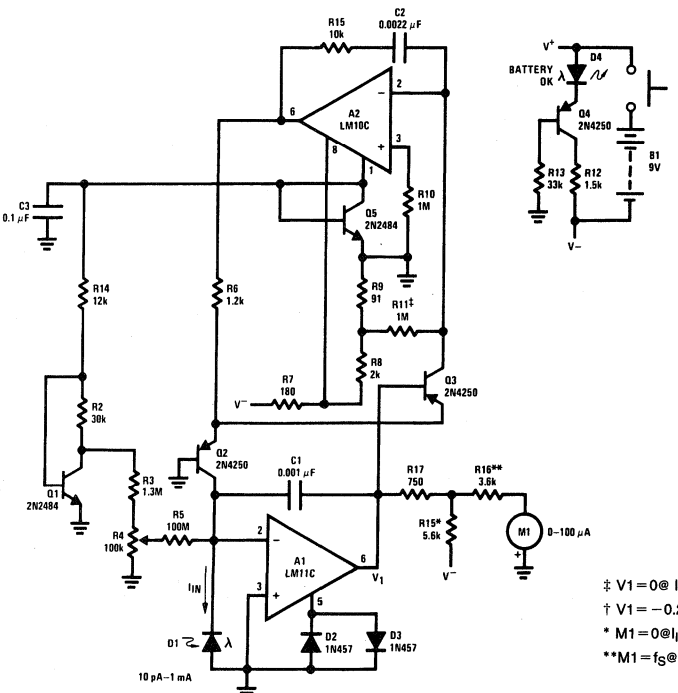
Logarithmic Amplifiers

Unusual frequency compensation gives this logarithmic converter a 100 μs, time constant from 1 mA down to 100 μA, increasing from 200 μs to 200 ms from 10 nA to 10 pA. Optional bias current compensation can give 10 pA resolution from −55°C to 100°C. Scale factor is 1V/decade and temperature compensated.



a. Set R11 for $V_{OUT} = 0$ at $I_{IN} = 100$ nA
b. Set R8 for $V_{OUT} = 3V$ at $I_{IN} = 100$ μA
c. Set R3 for $V_{OUT} = -4V$ at $I_{IN} = 10$ pA
† 3500 ppM/°C. Type Q81 available from Tel Labs Inc., Londonderry, N.H.

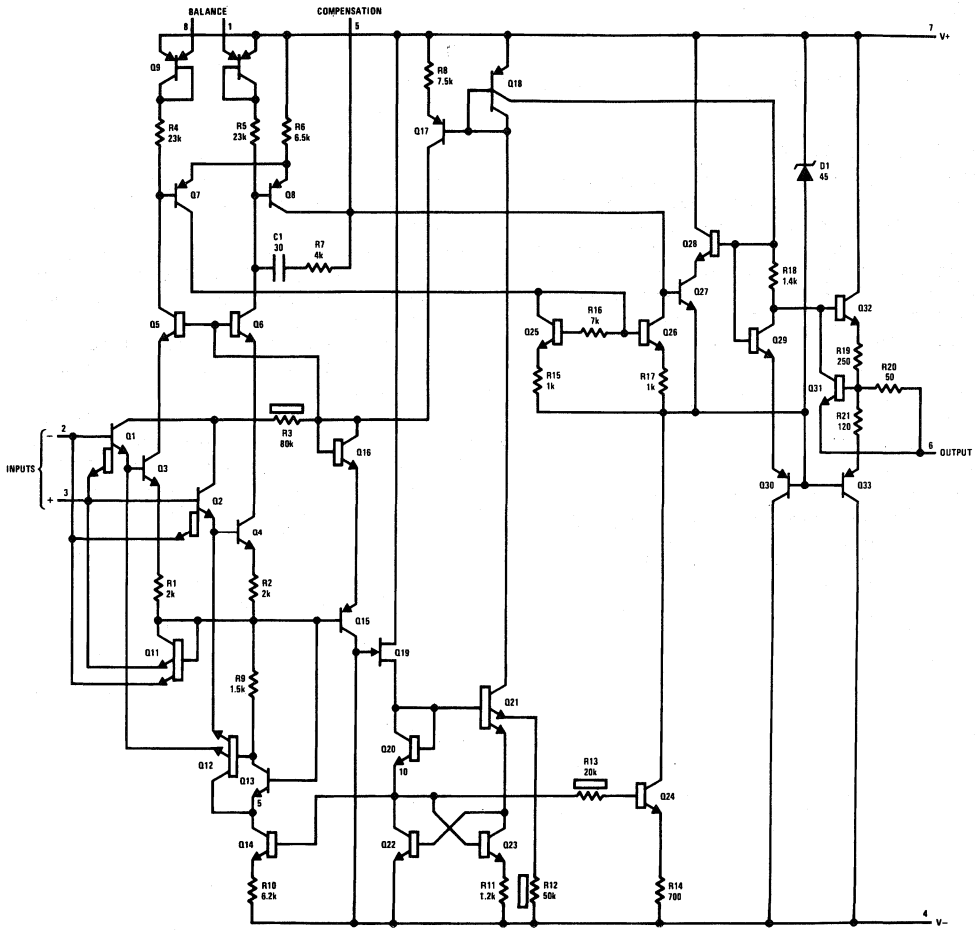
Light meter has eight-decade range. Bias current compensation can give input current resolution of better than ±2 pA over 15°C to 55°C.



‡ V1 = 0@ $I_{IN} = 100$ nA
† V1 = −0.24V@$I_{IN} = 10$ pA
* M1 = 0@$I_{IN} = 10$ pA
**M1 = f_S@$I_{IN} = 1$ mA

TL/H/5653–29

Schematic Diagram



TL/H/5653–30

Definition of Terms

Input offset voltage: That voltage which must be applied between the input terminals to bias the unloaded output in the linear region.

Input offset current: The difference in the currents at the input terminals when the output is unloaded in the linear region.

Input bias current: The absolute value of the average of the two input currents.

Input resistance: The ratio of the change in input voltage to the change in input current on either input with the other grounded.

Large signal voltage gain: The ratio of the specified output voltage swing to the change in differential input voltage required to produce it.

Common-mode rejection: The ratio of the input voltage range to the change in offset voltage between the extremes.

Temperature drift: The change of a parameter measured at 25°C and either temperature extreme divided by the temperature change.

Power Supply Rejection Ratio: The ratio of the specified supply-voltage change (either or both supplies) to the change in offset voltage between the extremes.

Supply current: The current required from the power source to operate the amplifier with the output unloaded and operating in the linear range.

National Semiconductor

LM12 (L) 80W Operational Amplifier

General Description

The LM12 is a power op amp capable of driving ±25V at ±10A while operating from ±30V supplies. The monolithic IC can deliver 80W of sine wave power into a 4Ω load with 0.01% distortion. Power bandwidth is 60 kHz. Further, a peak dissipation capability of 800W allows it to handle reactive loads such as transducers, actuators or small motors without derating. Important features include:

- input protection
- controlled turn on
- thermal limiting
- overvoltage shutdown
- output-current limiting
- dynamic safe-area protection

The IC delivers ±10A output current at any output voltage yet is completely protected against overloads, including shorts to the supplies. The dynamic safe-area protection is provided by instantaneous peak-temperature limiting within the power transistor array.

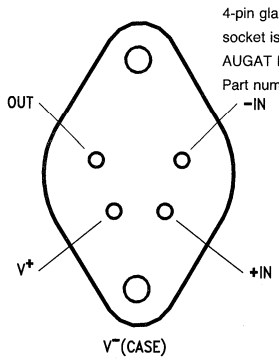
The turn-on characteristics are controlled by keeping the output open-circuited until the total supply voltage reaches 14V. The output is also opened as the case temperature exceeds 150°C or as the supply voltage approaches the BV_{CEO} of the output transistors. The IC withstands overvoltages to 80V.

This monolithic op amp is compensated for unity-gain feedback, with a small-signal bandwidth of 700 kHz. Slew rate is 9V/μs, even as a follower. Distortion and capacitive-load stability rival that of the best designs using complementary output transistors. Further, the IC withstands large differential input voltages and is well behaved should the common-mode range be exceeded.

The LM12 establishes that monolithic ICs can deliver considerable output power without resorting to complex switching schemes. Devices can be paralleled or bridged for even greater output capability. Applications include operational power supplies, high-voltage regulators, high-quality audio amplifiers, tape-head positioners, x-y plotters or other servo-control systems.

The LM12 is supplied in a four-lead, TO-3 package with V^- on the case. A gold-eutectic die-attach to a molybdenum interface is used to avoid thermal fatigue problems. The LM12 is specified for either military or commercial temperature range.

Connection Diagram



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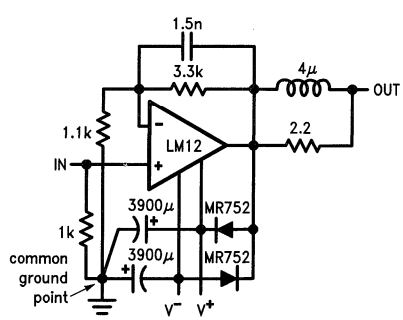
Bottom View

Order Number LM12LK or LM12CLK
See NS Package Number K04A

Typical Application*



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*Low distortion (0.01%) audio amplifier

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Total Supply Voltage (Note 1)	80V
Input Voltage	(Note 2)
Output Current	Internally Limited
Junction Temperature	(Note 3)
Storage Temperature Range	−65°C to 150°C
Lead Temperature (Soldering, 10 seconds)	300°C

Operating Ratings

Total Supply Voltage	15V to 60V

Electrical Characteristics (Note 4)

Parameter	Conditions	Typ 25°C	LM12L Limits	LM12CL Limits	Units
Input Offset Voltage	$\pm 10V \le V_S \le \pm 0.5\ V_{MAX}$, $V_{CM} = 0$	2	7/**15**	15/**20**	mV (max)
Input Bias Current	$V^- + 4V \le V_{CM} \le V^+ - 2V$	0.15	0.3/**1.0**	0.7/**1.0**	μA (max)
Input Offset Current	$V^- + 4V \le V_{CM} \le V^+ - 2V$	0.03	0.1/**0.3**	0.2/**0.3**	μA (max)
Common Mode Rejection	$V^- + 4V \le V_{CM} \le V^+ - 2V$	86	75/**70**	70/**65**	dB (min)
Power Supply Rejection	$V^+ = 0.5\ V_{MAX}$, $-6V \ge V^- \ge -0.5\ V_{MAX}$	90	75/**70**	70/**65**	dB (min)
	$V^- = -0.5\ V_{MAX}$, $6V \le V^+ \le 0.5\ V_{MAX}$	110	80/**75**	75/**70**	dB (min)
Output Saturation Threshold	$t_{ON} = 1$ ms, $\Delta V_{IN} = 5$ (**10**) mV, $I_{OUT} = 1A$	1.8	2.2/**2.5**	2.2/**2.5**	V (max)
	8A	4	5/**7**	5/**7**	V (max)
	10A	5	8		V (max)
Large Signal Voltage Gain	$t_{ON} = 2$ ms, $V_{SAT} = 2V$, $I_{OUT} = 0$	100	50/**30**	30/**20**	V/mV (min)
	$V_{SAT} = 8V$, $R_L = 4\Omega$	50	20/**15**	15/**10**	V/mV (min)
Thermal Gradient Feedback	$P_{DISS} = 50W$, $t_{ON} = 65$ ms	30	50	100	μV/W (max)
Output-Current Limit	$t_{ON} = 10$ ms, $V_{DISS} = 10V$	13	16	16	A (max)
	$t_{ON} = 100$ ms, $V_{DISS} = 58V$	1.5	1.0/**0.6**	0.9/**0.6**	A (min)
		1.5	1.7	1.7	A (max)
Power Dissipation Rating	$t_{ON} = 100$ ms, $V_{DISS} = 20V$	100	90/**40**	80/**55**	W (min)
	$V_{DISS} = 58V$	80	58/**35**	52/**35**	W (min)
DC Thermal Resistance	(Note 5) $V_{DISS} = 20V$	2.3	2.6	2.9	°C/W (max)
	$V_{DISS} = 58V$	2.7	4.0	4.5	°C/W (max)
AC Thermal Resistance	(Note 5)	1.6	1.9	2.1	°C/W (max)
Supply Current	$V_{OUT} = 0$, $I_{OUT} = 0$	60	80/**90**	120/**140**	mA (max)

Note 1: These are non-operating limits (over-voltage shut down); operating limits are as in Note 4. With inductive loads or output shorts, other restrictions described in applications section apply.

Note 2. Neither input should exceed the supply voltage by more than 50 volts nor should the voltage between one input and any other terminal exceed 60 volts.

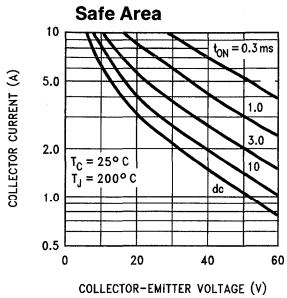
Note 3. Operating junction temperature is internally limited near 225°C within the power transistor and 160°C for the control circuitry.

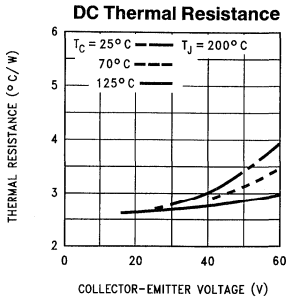
Note 4. The supply voltage is ±30V (V_{MAX} = 60V), unless otherwise specified. The voltage across the conducting output transistor (supply to output) is V_{DISS} and internal power dissipation is P_{DISS}. Temperature range is $-55°C \le T_C \le 125°C$ for the LM12L and $0°C \le T_C \le 70°C$ for LM12CL, where T_C is the case temperature. Standard typeface indicates limits at 25°C **while boldface type refers to limits or special conditions over full temperature range.** With no heat sink, the package will heat at a rate of 35°C/sec per 100W of internal dissipation.

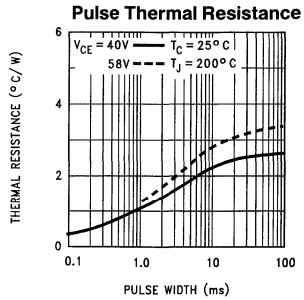
Note 5. This thermal resistance is based upon a peak temperature of 200°C in the center of the power transistor and a case temperature of 25°C measured at the center of the package bottom. The maximum junction temperature of the control circuitry can be estimated based upon a dc thermal resistance of 0.9°C/W or an ac thermal resistance of 0.6°C/W for any operating voltage.

Although the output and supply leads are resistant to electrostatic discharges from handling, the input leads are not. The part should be treated accordingly.

Output-Transistor Ratings (guaranteed)†







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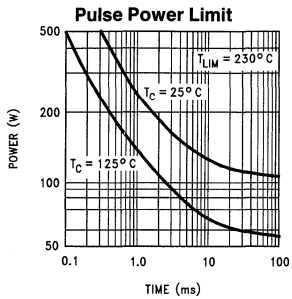
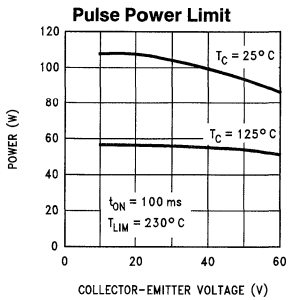
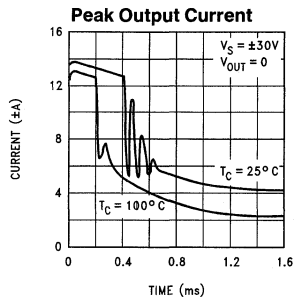
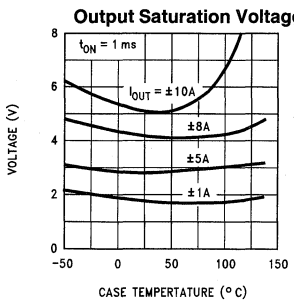
†LM12L. The power ratings of the LM12CL are 10-percent less at 20V and 15-percent less at 60V, with a corresponding increase in thermal resistance and decrease in safe area current.

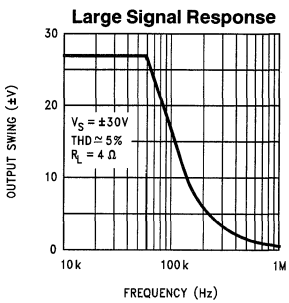
Typical Performance Characteristics

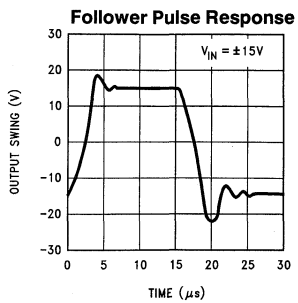












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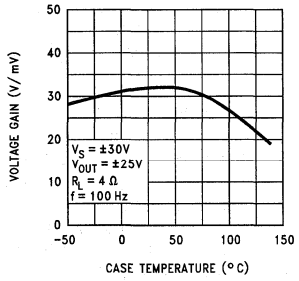
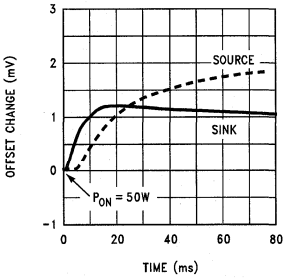
Typical Performance Characteristics (Continued)

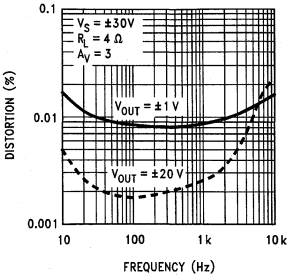
Large Signal Gain



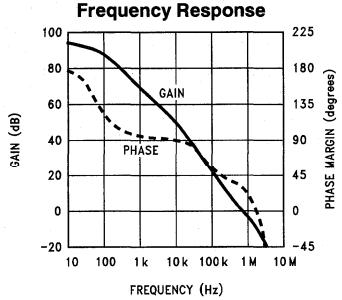
Thermal Response



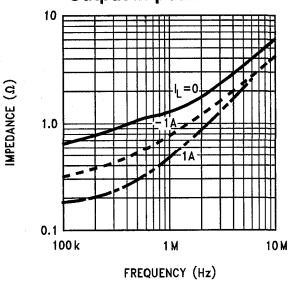
Total Harmonic Distortion



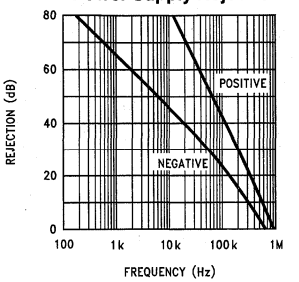
Frequency Response



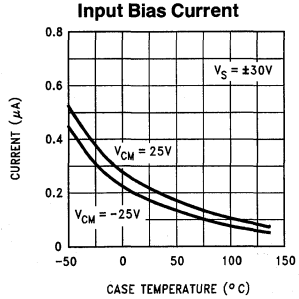
Output Impedance



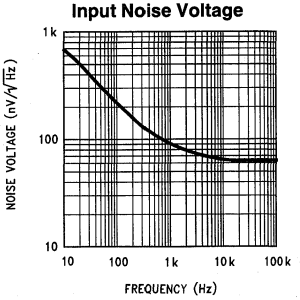
Power Supply Rejection



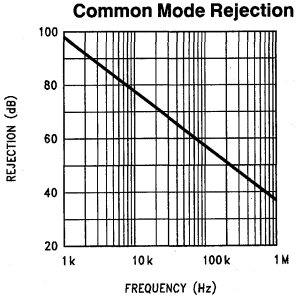
Input Bias Current



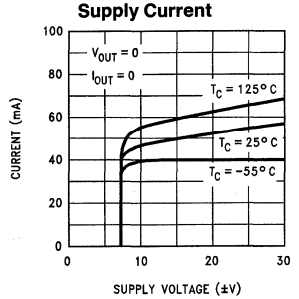
Input Noise Voltage



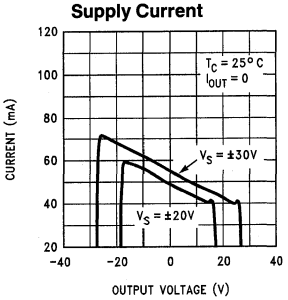
Common Mode Rejection



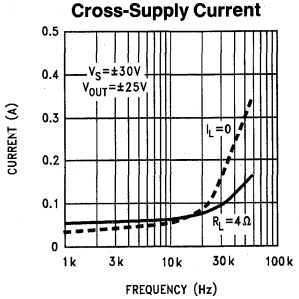
Supply Current



Supply Current



Cross-Supply Current



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Application Information

GENERAL

Twenty five years ago the operational amplifier was a specialized design tool used primarily for analog computation. However, the availability of low cost IC op amps in the late 1960's prompted their use in rather mundane applications, replacing a few discrete components. Once a few basic principles are mastered, op amps can be used to give exceptionally good results in a wide range of applications while minimizing both cost and design effort.

The availability of a monolithic power op amp now promises to extend these advantages to high-power designs. Some conventional applications are given here to illustrate op amp design principles as they relate to power circuitry. The inevitable fall in prices, as the economies of volume production are realized, will prompt their use in applications that might now seem trivial. Replacing single power transistors with an op amp will become economical because of improved performance, simplification of attendant circuitry, vastly improved fault protection, greater reliability and the reduction of design time.

Power op amps introduce new factors into the design equation. With current transients above 10A, both the inductance and resistance of wire interconnects become important in a number of ways. Further, power ratings are a crucial factor in determining performance. But the power capability of the IC cannot be realized unless it is properly mounted to an adequate heat sink. Thus, thermal design is of major importance with power op amps.

This application summary starts off by identifying the origin of strange problems observed while using the LM12 in a wide variety of designs with all sorts of fault conditions. A few simple precautions will eliminate these problems. **One would do well to read the section on supply bypassing, lead inductance, output clamp diodes, ground loops and reactive loading before doing any experimentation. Should there be problems with erratic operation, blow-outs, excessive distortion or oscillation, another look at these sections is in order.**

The management and protection circuitry can also affect operation. Should the total supply voltage exceed ratings or drop below 15–20V, the op amp shuts off completely. Case temperatures above 150°C also cause shut down until the temperature drops to 145°C. This may take several seconds, depending on the thermal system. Activation of the dynamic safe-area protection causes both the main feedback loop to lose control and a reduction in output power, with possible oscillations. In ac applications, the dynamic protection will cause waveform distortion. Since the LM12 is well protected against thermal overloads, the suggestions for determining power dissipation and heat sink requirements are presented last.

SUPPLY BYPASSING

All op amps should have their supply leads bypassed with low-inductance capacitors having short leads and located close to the package terminals to avoid spurious oscillation problems. Power op amps require larger bypass capacitors. The LM12 is stable with good-quality electrolytic bypass capacitors greater than 20 μF. Other considerations may require larger capacitors.

The current in the supply leads is a rectified component of the load current. If adequate bypassing is not provided, this distorted signal can be fed back into internal circuitry. Low distortion at high frequencies requires that the supplies be bypassed with 470 μF or more, at the package terminals.

LEAD INDUCTANCE

With ordinary op amps, lead-inductance problems are usually restricted to supply bypassing. Power op amps are also sensitive to inductance in the output lead, particularly with heavy capacitive loading. Feedback to the input should be taken directly from the output terminal, minimizing common inductance with the load. Sensing to a remote load must be accompanied by a high-frequency feedback path directly from the output terminal. Lead inductance can also cause voltage surges on the supplies. With long leads to the power source, energy stored in the lead inductance when the output is shorted can be dumped back into the supply bypass capacitors when the short is removed. The magnitude of this transient is reduced by increasing the size of the bypass capacitor near the IC. With 20 μF local bypass, these voltage surges are important only if the lead length exceeds a couple feet ($>$ 1 μH lead inductance). Twisting together the supply and ground leads minimizes the effect.

GROUND LOOPS

With fast, high-current circuitry, all sorts of problems can arise from improper grounding. In general, difficulties can be avoided by returning all grounds separately to a common point. Sometimes this is impractical. When compromising, special attention should be paid to the ground returns for the supply bypasses, load and input signal. Ground planes also help to provide proper grounding.

Many problems unrelated to system performance can be traced to the grounding of line-operated test equipment used for system checkout. Hidden paths are particularly difficult to sort out when several pieces of test equipment are used but can be minimized by using current probes or the new isolated oscilloscope pre-amplifiers. Eliminating any direct ground connection between the signal generator and the oscilloscope synchronization input solves one common problem.

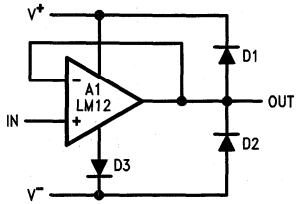
OUTPUT CLAMP DIODES

When a push-pull amplifier goes into power limit while driving an inductive load, the stored energy in the load inductance can drive the output outside the supplies. Although the LM12 has internal clamp diodes that can handle several amperes for a few milliseconds, extreme conditions can cause destruction of the IC. The internal clamp diodes are imperfect in that about half the clamp current flows into the supply to which the output is clamped while the other half flows across the supplies. Therefore, the use of external diodes to clamp the output to the power supplies is strongly recommended. This is particularly important with higher supply voltages.

Experience has demonstrated that hard-wire shorting the output to the supplies can induce random failures if these external clamp diodes are not used and the supply voltages are above $\pm$20V. Therefore it is prudent to use output-

Application Information (Continued)

clamp diodes even when the load is not particularly inductive. This also applies to experimental setups in that blowouts have been observed when diodes were not used. In packaged equipment, it may be possible to eliminate these diodes, providing that fault conditions can be controlled.



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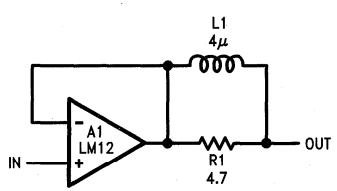
Heat sinking of the clamp diodes is usually unimportant in that they only clamp current transients. Forward drop with 15A fault transients is of greater concern. Usually, these transients die out rapidly. The clamp to the negative supply can have somewhat reduced effectiveness under worst case conditions should the forward drop exceed 1.0V. Mounting this diode to the power op amp heat sink improves the situation. Although the need has only been demonstrated with some motor loads, including a third diode (D3 above) will eliminate any concern about the clamp diodes. This diode, however, must be capable of dissipating continuous power as determined by the negative supply current of the op amp.

REACTIVE LOADING

The LM12 is normally stable with resistive, inductive or smaller capacitive loads. Larger capacitive loads interact with the open-loop output resistance (about 1Ω) to reduce the phase margin of the feedback loop, ultimately causing oscillation. The critical capacitance depends upon the feedback applied around the amplifier; a unity-gain follower can handle about 0.01 μF, while more than 1 μF does not cause problems if the loop gain is ten. With loop gains greater than unity, a speedup capacitor across the feedback resistor will aid stability. In all cases, the op amp will behave predictably only if the supplies are properly bypassed, ground loops are controlled and high-frequency feedback is derived directly from the output terminal, as recommended earlier.

So-called capacitive loads are not always capacitive. A high-Q capacitor in combination with long leads can present a series-resonant load to the op amp. In practice, this is not usually a problem; but the situation should be kept in mind.



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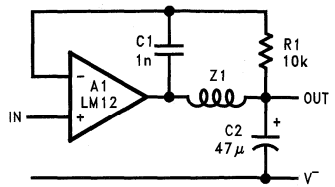
Large capacitive loads (including series-resonant) can be accommodated by isolating the feedback amplifier from the load as shown above. The inductor gives low output impedance at lower frequencies while providing an isolating impedance at high frequencies. The resistor kills the Q of series resonant circuits formed by capacitive loads. A low inductance, carbon-composition resistor is recommended. Optimum values of L and R depend upon the feedback gain and expected nature of the load, but are not critical. A 4 μH inductor is obtained with 14 turns of number 18 wire, close spaced, around a one-inch-diameter form.



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The LM12 can be made stable for all loads with a large capacitor on the output, as shown above. This compensation gives the lowest possible closed-loop output impedance at high frequencies and the best load-transient response. It is appropriate for such applications as voltage regulators.

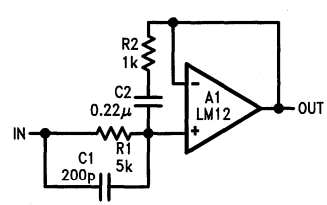
A feedback capacitor, C_1, is connected directly to the output pin of the IC. The output capacitor, C_2, is connected at the output terminal with short leads. Single-point grounding to avoid dc and ac ground loops is advised.

The impedance, Z_1, is the wire connecting the op amp output to the load capacitor. About 3-inches of number-18 wire (70 nH) gives good stability and 18-inches (400 nH) begins to degrade load-transient response. The minimum load capacitance is 47 μF, if a solid-tantalum capacitor with an equivalent series resistance (ESR) of 0.1Ω is used. Electrolytic capacitors work as well, although capacitance may have to be increased to 200 μF to bring ESR below 0.1Ω.

Loop stability is not the only concern when op amps are operated with reactive loads. With time-varying signals, power dissipation can also increase markedly. This is particularly true with the combination of capacitive loads and high-frequency excitation.

INPUT COMPENSATION

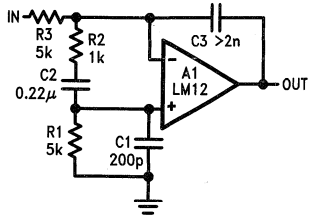
The LM12 is prone to low-amplitude oscillation bursts coming out of saturation if the high-frequency loop gain is near unity. The voltage follower connection is most susceptible. This glitching can be eliminated at the expense of small-signal bandwidth using input compensation. Input compensation can also be used in combination with LR load isolation to improve capacitive load stability.



TL/H/8704–9

An example of a voltage follower with input compensation is shown here. The R_2C_2 combination across the input works with R_1 to reduce feedback at high frequencies without greatly affecting response below 100 kHz. A lead capacitor, C_1, improves phase margin at the unity-gain crossover frequency. Proper operation requires that the output impedance of the circuitry driving the follower be well under 1 kΩ at frequencies up to a few hundred kilohertz.

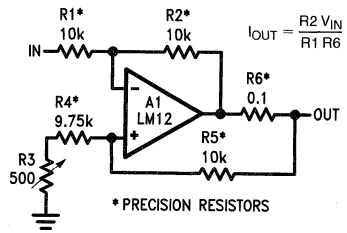
Application Information (Continued)



TL/H/8704–10

Extending input compensation to the integrator connection is shown here. Both the follower and this integrator will handle 1 μF capacitive loading without LR output isolation.

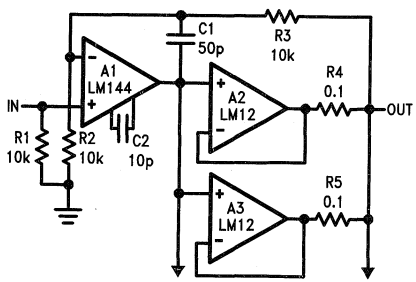
CURRENT DRIVE



TL/H/8704–11

This circuit provides an output current proportional to the input voltage. Current drive is sometimes preferred for servo motors because it aids in stabilizing the servo loop by reducing phase lag caused by motor inductance. In applications requiring high output resistance, such as operational power supplies running in the current mode, matching of the feedback resistors to 0.01% is required. Alternately, an adjustable resistor can be used for trimming.

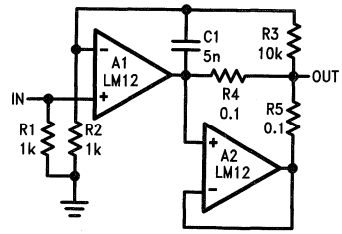
PARALLEL OPERATION



TL/H/8704–12

Output drive beyond the capability of one power amplifier can be provided as shown here. The power op amps are wired as followers and connected in parallel with the outputs coupled through equalization resistors. A standard, high-voltage op amp is used to provide voltage gain. Overall feedback compensates for the voltage dropped across the equalization resistors.

With parallel operation, there may be an increase in unloaded supply current related to the offset voltage across the equalization resistors. More output buffers, with individual equalization resistors, may be added to meet even higher drive requirements.

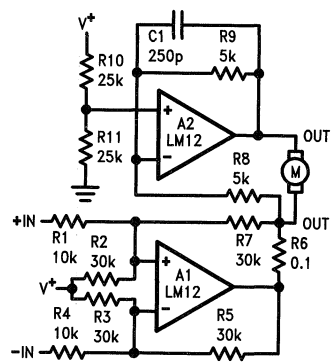


TL/H/8704–13

This connection allows increased output capability without requiring a separate control amplifier. The output buffer, A_2, provides load current through R_5 equal to that supplied by the main amplifier, A_1, through R_4. Again, more output buffers can be added.

Current sharing among paralleled amplifiers can be affected by gain error as the power-bandwidth limit is approached. In the first circuit, the operating current increase will depend upon the matching of high-frequency characteristics. In the second circuit, however, the entire input error of A_2 appears across R_4 and R_5. The supply current increase can cause power limiting to be activated as the slew limit is approached. This will not damage the LM12. It can be avoided in both cases by connecting A_1 as an inverting amplifier and restricting bandwidth with C_1.

SINGLE-SUPPLY OPERATION



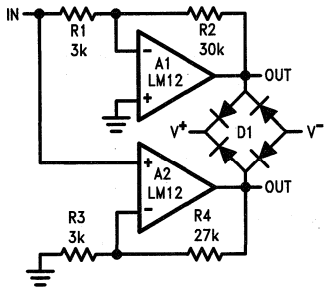
TL/H/8704–14

Although op amps are usually operated from dual supplies, single-supply operation is practical. This bridge amplifier supplies bi-directional current drive to a servo motor while operating from a single positive supply. The output is easily converted to voltage drive by shorting R_6 and connecting R_7 to the output of A_2, rather than A_1.

Either input may be grounded, with bi-directional drive provided to the other. It is also possible to connect one input to a positive reference, with the input signal varying about this voltage. If the reference voltage is above 5V, R_2 and R_3 are not required.

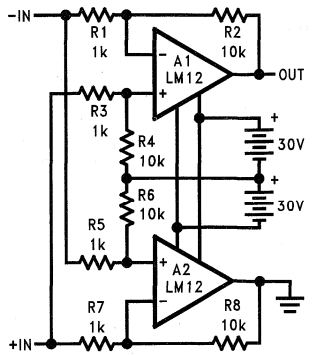
Application Information (Continued)

HIGH VOLTAGE AMPLIFIERS



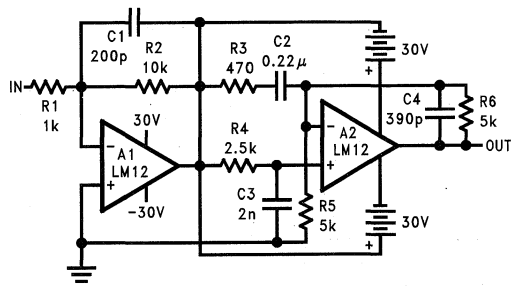
TL/H/8704–15

The voltage swing delivered to the load can be doubled by using the bridge connection shown here. Output clamping to the supplies can be provided by using a bridge-rectifier assembly.



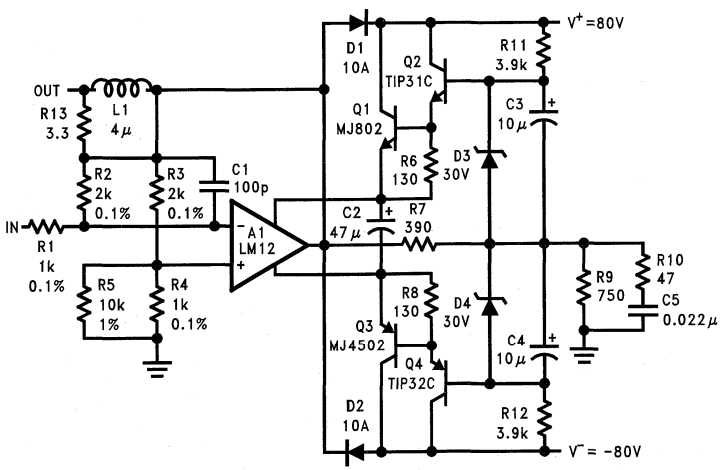
TL/H/8704–16

One limitation of the standard bridge connection is that the load cannot be returned to ground. This can be circumvented by operating the bridge with floating supplies, as shown above. For single-ended drive, either input can be grounded.



TL/H/8704–17

This circuit shows how two amplifiers can be cascaded to double output swing. The advantage over the bridge is that the output can be increased with any number of stages, although separate supplies are required for each.

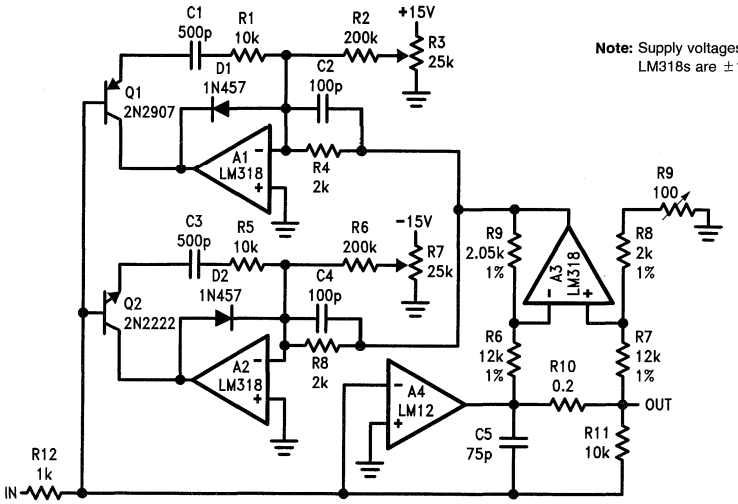


TL/H/8704–18

Discrete transistors can be used to increase output drive to ±70V at ±10A as shown above. With proper thermal design, the IC will provide safe-area protection for the external transistors. Voltage gain is about thirty.

Application Information (Continued)

OPERATIONAL POWER SUPPLY



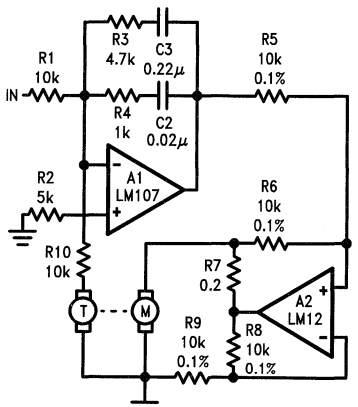
Note: Supply voltages for the LM318s are ±15V

TL/H/8704–19

External current limit can be provided for a power op amp as shown above. The positive and negative current limits can be set precisely and independently. Fast response is assured by D_1 and D_2. Adjustment range can be set down to zero with potentiometers R_3 and R_7. Alternately, the limit can be programmed from a voltage supplied to R_2 and R_6. This is the set up required for an operational power supply or voltage-programmable power source.

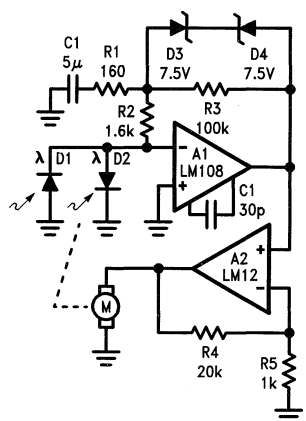
SERVO AMPLIFIERS

When making servo systems with a power op amp, there is a temptation to use it for frequency shaping to stabilize the servo loop. Sometimes this works; other times there are better ways; and occasionally it just doesn't fly. Usually it's a matter of how quickly and to what accuracy the servo must stabilize.



TL/H/8704–20

This motor/tachometer servo gives an output speed proportional to input voltage. A low-level op amp is used for frequency shaping while the power op amp provides current drive to the motor. Current drive eliminates loop phase shift due to motor inductance and makes high-performance servos easier to stabilize.

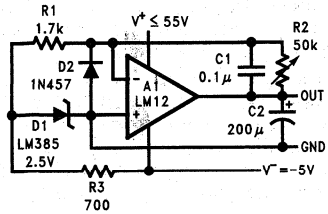


TL/H/8704–21

This position servo uses an op amp to develop the rate signal electrically instead of using a tachometer. In high-performance servos, rate signals must be developed with large error signals well beyond saturation of the motor drive. Using a separate op amp with a feedback clamp allows the rate signal to be developed properly with position errors more than an order of magnitude beyond the loop-saturation level as long as the photodiode sensors are positioned with this in mind.

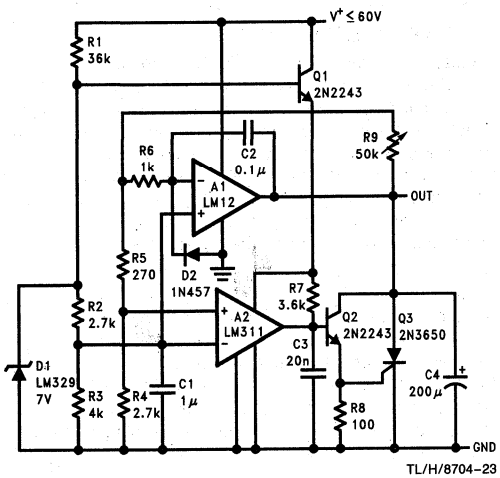
Application Information (Continued)

VOLTAGE REGULATORS



TL/H/8704–22

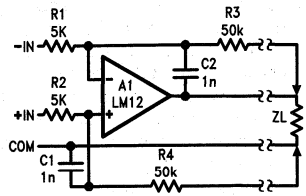
An op amp can be used as a positive or negative regulator. Unlike most regulators, it can sink current to absorb energy dumped back into the output. This positive regulator has a 0–50V output range.



TL/H/8704–23

Dual supplies are not required to use an op amp as a voltage regulator if zero output is not required. This 4V to 50V regulator operates from a single supply. Should the op amp not be able to absorb enough energy to control an overvoltage condition, a SCR will crowbar the output.

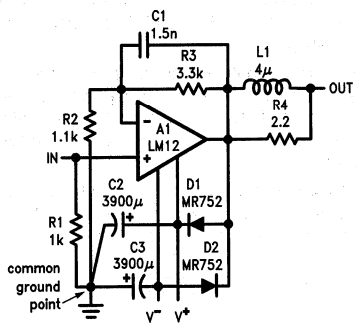
REMOTE SENSING



TL/H/8704–24

Remote sensing as shown above allows the op amp to correct for dc drops in cables connecting the load. Even so, cable drop will affect transient response. Degradation can be minimized by using twisted, heavy-gauge wires on the output line. Normally, common and one input are connected together at the sending end.

AUDIO AMPLIFIERS



TL/H/8704–25

A power amplifier suitable for use in high-quality audio equipment is shown above. Harmonic distortion is about 0.01-percent. Intermodulation distortion (60 Hz/7 kHz, 4:1) measured 0.015-percent. Transient response and saturation recovery are clean, and the 9 V/μs slew rate of the LM12 virtually eliminates transient intermodulation distortion. Using separate amplifiers to drive low- and high-frequency speakers gets rid of high-level crossover networks and attenuators. Further, it prevents clipping on the low-frequency channel from distorting the high frequencies.

Application Information (Continued)

DETERMINING MAXIMUM DISSIPATION

It is a simple matter to establish power requirements for an op amp driving a resistive load at frequencies well below 10 Hz. Maximum dissipation occurs when the output is at one-half the supply voltage with high-line conditions. The individual output transistors must be rated to handle this power continuously at the maximum expected case temperature. The power rating is limited by the maximum junction temperature as determined by

$$T_J = T_C + P_{DISS}\,\theta_{JC},$$

where T_C is the case temperature as measured at the center of the package bottom, P_{DISS} is the maximum power dissipation and θ_{JC} is the thermal resistance at the operating voltage of the output transistor. Recommended maximum junction temperatures are 200°C within the power transistor and 150°C for the control circuitry.

If there is ripple on the supply bus, it is valid to use the average value in worst-case calculations as long as the peak rating of the power transistor is not exceeded at the ripple peak. With 120 Hz ripple, this is 1.5 times the continuous power rating.

Dissipation requirements are not so easily established with time varying output signals, especially with reactive loads. Both peak and continuous dissipation ratings must be taken into account, and these depend on the signal waveform as well as load characteristics.

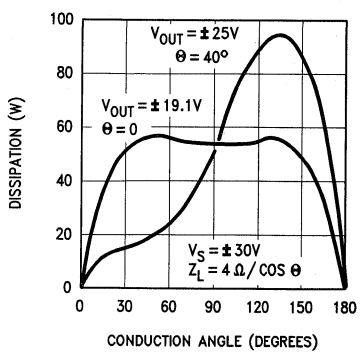
With a sine wave output, analysis is fairly straightforward. With supply voltages of $\pm V_S$, the maximum average power dissipation of both output transistors is

$$P_{MAX} = \frac{2V_S^2}{\pi^2 Z_L \cos\theta}, \quad \theta < 40°;$$

and

$$P_{MAX} = \frac{V_S^2}{2Z_L}\left[\frac{4}{\pi} - \cos\theta\right], \quad \theta \geq 40°,$$

where Z_L is the magnitude of the load impedance and θ its phase angle. Maximum average dissipation occurs below maximum output swing for $\theta < 40°$.



TL/H/8704–26

The instantaneous power dissipation over the conducting half cycle of one output transistor is shown here. Power dissipation is near zero on the other half cycle. The output level is that resulting in maximum peak and average dissipation. Plots are given for a resistive and a series RL load. The latter is representative of a 4Ω loudspeaker operating below resonance and would be the worst case condition in most audio applications. The peak dissipation of each transistor is about four times average. In ac applications, power capability is often limited by the peak ratings of the power transistor.

The pulse thermal resistance of the LM12 is specified for constant power pulse duration. Establishing an exact equivalency between constant-power pulses and those encountered in practice is not easy. However, for sine waves, reasonable estimates can be made at any frequency by assuming a constant power pulse amplitude given by:

$$P_{PK} \cong \frac{V_S^2}{2Z_L}\left[1\text{-}\cos(\phi - \theta)\right],$$

where $\phi = 60°$ and θ is the absolute value of the phase angle of Z_L. Equivalent pulse width is $t_{ON} \cong 0.4\tau$ for $\theta = 0$ and $t_{ON} \cong 0.2\tau$ for $\theta \geq 20°$, where τ is the period of the output waveform.

DISSIPATION DRIVING MOTORS

A motor with a locked rotor looks like an inductance in series with a resistance, for purposes of determining driver dissipation. With slow-response servos, the maximum signal amplitude at frequencies where motor inductance is significant can be so small that motor inductance does not have to be taken into account. If this is the case, the motor can be treated as a simple, resistive load as long as the rotor speed is low enough that the back emf is small by comparison to the supply voltage of the driver transistor.

A permanent-magnet motor can build up a back emf that is equal to the output swing of the op amp driving it. Reversing this motor from full speed requires the output drive transistor to operate, initially, along a loadline based upon the motor resistance and total supply voltage. Worst case, this loadline will have to be within the continuous dissipation rating of the drive transistor; but system dynamics may permit taking advantage of the higher pulse ratings. Motor inductance can cause added stress if system response is fast.

Shunt- and series-wound motors can generate back emf's that are considerably more than the total supply voltage, resulting in even higher peak dissipation than a permanent-magnet motor having the same locked-rotor resistance.

VOLTAGE REGULATOR DISSIPATION

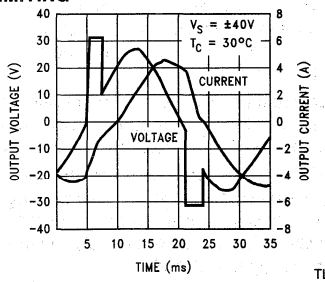
The pass transistor dissipation of a voltage regulator is easily determined in the operating mode. Maximum continuous dissipation occurs with high line voltage and maximum load current. As discussed earlier, ripple voltage can be averaged if peak ratings are not exceeded; however, a higher average voltage will be required to insure that the pass transistor does not saturate at the ripple minimum.

Conditions during start-up can be more complex. If the input voltage increases slowly such that the regulator does not go into current limit charging output capacitance, there are no problems. If not, load capacitance and load characteristics must be taken into account. This is also the case if automatic restart is required in recovering from overloads.

Automatic restart or start-up with fast-rising input voltages cannot be guaranteed unless the continuous dissipation rating of the pass transistor is adequate to supply the load current continuously at all voltages below the regulated output voltage. In this regard, the LM12 performs much better than IC regulators using foldback current limit, especially with high-line input voltage above 20V.

Application Information (Continued)

POWER LIMITING



TL/H/8704–27

Should the power ratings of the LM12 be exceeded, dynamic safe-area protection is activated. Waveforms with this power limiting are shown for the LM12 driving ±26V at 30 Hz into 3Ω in series with 24 mH (θ = 45°). With an inductive load, the output clamps to the supplies in power limit, as above. With resistive loads, the output voltage drops in limit. Behavior with more complex RCL loads is between these extremes.

Secondary thermal limit is activated should the case temperature exceed 150°C. This thermal limit shuts down the IC completely (open output) until the case temperature drops to about 145°C. Recovery may take several seconds.

POWER SUPPLIES

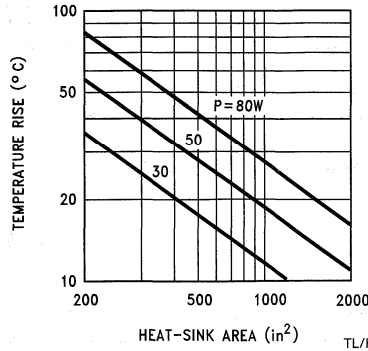
Power op amps do not require regulated supplies. However, the worst-case output power is determined by the low-line supply voltage in the ripple trough. The worst-case power dissipation is established by the average supply voltage with high-line conditions. The loss in power output that can be guaranteed is the square of the ratio of these two voltages.

Relatively simple off-line switching power supplies can provide voltage conversion, line isolation and 5-percent regulation while reducing size and weight.

The regulation against ripple and line variations can provide a substantial increase in the power output that can be guaranteed under worst-case conditions. In addition, switching power supplies can convert low-voltage power sources such as automotive batteries up to regulated, dual, high-voltage supplies optimized for powering power op amps.

HEAT SINKING

A semiconductor manufacturer has no control over heat sink design. Temperature rating can only be based upon case temperature as measured at the center of the package bottom. With power pulses of longer duration than 100 ms, case temperature is almost entirely dependent on heat sink design and the mounting of the IC to the heat sink.



TL/H/8704–28

The design of heat sink is beyond the scope of this work. Convection-cooled heat sinks are available commercially, and their manufacturers should be consulted for ratings. The preceding figure is a rough guide for temperature rise as a function of fin area (both sides) available for convection cooling.

Proper mounting of the IC is required to minimize the thermal drop between the package and the heat sink. The heat sink must also have enough metal under the package to conduct heat from the center of the package bottom to the fins without excessive temperature drop.

A thermal grease such as Wakefield type 120 or Thermalloy Thermacote should be used when mounting the package to the heat sink. Without this compound, thermal resistance will be no better than 0.5°C/W, and probably much worse. With the compound, thermal resistance will be 0.2°C/W or less, assuming under 0.005 inch combined flatness runout for the package and heat sink. Proper torquing of the mounting bolts is important. Four to six inch-pounds is recommended.

Should it be necessary to isolate V^- from the heat sink, an insulating washer is required. Hard washers like berylium oxide, anodized aluminum and mica require the use of thermal compound on both faces. Two-mil mica washers are most common, giving about 0.4°C/W interface resistance with the compound. Silicone-rubber washers are also available. A 0.5°C/W thermal resistance is claimed without thermal compound. Experience has shown that these rubber washers deteriorate and must be replaced should the IC be dismounted.

"Isostrate" insulating pads for four-lead TO-3 packages are available from Power Devices, Inc. Thermal grease is not required, and the insulators should not be reused.

Definition of Terms

Input offset voltage: The absolute value of the voltage between the input terminals with the output voltage and current at zero.

Input bias current: The absolute value of the average of the two input currents with the output voltage and current at zero.

Input offset current: The absolute value of the difference in the two input currents with the output voltage and current at zero.

Common-mode rejection: The ratio of the input voltage range to the change in offset voltage between the extremes.

Supply-voltage rejection: The ratio of the specified supply-voltage change to the change in offset voltage between the extremes.

Output saturation threshold: The output swing limit for a specified input drive beyond that required for zero output. It is measured with respect to the supply to which the output is swinging.

Large signal voltage gain: The ratio of the output voltage swing to the differential input voltage required to drive the output from zero to either swing limit. The output swing limit is the supply voltage less a specified quasi-saturation voltage. A pulse of short enough duration to minimize thermal effects is used as a measurement signal.

Thermal gradient feedback: The input offset voltage change caused by thermal gradients generated by heating of the output transistors, but not the package. This effect is delayed by several milliseconds and results in increased gain error below 100 Hz.

Output-current limit: The output current with a fixed output voltage and a large input overdrive. The limiting current drops with time once the protection circuitry is activated.

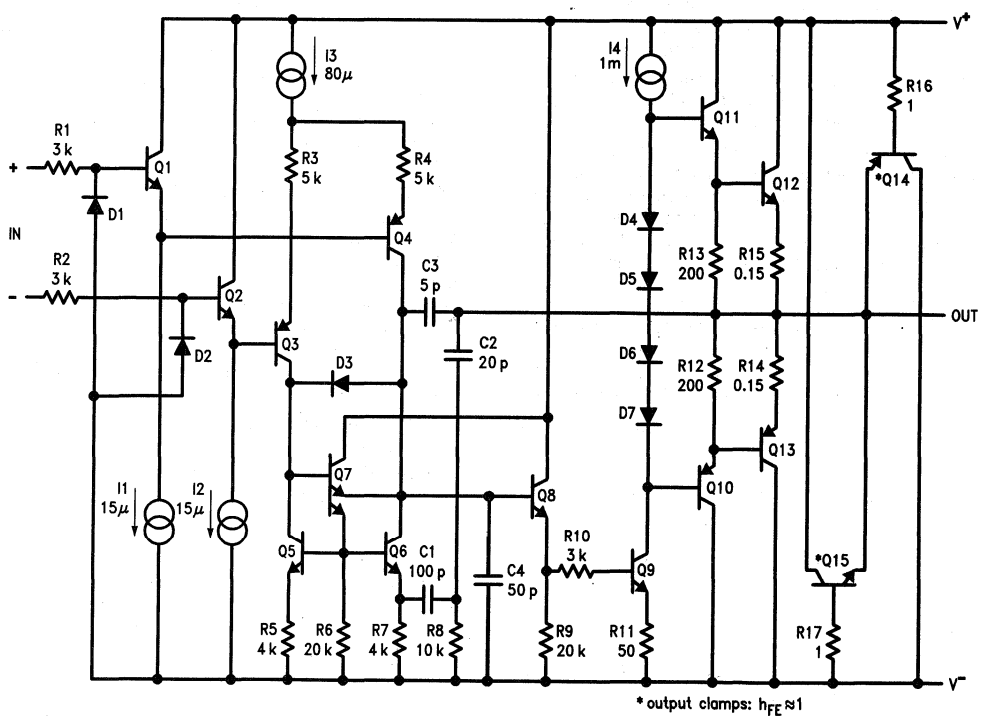
Power dissipation rating: The power that can be dissipated for a specified time interval without activating the protection circuitry. For time intervals in excess of 100 ms, dissipation capability is determined by heat sinking of the IC package rather than by the IC itself.

Thermal resistance: The peak, junction-temperature rise, per unit of internal power dissipation, above the case temperature as measured at the center of the package bottom.

The dc thermal resistance applies when one output transistor is operating continuously. The ac thermal resistance applies with the output transistors conducting alternately at a high enough frequency that the peak capability of neither transistor is exceeded.

Supply current: The current required from the power source to operate the amplifier with the output voltage and current at zero.

Equivalent Schematic (excluding active protection circuitry)



TL/H/8704–29

National Semiconductor

LM101A/LM201A/LM301A Operational Amplifiers

General Description

The LM101A series are general purpose operational amplifiers which feature improved performance over industry standards like the LM709. Advanced processing techniques make possible an order of magnitude reduction in input currents, and a redesign of the biasing circuitry reduces the temperature drift of input current. Improved specifications include:

- Offset voltage 3 mV maximum over temperature (LM101A/LM201A)
- Input current 100 nA maximum over temperature (LM101A/LM201A)
- Offset current 20 nA maximum over temperature (LM101A/LM201A)
- Guaranteed drift characteristics
- Offsets guaranteed over entire common mode and supply voltage ranges
- Slew rate of 10V/μs as a summing amplifier

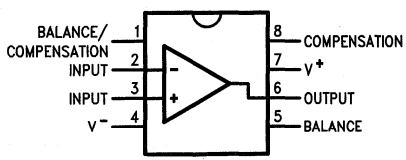
This amplifier offers many features which make its application nearly foolproof: overload protection on the input and output, no latch-up when the common mode range is exceeded, and freedom from oscillations and compensation with a single 30 pF capacitor. It has advantages over internally compensated amplifiers in that the frequency compensation can be tailored to the particular application. For example, in low frequency circuits it can be overcompensated for increased stability margin. Or the compensation can be optimized to give more than a factor of ten improvement in high frequency performance for most applications.

In addition, the device provides better accuracy and lower noise in high impedance circuitry. The low input currents also make it particularly well suited for long interval integrators or timers, sample and hold circuits and low frequency waveform generators. Further, replacing circuits where matched transistor pairs buffer the inputs of conventional IC op amps, it can give lower offset voltage and a drift at a lower cost.

The LM101A is guaranteed over a temperature range of −55°C to +125°C, the LM201A from −25°C to +85°C, and the LM301A from 0°C to +70°C.

Connection Diagrams (Top View)

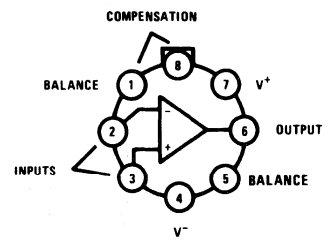
Dual-In-Line Package



TL/H/7752–4

Order Number LM101AJ, LM101J/883*, LM301AJ, LM201AN or LM301AN
See NS Package Number J08A or N08A

Metal Can Package

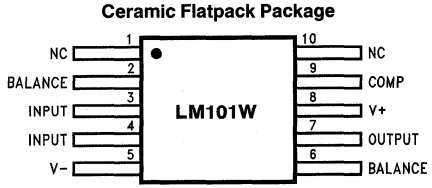


TL/H/7752–2

Note: Pin 4 connected to case.

Order Number LM101AH, LM101AH/883*, LM201AH or LM301AH
See NS Package Number H08C

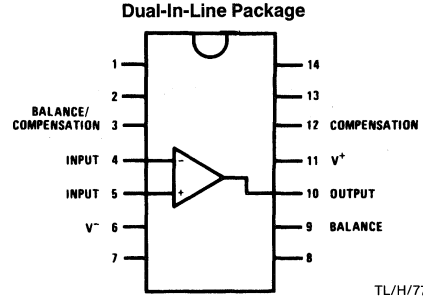
Ceramic Flatpack Package



TL/H/7752–4

Order Number LM101AW/883 or LM101W/883
See NS Package Number W10A

Dual-In-Line Package



TL/H/7752–3

Order Number LM101AJ-14/883*
See NS Package Number J14A

*Available per JM38510/10103.

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

	LM101A/LM201A	LM301A
Supply Voltage	±22V	±18V
Differential Input Voltage	±30V	±30V
Input Voltage (Note 1)	±15V	±15V
Output Short Circuit Duration (Note 2)	Continuous	Continuous
Operating Ambient Temp. Range	−55°C to +125°C (LM101A) −25°C to +85°C (LM201A)	0°C to +70°C
T_J Max		
H-Package	150°C	100°C
N-Package	150°C	100°C
J-Package	150°C	100°C
Power Dissipation at T_A = 25°C		
H-Package (Still Air)	500 mW	300 mW
(400 LF/Min Air Flow)	1200 mW	700 mW
N-Package	900 mW	500 mW
J-Package	1000 mW	650 mW
Thermal Resistance (Typical) θ_{jA}		
H-Package (Still Air)	165°C/W	165°C/W
(400 LF/Min Air Flow)	67°C/W	67°C/W
N Package	135°C/W	135°C/W
J-Package	110°C/W	110°CmW
(Typical) θ_{jC}		
H-Package	25°C/W	25°C/W
Storage Temperature Range	−65°C to +150°C	−65°C to +150°C
Lead Temperature (Soldering, 10 sec.)		
Metal Can or Ceramic	300°C	300°C
Plastic	260°C	260°C
ESD Tolerance (Note 5)	2000V	2000V

Electrical Characteristics (Note 3) $T_A = T_J$

Parameter	Conditions		LM101A/LM201A			LM301A			Units
			Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	T_A = 25°C, $R_S \leq 50\ k\Omega$			0.7	2.0		2.0	7.5	mV
Input Offset Current	T_A = 25°C			1.5	10		3.0	50	nA
Input Bias Current	T_A = 25°C			30	75		70	250	nA
Input Resistance	T_A = 25°C		1.5	4.0		0.5	2.0		MΩ
Supply Current	T_A = 25°C	V_S = ±20V		1.8	3.0				mA
		V_S = ±15V					1.8	3.0	mA
Large Signal Voltage Gain	T_A = 25°C, V_S = ±15V V_{OUT} = ±10V, $R_L \geq 2\ k\Omega$		50	160		25	160		V/mV
Input Offset Voltage	$R_S \leq 50\ k\Omega$				3.0			10	mV
Average Temperature Coefficient of Input Offset Voltage	$R_S \leq 50\ k\Omega$			3.0	15		6.0	30	µV/°C
Input Offset Current					20			70	nA
Average Temperature Coefficient of Input Offset Current	25°C ≤ $T_A \leq T_{MAX}$			0.01	0.1		0.01	0.3	nA/°C
	$T_{MIN} \leq T_A \leq$ 25°C			0.02	0.2		0.02	0.6	nA/°C

Electrical Characteristics (Note 3) $T_A = T_J$ (Continued)

Parameter	Conditions		LM101A/LM201A			LM301A			Units
			Min	Typ	Max	Min	Typ	Max	
Input Bias Current					0.1			0.3	μA
Supply Current	$T_A = T_{MAX}$, $V_S = \pm 20V$			1.2	2.5				mA
Large Signal Voltage Gain	$V_S = \pm 15V$, $V_{OUT} = \pm 10V$ $R_L \geq 2k$		25			15			V/mV
Output Voltage Swing	$V_S = \pm 15V$	$R_L = 10\ k\Omega$	±12	±14		±12	±14		V
		$R_L = 2\ k\Omega$	±10	±13		±10	±13		V
Input Voltage Range	$V_S = \pm 20V$		±15						V
	$V_S = \pm 15V$			+15, −13		±12	+15, −13		V
Common-Mode Rejection Ratio	$R_S \leq 50\ k\Omega$		80	96		70	90		dB
Supply Voltage Rejection Ratio	$R_S \leq 50\ k\Omega$		80	96		70	96		dB

Note 1: For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

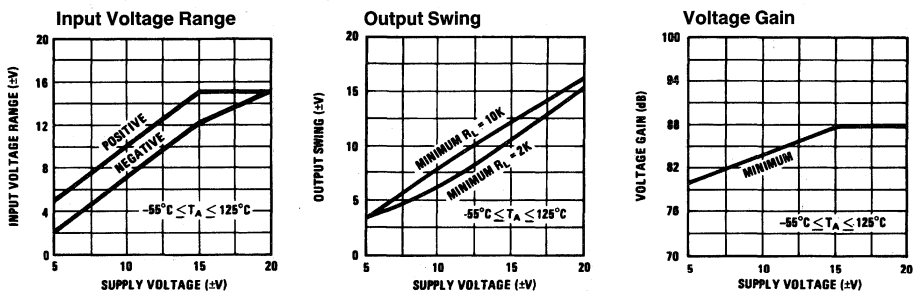
Note 2: Continuous short circuit is allowed for case temperatures to 125°C and ambient temperatures to 75°C for LM101A/LM201A, and 70°C and 55°C respectively for LM301A.

Note 3: Unless otherwise specified, these specifications apply for C1 = 30 pF, $\pm 5V \leq V_S \leq \pm 20V$ and $-55°C \leq T_A \leq +125°C$ (LM101A), $\pm 5V \leq V_S \leq \pm 20V$ and $-25°C \leq T_A \leq +85°C$ (LM201A), $\pm 5V \leq V_S \leq \pm 15V$ and $0°C \leq T_A \leq +70°C$ (LM301A).

Note 4: Refer to RETS101AX for LM101A military specifications and RETS101X for LM101 military specifications.

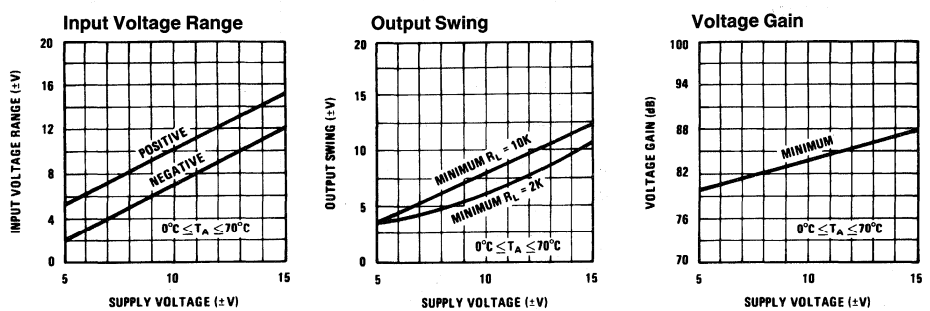
Note 5: Human body model, 100 pF discharged through 1.5 kΩ.

Guaranteed Performance Characteristics LM101A/LM201A



TL/H/7752–5

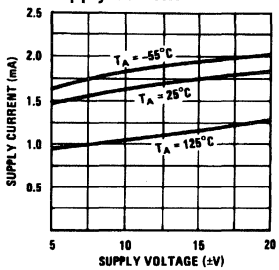
Guaranteed Performance Characteristics LM301A



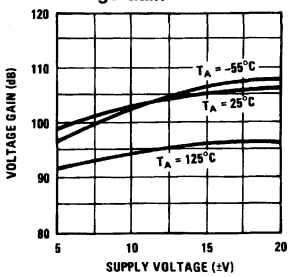
TL/H/7752–6

Typical Performance Characteristics

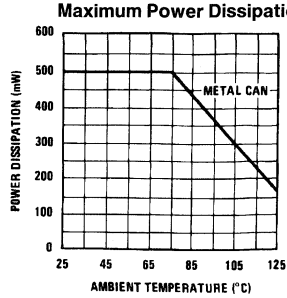
Supply Current



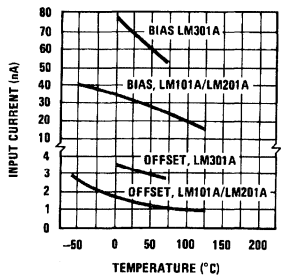
Voltage Gain



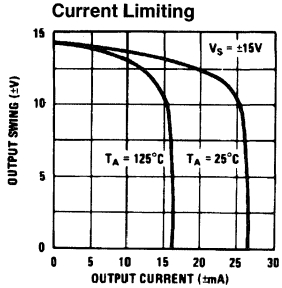
Maximum Power Dissipation



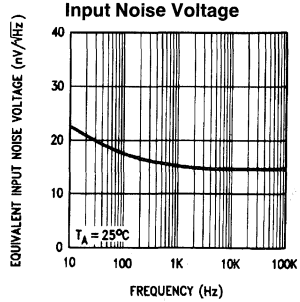
Input Current, LM101A/LM201A/LM301A



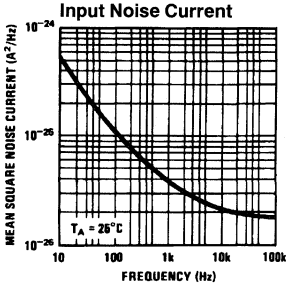
Current Limiting



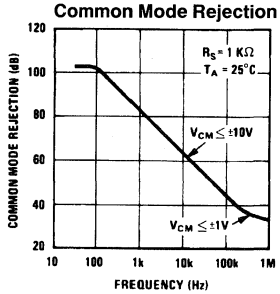
Input Noise Voltage



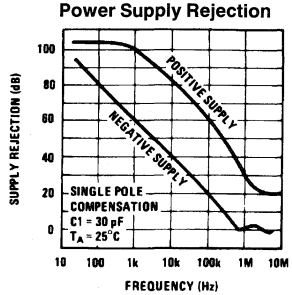
Input Noise Current



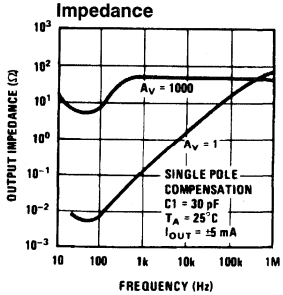
Common Mode Rejection



Power Supply Rejection



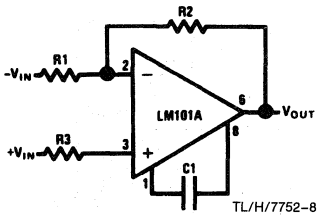
Closed Loop Output Impedance



TL/H/7752–7

Typical Performance Characteristics for Various Compensation Circuits**

Single Pole Compensation

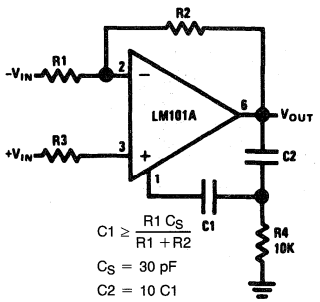


TL/H/7752-8

$$C1 \geq \frac{R1\ C_S}{R1 + R2}$$

C_S = 30 pF

Two Pole Compensation



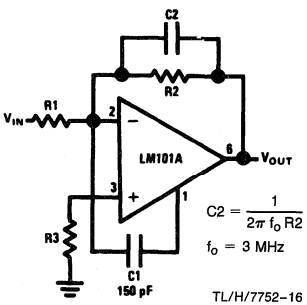
$$C1 \geq \frac{R1\ C_S}{R1 + R2}$$

C_S = 30 pF

C2 = 10 C1

TL/H/7752-12

Feedforward Compensation

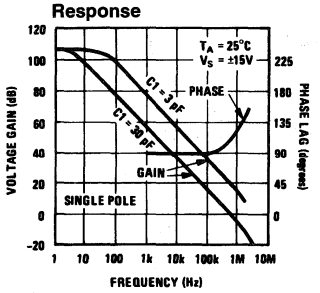


$$C2 = \frac{1}{2\pi\ f_o\ R2}$$

f_o = 3 MHz

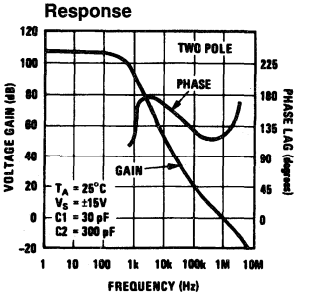
TL/H/7752-16

Open Loop Frequency Response



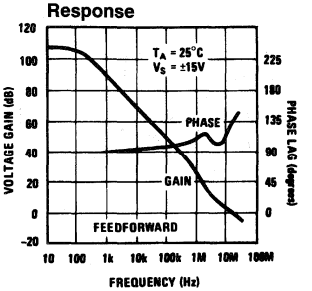
TL/H/7752-9

Open Loop Frequency Response



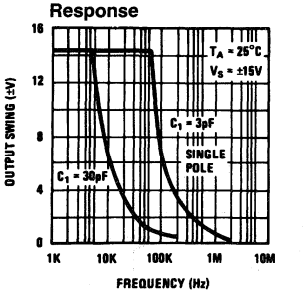
TL/H/7752-13

Open Loop Frequency Response



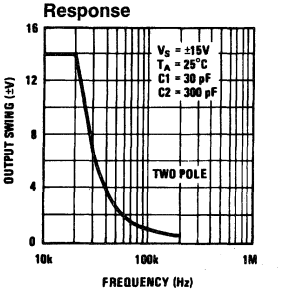
TL/H/7752-17

Large Signal Frequency Response



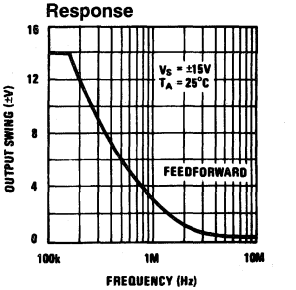
TL/H/7752-10

Large Signal Frequency Response



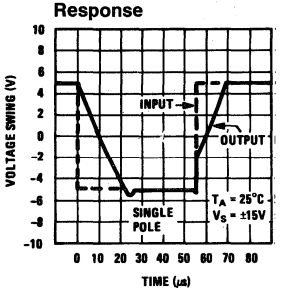
TL/H/7752-14

Large Signal Frequency Response



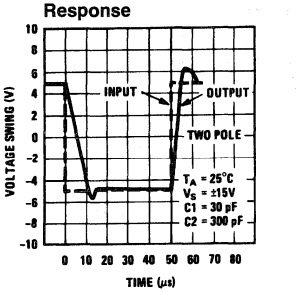
TL/H/7752-18

Voltage Follower Pulse Response



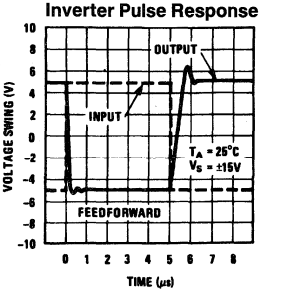
TL/H/7752-11

Voltage Follower Pulse Response



TL/H/7752-15

Inverter Pulse Response



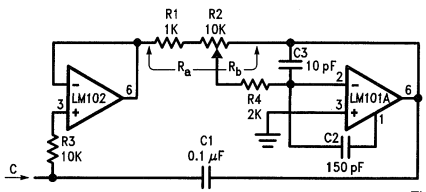
TL/H/7752-19

**Pin connections shown are for 8-pin packages.

Typical Applications**

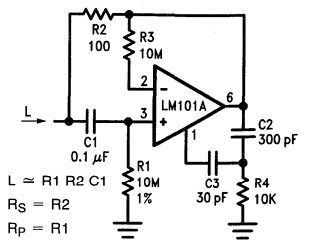
Variable Capacitance Multiplier

$$C = 1 + \frac{R_b}{R_a} C1$$



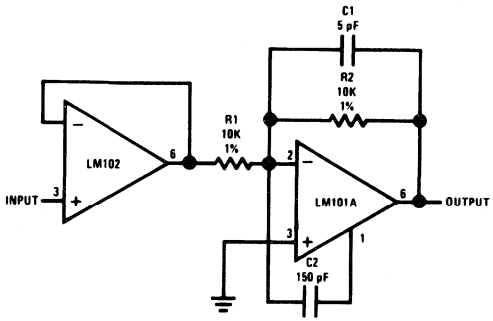
TL/H/7752-20

Simulated Inductor



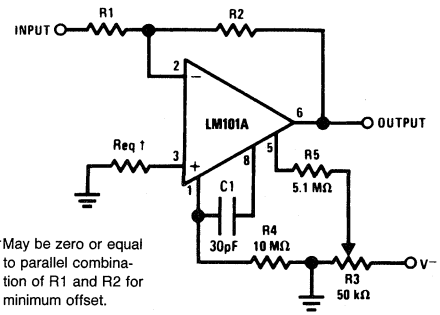
TL/H/7752-21

Fast Inverting Amplifier with High Input Impedance



TL/H/7752-22

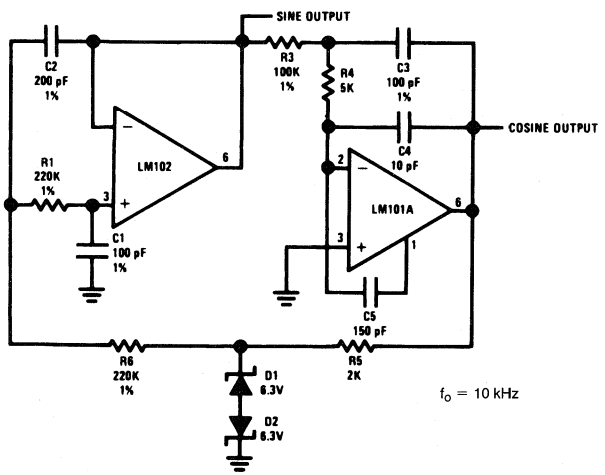
Inverting Amplifier with Balancing Circuit



†May be zero or equal to parallel combination of R1 and R2 for minimum offset.

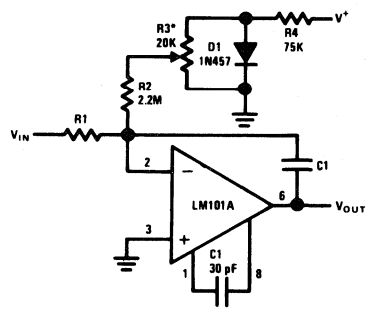
TL/H/7752-23

Sine Wave Oscillator



$f_O = 10$ kHz

Integrator with Bias Current Compensation



TL/H/7752-25

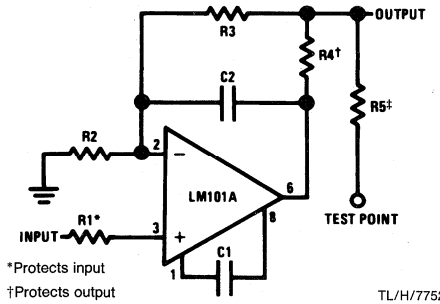
*Adjust for zero integrator drift. Current drift typically 0.1 nA/°C over −55°C to +125°C temperature range.

TL/H/7752-24

**Pin connections shown are for 8-pin packages.

Application Hints**

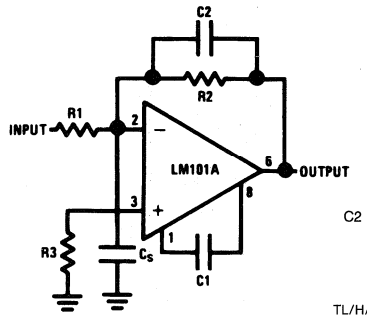
Protecting Against Gross Fault Conditions



*Protects input
†Protects output
‡Protects output—not needed when R4 is used.

TL/H/7752–26

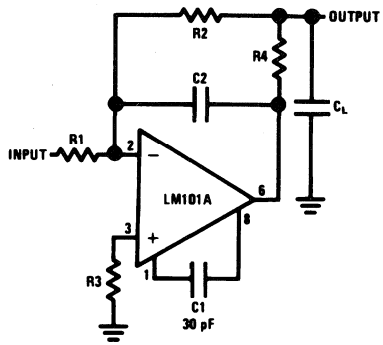
Compensating for Stray Input Capacitances or Large Feedback Resistor



$$C2 = \frac{R1\,C_S}{R2}$$

TL/H/7752–27

Isolating Large Capacitive Loads



TL/H/7752–28

Although the LM101A is designed for trouble free operation, experience has indicated that it is wise to observe certain precautions given below to protect the devices from abnormal operating conditions. It might be pointed out that the advice given here is applicable to practically any IC op amp, although the exact reason why may differ with different devices.

When driving either input from a low-impedance source, a limiting resistor should be placed in series with the input lead to limit the peak instantaneous output current of the source to something less than 100 mA. This is especially important when the inputs go outside a piece of equipment where they could accidentally be connected to high voltage sources. Large capacitors on the input (greater than 0.1 μF) should be treated as a low source impedance and isolated with a resistor. Low impedance sources do not cause a problem unless their output voltage exceeds the supply voltage. However, the supplies go to zero when they are turned off, so the isolation is usually needed.

The output circuitry is protected against damage from shorts to ground. However, when the amplifier output is connected to a test point, it should be isolated by a limiting resistor, as test points frequently get shorted to bad places. Further, when the amplifer drives a load external to the equipment, it is also advisable to use some sort of limiting resistance to preclude mishaps.

Precautions should be taken to insure that the power supplies for the integrated circuit never become reversed—even under transient conditions. With reverse voltages greater than 1V, the IC will conduct excessive current, fusing internal aluminum interconnects. If there is a possibility of this happening, clamp diodes with a high peak current rating should be installed on the supply lines. Reversal of the voltage between V^+ and V^- will always cause a problem, although reversals with respect to ground may also give difficulties in many circuits.

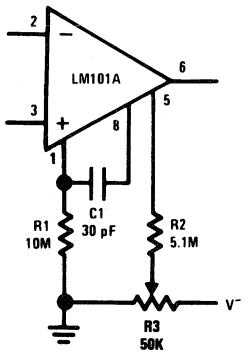
The minimum values given for the frequency compensation capacitor are stable only for source resistances less than 10 kΩ, stray capacitances on the summing junction less than 5 pF and capacitive loads smaller than 100 pF. If any of these conditions are not met, it becomes necessary to overcompensate the amplifier with a larger compensation capacitor. Alternately, lead capacitors can be used in the feedback network to negate the effect of stray capacitance and large feedback resistors or an RC network can be added to isolate capacitive loads.

Although the LM101A is relatively unaffected by supply bypassing, this cannot be ignored altogether. Generally it is necessary to bypass the supplies to ground at least once on every circuit card, and more bypass points may be required if more than five amplifiers are used. When feed-forward compensation is employed, however, it is advisable to bypass the supply leads of each amplifier with low inductance capacitors because of the higher frequencies involved.

**Pin connections shown are for 8-pin packages.

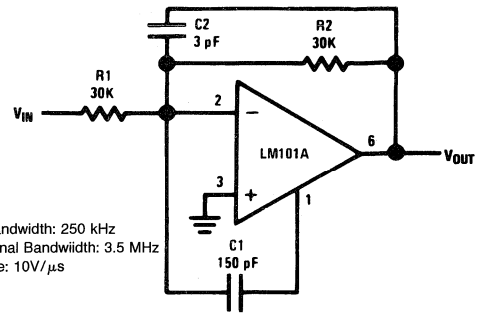
Typical Applications** (Continued)

Standard Compensation and Offset Balancing Circuit



TL/H/7752–29

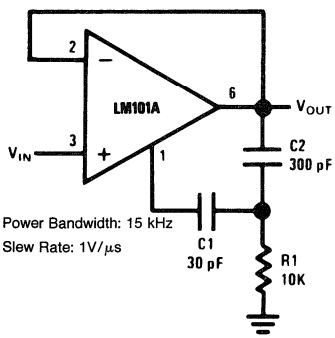
Fast Summing Amplifier



Power Bandwidth: 250 kHz
Small Signal Bandwiidth: 3.5 MHz
Slew Rate: 10V/μs

TL/H/7752–30

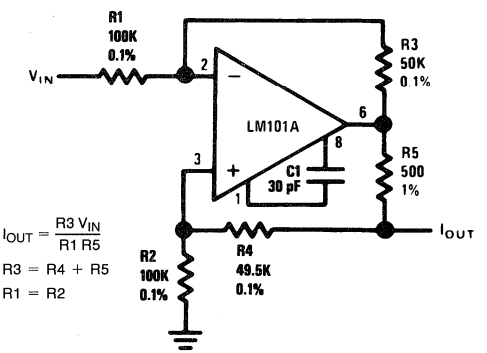
Fast Voltage Follower



Power Bandwidth: 15 kHz
Slew Rate: 1V/μs

TL/H/7752–31

Bilateral Current Source

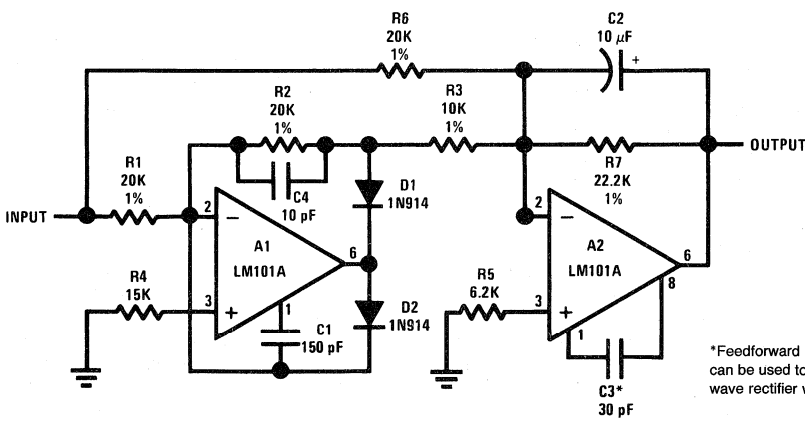


$I_{OUT} = \frac{R3\ V_{IN}}{R1\ R5}$

R3 = R4 + R5
R1 = R2

TL/H/7752–32

Fast AC/DC Converter*



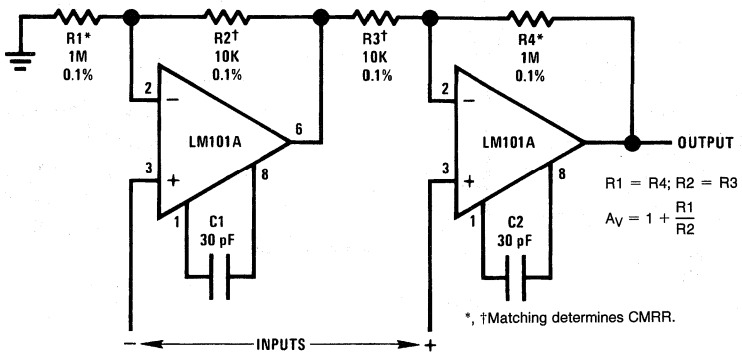
*Feedforward compensation can be used to make a fast full wave rectifier without a filter.

TL/H/7752–33

**Pin connections shown are for 8-pin packages.

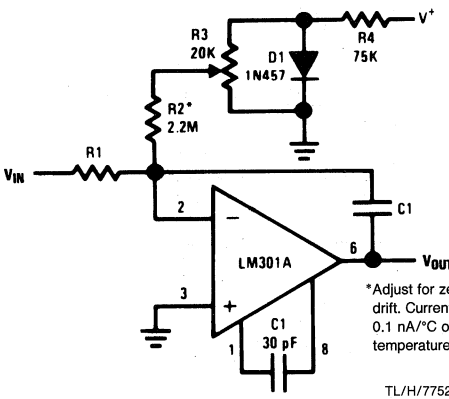
Typical Applications** (Continued)

Instrumentation Amplifier



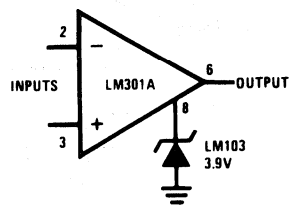
TL/H/7752–34

Integrator with Bias Current Compensation



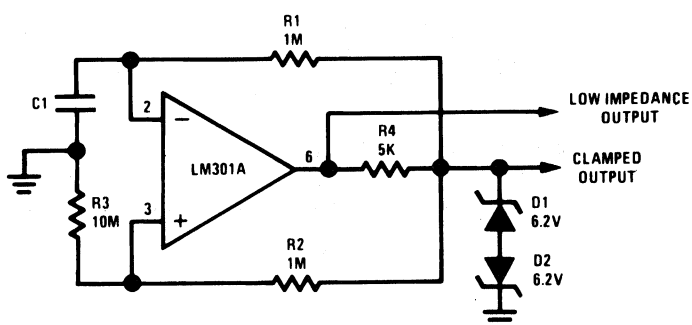
TL/H/7752–35

Voltage Comparator for Driving RTL Logic or High Current Driver



TL/H/7752–37

Low Frequency Square Wave Generator

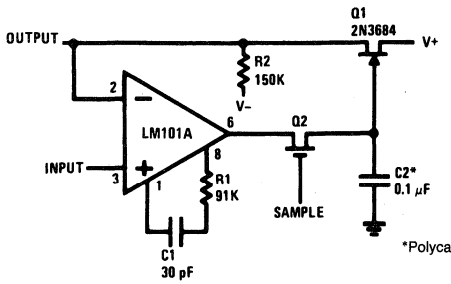


TL/H/7752–36

**Pin connections shown are for 8-pin packages.

Typical Applications** (Continued)

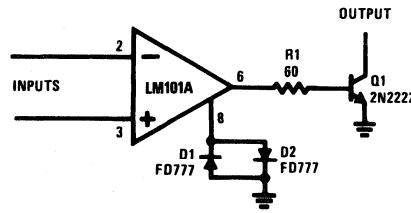
Low Drift Sample and Hold



*Polycarbonate-dielectric capacitor

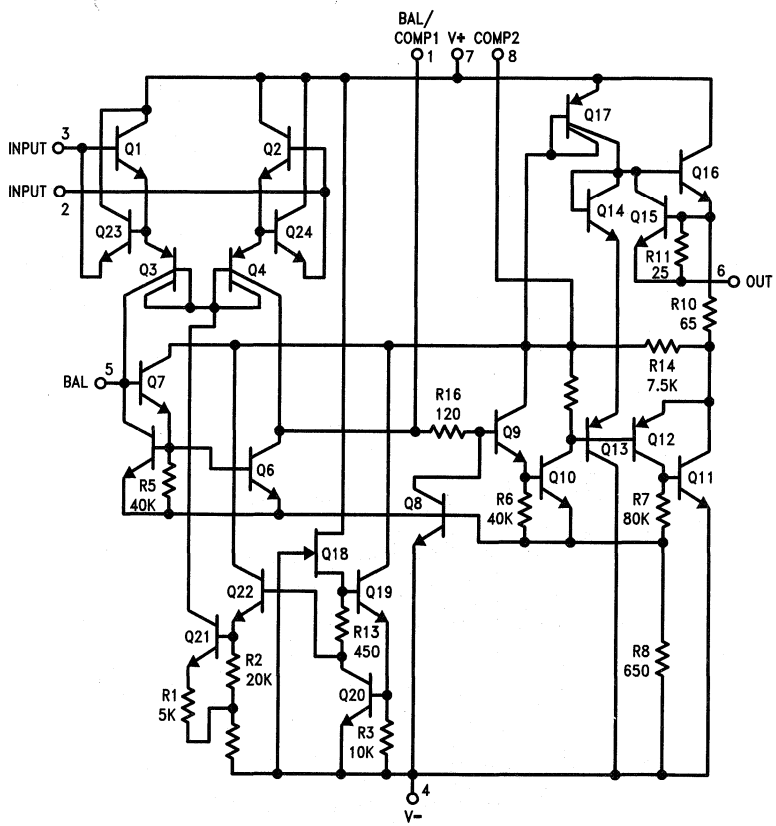
TL/H/7752-38

Voltage Comparator for Driving DTL or TTL Integrated Circuits



TL/H/7752-39

Schematic**



TL/H/7752-1

**Pin connections shown are for 8-pin packages.

National Semiconductor

LM107/LM207/LM307 Operational Amplifiers

General Description

The LM107 series are complete, general purpose operational amplifiers, with the necessary frequency compensation built into the chip. Advanced processing techniques make the input currents a factor of ten lower than industry standards like the 709. Yet, they are a direct, plug-in replacement for the 709, LM101A and 741.

The LM107 series offers the features of the LM101A, which makes its application nearly foolproof. In addition, the device provides better accuracy and lower noise in high impedance circuitry. The low input currents also make it particularly well suited for long interval integrators or timers, sample and hold circuits and low frequency waveform generators. Further, replacing circuits where matched transistor pairs buffer the inputs of conventional IC op amps, it can give lower offset voltage and drift at a lower cost.

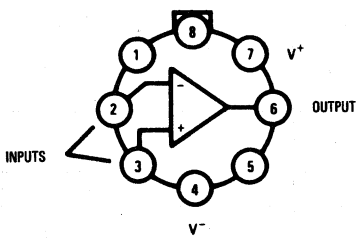
The LM107 is guaranteed over a −55°C to +125°C temperature range, the LM207 from −25°C to +85°C and the LM307 from 0°C to +70°C.

Features

- Offset voltage 3 mV maximum over temperature
- Input current 100 nA maximum over temperature
- Offset current 20 nA maximum over temperature
- Guaranteed drift characteristics

Connection Diagrams

Metal Can Package



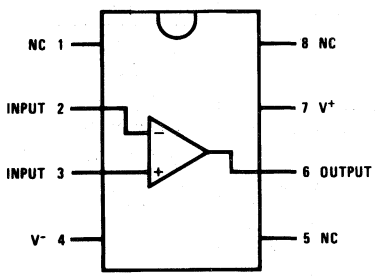
TL/H/7757–2

Note: Pin 4 connected to case.

Top View

Order Number LM107H, LM107H/883,* LM207H or LM307H
See NS Package Number H08C

Dual-in-Line Package



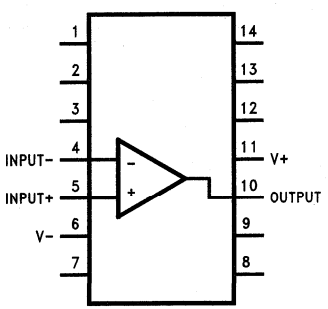
TL/H/7757–3

Top View

Order Number LM107J, LM107J/883,* LM207J or LM307J
See NS Package Number J08A

Order Number LM307N
See NS Package Number N08A

Dual-in-Line Package



TL/H/7757–13

Order Number LM107J-14/883*
See NS Package Number J14A

*Available per SMD# 5962-8958901.

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.
(Note 4)

	LM107/LM207	LM307
Supply Voltage	±22V	±18V
Power Dissipation (Note 1)	500 mW	500 mW
Differential Input Voltage	±30V	±30V
Input Voltage (Note 2)	±15V	±15V
Output Short Circuit Duration	Continuous	Continuous
Operating Temperature Range (T_A)		
(LM107)	−55°C to +125°C	0°C to +70°C
(LM207)	−25°C to +85°C	
Storage Temperature Range	−65°C to +150°C	−65°C to +150°C
Lead Temperature (Soldering, 10 sec)	260°C	260°C

	T_{MIN}	T_{MAX}
LM107	−55°C	+125°C
LM207	−25°C	+85°C
LM307	0°C	+70°C

ESD rating to be determined.

Electrical Characteristics (Note 3)

Parameter	Conditions	LM107/LM207			LM307			Units
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	$T_A = 25°C$, $R_S \leq 50\ k\Omega$		0.7	2.0		2.0	7.5	mV
Input Offset Current	$T_A = 25°C$		1.5	10		3.0	50	nA
Input Bias Current	$T_A = 25°C$		30	75		70	250	nA
Input Resistance	$T_A = 25°C$	1.5	4.0		0.5	2.0		MΩ
Supply Current	$T_A = 25°C$ $V_S = \pm 20V$ $V_S = \pm 15V$		1.8	3.0		1.8	3.0	 mA mA
Large Signal Voltage Gain	$T_A = 25°C$, $V_S = \pm 15V$ $V_{OUT} = \pm 10V$, $R_L \geq 2\ k\Omega$	50	160		25	160		V/mV
Input Offset Voltage	$R_S \leq 50\ k\Omega$			3.0			10	mV
Average Temperature Coefficient of Input Offset Voltage			3.0	15		6.0	30	μV/°C
Input Offset Current				20			70	nA
Average Temperature Coefficient of Input Offset Current	$25°C \leq T_A \leq T_{MAX}$ $T_{MIN} \leq T_A \leq 25°C$		0.01 0.02	0.1 0.2		0.01 0.02	0.3 0.6	nA/°C nA/°C
Input Bias Current				100			300	nA
Supply Current	$T_A = +125°C$, $V_S = \pm 20V$		1.2	2.5				mA

Electrical Characteristics (Note 3) (Continued)

Parameter	Conditions	LM107/LM207			LM307			Units
		Min	Typ	Max	Min	Typ	Max	
Large Signal Voltage Gain	$V_S = \pm 15V$, $V_{OUT} = \pm 10V$ $R_L \geq 2\ k\Omega$	25			15			V/mV
Output Voltage Swing	$V_S = \pm 15V$ $R_L = 10\ k\Omega$ $R_L = 2\ k\Omega$	±12 ±10	±14 ±13		±12 ±10	±14 ±13		V V
Input Voltage Range	$V_S = \pm 20V$ $V_S = \pm 15V$	±15	+15 −13		±12	+15 −13		V V
Common Mode Rejection Ratio	$R_S \leq 50\ k\Omega$	80	96		70	90		dB
Supply Voltage Rejection Ratio	$R_S \leq 50\ k\Omega$	80	96		70	96		dB

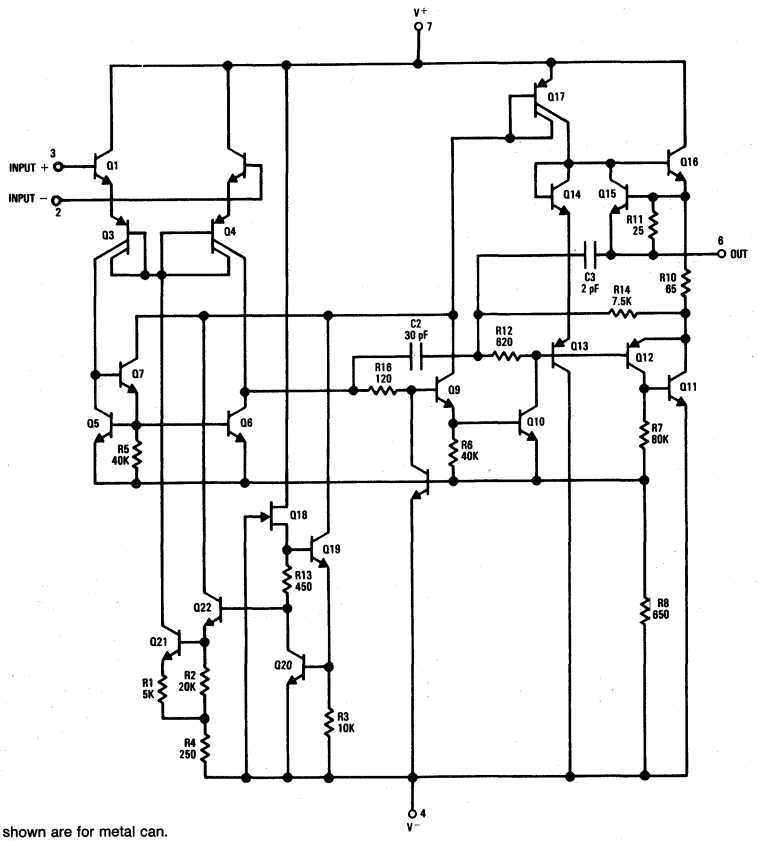
Note 1: The maximum junction temperature of the LM107 is 150°C, and the LM207/LM307 is 100°C. For operating at elevated temperatures, devices in the H08 package must be derated based on a thermal resistance of 165°C/W, junction to ambient, or 30°C/W, junction to case. The thermal resistance of the dual-in-line package is 100°C/W, junction to ambient.

Note 2: For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

Note 3: These specifications apply for $\pm 5V \leq V_S \leq +20V$ and $-55°C \leq T_A \leq +125°C$ for the LM107 or $-25°C \leq T_A +85°C$ for the LM207, and $0°C \leq T_A \leq +70°C$ and $\pm 5V \leq V_S \leq \pm 15V$ for the LM307 unless otherwise specified.

Note 4: Refer to RETS107X for LM107H and LM107J military specifications.

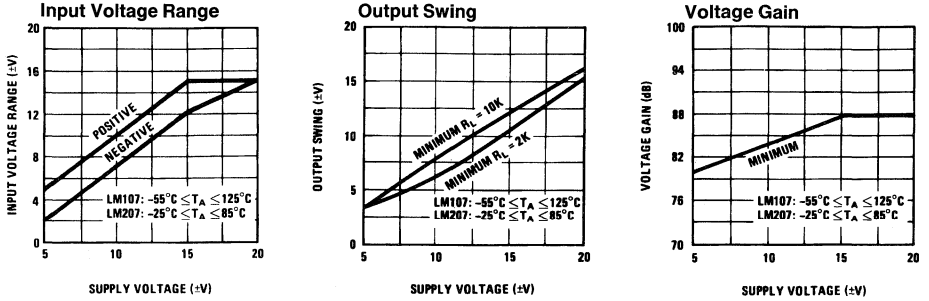
Schematic Diagram*



*Pin connections shown are for metal can.

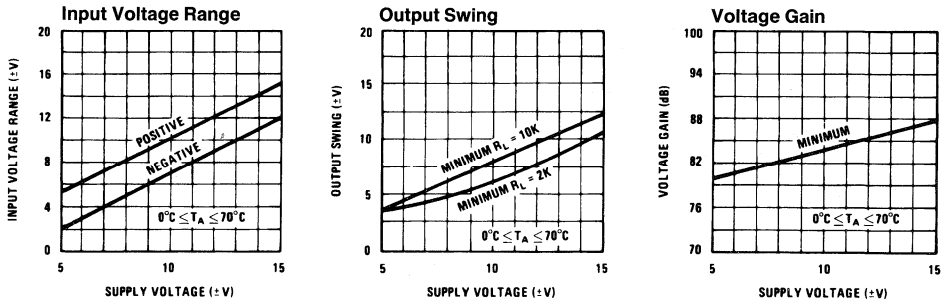
TL/H/7757–1

Guaranteed Performance Characteristics LM107/LM207



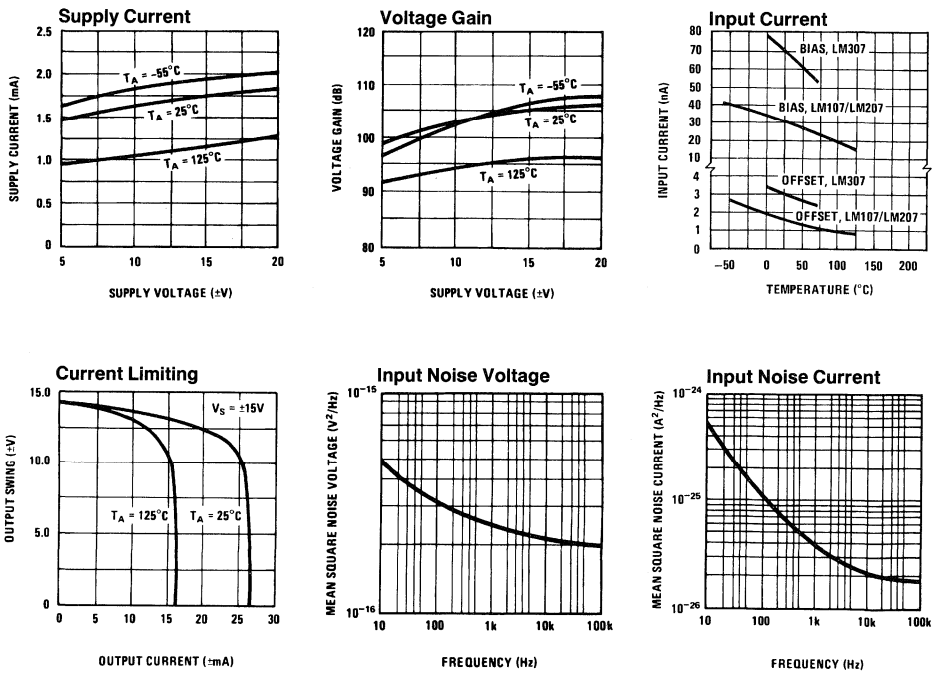
TL/H/7757–4

Guaranteed Performance Characteristics LM307



TL/H/7757–5

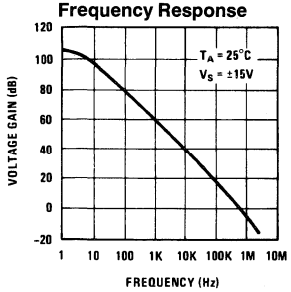
Typical Performance Characteristics



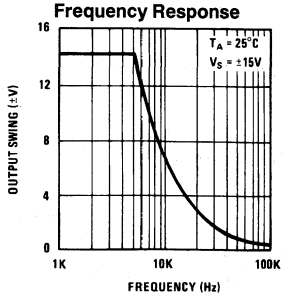
TL/H/7757–6

Typical Performance Characteristics (Continued)

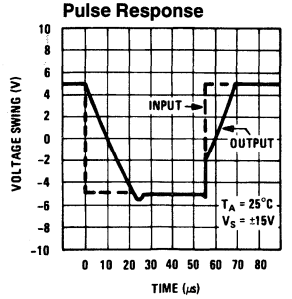
Open Loop Frequency Response



Large Signal Frequency Response



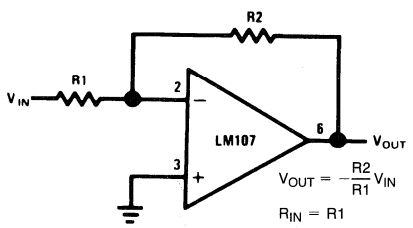
Voltage Follower Pulse Response



TL/H/7757–7

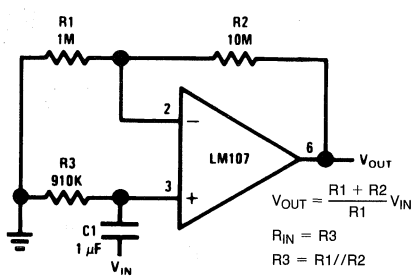
Typical Applications**

Inverting Amplifier



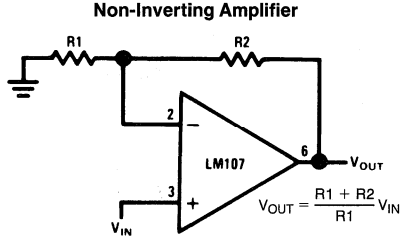
TL/H/7757–8

Non-Inverting AC Amplifier



TL/H/7757–9

Non-Inverting Amplifier

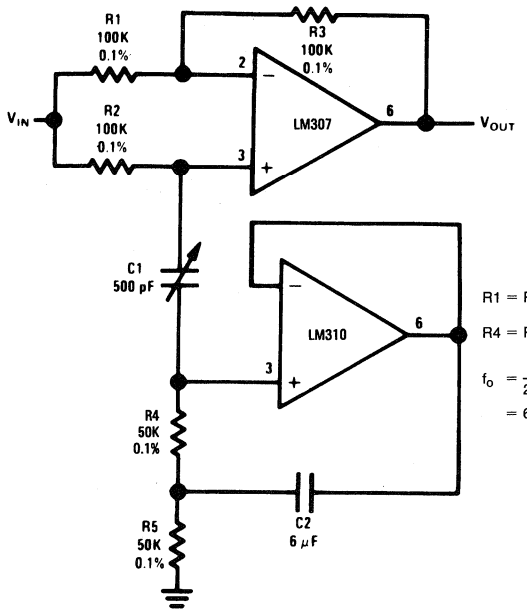


TL/H/7757–10

**Pin connections shown are for metal can.

Typical Applications** (Continued)

Turntable Notch Filter



$R1 = R2 = R3$

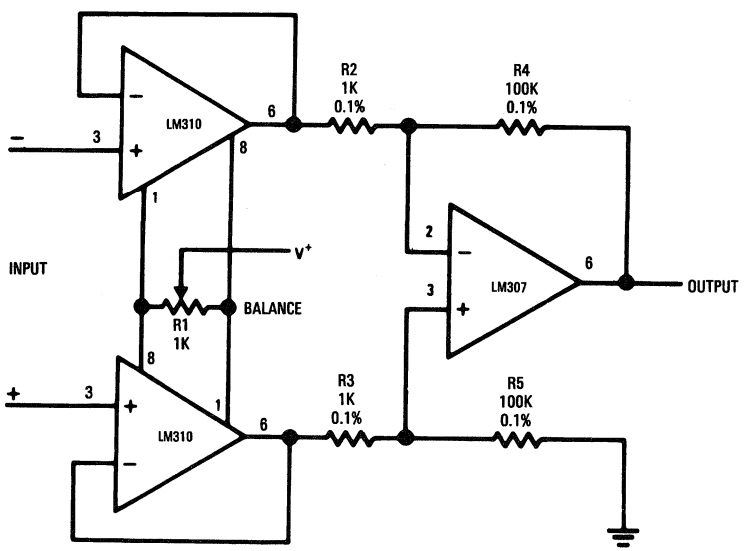
$R4 = R5 = \frac{R1}{2}$

$f_o = \frac{1}{2\pi\sqrt{C_1 C_2 R_4 R_5}}$

$= 60\ Hz$

TL/H/7757–11

Differential Input Instrumentation Amplifier



TL/H/7757–12

**Pin connections shown are for metal can.

National Semiconductor

LM108/LM208/LM308 Operational Amplifiers

General Description

The LM108 series are precision operational amplifiers having specifications a factor of ten better than FET amplifiers over a −55°C to +125°C temperature range.

The devices operate with supply voltages from ±2V to ±20V and have sufficient supply rejection to use unregulated supplies. Although the circuit is interchangeable with and uses the same compensation as the LM101A, an alternate compensation scheme can be used to make it particularly insensitive to power supply noise and to make supply bypass capacitors unnecessary.

The low current error of the LM108 series makes possible many designs that are not practical with conventional amplifiers. In fact, it operates from 10 MΩ source resistances, introducing less error than devices like the 709 with 10 kΩ sources. Integrators with drifts less than 500 μV/sec and analog time delays in excess of one hour can be made using capacitors no larger than 1 μF.

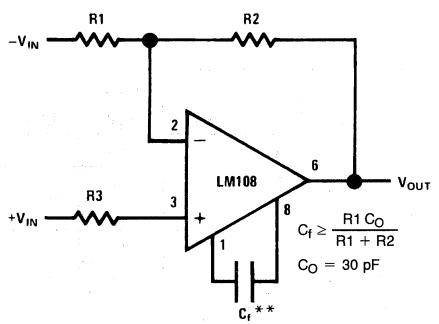
The LM108 is guaranteed from −55°C to +125°C, the LM208 from −25°C to +85°C, and the LM308 from 0°C to +70°C.

Features

- Maximum input bias current of 3.0 nA over temperature
- Offset current less than 400 pA over temperature
- Supply current of only 300 μA, even in saturation
- Guaranteed drift characteristics

Compensation Circuits

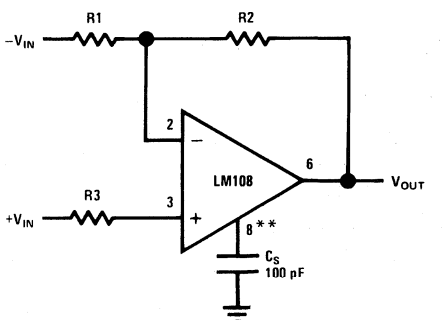
Standard Compensation Circuit



TL/H/7758–1

**Bandwidth and slew rate are proportional to $1/C_f$

Alternate* Frequency Compensation

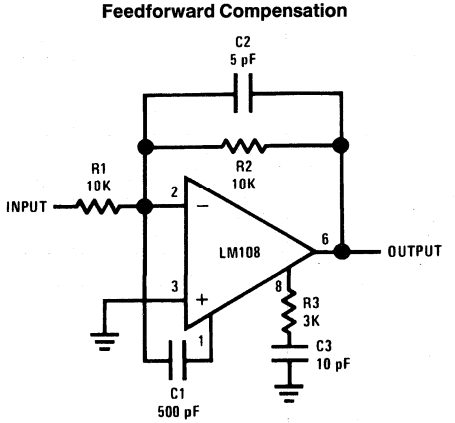


TL/H/7758–2

*Improves rejection of power supply noise by a factor of ten.

**Bandwidth and slew rate are proportional to $1/C_S$

Feedforward Compensation



TL/H/7758–3

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.
(Note 5)

	LM108/LM208	LM308
Supply Voltage	±20V	±18V
Power Dissipation (Note 1)	500 mW	500 mW
Differential Input Current (Note 2)	±10 mA	±10 mA
Input Voltage (Note 3)	±15V	±15V
Output Short-Circuit Duration	Continuous	Continuous
Operating Temperature Range (LM108)	−55°C to +125°C	0°C to +70°C
(LM208)	−25°C to + 85°C	
Storage Temperature Range	−65°C to +150°C	−65°C to +150°C
Lead Temperature (Soldering, 10 sec)		
DIP	260°C	260°C
H Package Lead Temp		
(Soldering 10 seconds)	300°C	300°C
Soldering Information		
Dual-In-Line Package		
Soldering (10 seconds)	260°C	
Small Outline Package		
Vapor Phase (60 seconds)	215°C	
Infrared (15 seconds)	220°C	
See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.		
ESD Tolerance (Note 6)	2000V	

Electrical Characteristics (Note 4)

Parameter	Condition	LM108/LM208			LM308			Units
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	$T_A = 25°C$		0.7	2.0		2.0	7.5	mV
Input Offset Current	$T_A = 25°C$		0.05	0.2		0.2	1	nA
Input Bias Current	$T_A = 25°C$		0.8	2.0		1.5	7	nA
Input Resistance	$T_A = 25°C$	30	70		10	40		MΩ
Supply Current	$T_A = 25°C$		0.3	0.6		0.3	0.8	mA
Large Signal Voltage Gain	$T_A = 25°C$, $V_S = \pm 15V$ $V_{OUT} = \pm 10V$, $R_L \geq 10\ k\Omega$	50	300		25	300		V/mV
Input Offset Voltage				3.0			10	mV
Average Temperature Coefficient of Input Offset Voltage			3.0	15		6.0	30	μV/°C
Input Offset Current				0.4			1.5	nA
Average Temperature Coefficient of Input Offset Current			0.5	2.5		2.0	10	pA/°C
Input Bias Current				3.0			10	nA
Supply Current	$T_A = +125°C$		0.15	0.4				mA
Large Signal Voltage Gain	$V_S = \pm 15V$, $V_{OUT} = \pm 10V$ $R_L \geq 10\ k\Omega$	25			15			V/mV
Output Voltage Swing	$V_S = \pm 15V$, $R_L = 10\ k\Omega$	±13	±14		±13	±14		V

Electrical Characteristics (Note 4) (Continued)

Parameter	Condition	LM108/LM208			LM308			Units
		Min	Typ	Max	Min	Typ	Max	
Input Voltage Range	$V_S = \pm 15V$	±13.5			±14			V
Common Mode Rejection Ratio		85	100		80	100		dB
Supply Voltage Rejection Ratio		80	96		80	96		dB

Note 1: The maximum junction temperature of the LM108 is 150°C, for the LM208, 100°C and for the LM308, 85°C. For operating at elevated temperatures, devices in the H08 package must be derated based on a thermal resistance of 160°C/W, junction to ambient, or 20°C/W, junction to case. The thermal resistance of the dual-in-line package is 100°C/W, junction to ambient.

Note 2: The inputs are shunted with back-to-back diodes for overvoltage protection. Therefore, excessive current will flow if a differential input voltage in excess of 1V is applied between the inputs unless some limiting resistance is used.

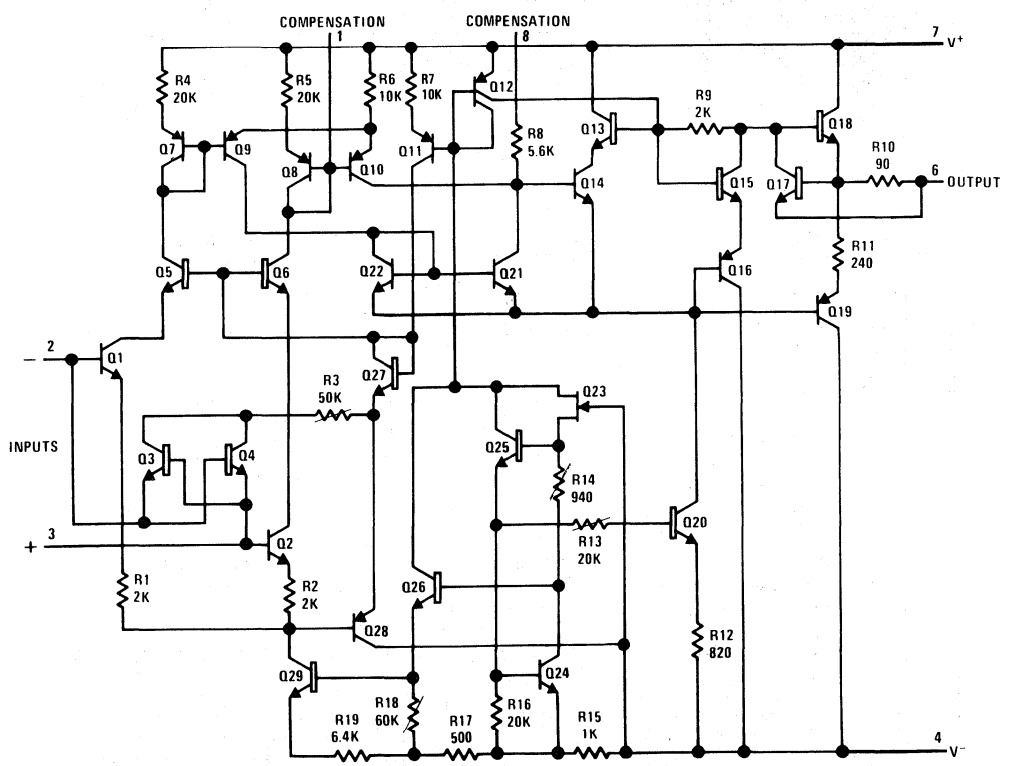
Note 3: For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

Note 4: These specifications apply for $\pm 5V \leq V_S \leq \pm 20V$ and $-55°C \leq T_A \leq +125°C$, unless otherwise specified. With the LM208, however, all temperature specifications are limited to $-25°C \leq T_A \leq 85°C$, and for the LM308 they are limited to $0°C \leq T_A \leq 70°C$.

Note 5: Refer to RETS108X for LM108 military specifications and RETs 108AX for LM108A military specifications.

Note 6: Human body model, 1.5 kΩ in series with 100 pF.

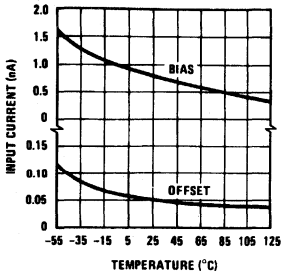
Schematic Diagram



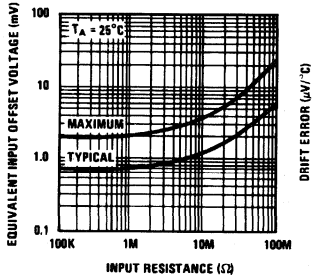
TL/H/7758–8

Typical Performance Characteristics LM108/LM208

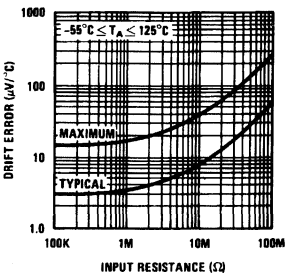
Input Currents



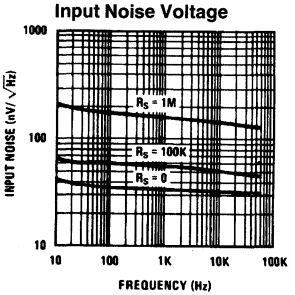
Offset Error



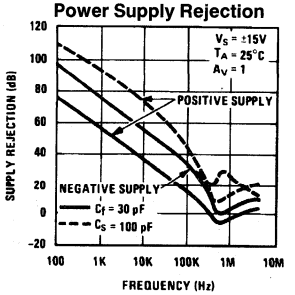
Drift Error



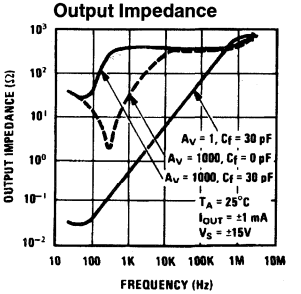
Input Noise Voltage



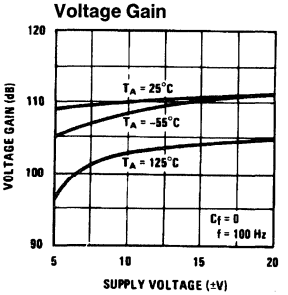
Power Supply Rejection



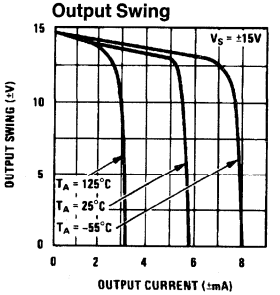
Closed Loop Output Impedance



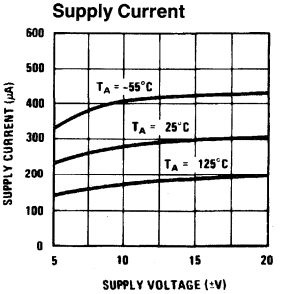
Voltage Gain



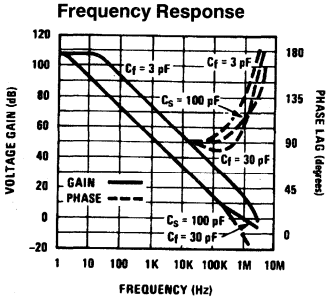
Output Swing



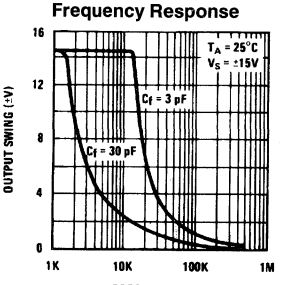
Supply Current



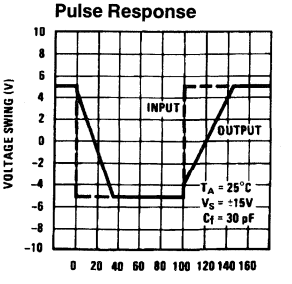
Open Loop Frequency Response



Large Signal Frequency Response



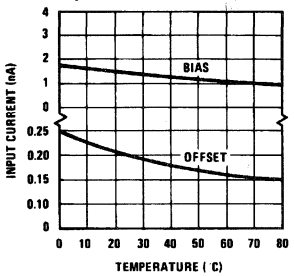
Voltage Follower Pulse Response



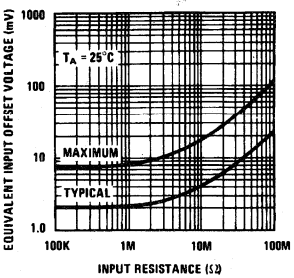
TL/H/7758–6

Typical Performance Characteristics LM308

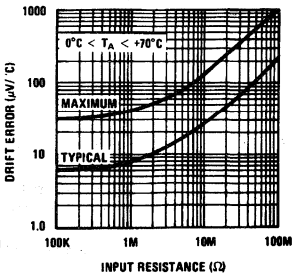
Input Currents



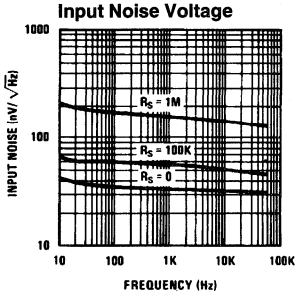
Offset Error



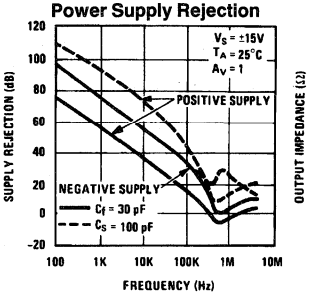
Drift Error



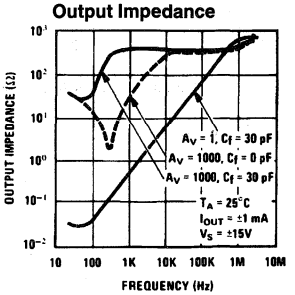
Input Noise Voltage



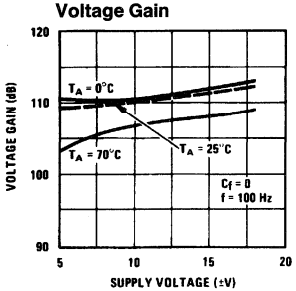
Power Supply Rejection



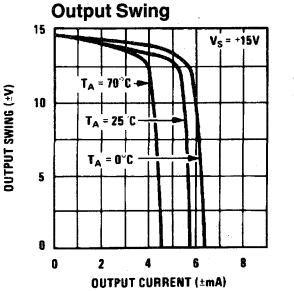
Closed Loop Output Impedance



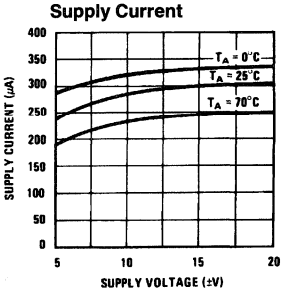
Voltage Gain



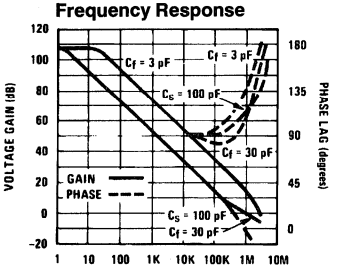
Output Swing



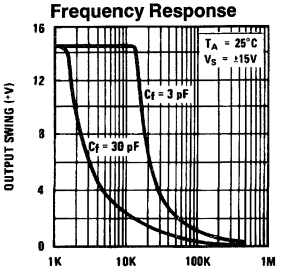
Supply Current



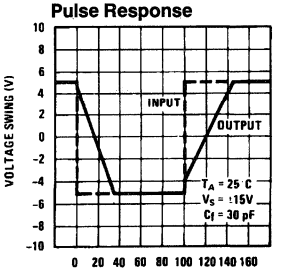
Open Loop Frequency Response



Large Signal Frequency Response



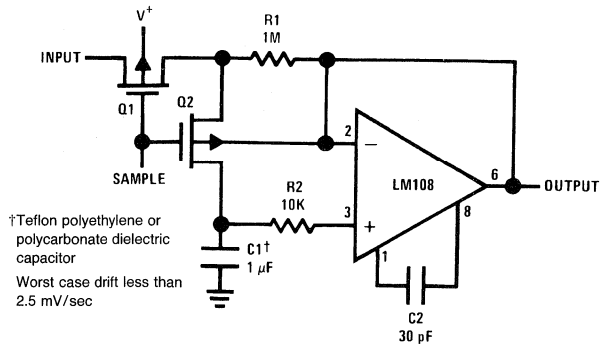
Voltage Follower Pulse Response



TL/H/7758–7

Typical Applications

Sample and Hold

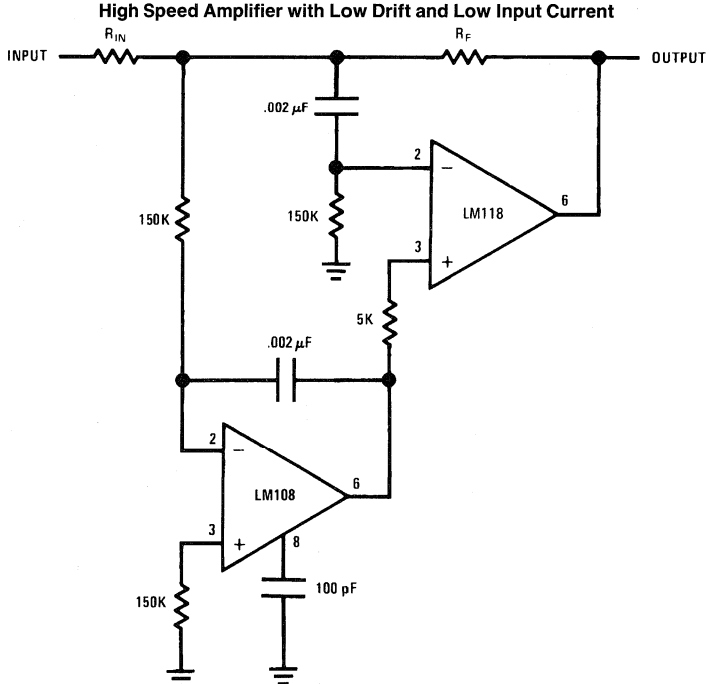


†Teflon polyethylene or polycarbonate dielectric capacitor

Worst case drift less than 2.5 mV/sec

TL/H/7758–4

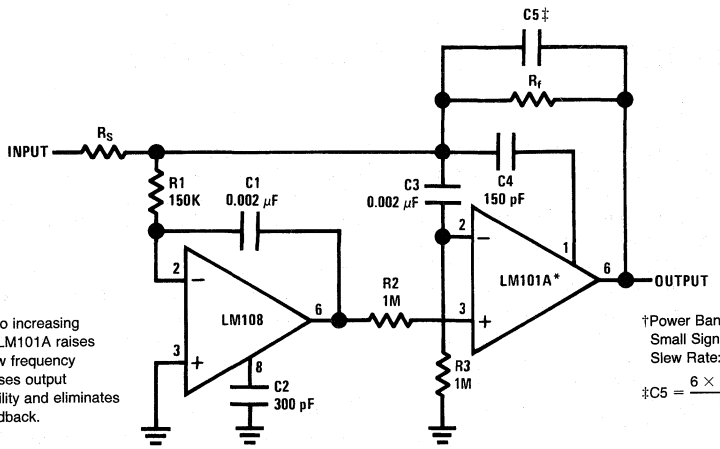
High Speed Amplifier with Low Drift and Low Input Current



TL/H/7758–5

Typical Applications (Continued)

Fast† Summing Amplifier



*In addition to increasing speed, the LM101A raises high and low frequency gain, increases output drive capability and eliminates thermal feedback.

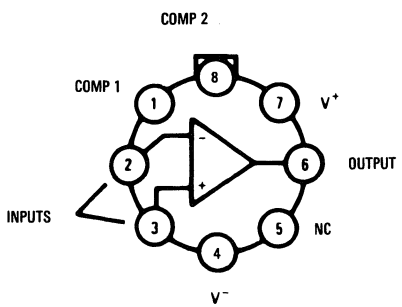
†Power Bandwidth: 250 KHz
Small Signal Bandwidth: 3.5 MHz
Slew Rate: 10V/μS

$$\ddagger C5 = \frac{6 \times 10^{-8}}{R_f}$$

TL/H/7758–12

Connection Diagrams

Metal Can Package

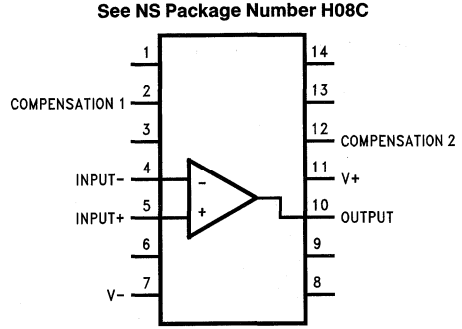


TL/H/7758–13

*Package is connected to Pin 4 (V−)

**Unused pin (no internal connection) to allow for input anti-leakage guard ring on printed circuit board layout.

Order Number LM108H, LM108AH/883†, LM108H/883, LM208H, LM308AH or LM308H
See NS Package Number H08C

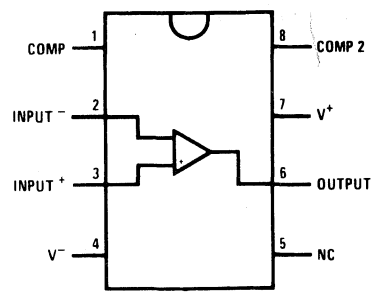


TL/H/7758–16

Top View

Order Number LM108AJ/883† or LM108J/883
See NS Package Number J14A

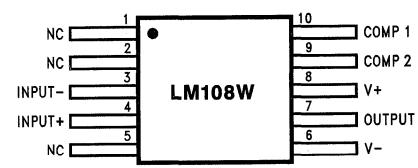
Dual-In-Line Package



TL/H/7758–15

Top View

Order Number LM108J-8, LM108AJ-8/883†, LM108J-8/883, LM308J-8, LM308M or LM308N
See NS Package Number J08A, M08A or N08E



TL/H/7758–17

Order Number LM108AW/883† or LM108W/883
See NS Package Number W10A

†Also available per JM38510/10104

1

National Semiconductor

LM112/LM212/LM312 Operational Amplifiers

General Description

The LM112 series are micropower operational amplifiers with very low offset-voltage and input-current errors—at least a factor of ten better than FET amplifiers over a −55°C to +125°C temperature range. Similar to the LM108 series, that also use supergain transistors, they differ in that they include internal frequency compensation and have provisions for offset adjustment with a single potentiometer.

These amplifiers will operate on supply voltages of ±2V to ±20V, drawing a quiescent current of only 300 μA. Performance is not appreciably affected over this range of voltages, so operation from unregulated power sources is easily accomplished. They can also be run from a single supply like the 5V used for digital circuits.

The LM112 series are the first IC amplifiers to improve reliability by including overvoltage protection for the MOS compensation capacitor. Without this feature, IC's have been known to suffer catastrophic failure caused by short-duration overvoltage spikes on the supplies. Unlike other internally-compensated IC amplifiers, it is possible to overcompensate with an external capacitor to increase stability margin.

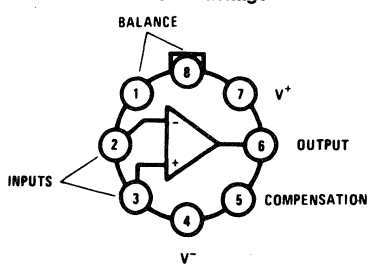
The LM212 is identical to the LM112, except that the LM212 has its performance guaranteed over a −25°C to +85°C temperature range instead of −55°C to +125°C. The LM312 is guaranteed over a 0°C to +70°C temperature range.

Features

- Maximum input bias current of 3 nA over temperature
- Offset current less than 400 pA over temperature
- Low noise
- Guaranteed drift specifications

Connection Diagram

Metal Can Package



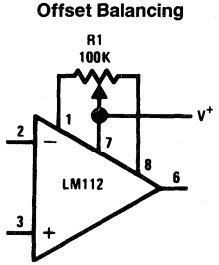
TL/H/7751–4

Top View

Order Number LM112H, LM212H, LM312H or LM112H/883
See NS Package Number H08C

Auxiliary Circuits

Offset Balancing



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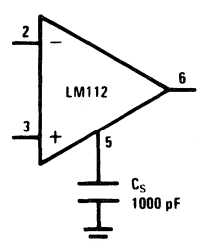
Overcompensation for Greater Stability Margin



TL/H/7751–3

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.
(Note 5)

	LM112/LM212	LM312
Supply Voltage	±20V	±18V
Power Dissipation (Note 1)	500 mW	500 mW
Differential Input Current (Note 2)	±10 mA	±10 mA
Input Voltage (Note 3)	±15V	±15V
Output Short-Circuit Duration	Continuous	Continuous
Operating Temperature Range		
LM112	−55°C to +125°C	0°C to +70°C
LM212	−25°C to +85°C	
Storage Temperature Range	−65°C to +150°C	−65°C to +150°C
Lead Temperature (Soldering, 10 sec.)	300°C	300°C

ESD rating to be determined.

Electrical Characteristics (Note 4)

Parameter	Conditions	LM112/LM212			LM312			Units
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	$T_A = 25°C$		0.7	2.0		2.0	7.5	mV
Input Offset Current	$T_A = 25°C$		0.05	0.2		0.2	1	nA
Input Bias Current	$T_A = 25°C$		0.8	2.0		1.5	7	nA
Input Resistance	$T_A = 25°C$	30	70		10	40		MΩ
Supply Current	$T_A = 25°C$		0.3	0.6		0.3	0.8	mA
Large Signal Voltage Gain	$T_A = 25°C$, $V_S = \pm 15V$ $V_{OUT} = \pm 10V$, $R_L \geq 10\ k\Omega$	50	300		25	300		V/mV
Input Offset Voltage				3.0			10	mV
Average Temperature Coefficient of Input Offset Voltage			3.0	15		6.0	30	μV/°C
Input Offset Current				0.4			1.5	nA
Average Temperature Coefficient of Input Offset Current			0.5	2.5		2.0	10	pA/°C
Input Bias Current				3.0			10	nA
Supply Current	$T_A = 125°C$		0.15	0.4				mA
Large Signal Voltage Gain	$V_S = \pm 15V$, $V_{OUT} = \pm 10V$ $R_L \geq 10\ k\Omega$	25			15			V/mV
Output Voltage Swing	$V_S = \pm 15V$, $R_L = 10\ k\Omega$	±13	±14		±13	±14		V
Input Voltage Range	$V_S = \pm 15V$	±13.5			±14			V
Common-Mode Rejection Ratio		85	100		80	100		dB
Supply Voltage Rejection Ratio		80	96		80	96		dB

Note 1: The maximum junction temperature of the LM112 is 150°C, LM212 is 100°C and LM312 is 85°C. For operating at elevated temperatures, devices in the H08 package must be derated based on a thermal resistance of 160°C/W, junction to ambient, or 20°C/W, junction to case.

Note 2: The inputs are shunted with shunt diodes for overvoltage protection. Therefore, excessive current will flow if a differential input voltage in excess of 1V is applied between the inputs unless some limiting resistance is used.

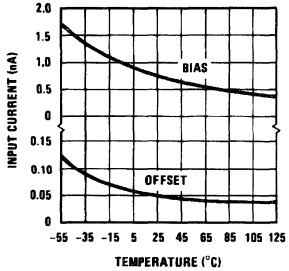
Note 3: For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

Note 4: These specifications apply for $\pm 5V \leq V_S \leq \pm 20V$ and $-55°C \leq T_A \leq +125°C$ (LM112), $-25°C \leq T_A \leq +85°C$ (LM212), $\pm 5V \leq V_S \leq \pm 15V$ and $0°C \leq T_A \leq +70°C$ (LM312) unless otherwise noted.

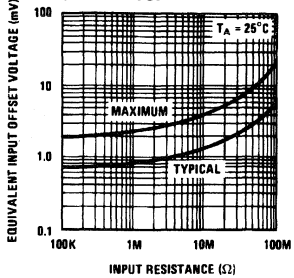
Note 5: Refer to RETS112X for LM112H military specifications.

Typical Performance Characteristics LM112/LM212

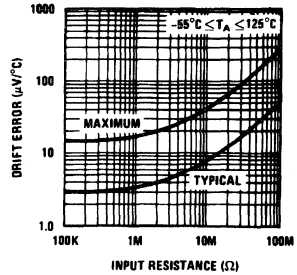
Input Currents



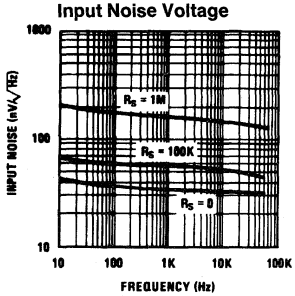
Offset Error



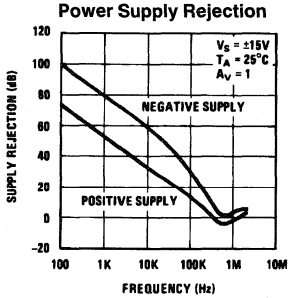
Drift Error



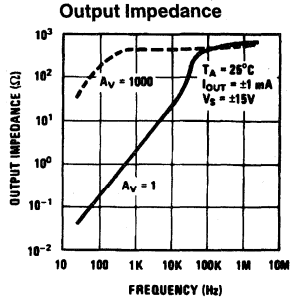
Input Noise Voltage



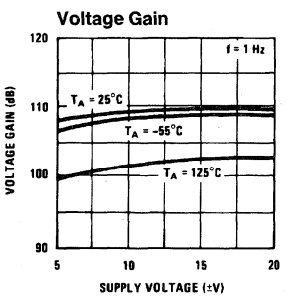
Power Supply Rejection



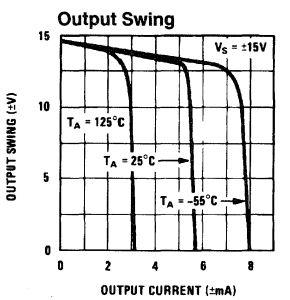
Closed Loop Output Impedance



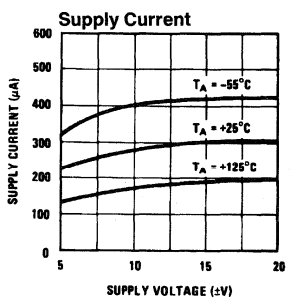
Voltage Gain



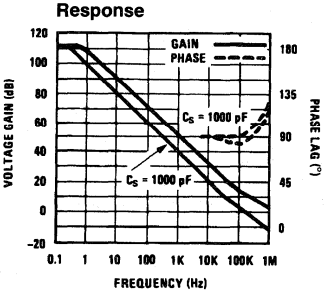
Output Swing



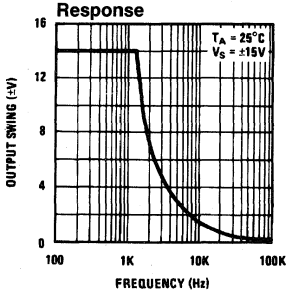
Supply Current



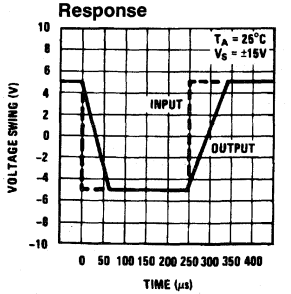
Open Loop Frequency Response



Large Signal Frequency Response



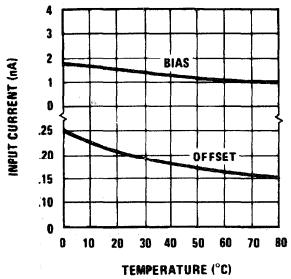
Voltage Follower Pulse Response



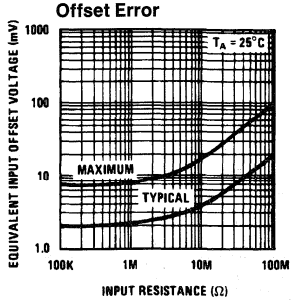
TL/H/7751–5

Typical Performance Characteristics LM312

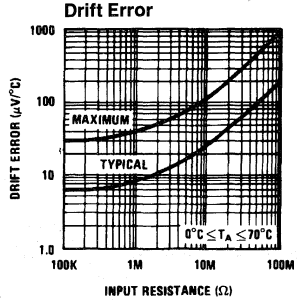
Input Currents



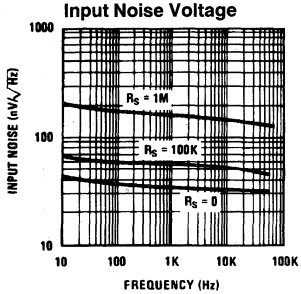
Offset Error



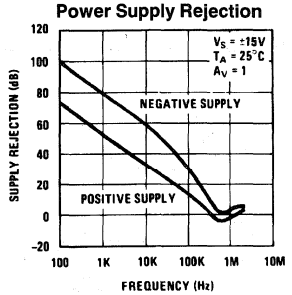
Drift Error



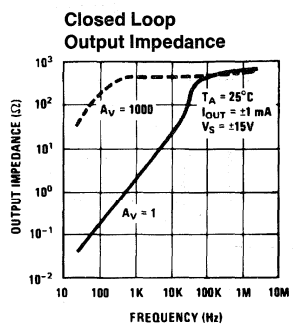
Input Noise Voltage



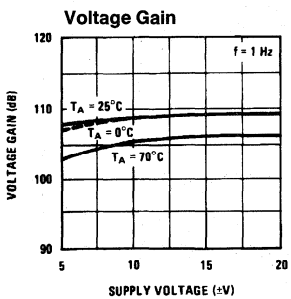
Power Supply Rejection



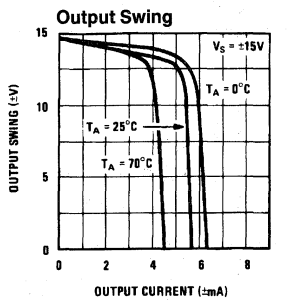
Closed Loop Output Impedance



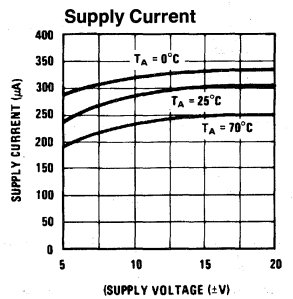
Voltage Gain



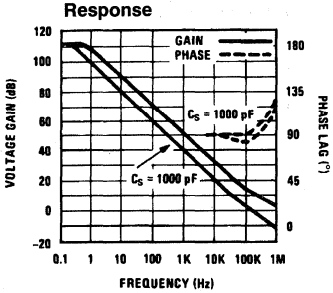
Output Swing



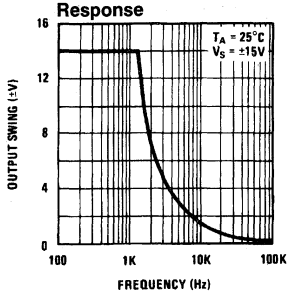
Supply Current



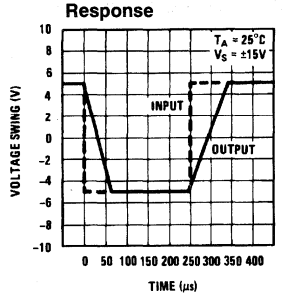
Open Loop Frequency Response



Large Signal Frequency Response



Voltage Follower Pulse Response



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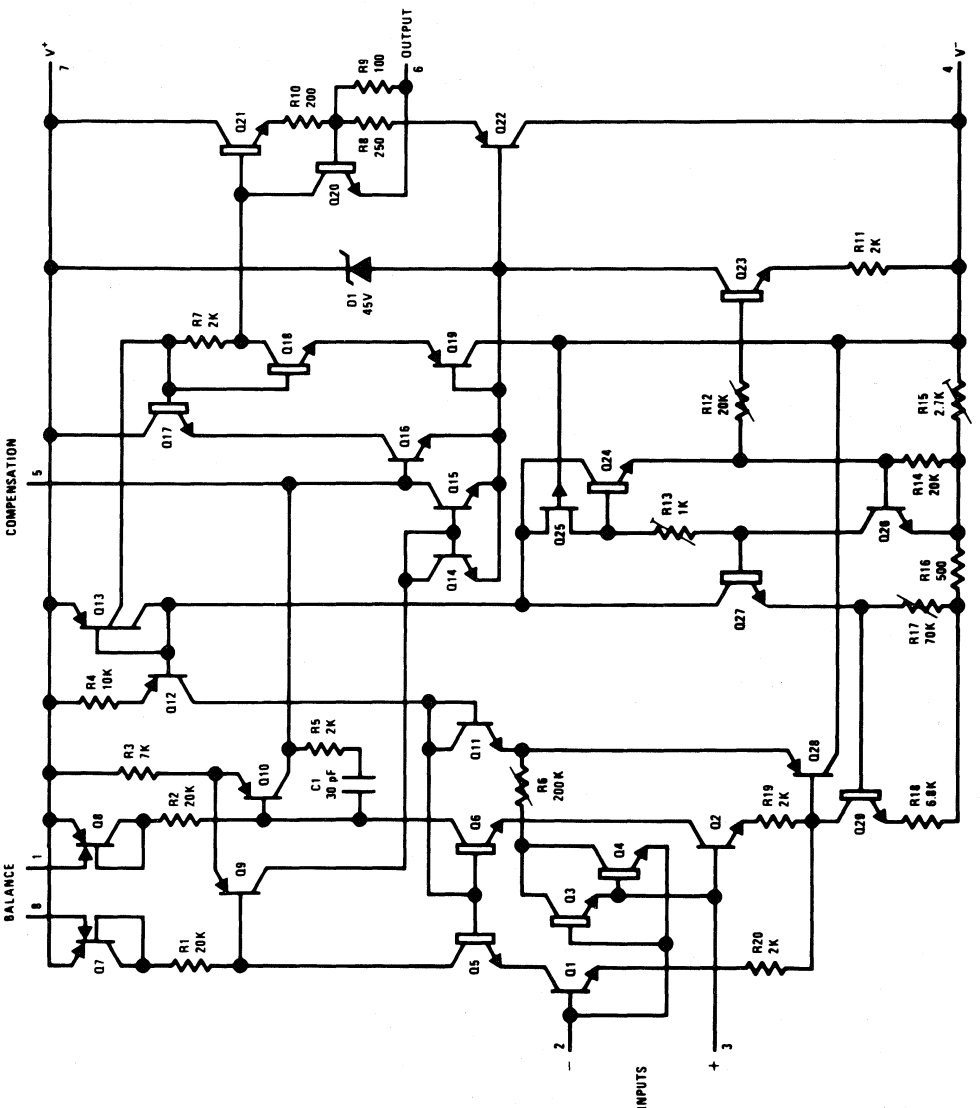
Schematic Diagram



TL/H/7751–1

National Semiconductor

LM118/LM218/LM318 Operational Amplifiers

General Description

The LM118 series are precision high speed operational amplifiers designed for applications requiring wide bandwidth and high slew rate. They feature a factor of ten increase in speed over general purpose devices without sacrificing DC performance.

The LM118 series has internal unity gain frequency compensation. This considerably simplifies its application since no external components are necessary for operation. However, unlike most internally compensated amplifiers, external frequency compensation may be added for optimum performance. For inverting applications, feedforward compensation will boost the slew rate to over 150V/μs and almost double the bandwidth. Overcompensation can be used with the amplifier for greater stability when maximum bandwidth is not needed. Further, a single capacitor can be added to reduce the 0.1% settling time to under 1 μs.

The high speed and fast settling time of these op amps make them useful in A/D converters, oscillators, active filters, sample and hold circuits, or general purpose amplifiers. These devices are easy to apply and offer an order of magnitude better AC performance than industry standards such as the LM709.

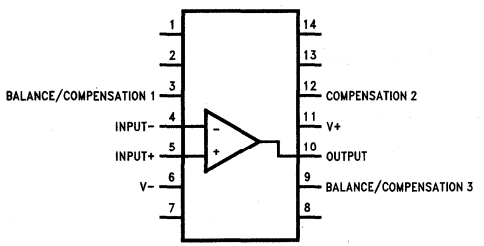
The LM218 is identical to the LM118 except that the LM218 has its performance specified over a −25°C to +85°C temperature range. The LM318 is specified from 0°C to +70°C.

Features

- 15 MHz small signal bandwidth
- Guaranteed 50V/μs slew rate
- Maximum bias current of 250 nA
- Operates from supplies of ±5V to ±20V
- Internal frequency compensation
- Input and output overload protected
- Pin compatible with general purpose op amps

Connection Diagrams

Dual-In-Line Package

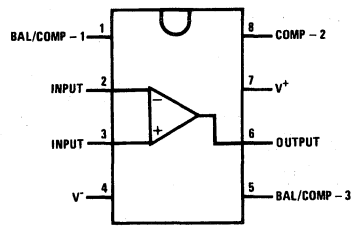


TL/H/7766–24

Top View

Order Number LM118J/883*
See NS Package Number J14A

Dual-In-Line Package

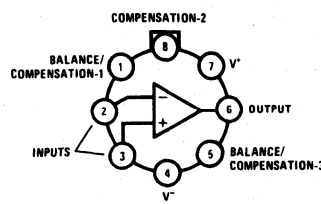


TL/H/7766–3

Top View

Order Number LM118J-8, LM118J-8/883*
LM318J-8, LM318M or LM318N
See NS Package Number J08A, M08A or N08B

Metal Can Package**



TL/H/7766–2

Top View

**Pin connections shown on schematic diagram and typical applications are for TO-5 package.

Order Number LM118H, LM118H/883*
LM218H or LM318H
See NS Package Number H08C

*Available per JM38510/10107.

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications. (Note 6)

Supply Voltage	±20V
Power Dissipation (Note 1)	500 mW
Differential Input Current (Note 2)	±10 mA
Input Voltage (Note 3)	±15V
Output Short-Circuit Duration	Continuous

Operating Temperature Range	
LM118	−55°C to +125°C
LM218	−25°C to +85°C
LM318	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec.)	
Hermetic Package	300°C
Plastic Package	260°C
Soldering Information	
Dual-In-Line Package	
Soldering (10 sec.)	260°C
Small Outline Package	
Vapor Phase (60 sec.)	215°C
Infrared (15 sec.)	220°C

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

ESD Tolerance (Note 7) 2000V

Electrical Characteristics (Note 4)

Parameter	Conditions	LM118/LM218			LM318			Units
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	$T_A = 25°C$		2	4		4	10	mV
Input Offset Current	$T_A = 25°C$		6	50		30	200	nA
Input Bias Current	$T_A = 25°C$		120	250		150	500	nA
Input Resistance	$T_A = 25°C$	1	3		0.5	3		MΩ
Supply Current	$T_A = 25°C$		5	8		5	10	mA
Large Signal Voltage Gain	$T_A = 25°C$, $V_S = \pm 15V$ $V_{OUT} = \pm 10V$, $R_L \geq 2\ k\Omega$	50	200		25	200		V/mV
Slew Rate	$T_A = 25°C$, $V_S = \pm 15V$, $A_V = 1$ (Note 5)	50	70		50	70		V/μs
Small Signal Bandwidth	$T_A = 25°C$, $V_S = \pm 15V$		15			15		MHz
Input Offset Voltage				6			15	mV
Input Offset Current				100			300	nA
Input Bias Current				500			750	nA
Supply Current	$T_A = 125°C$		4.5	7				mA
Large Signal Voltage Gain	$V_S = \pm 15V$, $V_{OUT} = \pm 10V$ $R_L \geq 2\ k\Omega$	25			20			V/mV
Output Voltage Swing	$V_S = \pm 15V$, $R_L = 2\ k\Omega$	±12	±13		±12	±13		V
Input Voltage Range	$V_S = \pm 15V$	±11.5			±11.5			V
Common-Mode Rejection Ratio		80	100		70	100		dB
Supply Voltage Rejection Ratio		70	80		65	80		dB

Note 1: The maximum junction temperature of the LM118 is 150°C, the LM218 is 110°C, and the LM318 is 110°C. For operating at elevated temperatures, devices in the H08 package must be derated based on a thermal resistance of 160°C/W, junction to ambient, or 20°C/W, junction to case. The thermal resistance of the dual-in-line package is 100°C/W, junction to ambient.

Note 2: The inputs are shunted with back-to-back diodes for overvoltage protection. Therefore, excessive current will flow if a differential input voltage in excess of 1V is applied between the inputs unless some limiting resistance is used.

Note 3: For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

Note 4: These specifications apply for $\pm 5V \leq V_S \leq \pm 20V$ and $-55°C \leq T_A \leq +125°C$ (LM118), $-25°C \leq T_A \leq +85°C$ (LM218), and $0°C \leq T_A \leq +70°C$ (LM318). Also, power supplies must be bypassed with 0.1 μF disc capacitors.

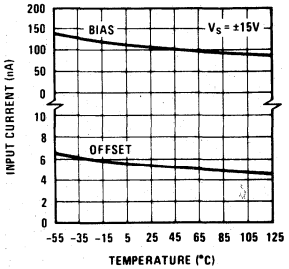
Note 5: Slew rate is tested with $V_S = \pm 15V$. The LM118 is in a unity-gain non-inverting configuration. V_{IN} is stepped from −7.5V to +7.5V and vice versa. The slew rates between −5.0V and +5.0V and vice versa are tested and guaranteed to exceed 50V/μs.

Note 6: Refer to RETS118X for LM118H and LM118J military specifications.

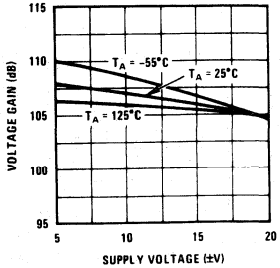
Note 7: Human body model, 1.5 kΩ in series with 100 pF.

Typical Performance Characteristics LM118, LM218

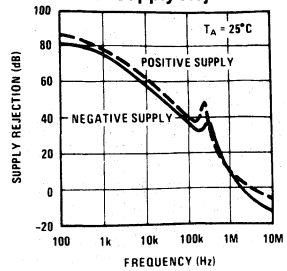
Input Current



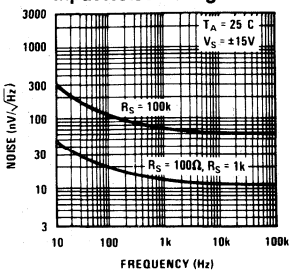
Voltage Gain



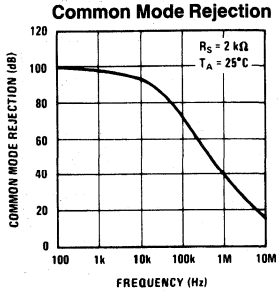
Power Supply Rejection



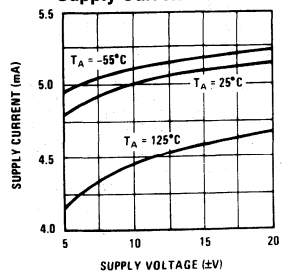
Input Noise Voltage



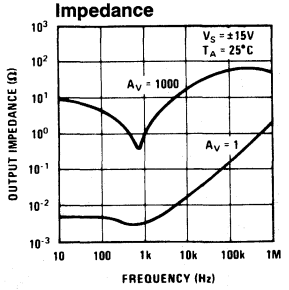
Common Mode Rejection



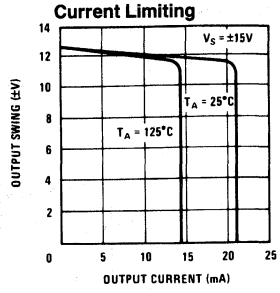
Supply Current



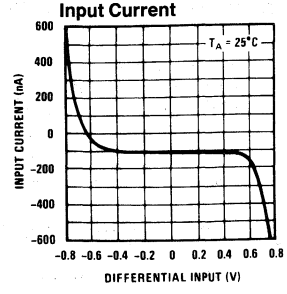
Closed Loop Output Impedance



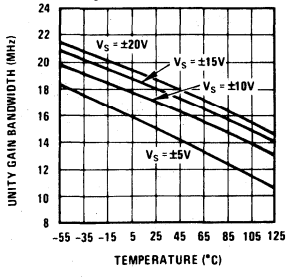
Current Limiting



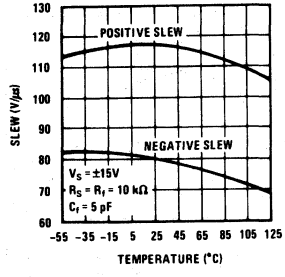
Input Current



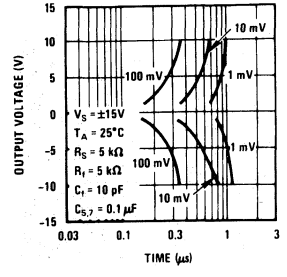
Unity Gain Bandwidth



Voltage Follower Slew Rate



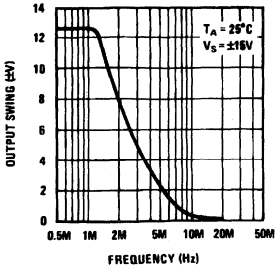
Inverter Settling Time



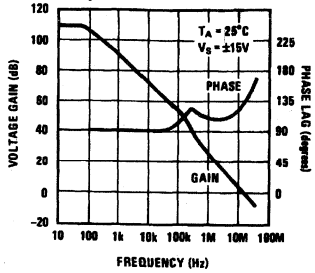
TL/H/7766–4

Typical Performance Characteristics LM118, LM218 (Continued)

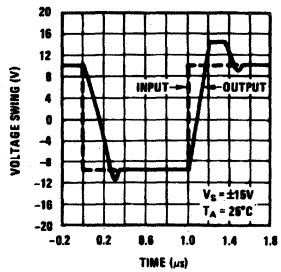
Large Signal Frequency Response



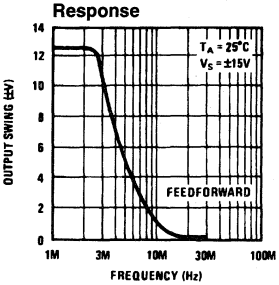
Open Loop Frequency Response



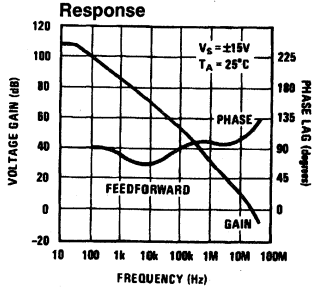
Voltage Follower Pulse Response



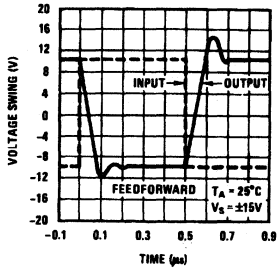
Large Signal Frequency Response



Open Loop Frequency Response



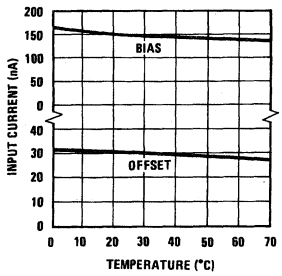
Inverter Pulse Response



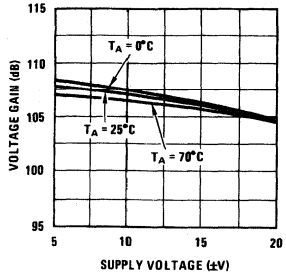
TL/H/7766–5

Typical Performance Characteristics LM318

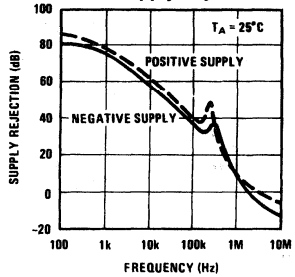
Input Current



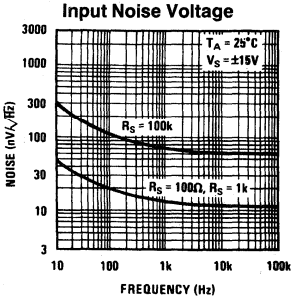
Voltage Gain



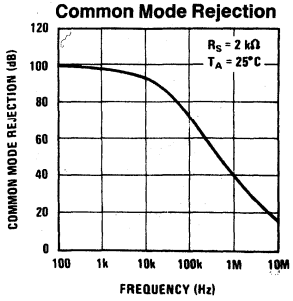
Power Supply Rejection



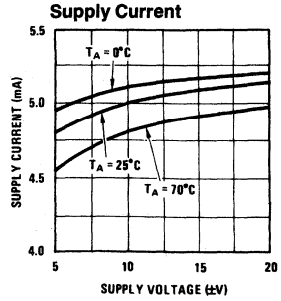
Input Noise Voltage



Common Mode Rejection



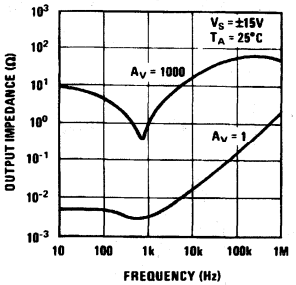
Supply Current



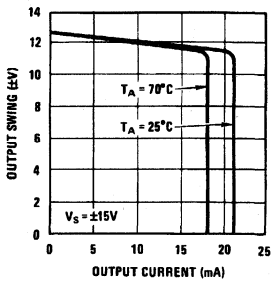
TL/H/7766–6

Typical Performance Characteristics LM318 (Continued)

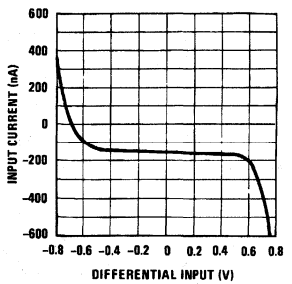
Closed Loop Output Impedance



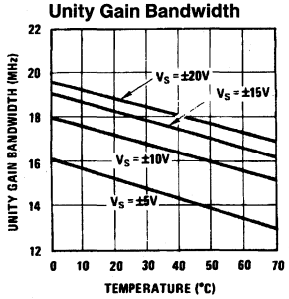
Current Limiting



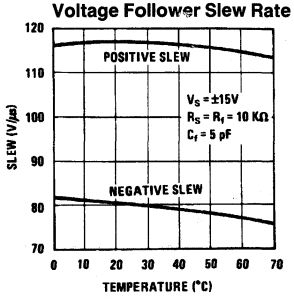
Input Current



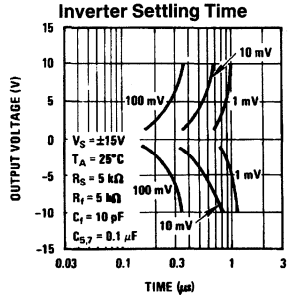
Unity Gain Bandwidth



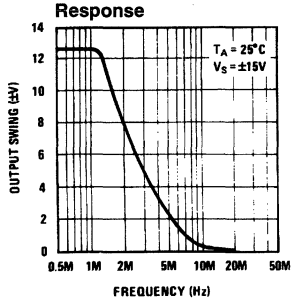
Voltage Follower Slew Rate



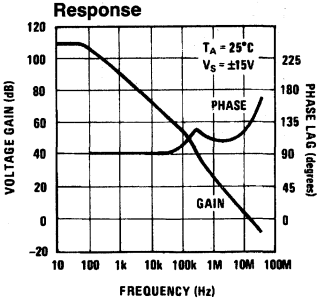
Inverter Settling Time



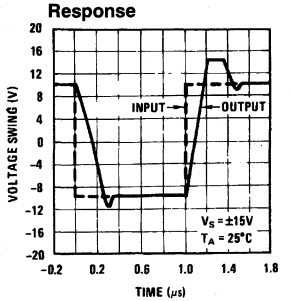
Large Signal Frequency Response



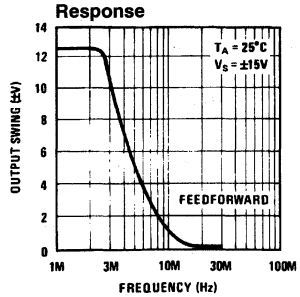
Open Loop Frequency Response



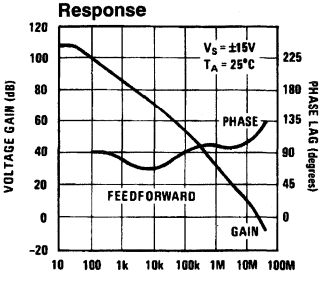
Voltage Follower Pulse Response



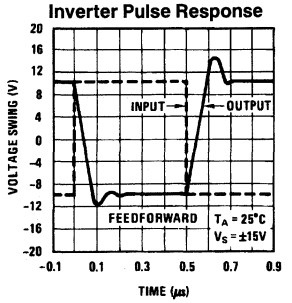
Large Signal Frequency Response



Open Loop Frequency Response



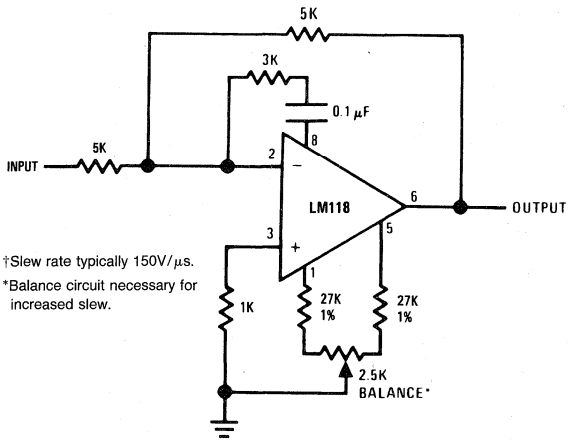
Inverter Pulse Response



TL/H/7766–7

Auxiliary Circuits

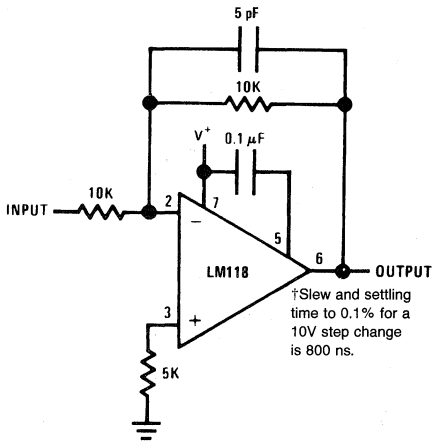
Feedforward Compensation for Greater Inverting Slew Rate†



†Slew rate typically 150V/μs.
*Balance circuit necessary for increased slew.

TL/H/7766–8

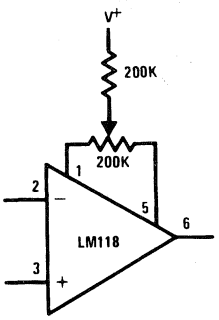
Compensation for Minimum Settling† Time



†Slew and settling time to 0.1% for a 10V step change is 800 ns.

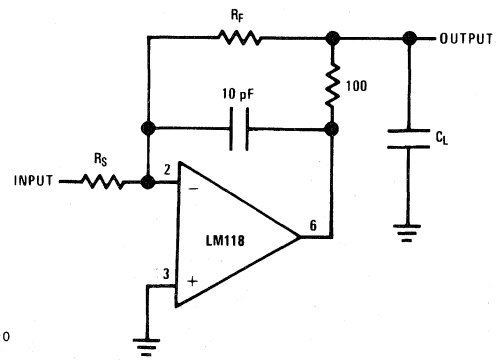
TL/H/7766–9

Offset Balancing



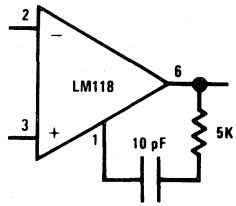
TL/H/7766–10

Isolating Large Capacitive Loads



TL/H/7766–11

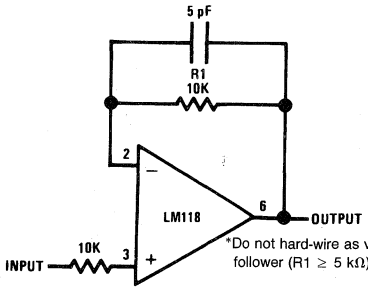
Overcompensation



TL/H/7766–12

Typical Applications

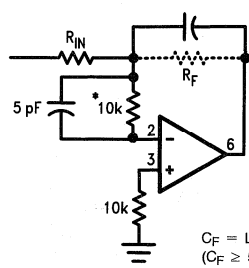
Fast Voltage Follower*



*Do not hard-wire as voltage follower (R1 ≥ 5 kΩ)

TL/H/7766–13

Integrator or Slow Inverter



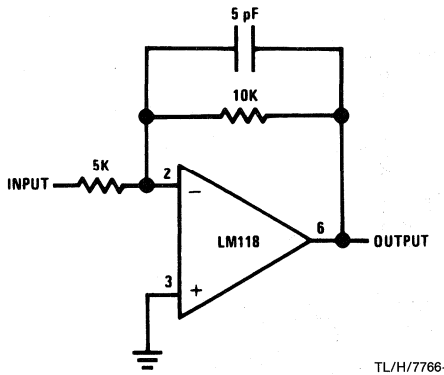
C_F = Large ($C_F \geq 50$ pF)

TL/H/7766–14

*Do not hard-wire as integrator or slow inverter; insert a 10k-5 pF network in series with the input, to prevent oscillation.

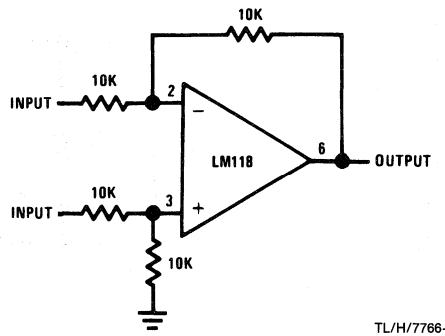
Typical Applications (Continued)

Fast Summing Amplifier



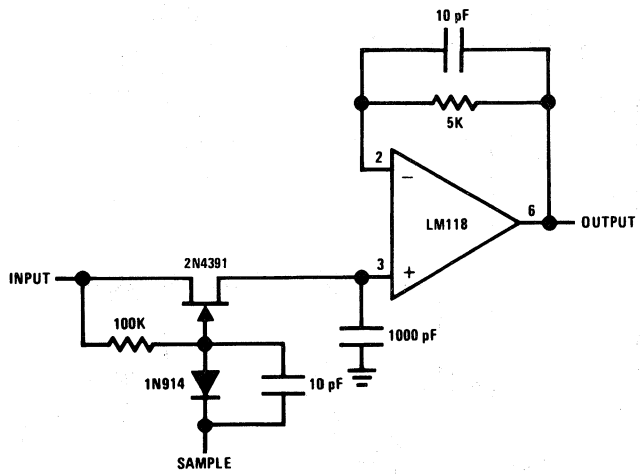
TL/H/7766–15

Differential Amplifier



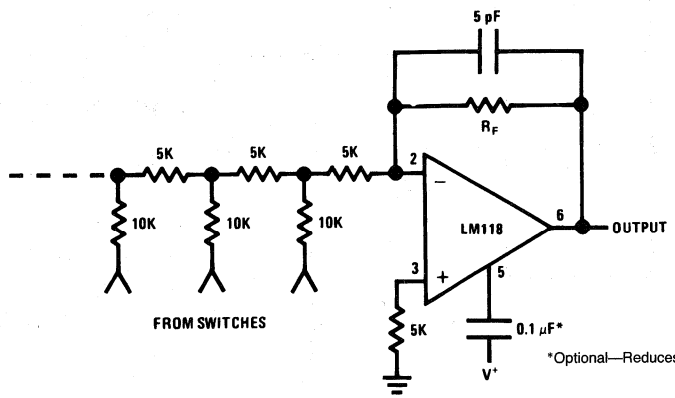
TL/H/7766–16

Fast Sample and Hold



TL/H/7766–18

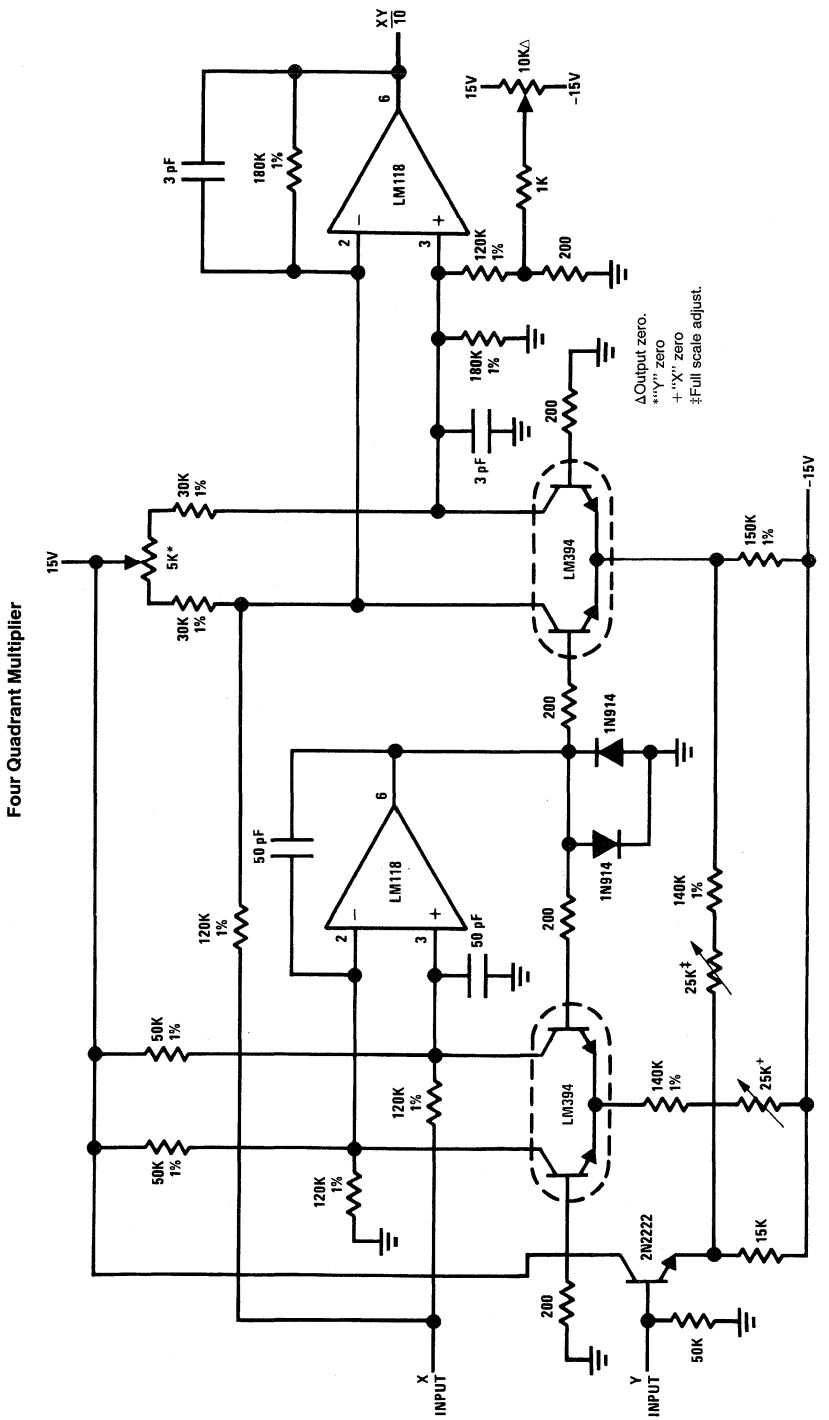
D/A Converter Using Ladder Network



*Optional—Reduces settling time.

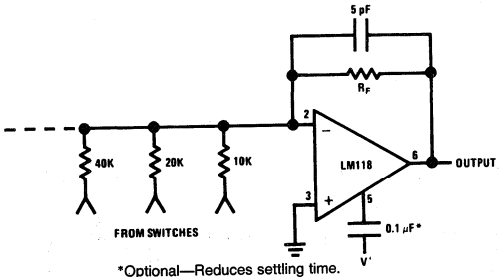
TL/H/7766–19

Typical Applications (Continued)



Typical Applications (Continued)

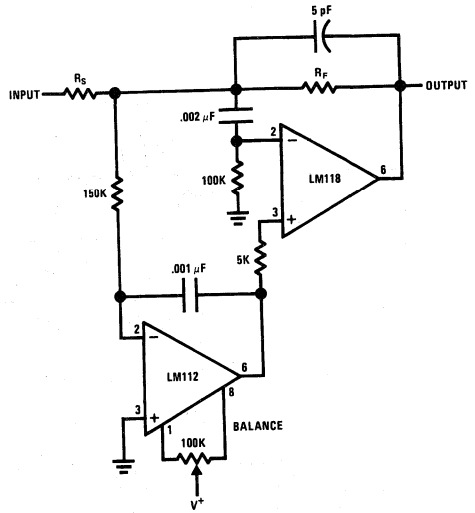
D/A Converter Using Binary Weighted Network



*Optional—Reduces settling time.

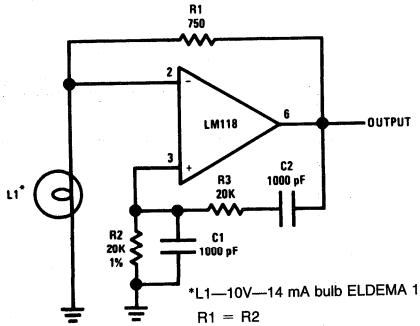
TL/H/7766–20

Fast Summing Amplifier with Low Input Current



TL/H/7766–21

Wein Bridge Sine Wave Oscillator



*L1—10V—14 mA bulb ELDEMA 1869

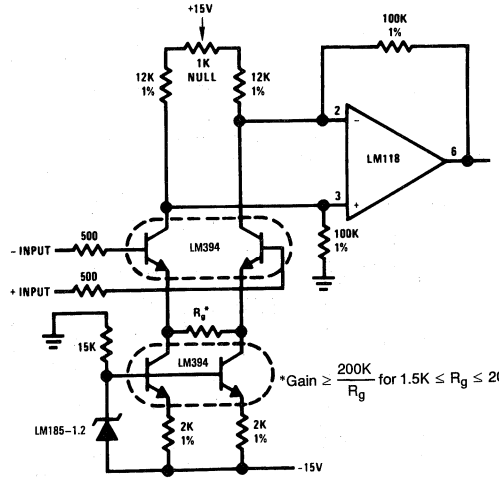
R1 = R2

C1 = C2

$$f = \frac{1}{2\pi R2\, C1}$$

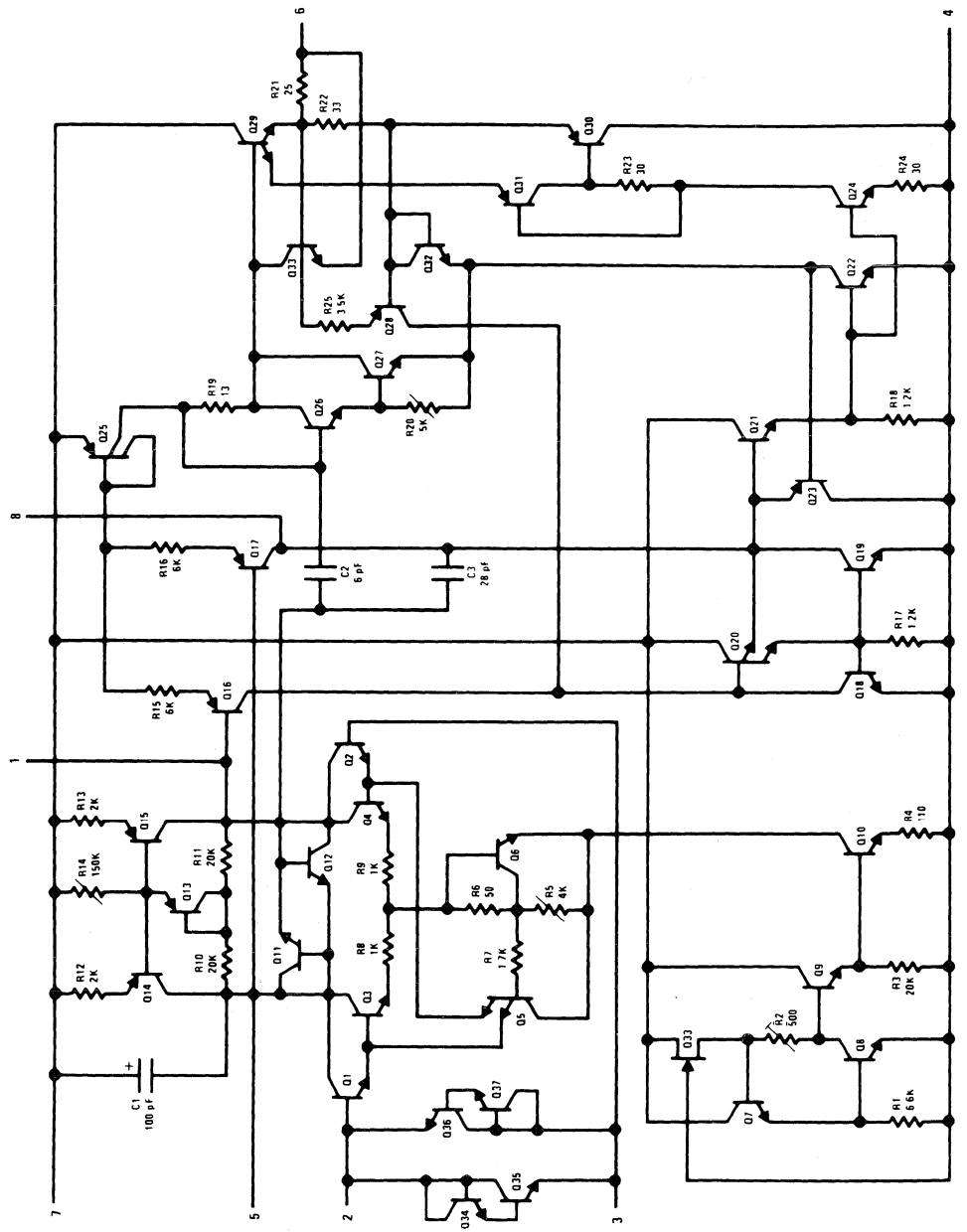
TL/H/7766–22

Instrumentation Amplifier



TL/H/7766–23

Schematic Diagram



National Semiconductor

LM124/LM224/LM324, LM2902
Low Power Quad Operational Amplifiers

General Description

The LM124 series consists of four independent, high gain, internally frequency compensated operational amplifiers which were designed specifically to operate from a single power supply over a wide range of voltages. Operation from split power supplies is also possible and the low power supply current drain is independent of the magnitude of the power supply voltage.

Application areas include transducer amplifiers, DC gain blocks and all the conventional op amp circuits which now can be more easily implemented in single power supply systems. For example, the LM124 series can be directly operated off of the standard +5 V_{DC} power supply voltage which is used in digital systems and will easily provide the required interface electronics without requiring the additional ±15 V_{DC} power supplies.

Unique Characteristics

- In the linear mode the input common-mode voltage range includes ground and the output voltage can also swing to ground, even though operated from only a single power supply voltage
- The unity gain cross frequency is temperature compensated
- The input bias current is also temperature compensated

Advantages

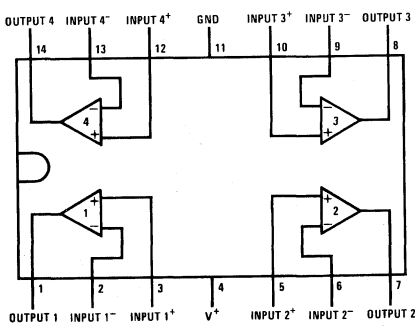
- Eliminates need for dual supplies
- Four internally compensated op amps in a single package
- Allows directly sensing near GND and V_{OUT} also goes to GND
- Compatible with all forms of logic
- Power drain suitable for battery operation

Features

- Internally frequency compensated for unity gain
- Large DC voltage gain 100 dB
- Wide bandwidth (unity gain) 1 MHz (temperature compensated)
- Wide power supply range:
  - Single supply 3 V_{DC} to 32 V_{DC}
  - or dual supplies ±1.5 V_{DC} to ±16 V_{DC}
- Very low supply current drain (700 μA)—essentially independent of supply voltage
- Low input biasing current 45 nA_{DC} (temperature compensated)
- Low input offset voltage 2 mV_{DC}
  and offset current 5 nA_{DC}
- Input common-mode voltage range includes ground
- Differential input voltage range equal to the power supply voltage
- Large output voltage swing 0 V_{DC} to V^+ − 1.5 V_{DC}

Connection Diagram

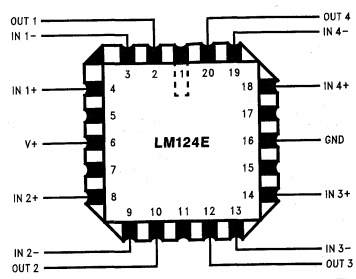
Dual-In-Line Package



TL/H/9299–1

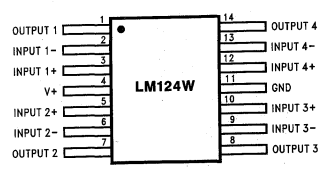
Top View

Order Number LM124J, LM124AJ, LM124J/883, LM124AJ/883*, LM224J, LM224AJ, LM324J, LM324AJ, LM324M, LM324AM, LM2902M, LM324N, LM324AN or LM2902N**
See NS Package Number J14A, M14A or N14A



TL/H/9299–32

Order Number LM124AE/883 or LM124E/883
See NS Package Number E20A



TL/H/9299–33

Order Number LM124AW/883 or LM124W/883
See NS Package Number W14B

*LM124A available per JM38510/11006
**LM124 available per JM38510/11005

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications. (Note 9)

	LM124/LM224/LM324 LM124A/LM224A/LM324A	LM2902
Supply Voltage, V^+	32 V_{DC} or ±16 V_{DC}	26 V_{DC} or ±13 V_{DC}
Differential Input Voltage	32 V_{DC}	26 V_{DC}
Input Voltage	−0.3 V_{DC} to +32 V_{DC}	−0.3 V_{DC} to +26 V_{DC}
Input Current (V_{IN} < −0.3 V_{DC}) (Note 3)	50 mA	50 mA
Power Dissipation (Note 1)		
Molded DIP	1130 mW	1130 mW
Cavity DIP	1260 mW	1260 mW
Small Outline Package	800 mW	800 mW
Output Short-Circuit to GND (One Amplifier) (Note 2) $V^+ \leq 15\ V_{DC}$ and $T_A = 25°C$	Continuous	Continuous
Operating Temperature Range		−40°C to +85°C
LM324/LM324A	0°C to +70°C	
LM224/LM224A	−25°C to +85°C	
LM124/LM124A	−55°C to +125°C	

	LM124/LM224/LM324 LM124A/LM224A/LM324A	LM2902
Storage Temperature Range	−65°C to +150°C	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	260°C	260°C
Soldering Information		
Dual-In-Line Package		
Soldering (10 seconds)	260°C	260°C
Small Outline Package		
Vapor Phase (60 seconds)	215°C	215°C
Infrared (15 seconds)	220°C	220°C

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

ESD Tolerance (Note 10)	250V	250V

Electrical Characteristics $V^+ = +5.0\ V_{DC}$, (Note 4), unless otherwise stated

Parameter	Conditions	LM124A		LM224A		LM324A		LM124/LM224		LM324		LM2902		Units
		Min Typ	Max	Min Typ	Max	Min Typ	Max	Min Typ	Max	Min Typ	Max	Min Typ	Max	
Input Offset Voltage	(Note 5) $T_A = 25°C$	±1	±2	±1	±3	±2	±3	±2	±5	±2	±7	±2	±7	mV_{DC}
Input Bias Current (Note 6)	$I_{IN(+)}$ or $I_{IN(-)}$, $V_{CM} = 0V$, $T_A = 25°C$	20	50	40	80	45	100	45	150	45	250	45	250	nA_{DC}
Input Offset Current	$I_{IN(+)} - I_{IN(-)}$, $V_{CM} = 0V$, $T_A = 25°C$	±2	±10	±2	±15	±5	±30	±3	±30	±5	±50	±5	±50	nA_{DC}
Input Common-Mode Voltage Range (Note 7)	$V^+ = 30\ V_{DC}$, (LM2902, $V^+ = 26\ V_{DC}$), $T_A = 25°C$	0	$V^+ - 1.5$	0	$V^+ - 1.5$	0	$V^+ - 1.5$	0	$V^+ - 1.5$	0	$V^+ - 1.5$	0	$V^+ - 1.5$	V_{DC}
Supply Current	Over Full Temperature Range $R_L = \infty$ On All Op Amps													
	$V^+ = 30V$ (LM2902 $V^+ = 26V$)	1.5	3	1.5	3	1.5	3	1.5	3	1.5	3	1.5	3	mA_{DC}
	$V^+ = 5V$	0.7	1.2	0.7	1.2	0.7	1.2	0.7	1.2	0.7	1.2	0.7	1.2	
Large Signal Voltage Gain	$V^+ = 15\ V_{DC}$, $R_L \geq 2\ k\Omega$, ($V_O = 1\ V_{DC}$ to 11 V_{DC}), $T_A = 25°C$	50	100	50	100	25	100	50	100	25	100	25	100	V/mV
Common-Mode Rejection Ratio	DC, $V_{CM} = 0V$ to $V^+ - 1.5\ V_{DC}$, $T_A = 25°C$	70	85	70	85	65	85	70	85	65	85	50	70	dB
Power Supply Rejection Ratio	DC, $V^+ = 5\ V_{DC}$ to 30 V_{DC} (LM2902, $V^+ = 5\ V_{DC}$ to 26 V_{DC}), $T_A = 25°C$	65	100	65	100	65	100	65	100	65	100	50	100	dB

Electrical Characteristics $V^+ = +5.0\ V_{DC}$ (Note 4) unless otherwise stated (Continued)

Parameter		Conditions	LM124A			LM224A			LM324A			LM124/LM224			LM324			LM2902			Units
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Amplifier-to-Amplifier Coupling (Note 8)		f = 1 kHz to 20 kHz, $T_A = 25°C$ (Input Referred)		−120			−120			−120			−120			−120			−120		dB
Output Current	Source	$V_{IN}^+ = 1\ V_{DC}$, $V_{IN}^- = 0\ V_{DC}$, $V^+ = 15\ V_{DC}$, $V_O = 2\ V_{DC}$, $T_A = 25°C$	20	40		20	40		20	40		20	40		20	40		20	40		mA_{DC}
	Sink	$V_{IN}^- = 1\ V_{DC}$, $V_{IN}^+ = 0\ V_{DC}$, $V^+ = 15\ V_{DC}$, $V_O = 2\ V_{DC}$, $T_A = 25°C$	10	20		10	20		10	20		10	20		10	20		10	20		mA_{DC}
		$V_{IN}^- = 1\ V_{DC}$, $V_{IN}^+ = 0\ V_{DC}$, $V^+ = 15\ V_{DC}$, $V_O = 200\ mV_{DC}$, $T_A = 25°C$	12	50		12	50		12	50		12	50		12	50		12	50		μA_{DC}
Short Circuit to Ground		(Note 2) $V^+ = 15\ V_{DC}$, $T_A = 25°C$		40	60		40	60		40	60		40	60		40	60		40	60	mA_{DC}
Input Offset Voltage		(Note 5)			±4			±4			±5			±7			±9			±10	mV_{DC}
Input Offset Voltage Drift		$R_S = 0\Omega$		±7	±20		±7	±20		±7	±30		±7			±7			±7		$\mu V/°C$
Input Offset Current		$I_{IN(+)} - I_{IN(-)}$, $V_{CM} = 0V$			±30			±30			±75			±100			±150		±45	±200	nA_{DC}
Input Offset Current Drift		$R_S = 0\Omega$		±10	±200		±10	±200		±10	±300		±10			±10			±10		$pA_{DC}/°C$
Input Bias Current		$I_{IN(+)}$ or $I_{IN(-)}$		40	100		40	100		40	200		40	300		40	500		40	500	nA_{DC}
Input Common-Mode Voltage Range (Note 7)		$V^+ = +30\ V_{DC}$ (LM2902, $V^+ = 26\ V_{DC}$)	0		$V^+ - 2$	0		$V^+ - 2$	0		$V^+ - 2$	0		$V^+ - 2$	0		$V^+ - 2$	0		$V^+ - 2$	V_{DC}
Large Signal Voltage Gain		$V^+ = +15\ V_{DC}$ (V_O Swing = 1 V_{DC} to 11 V_{DC}) $R_L \geq 2\ k\Omega$	25			25			15			25			15			15			V/mV
Output Voltage Swing	V_{OH}	$V^+ = +30\ V_{DC}$, $R_L = 2\ k\Omega$	26			26			26			26			26			22			V_{DC}
		$R_L \geq 10\ k\Omega$ (LM2902, $V^+ = 26\ V_{DC}$)	27	28		27	28		27	28		27	28		27	28		23	24		
	V_{OL}	$V^+ = 5\ V_{DC}$, $R_L \geq 10\ k\Omega$		5	20		5	20		5	20		5	20		5	20		5	100	mV_{DC}

Electrical Characteristics $V^+ = +5.0\ V_{DC}$ (Note 4) unless otherwise stated (Continued)

Parameter		Conditions		LM124A			LM224A			LM324A			LM124/LM224			LM324			LM2902			Units
				Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Output Current	Source	$V_O = 2\ V_{DC}$	$V_{IN}^+ = +1\ V_{DC}$, $V_{IN}^- = 0\ V_{DC}$, $V^+ = 15\ V_{DC}$	10	20		10	20		10	20		10	20		10	20		10	20		mA_{DC}
	Sink		$V_{IN}^- = +1\ V_{DC}$, $V_{IN}^+ = 0\ V_{DC}$, $V^+ = 15\ V_{DC}$	10	15		5	8		5	8		5	8		5	8		5	8		

Note 1: For operating at high temperatures, the LM324/LM324A, LM2902 must be derated based on a +125°C maximum junction temperature and a thermal resistance of 88°C/W which applies for the device soldered in a printed circuit board, operating in a still air ambient. The LM224/LM224A and LM124/LM124A can be derated based on a +150°C maximum junction temperature. The dissipation is the total of all four amplifiers—use external resistors, where possible, to allow the amplifier to saturate of to reduce the power which is dissipated in the integrated circuit.

Note 2: Short circuits from the output to V^+ can cause excessive heating and eventual destruction. When considering short circuits to ground, the maximum output current is approximately 40 mA independent of the magnitude of V^+. At values of supply voltage in excess of $+15\ V_{DC}$, continuous short-circuits can exceed the power dissipation ratings and cause eventual destruction. Destructive dissipation can result from simultaneous shorts on all amplifiers.

Note 3: This input current will only exist when the voltage at any of the input leads is driven negative. It is due to the collector-base junction of the input PNP transistors becoming forward biased and thereby acting as input diode clamps. In addition to this diode action, there is also lateral NPN parasitic transistor action on the IC chip. This transistor action can cause the output voltages of the op amps to go to the V^+ voltage level (or to ground for a large overdrive) for the time duration that an input is driven negative. This is not destructive and normal output states will re-establish when the input voltage, which was negative, again returns to a value greater than $-0.3\ V_{DC}$ (at 25°C).

Note 4: These specifications are limited to $-55°C \leq T_A \leq +125°C$ for the LM124/LM124A. With the LM224/LM224A, all temperature specifications are limited to $-25°C \leq T_A \leq +85°C$, the LM324/LM324A temperature specifications are limited to $0°C \leq T_A \leq +70°C$, and the LM2902 specifications are limited to $-40°C \leq T_A \leq +85°C$.

Note 5: $V_O \cong 1.4\ V_{DC}$, $R_S = 0\Omega$ with V^+ from $5\ V_{DC}$ to $30\ V_{DC}$; and over the full input common-mode range ($0\ V_{DC}$ to $V^+ - 1.5\ V_{DC}$) for LM2902, V^+ from $5\ V_{DC}$ to $26\ V_{DC}$.

Note 6: The direction of the input current is out of the IC due to the PNP input stage. This current is essentially constant, independent of the state of the output so no loading change exists on the input lines.

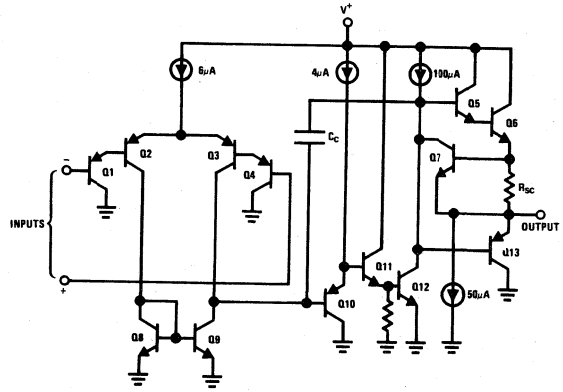
Note 7: The input common-mode voltage of either input signal voltage should not be allowed to go negative by more than 0.3V (at 25°C). The upper end of the common-mode voltage range is $V^+ - 1.5V$ (at 25°C), but either or both inputs can go to $+32\ V_{DC}$ without damage ($+26\ V_{DC}$ for LM2902), independent of the magnitude of V^+.

Note 8: Due to proximity of external components, insure that coupling is not originating via stray capacitance between these external parts. This typically can be detected as this type of capacitance increases at higher frequencies.

Note 9: Refer to RETS124AX for LM124A military specifications and refer to RETS124X for LM124 military specifications.

Note 10: Human body model, 1.5 kΩ in series with 100 pF.

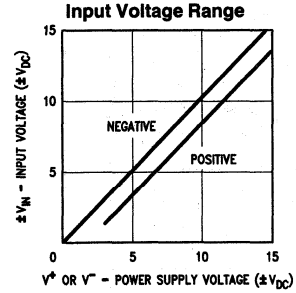
Schematic Diagram (Each Amplifier)



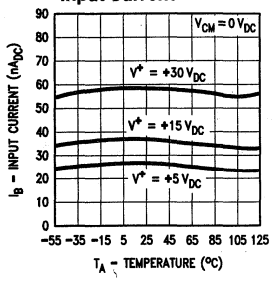
TL/H/9299–2

Typical Performance Characteristics

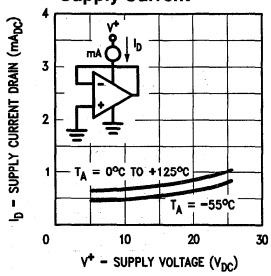
Input Voltage Range



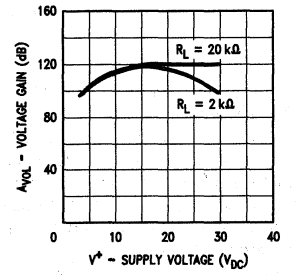
Input Current



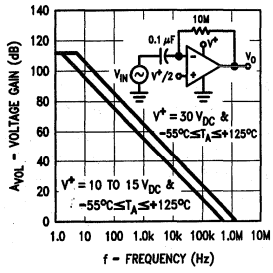
Supply Current



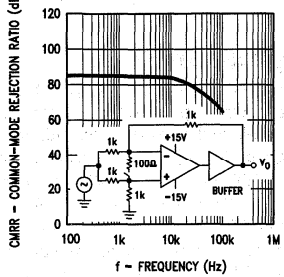
Voltage Gain



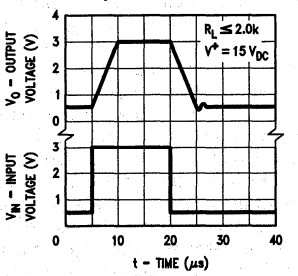
Open Loop Frequency Response



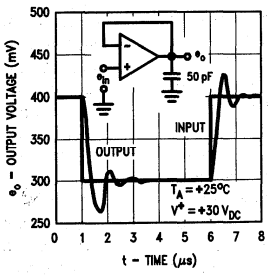
Common Mode Rejection Ratio



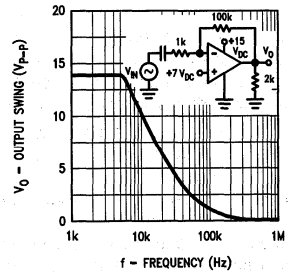
Voltage Follower Pulse Response



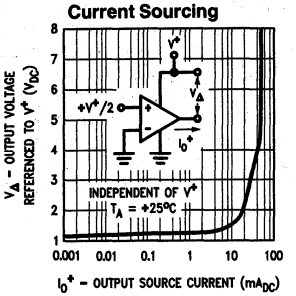
Voltage Follower Pulse Response (Small Signal)



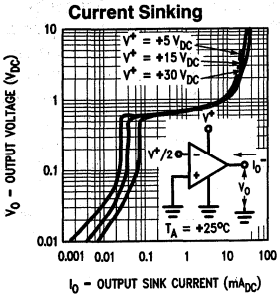
Large Signal Frequency Response



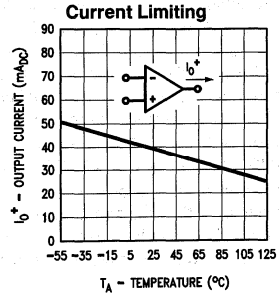
Output Characteristics Current Sourcing



Output Characteristics Current Sinking

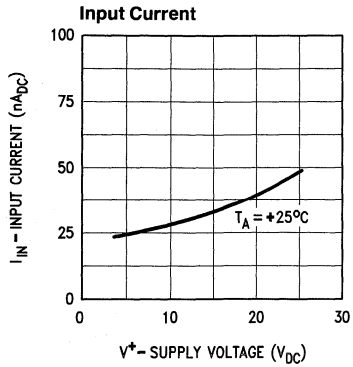


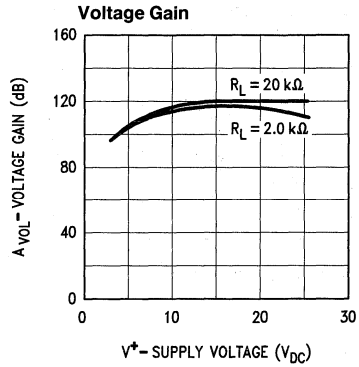
Current Limiting



TL/H/9299–3

Typical Performance Characteristics (LM2902 only)





TL/H/9299–4

Application Hints

The LM124 series are op amps which operate with only a single power supply voltage, have true-differential inputs, and remain in the linear mode with an input common-mode voltage of 0 V_{DC}. These amplifiers operate over a wide range of power supply voltage with little change in performance characteristics. At 25°C amplifier operation is possible down to a minimum supply voltage of 2.3 V_{DC}.

The pinouts of the package have been designed to simplify PC board layouts. Inverting inputs are adjacent to outputs for all of the amplifiers and the outputs have also been placed at the corners of the package (pins 1, 7, 8, and 14).

Precautions should be taken to insure that the power supply for the integrated circuit never becomes reversed in polarity or that the unit is not inadvertently installed backwards in a test socket as an unlimited current surge through the resulting forward diode within the IC could cause fusing of the internal conductors and result in a destroyed unit.

Large differential input voltages can be easily accommodated and, as input differential voltage protection diodes are not needed, no large input currents result from large differential input voltages. The differential input voltage may be larger than V^+ without damaging the device. Protection should be provided to prevent the input voltages from going negative more than -0.3 V_{DC} (at 25°C). An input clamp diode with a resistor to the IC input terminal can be used.

To reduce the power supply drain, the amplifiers have a class A output stage for small signal levels which converts to class B in a large signal mode. This allows the amplifiers to both source and sink large output currents. Therefore both NPN and PNP external current boost transistors can be used to extend the power capability of the basic amplifiers. The output voltage needs to raise approximately 1 diode drop above ground to bias the on-chip vertical PNP transistor for output current sinking applications.

For ac applications, where the load is capacitively coupled to the output of the amplifier, a resistor should be used, from the output of the amplifier to ground to increase the class A bias current and prevent crossover distortion.

Where the load is directly coupled, as in dc applications, there is no crossover distortion.

Capacitive loads which are applied directly to the output of the amplifier reduce the loop stability margin. Values of 50 pF can be accommodated using the worst-case non-inverting unity gain connection. Large closed loop gains or resistive isolation should be used if larger load capacitance must be driven by the amplifier.

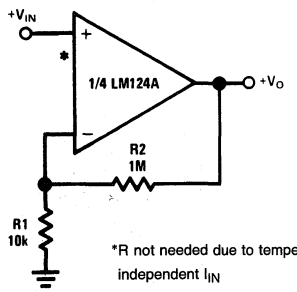
The bias network of the LM124 establishes a drain current which is independent of the magnitude of the power supply voltage over the range of from 3 V_{DC} to 30 V_{DC}.

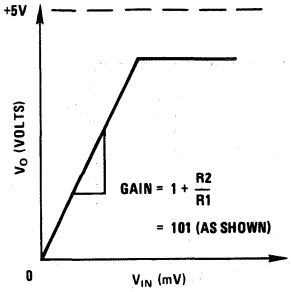
Output short circuits either to ground or to the positive power supply should be of short time duration. Units can be destroyed, not as a result of the short circuit current causing metal fusing, but rather due to the large increase in IC chip dissipation which will cause eventual failure due to excessive junction temperatures. Putting direct short-circuits on more than one amplifier at a time will increase the total IC power dissipation to destructive levels, if not properly protected with external dissipation limiting resistors in series with the output leads of the amplifiers. The larger value of output source current which is available at 25°C provides a larger output current capability at elevated temperatures (see typical performance characteristics) than a standard IC op amp.

The circuits presented in the section on typical applications emphasize operation on only a single power supply voltage. If complementary power supplies are available, all of the standard op amp circuits can be used. In general, introducing a pseudo-ground (a bias voltage reference of $V^+/2$) will allow operation above and below this value in single power supply systems. Many application circuits are shown which take advantage of the wide input common-mode voltage range which includes ground. In most cases, input biasing is not required and input voltages which range to ground can easily be accommodated.

Typical Single-Supply Applications ($V^+ = 5.0\ V_{DC}$)

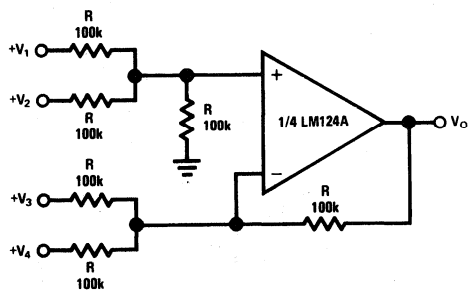
Non-Inverting DC Gain (0V Input = 0V Output)





TL/H/9299–5

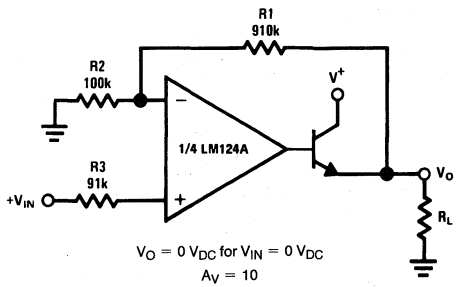
DC Summing Amplifier
($V_{IN'S} \geq 0\ V_{DC}$ and $V_O \geq V_{DC}$)



TL/H/9299–6

Where: $V_O = V_1 + V_2 - V_3 - V_4$
$(V_1 + V_2) \geq (V_3 + V_4)$ to keep $V_O > 0\ V_{DC}$

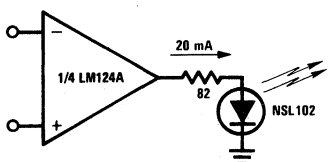
Power Amplifier



$V_O = 0\ V_{DC}$ for $V_{IN} = 0\ V_{DC}$
$A_V = 10$

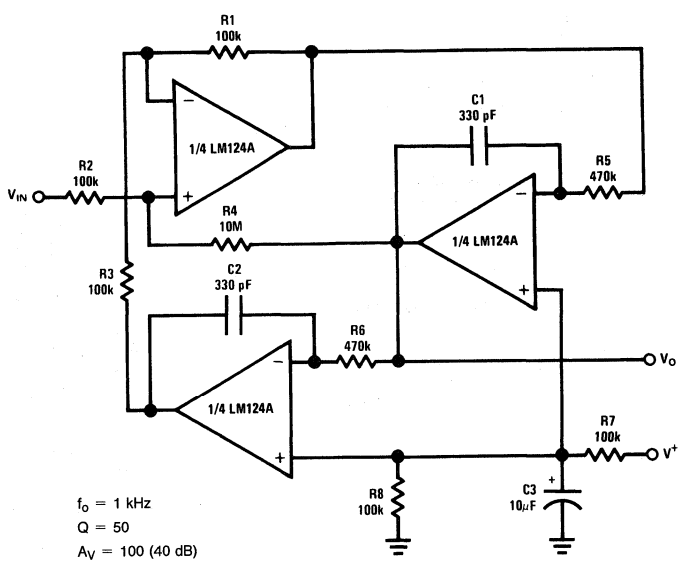
TL/H/9299–7

LED Driver



TL/H/9299–8

"BI-QUAD" RC Active Bandpass Filter

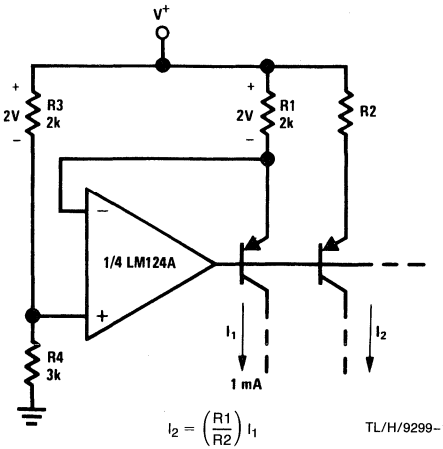


$f_o = 1$ kHz
$Q = 50$
$A_V = 100$ (40 dB)

TL/H/9299–9

Typical Single-Supply Applications (V^+ = 5.0 V_{DC}) (Continued)

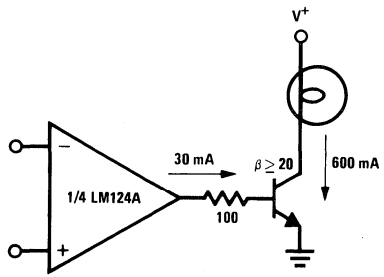
Fixed Current Sources



$$I_2 = \left(\frac{R1}{R2}\right) I_1$$

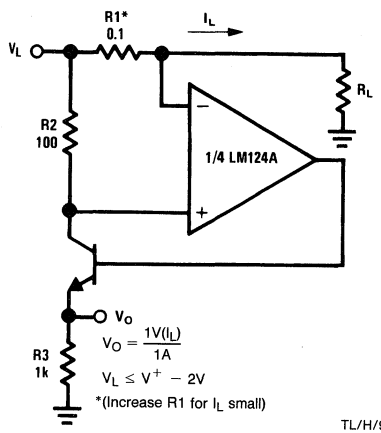
TL/H/9299–10

Lamp Driver



TL/H/9299–11

Current Monitor



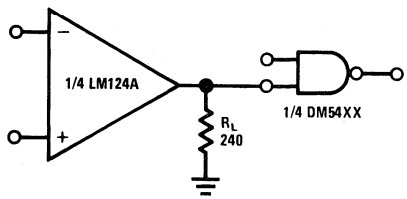
$$V_O = \frac{1V(I_L)}{1A}$$

$V_L \leq V^+ - 2V$

*(Increase R1 for I_L small)

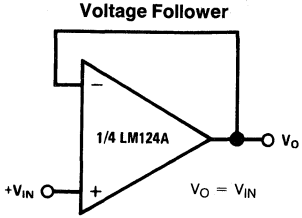
TL/H/9299–12

Driving TTL



TL/H/9299–13

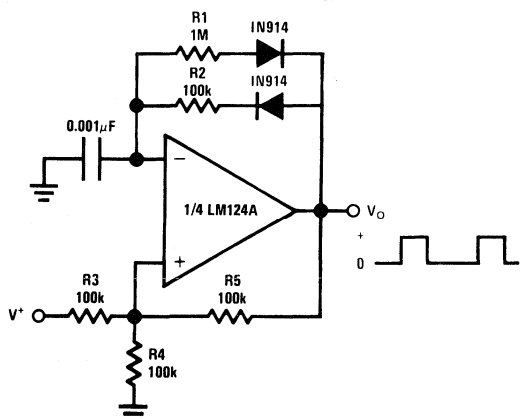
Voltage Follower



$V_O = V_{IN}$

TL/H/9299–14

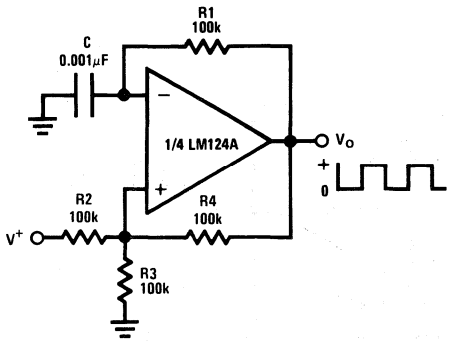
Pulse Generator



TL/H/9299–15

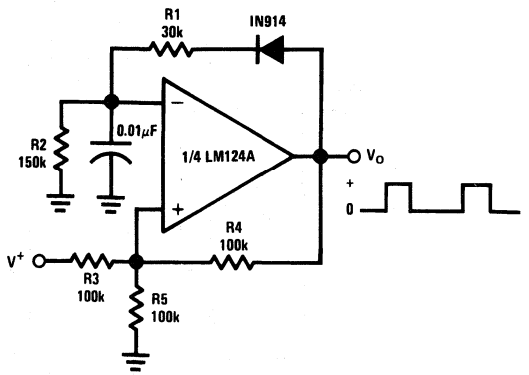
Typical Single-Supply Applications (V^+ = 5.0 V_{DC}) (Continued)

Squarewave Oscillator



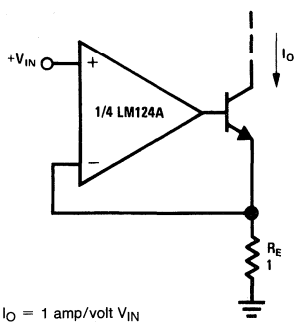
TL/H/9299–16

Pulse Generator



TL/H/9299–17

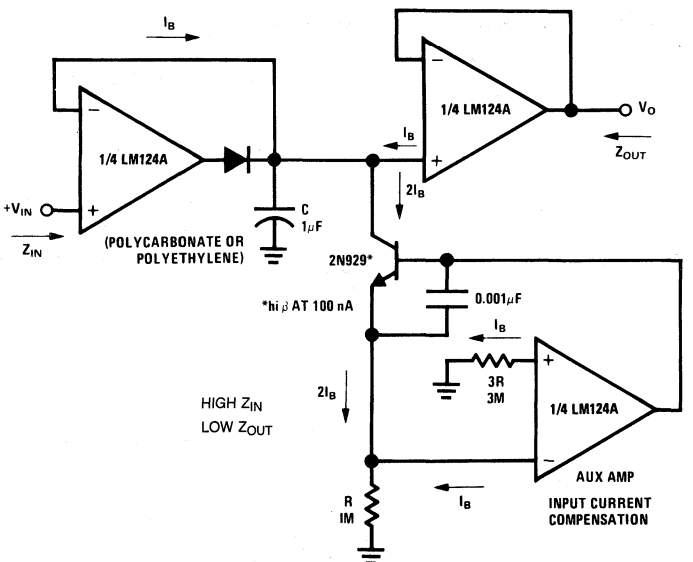
High Compliance Current Sink



I_O = 1 amp/volt V_{IN}
(Increase R_E for I_o small)

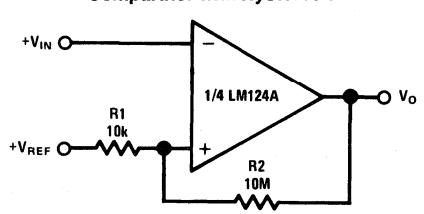
TL/H/9299–18

Low-Drift Peak Detector



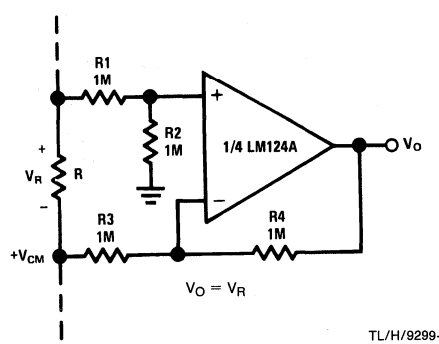
TL/H/9299–19

Comparator with Hysteresis



TL/H/9299–20

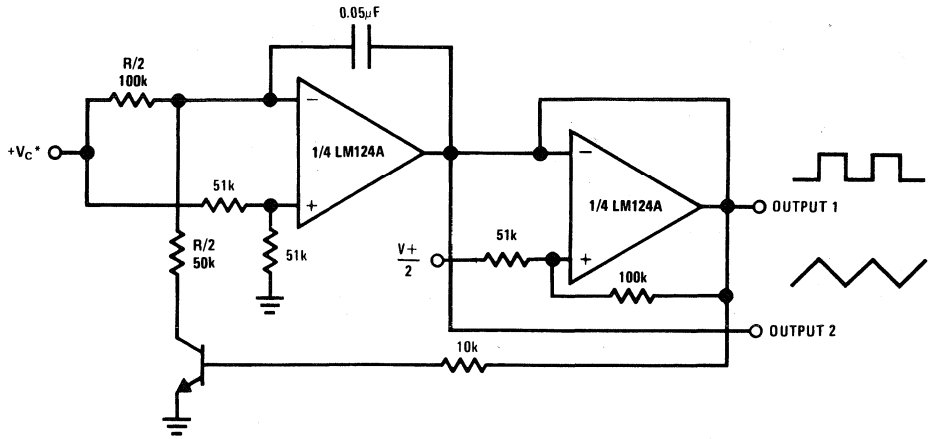
Ground Referencing a Differential Input Signal



TL/H/9299–21

Typical Single-Supply Applications (V^+ = 5.0 V_{DC}) (Continued)

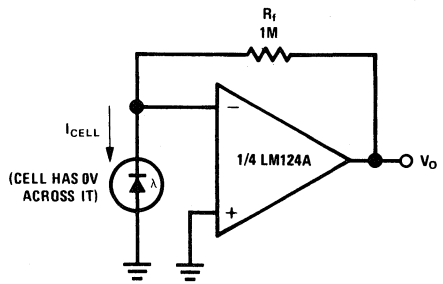
Voltage Controlled Oscillator Circuit



TL/H/9299–22

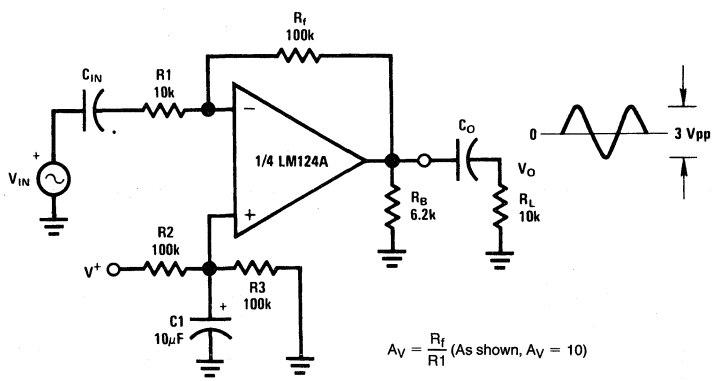
*Wide control voltage range: 0 $V_{DC} \leq V_C \leq 2\ (V^+ - 1.5\ V_{DC})$

Photo Voltaic-Cell Amplifier



TL/H/9299–23

AC Coupled Inverting Amplifier

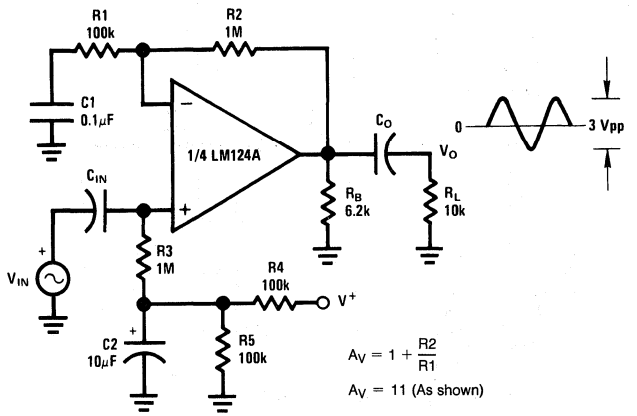


$A_V = \frac{R_f}{R1}$ (As shown, A_V = 10)

TL/H/9299–24

Typical Single-Supply Applications (V^+ = 5.0 V_{DC}) (Continued)

AC Coupled Non-Inverting Amplifier

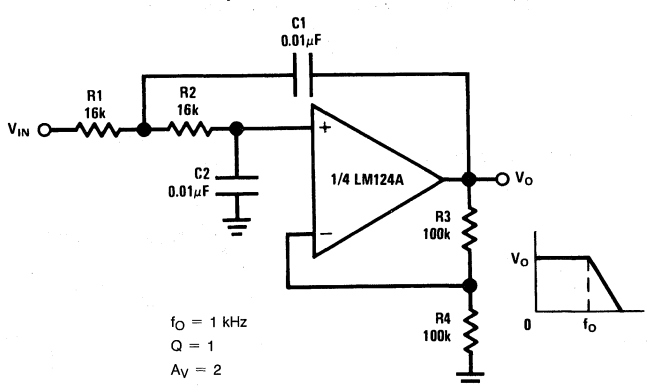


$A_V = 1 + \frac{R2}{R1}$

A_V = 11 (As shown)

TL/H/9299–25

DC Coupled Low-Pass RC Active Filter



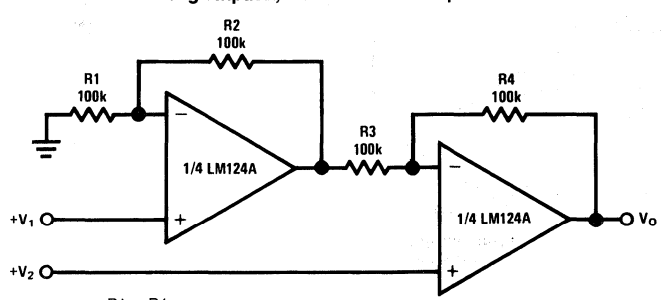
f_O = 1 kHz

Q = 1

A_V = 2

TL/H/9299–26

High Input Z, DC Differential Amplifier



For $\frac{R1}{R2} = \frac{R4}{R3}$ (CMRR depends on this resistor ratio match)

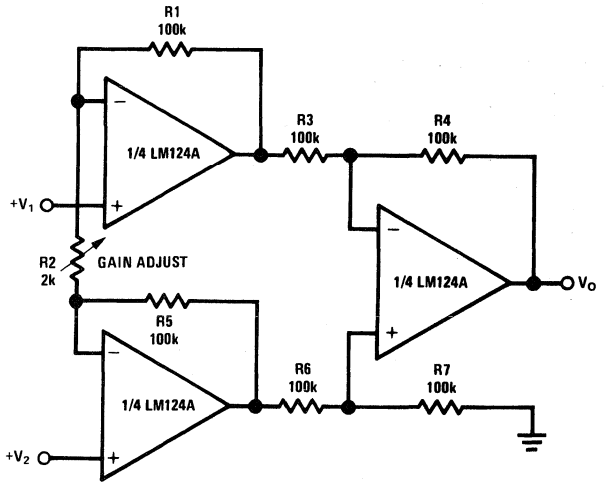
$V_O = 1 + \frac{R4}{R3}(V_2 - V_1)$

As shown: $V_O = 2(V_2 - V_1)$

TL/H/9299–27

Typical Single-Supply Applications (V^+ = 5.0 V_{DC}) (Continued)

High Input Z Adjustable-Gain DC Instrumentation Amplifier



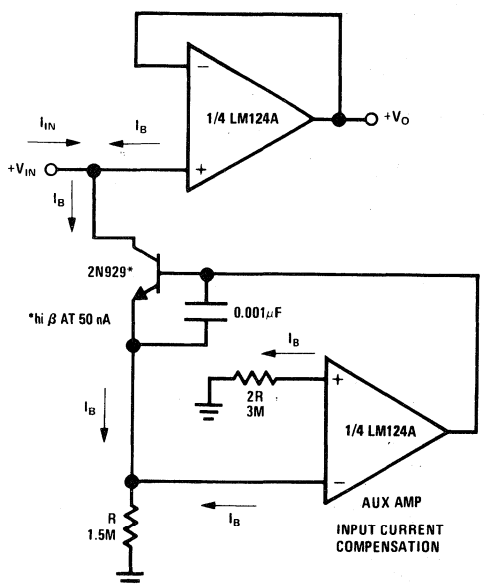
If R1 = R5 & R3 = R4 = R6 = R7 (CMRR depends on match)

TL/H/9299–28

$$V_O = 1 + \frac{2R1}{R2}(V_2 - V_1)$$

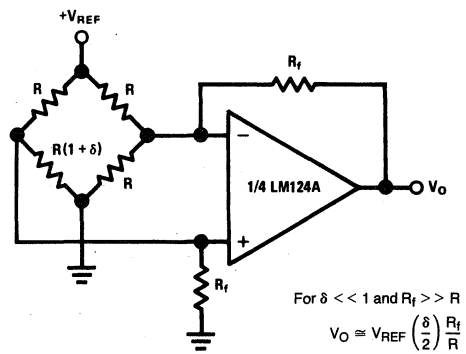
As shown $V_O = 101\,(V_2 - V_1)$

Using Symmetrical Amplifiers to Reduce Input Current (General Concept)



TL/H/9299–29

Bridge Current Amplifier



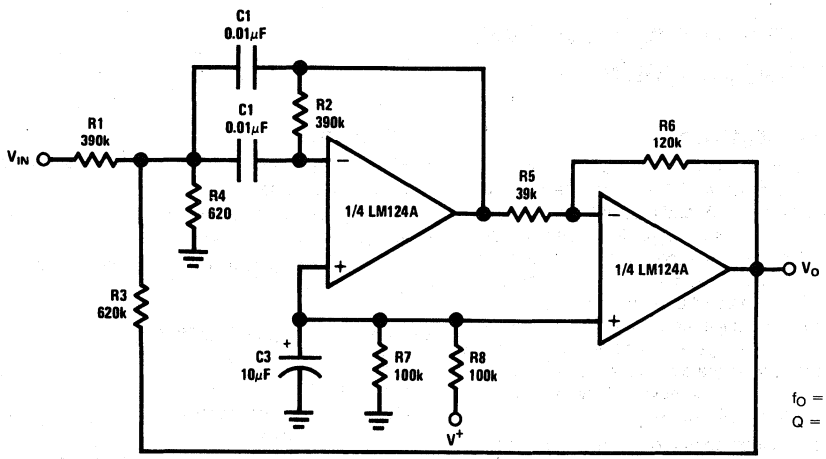
For $\delta << 1$ and $R_f >> R$

$$V_O \cong V_{REF}\left(\frac{\delta}{2}\right)\frac{R_f}{R}$$

TL/H/9299–30

Typical Single-Supply Applications (V^+ = 5.0 V_{DC}) (Continued)

Bandpass Active Filter



f_O = 1 kHz
Q = 25

TL/H/9299–31

National Semiconductor

LM143/LM343 High Voltage Operational Amplifier

General Description

The LM143 is a general purpose high voltage operational amplifier featuring operation to ±40V, complete input overvoltage protection up to ±40V and input currents comparable to those of other super-β op amps. Increased slew rate, together with higher common-mode and supply rejection, insure improved performance at high supply voltages. Operating characteristics, in particular supply current, slew rate and gain, are virtually independent of supply voltage and temperature. Furthermore, gain is unaffected by output loading at high supply voltages due to thermal symmetry on the die. The LM143 is pin compatible with general purpose op amps and has offset null capability.

Application areas include those of general purpose op amps, but can be extended to higher voltages and higher output power when externally boosted. For example, when used in audio power applications, the LM143 provides a power bandwidth that covers the entire audio spectrum. In addition, the LM143 can be reliably operated in environments with large overvoltage spikes on the power supplies, where other internally-compensated op amps would suffer catastrophic failure.

The LM343 is similar to the LM143 for applications in less severe supply voltage and temperature environments.

Features

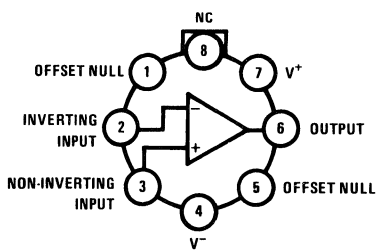
- Wide supply voltage range ±4.0V to ±40V
- Large output voltage swing ±37V
- Wide input common-mode range ±38V
- Input overvoltage protection Full ±40V
- Supply current is virtually independent of supply voltage and temperature

Unique Characteristics

- Low input bias current 8.0 nA
- Low input offset current 1.0 nA
- High slew rate—essentially independent of temperature and supply voltage 2.5V/μs
- High voltage gain—virtually independent of resistive loading, temperature, and supply voltage 100k min
- Internally compensated for unity gain
- Output short circuit protection
- Pin compatible with general purpose op amps

Connection Diagram

Metal Can Package
Top View



TL/H/7783–1

Order Number LM143H, LM143H/883* or LM343H
See NS Package Number H08C

*Available per SMD# 7800303

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.
(Note 4)

	LM143	LM343
Supply Voltage	±40V	±34V
Power Dissipation (Note 1)	680 mW	680 mW
Differential Input Voltage (Note 2)	80V	68V
Input Voltage (Note 2)	±40V	±34V
Operating Temperature Range	−55°C to +125°C	0°C to +70°C
Storage Temperature Range	−65°C to +150°C	−65°C to +150°C
Output Short Circuit Duration	5 seconds	5 seconds
Lead Temperature (Soldering, 10 sec.)	300°C	300°C
ESD rating to be determined.		

Electrical Characteristics (Note 3)

Parameter	Conditions	LM143			LM343			Units
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	$T_A = 25°C$		2.0	5.0		2.0	8.0	mV
Input Offset Current	$T_A = 25°C$		1.0	3.0		1.0	10	nA
Input Bias Current	$T_A = 25°C$		8.0	20		8.0	40	nA
Supply Voltage Rejection Ratio	$T_A = 25°C$		10	100		10	200	μV/V
Output Voltage Swing	$T_A = 25°C$, $R_L \geq 5\ k\Omega$	22	25		20	25		V
Large Signal Voltage Gain	$T_A = 25°C$, $V_{OUT} = \pm 10V$, $R_L \geq 100\ k\Omega$	100k	180k		70k	180k		V/V
Common-Mode Rejection Ratio	$T_A = 25°C$	80	90		70	90		dB
Input Voltage Range	$T_A = 25°C$	±24	±26		±22	±26		V
Supply Current (Note 5)	$T_A = 25°C$		2.0	4.0		2.0	5.0	mA
Short Circuit Current	$T_A = 25°C$		20			20		mA
Slew Rate	$T_A = 25°C$, $A_V = 1$		2.5			2.5		V/μs
Power Bandwidth	$T_A = 25°C$, $V_{OUT} = 40\ V_{p-p}$, $R_L = 5\ k\Omega$, THD ≤ 1%		20k			20k		Hz
Unity Gain Frequency	$T_A = 25°C$		1.0M			1.0M		Hz
Input Offset Voltage	T_A = Max T_A = Min			6.0 6.0			10 10	mV
Input Offset Current	T_A = Max T_A = Min		0.8 1.8	4.5 7.0		0.8 1.8	14 14	nA
Input Bias Current	T_A = Max T_A = Min		5.0 16	35 35		5.0 16	55 55	nA
Large Signal Voltage Gain	$R_L \geq 100\ k\Omega$, T_A = Max $R_L \geq 100\ k\Omega$, T_A = Min	50k 50k	150k 220k		50k 50k	150k 220k		V/V
Output Voltage Swing	$R_L \geq 5.0\ k\Omega$, T_A = Max $R_L \geq 5.0\ k\Omega$, T_A = Min	22 22	26 25		20 20	26 25		V

Note 1: Absolute maximum ratings are not necessarily concurrent, and care must be taken not to exceed the maximum junction temperature of the LM143 (150°C) or the LM343 (100°C). For operating at elevated temperatures, devices in the H08 package must be derated based on a thermal resistance of 155°C/W, junction to ambient, or 20°C/W, junction to case.

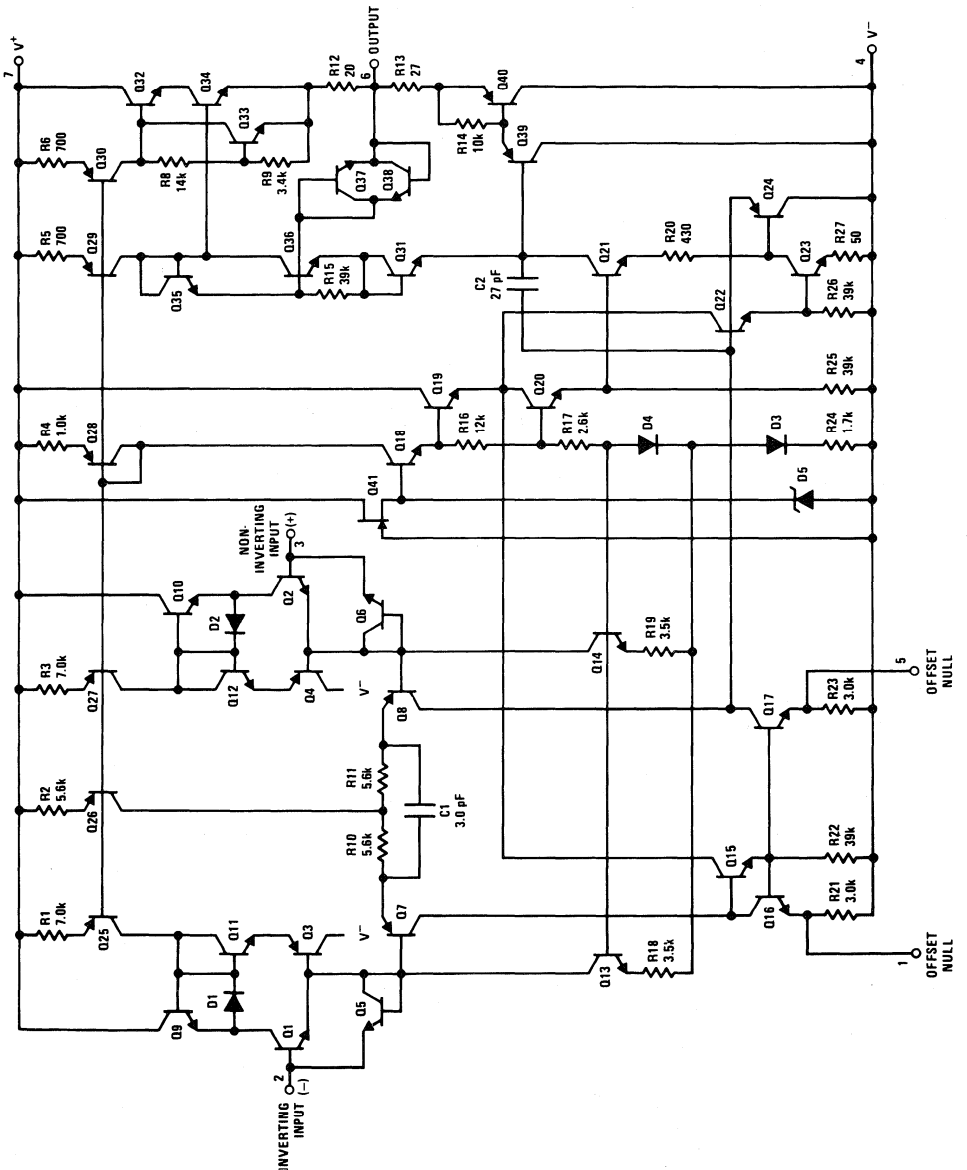
Note 2: For supply voltage less than ±40V for the LM143 and less than ±34V for the LM343, the absolute maximum input voltage is equal to the supply voltage.

Note 3: These specifications apply for $V_S = \pm 28V$. For LM143, T_A = max = 125°C and T_A = min = −55°C. For LM343, T_A = max = 70°C and T_A = min = 0°C.

Note 4: Refer to RETS143X for LM143H and LM1536H military specifications.

Note 5: The maximum supply currents are guaranteed at $V_S = \pm 40V$ for the LM143 and $V_S = \pm 34V$ for the LM343.

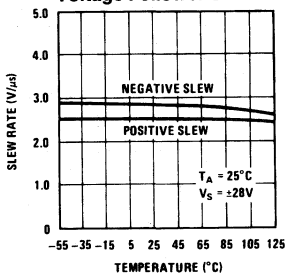
Schematic Diagram



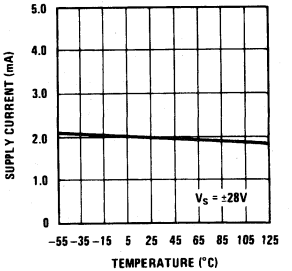
TL/H/7783–2

Typical Performance Characteristics

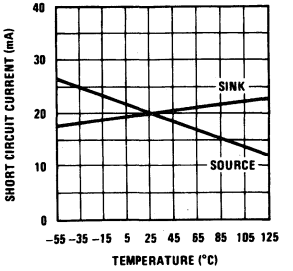
Voltage Follower Slew Rate



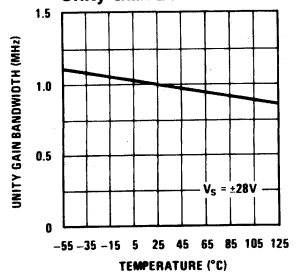
Supply Current



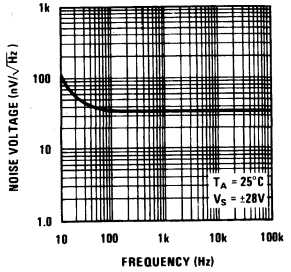
Short Circuit Current



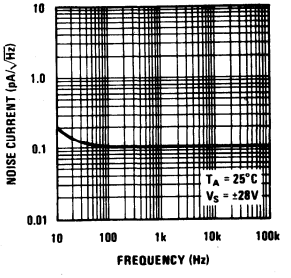
Unity Gain Bandwidth



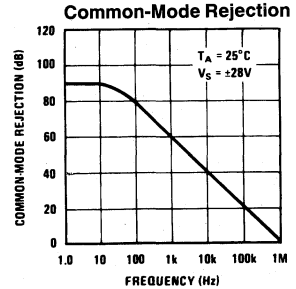
Input Noise Voltage



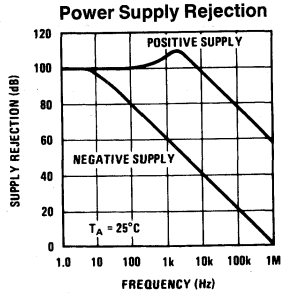
Input Noise Current



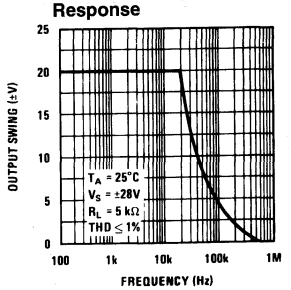
Common-Mode Rejection



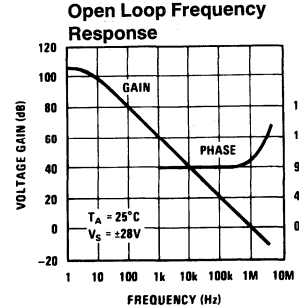
Power Supply Rejection



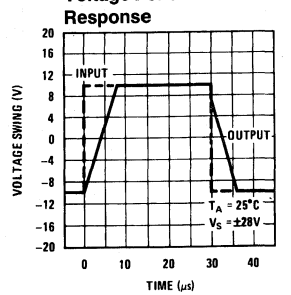
Large Signal Frequency Response



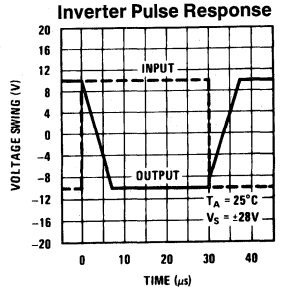
Open Loop Frequency Response



Voltage Follower Pulse Response



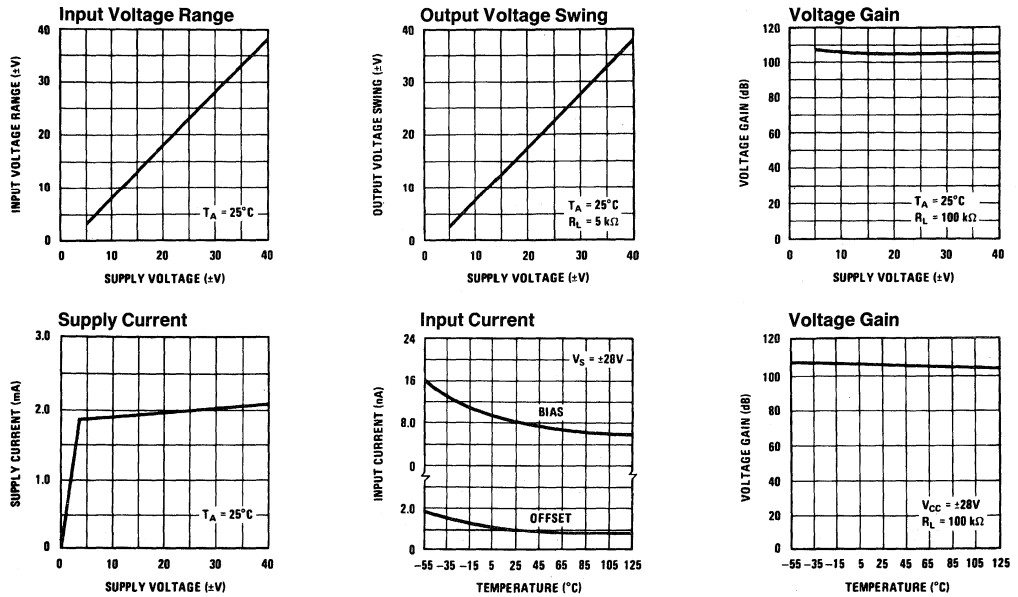
Inverter Pulse Response



TL/H/7783–4

1

Typical Performance Characteristics (Continued)



TL/H/7783–3

Application Hints (See AN-127)

The LM143 is designed for trouble free operation at any supply voltage up to and including the guaranteed maximum of ±40V. Input overvoltage protection, both common-mode and differential, is 100% tested and guaranteed at the maximum supply voltage. Furthermore, all possible high voltage destructive modes during supply voltage turn-on have been eliminated by design. As with most IC op amps, however, certain precautions should be observed to insure that the LM143 remains virtually blow-out proof.

Although output short circuits to ground or either supply can be sustained indefinitely at lower supply voltages, these short circuits should be of limited duration when operating at higher supply voltages. Units can be destroyed by any combination of high ambient temperature, high supply voltages, and high power dissipation which results in excessive die temperature. This is also true when driving low impedance or reactive loads or loads that can revert to low impedance; for example, the LM143 can drive most general purpose op amps outside of the maximum input voltage range, causing heavy current to flow and possibly destroying both devices.

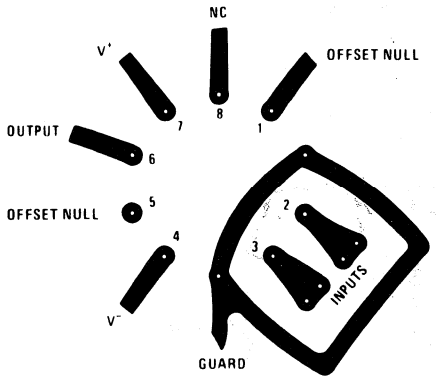
Precautions should be taken to insure that the power supplies never become reversed in polarity—even under transient conditions. With reverse voltage, the IC will conduct excessive current, fusing the internal aluminum interconnects. Voltage reversal between the power supplies will almost always result in a destroyed unit.

In high voltage applications which are sensitive to very low input currents, special precautions should be exercised. For example, with high source resistances, care should be taken to prevent the magnitude of the PC board leakage currents, although quite small, from approaching those of the op amp input currents. These leakage currents become larger at 125°C and are made worse by high supply voltages. To prevent this, PC boards should be properly cleaned and coated to prevent contamination and to provide protection from condensed water vapor when operating below 0°C. A guard ring is also recommended to significantly reduce leakage currents from the op amp input pins to the adjacent high voltage pins in the standard op amp pin connection as shown in *Figure 1. Figures 2, 3* and *4* show how the guard ring is connected for the three most common op amp configurations.

Finally, caution should be exercised in high voltage applications as electrical shock hazards are present. Since the negative supply is connected to the case, users may inadvertantly contact voltages equal to those across the power supplies.

The LM143 can be used as a plug-in replacement in most general purpose op amp applications. The circuits presented in the following section emphasize those applications which take advantage of the unique high voltage abilities of the LM143.

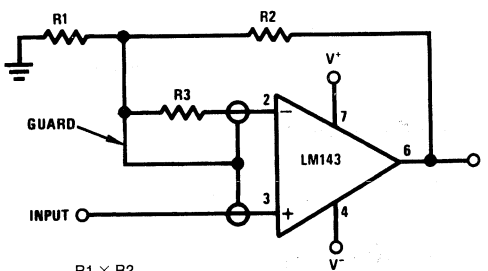
Application Hints (See AN-127) (Continued)



TL 'H/7783–5

Bottom View

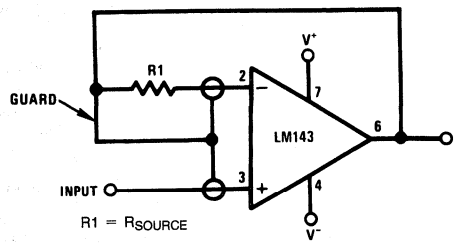
FIGURE 1. Printed Circuit Layout for Input Guarding with TO-5 Package



$$R3 + \frac{R1 \times R2}{R1 + R2} = R_{SOURCE}$$

TL/H/7783–7

FIGURE 3. Guarded Non-Inverting Amplifier



$R1 = R_{SOURCE}$

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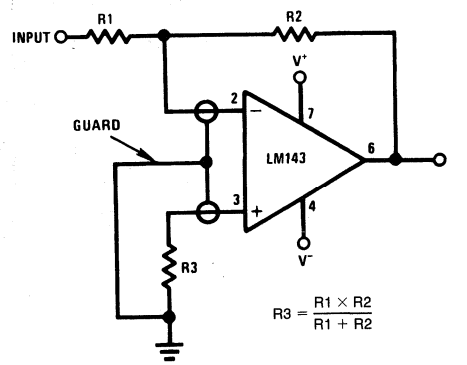
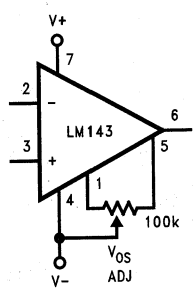
FIGURE 2. Guarded Voltage Follower



$$R3 = \frac{R1 \times R2}{R1 + R2}$$

TL/H/7783–8

FIGURE 4. Guarded Inverting Amplifier

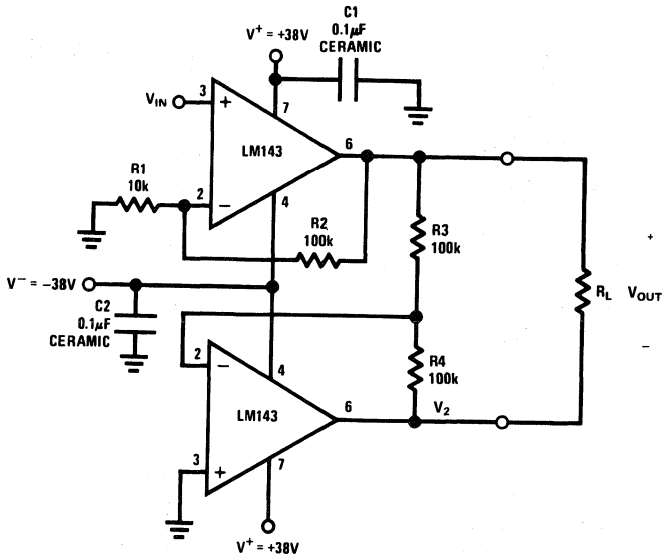


TL/H/7783–14

FIGURE 5. Offset Voltage Adjustment

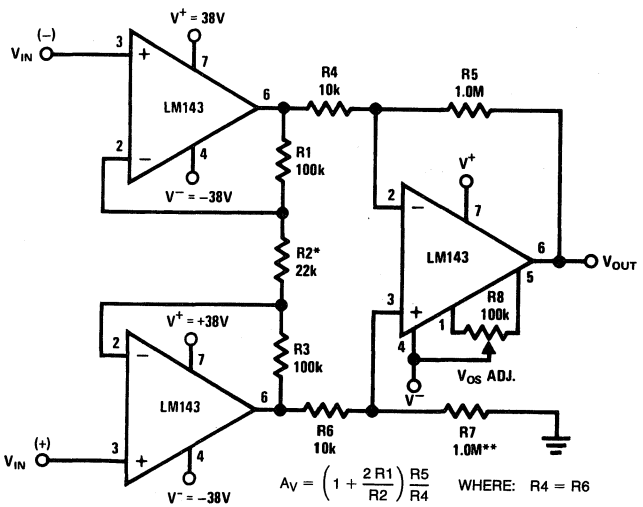
Typical Applications ‡ (For more detail see AN-127)

130 V_{p-p} Drive Across a Floating Load



TL/H/7783–9

±34V Common-Mode Instrumentation Amplifier



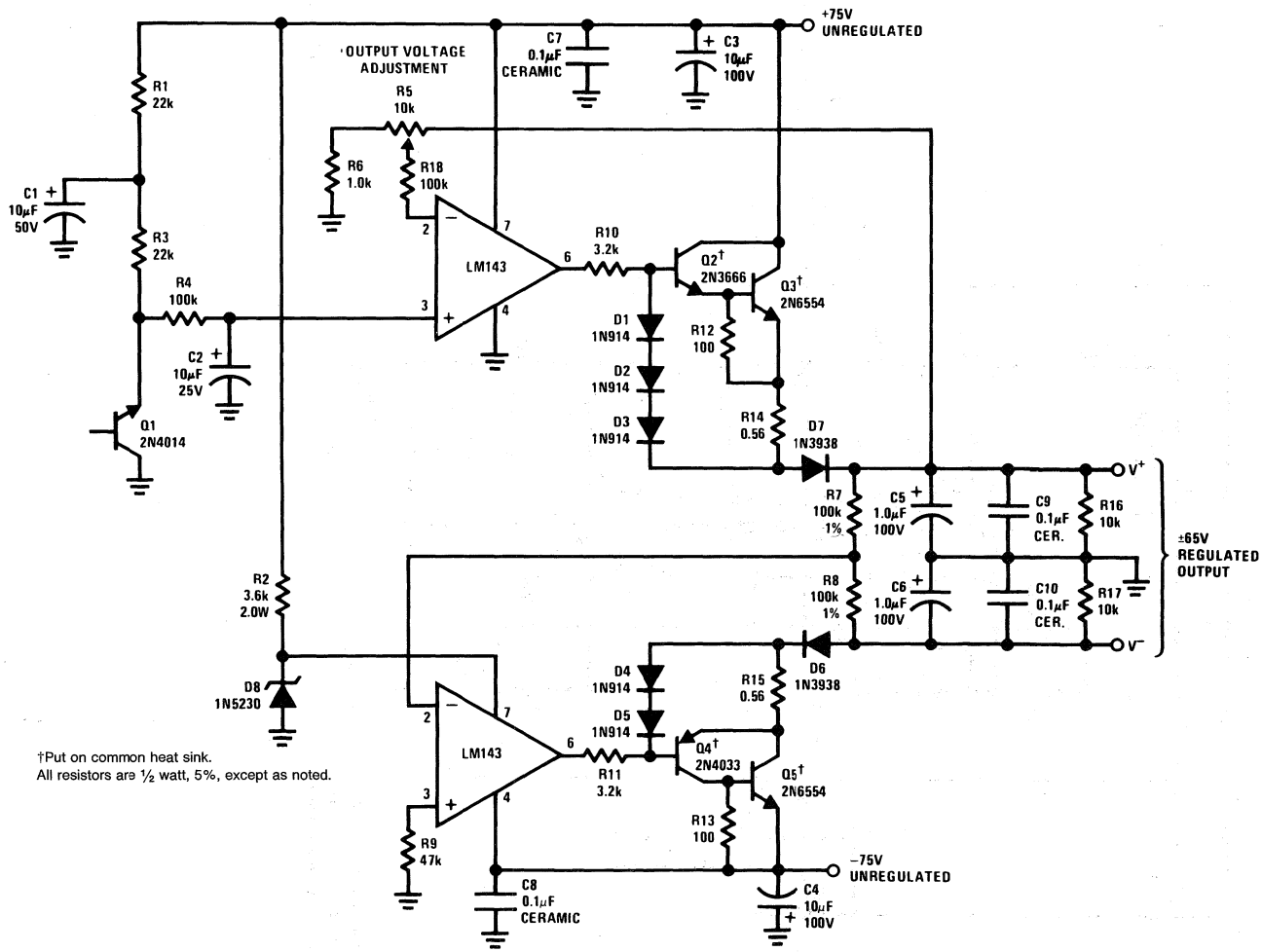
TL/H/7783–10

*R2 may be adjustable to trim the gain.

**R7 may be adjusted to compensate for the resistance tolerance of R4–R7 for best CMR.

‡The 38V supplies allow for a 5% voltage tolerance. All resistors are ½ watt, except as noted.

Tracking ±65V, 1 Amp Power Supply with Short Circuit Protection



†Put on common heat sink.
All resistors are ½ watt, 5%, except as noted.

‡The 38V supplies allow for a 5% voltage tolerance. All resistors are ½ watt, except as noted.

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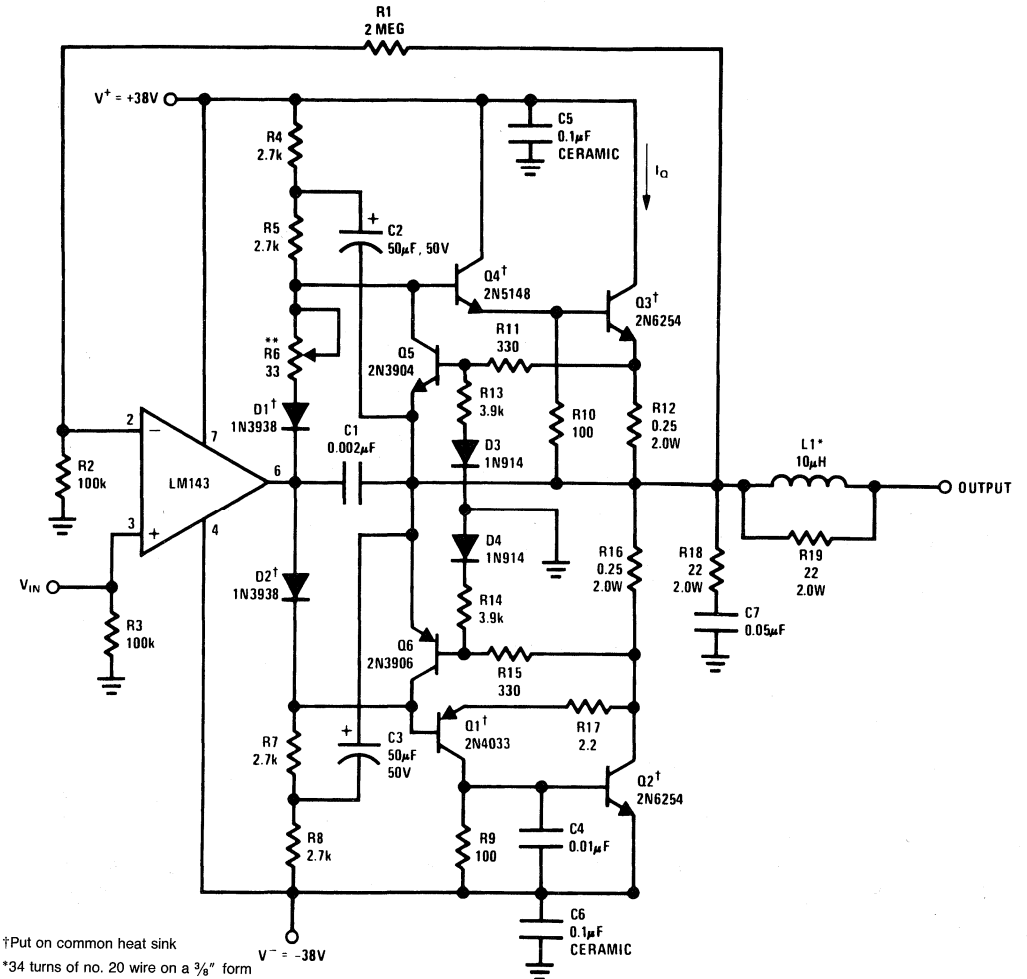
Typical Applications ‡ (Continued) (For more detail see AN-127)

90W Audio Power Amplifier with Safe Area Protection



†Put on common heat sink

*34 turns of no. 20 wire on a ⅜" form

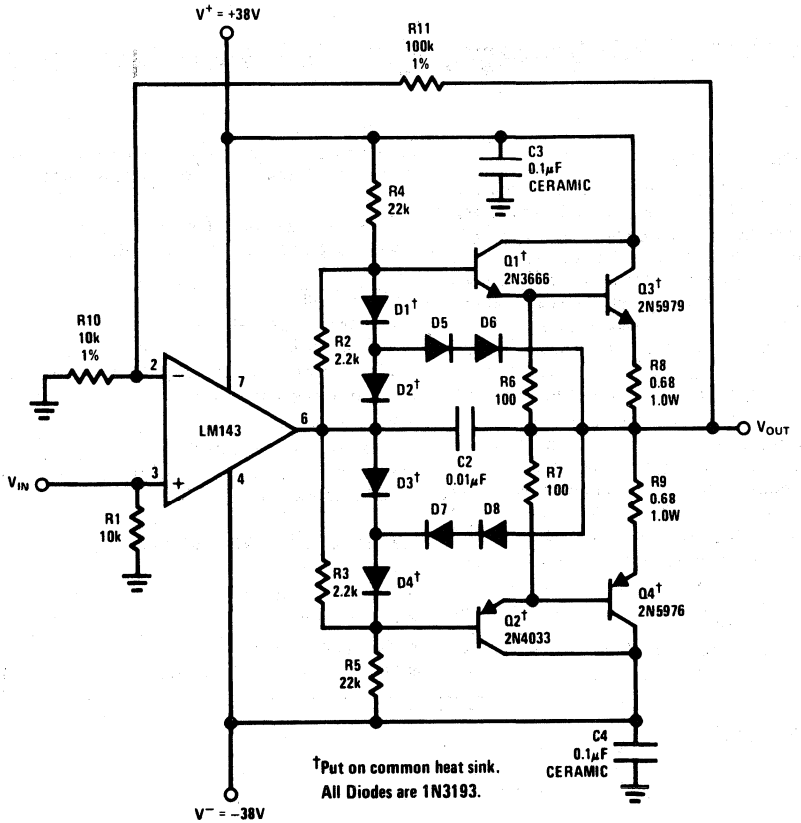
**Adjust R6 to set I_Q = 100 mA

TL/H/7783–12

‡The 38V supplies allow for a 5% voltage tolerance. All resistors are ½ watt, except as noted.

Typical Applications ‡ (Continued) (For more detail see AN-127)

1 Amp Power Amplifier with Short Circuit Protection



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‡The 38V supplies allow for a 5% voltage tolerance. All resistors are ½ watt, except as noted.

National Semiconductor

LM144/LM344 High Voltage, High Slew Rate Operational Amplifier

General Description

The LM144 is a general purpose high voltage, uncompensated operational amplifier featuring operation to ±36V, complete input overvoltage protection up to the supply voltages and input currents comparable to those of other super-β op amps. Increased slew rate, together with high common-mode and supply rejection, insure excellent performance at high supply voltages. Operating characteristics, in particular supply current, slew rate and gain, are virtually independent of supply voltage and temperature. Furthermore, due to thermal symmetry on the die, gain is unaffected by output loading at high supply voltages.

With the unique advantages of low input current, high gain, and high slew rate, the LM144 can increase accuracy and useful frequency range in many existing applications. For example, the LM144 is a plug-in replacement for the LM101A, as well as other general purpose op amps.

The LM144 can be compensated with a single capacitor, thus giving the user the ability to optimize ac parameters to suit the application. For example, in applications such as audio power amplifiers, the LM144 with a gain of 10 can provide a ±30V output swing, a slew rate of approximately 30V/μs, and a 120 kHz full power bandwidth. In applications where capacitive loads or cables must be driven, the LM144 can be overcompensated for increased stability.

The LM344 is similar to the LM144 for applications in less severe supply voltage and temperature environments.

Features

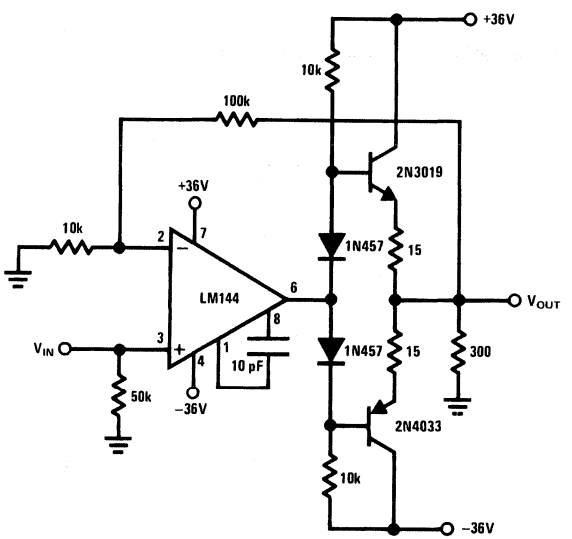
- External compensation provides large power bandwidth ($A_V \geq 10$) — 120 kHz
- Wide operating voltage range — ±4.0V to ±36V
- Large output voltage swing — ±30V
- Wide input common-mode range
- Input overvoltage protection
- Electrical characteristics independent of supply voltage and temperature

Unique Characteristics

- Low input bias current — 8.0 nA
- Low input offset current — 1.0 nA
- High slew rate ($A_V \geq 10$) — 30V/μs
- High voltage gain — 100k min
- Offset voltage null capability

Typical Application

Large Power Bandwidth, Current Boosted Audio Line Driver



TL/H/7784–1

Absolute Maximum Ratings (These ratings are not concurrent)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.
(Note 4)

	LM144	LM344
Supply Voltage	±40V	±34V
Power Dissipation (Note 1)	680 mW	680 mW
Differential Input Voltage (Note 2)	80V	68V
Input Voltage (Note 2)	±40V	±34V
Operating Temperature Range	−55°C to +125°C	0°C to +70°C
Storage Temperature Range	−65°C to +150°C	−65°C to +150°C
Output Short Circuit Duration	5 seconds	5 seconds
Lead Temperature (Soldering, 10 sec)	300°C	300°C

ESD rating to be determined.

Electrical Characteristics (Note 3)

Parameter	Conditions	LM144			LM344			Units
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	$T_A = 25°C$		2.0	5.0		2.0	8.0	mV
Input Offset Current	$T_A = 25°C$		1.0	3.0		1.0	10	nA
Input Bias Current	$T_A = 25°C$		8.0	20		8.0	40	nA
Supply Voltage Rejection Ratio	$T_A = 25°C$		10	100		10	200	μV/V
Output Voltage Swing	$T_A = 25°C$, $R_L \geq 5\ k\Omega$	22	25		20	25		V
Large Signal Voltage Gain	$T_A = 25°C$, $V_{OUT} = \pm 10V$, $R_L \geq 100\ k\Omega$	100k	180k		70k	180k		V/V
Common-Mode Rejection Ratio	$T_A = 25°C$	80	90		70	90		dB
Input Voltage Range	$T_A = 25°C$	24	26		22	26		V
Supply Current	$T_A = 25°C$		2.0	4.0		2.0	5.0	mA
Short Circuit Current	$T_A = 25°C$		20			20		mA
Slew Rate	$T_A = 25°C$, $A_V = 1$ $T_A = 25°C$, $A_V = 10$, C1 = 3 pF		2.5 30			2.5 30		V/μs V/μs
Power Bandwidth	$T_A = 25°C$, $V_{OUT} = 40\ V_{p-p}$, $R_L = 5\ k\Omega$, THD ≤ 1%, $A_V = 1$		20			20		kHz
Unity Gain Frequency	$T_A = 25°C$		1.0			1.0		MHz
Input Offset Voltage	T_A = Max T_A = Min			6.0 6.0			10 10	mV mV
Input Offset Current	T_A = Max T_A = Min		0.8 1.8	4.5 7.0		0.8 1.8	14 14	nA nA
Input Bias Current	T_A = Max T_A = Min		5.0 16	35 35		5.0 16	55 55	nA nA
Large Signal Voltage Gain	$R_L \geq 100\ k\Omega$, T_A = Max $R_L \geq 100\ k\Omega$, T_A = Min	50k 50k	150k 220k		50k 50k	150k 220k		V/V V/V
Output Voltage Swing	$R_L \geq 5.0\ k\Omega$, T_A = Max $R_L \geq 5.0\ k\Omega$, T_A = Min	22 22	26 25		20 20	26 25		V V

Note 1: The maximum junction temperature of the LM144 is 150°C, while that of the LM344 is 100°C. For operating at elevated temperatures, devices in the H08 package must be derated based on a thermal resistance of 150°C/W, junction to ambient, or 20°C/W, junction to case.

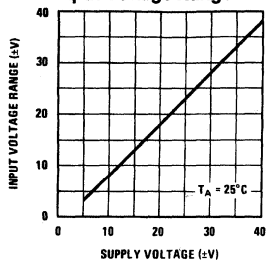
Note 2: For supply voltage less than ±40V for the LM144 and less than ±34V for the LM344, the absolute maximum input voltage is equal to the supply voltage.

Note 3: These specifications apply for $V_S = \pm 28V$. For the LM144, T_A = max = 125°C and T_A = min = −55°C. For the LM344, T_A = max = 70°C and T_A = min = 0°C.

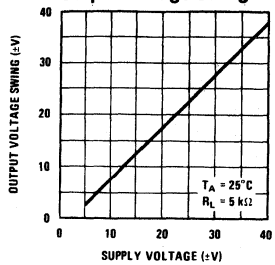
Note 4: Refer to RETS144X for LM144H specifications.

Typical Performance Characteristics

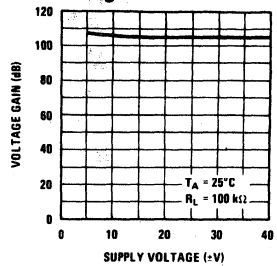
Input Voltage Range



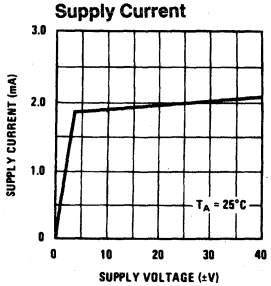
Output Voltage Swing



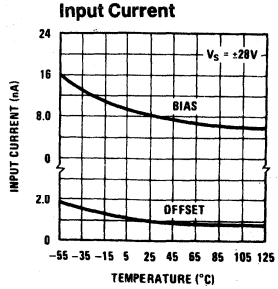
Voltage Gain



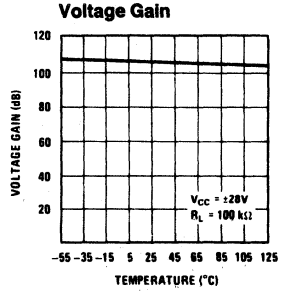
Supply Current



Input Current



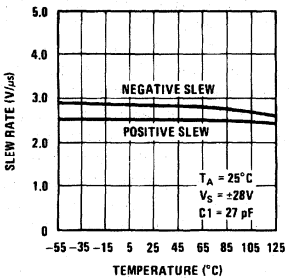
Voltage Gain



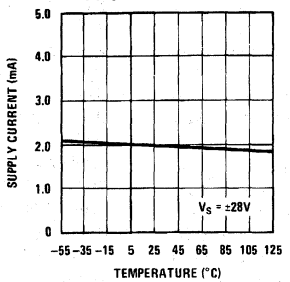
TL/H/7784–3

Typical Performance Characteristics (Continued)

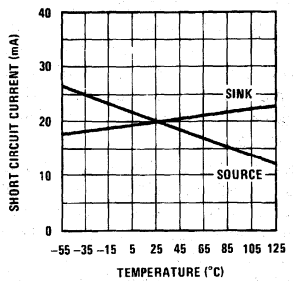
Voltage Follower Slew Rate



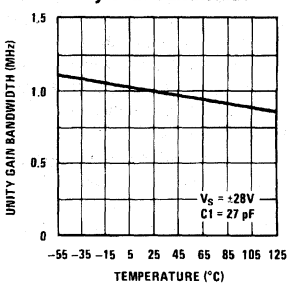
Supply Current



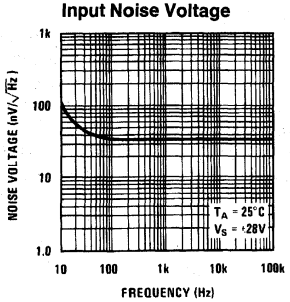
Short Circuit Current



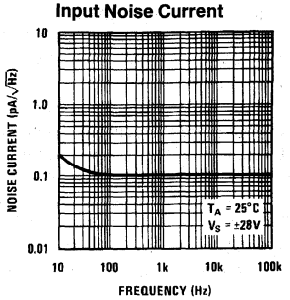
Unity Gain Bandwidth



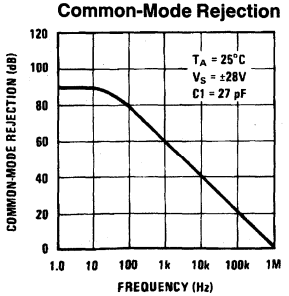
Input Noise Voltage



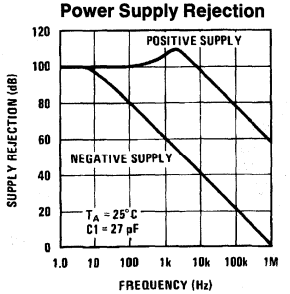
Input Noise Current



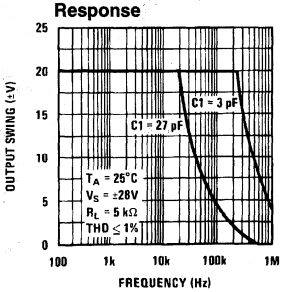
Common-Mode Rejection



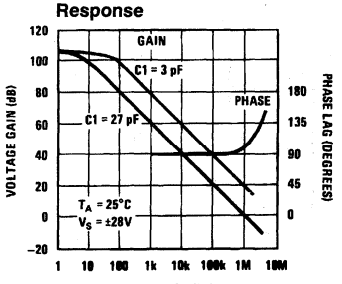
Power Supply Rejection



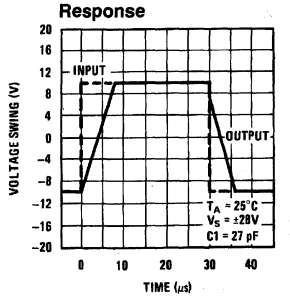
Large Signal Frequency Response



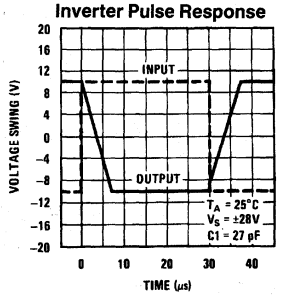
Open Loop Frequency Response



Voltage Follower Pulse Response



Inverter Pulse Response



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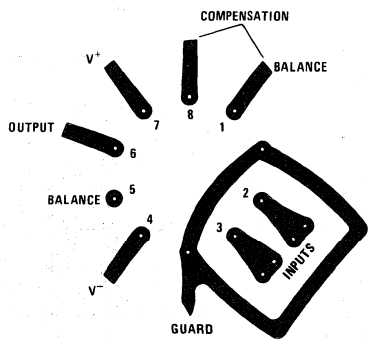
Application Hints (See Also AN-127)

The LM144 is designed for trouble-free operation at any supply voltage up to a maximum of ±40V. Input overvoltage protection, both common-mode and differential, is 100% tested and guaranteed at the maximum supply voltage. Furthermore, all possible high voltage destructive modes during supply voltage turn-on have been eliminated by design. As with most IC op amps, however, certain precautions should be observed to insure that the LM144 remains virtually blow-out proof.

Although output short circuits to ground or either supply can be sustained indefinitely for supply voltages, below ±18V, these short circuits should be of limited duration when operating at higher supply voltages. Units can be destroyed by any combination of high ambient temperature, high supply voltages, and high power dissipation which results in excessive die temperature. This is also true when driving low impedance or reactive loads or loads that can revert to low impedance; for example, the LM144 can drive most general purpose op amps outside of their maximum input voltage range, causing heavy current to flow and possibly destroying both devices.

Precautions should be taken to insure that the power supplies never become reversed in polarity—even under transient conditions. With reverse voltage, the IC will conduct excessive current, fusing the internal aluminum interconnects. Voltage reversal between the power supplies will almost always result in a destroyed unit.

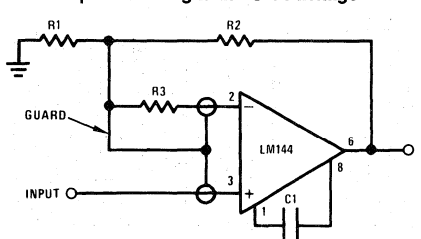
In high voltage applications which are sensitive to very low input currents, special precautions should be exercised.



TL/H/7784–5

Bottom View

FIGURE 1. Printed Circuit Layout for Input Guarding with TO-5 Package



$$R3 + \frac{R1 \times R2}{R1 + R2} = R_{SOURCE}$$

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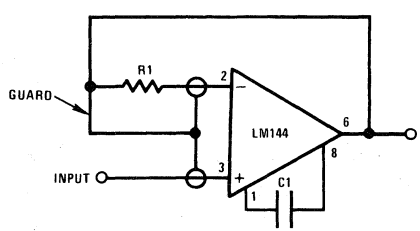
FIGURE 3. Guarded Non-Inverting Amplifier

For example, with high source resistances, care should be taken to prevent the magnitude of the PC board leakage currents, although quite small, from approaching those of the op amp input currents. These leakage currents become larger at 125°C and are made worse by high supply voltages. To prevent this, PC boards should be properly cleaned and coated to prevent contamination and to provide protection from condensed water vapor when operating below 0°C. A guard ring is also recommended to significantly reduce leakage currents from the op amp input pins to the adjacent high voltge pins in the standard op amp pin connection as shown in *Figure 1. Figures 2, 3 and 4* show how the guard ring is connected for the three most common op amp configurations.

The minimum values given for the frequency compensation capacitor are stable only for source resistances less than 10 kΩ, stray capacitances on the summing junction less than 5 pF and capacitive loads smaller than 100 pF. If any of these conditions are not met, it becomes necessary to overcompensate the amplifier with a larger compensation capacitor. Alternately, lead capacitors can be used in the feedback network to negate the effect of stray capacitance and large feedback resistors or an RC network can be added to isolate capacitive loads. See *Figures 5, 6 and 7.*

Finally, caution should be exercised in high voltage applications as electrical shock hazards are present. Since the negative supply is connected to the case, users may inadvertantly contact voltages equal to those across the power supplies.



$R1 = R_{SOURCE}$

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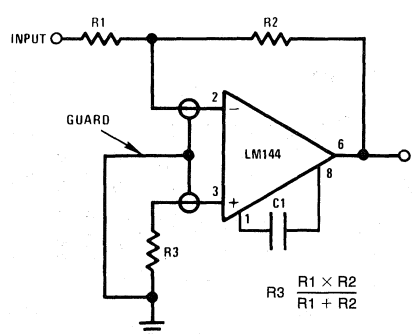
FIGURE 2. Guarded Voltage Follower

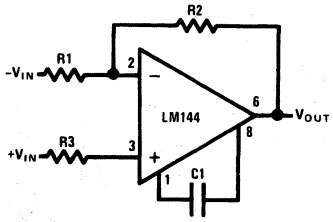


$$R3\ \frac{R1 \times R2}{R1 + R2}$$

TL/H/7784–8

FIGURE 4. Guarded Inverting Amplifier

Application Hints (Continued)



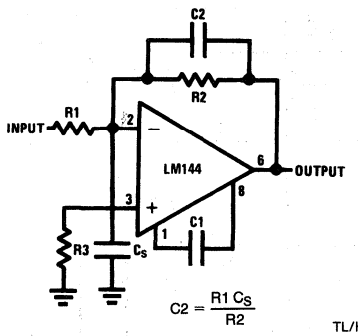
$$C1 = \frac{R1\ C_C}{R1 + R2} \quad \text{NON-INVERTING}$$

$$C1 = \frac{R1\ C_C}{R2} \quad \text{INVERTING}$$

$C_C = 27\ PF$

TL/H/7784–9

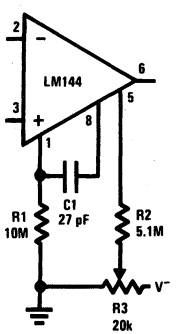
FIGURE 5. Single Pole Compensation



$$C2 = \frac{R1\ C_S}{R2}$$

TL/H/7784–11

FIGURE 7. Compensating For Stray Input Capacitances or Large Feedback Resistor



TL/H/7784–13

FIGURE 9. Balancing Circuit

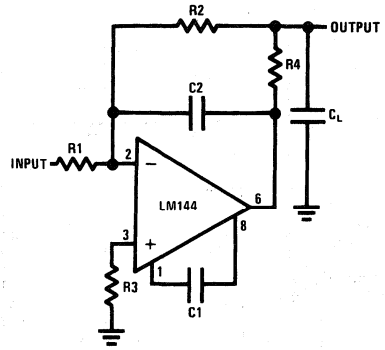


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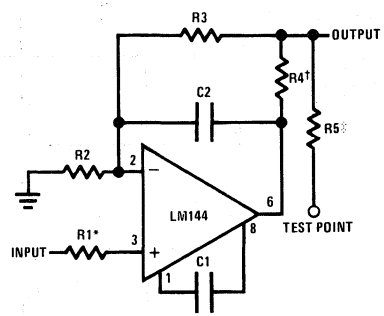
FIGURE 6. Isolating Large Capacitive Loads



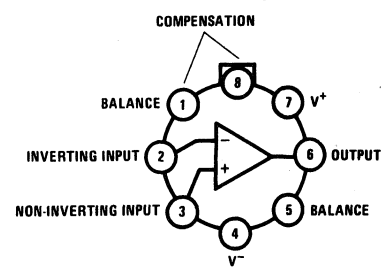
*Protects input
†Protects output
∴Protects output—not needed when R4 is used

TL/H/7784–12

FIGURE 8. Protecting Against Gross Fault Conditions

Connection Diagram

Metal Can Package



TL/H/7784–14

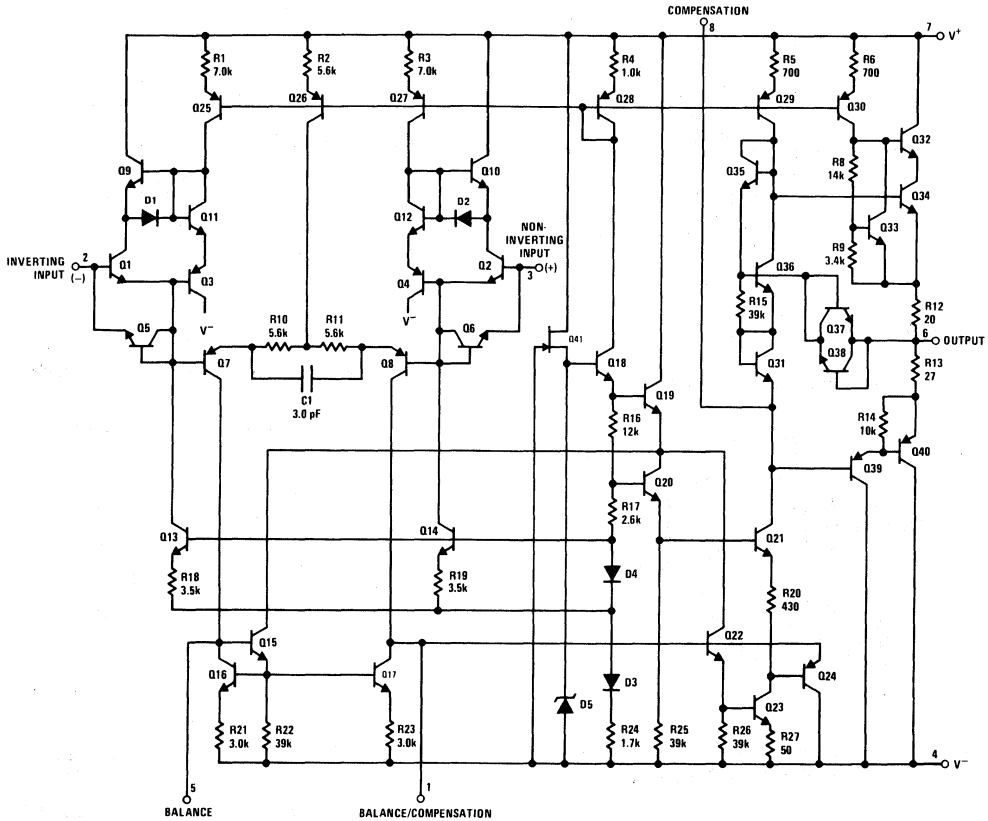
Top View

Pin 4 is connected to case

Order Number LM144H, LM144H/883* or LM344H
See NS Package Number H08C

***Available per SMD# 7800301**

Schematic Diagram



TL/H/7784–2

National Semiconductor

LM146/LM246/LM346 Programmable Quad Operational Amplifiers

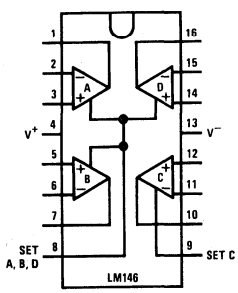
General Description

The LM146 series of quad op amps consists of four independent, high gain, internally compensated, low power, programmable amplifiers. Two external resistors (R_{SET}) allow the user to program the gain bandwidth product, slew rate, supply current, input bias current, input offset current and input noise. For example, the user can trade-off supply current for bandwidth or optimize noise figure for a given source resistance. In a similar way, other amplifier characteristics can be tailored to the application. Except for the two programming pins at the end of the package, the LM146 pin-out is the same as the LM124 and LM148.

Features (I_{SET} = 10 μA)

- Programmable electrical characteristics
- Battery-powered operation
- Low supply current — 350 μA/amplifier
- Guaranteed gain bandwidth product — 0.8 MHz min
- Large DC voltage gain — 120 dB
- Low noise voltage — 28 nV/√Hz
- Wide power supply range — ±1.5V to ±22V
- Class AB output stage–no crossover distortion
- Ideal pin out for Biquad active filters
- Input bias currents are temperature compensated

Connection Diagram (Dual-In-Line Package, Top View)



TL/H/5654–1

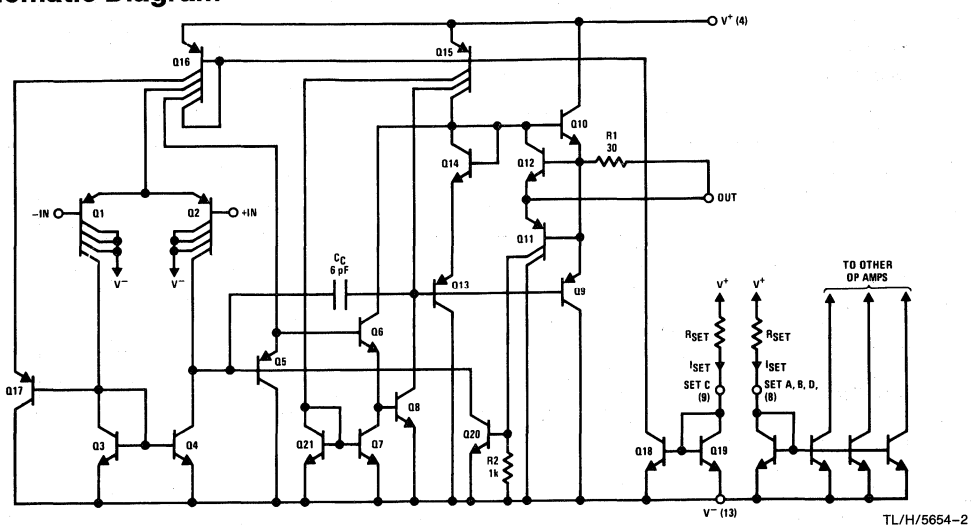
Order Number LM146J, LM146J/883, LM246J, LM346J, LM346M or LM346N
See NS Package Number J16A, M16A or N16A

PROGRAMMING EQUATIONS

Total Supply Current = 1.4 mA (I_{SET}/10 μA)
Gain Bandwidth Product = 1 MHz (I_{SET}/10 μA)
Slew Rate = 0.4V/μs (I_{SET}/10 μA)
Input Bias Current ≅ 50 nA (I_{SET}/10 μA)
I_{SET} = Current into pin 8, pin 9 (see schematic-diagram)

$$I_{SET} = \frac{V^+ - V^- - 0.6V}{R_{SET}}$$

Schematic Diagram



TL/H/5654–2

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.
(Note 5)

	LM146	LM246	LM346
Supply Voltage	±22V	±18V	±18V
Differential Input Voltage (Note 1)	±30V	±30V	±30V
CM Input Voltage (Note 1)	±15V	±15V	±15V
Power Dissipation (Note 2)	900 mW	500 mW	500 mW
Output Short-Circuit Duration (Note 3)	Continuous	Continuous	Continuous
Operating Temperature Range	−55°C to +125°C	−25°C to +85°C	0°C to +70°C
Maximum Junction Temperature	150°C	110°C	100°C
Storage Temperature Range	−65°C to +150°C	−65°C to +150°C	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	260°C	260°C	260°C
Thermal Resistance (θ_{jA}), (Note 2)			
Cavity DIP (J) Pd	900 mW	900 mW	900 mW
θ_{jA}	100°C/W	100°C/W	100°C/W
Small Outline (M) θ_{jA}			115°C/W
Molded DIP (N) Pd			500 mW
θ_{jA}			90°C/W
Soldering Information			
Dual-In-Line Package			
Soldering (10 seconds)	+260°C	+260°C	+260°C
Small Outline Package			
Vapor Phase (60 seconds)	+215°C	+215°C	+215°C
Infrared (15 seconds)	+220°C	+220°C	+220°C

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

ESD rating is to be determined.

DC Electrical Characteristics ($V_S = \pm 15V$, $I_{SET} = 10\ \mu A$, Note 4)

Parameter	Conditions	LM146			LM246/LM346			Units
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	$V_{CM} = 0V$, $R_S \leq 50\Omega$, $T_A = 25°C$		0.5	5		0.5	6	mV
Input Offset Current	$V_{CM} = 0V$, $T_A = 25°C$		2	20		2	100	nA
Input Bias Current	$V_{CM} = 0V$, $T_A = 25°C$		50	100		50	250	nA
Supply Current (4 Op Amps)	$T_A = 25°C$		1.4	2.0		1.4	2.5	mA
Large Signal Voltage Gain	$R_L = 10\ k\Omega$, $\Delta V_{OUT} = \pm 10V$, $T_A = 25°C$	100	1000		50	1000		V/mV
Input CM Range	$T_A = 25°C$	±13.5	±14		±13.5	±14		V
CM Rejection Ratio	$R_S \leq 10\ k\Omega$, $T_A = 25°C$	80	100		70	100		dB
Power Supply Rejection Ratio	$R_S \leq 10\ k\Omega$, $T_A = 25°C$, $V_S = \pm 5$ to $\pm 15V$	80	100		74	100		dB
Output Voltage Swing	$R_L \geq 10\ k\Omega$, $T_A = 25°C$	±12	±14		±12	±14		V
Short-Circuit	$T_A = 25°C$	5	20	35	5	20	35	mA
Gain Bandwidth Product	$T_A = 25°C$	0.8	1.2		0.5	1.2		MHz
Phase Margin	$T_A = 25°C$		60			60		Deg
Slew Rate	$T_A = 25°C$		0.4			0.4		V/μs
Input Noise Voltage	$f = 1$ kHz, $T_A = 25°C$		28			28		nV/√Hz
Channel Separation	$R_L = 10\ k\Omega$, $\Delta V_{OUT} = 0V$ to $\pm 12V$, $T_A = 25°C$		120			120		dB
Input Resistance	$T_A = 25°C$		1.0			1.0		MΩ
Input Capacitance	$T_A = 25°C$		2.0			2.0		pF
Input Offset Voltage	$V_{CM} = 0V$, $R_S \leq 50\Omega$		0.5	6		0.5	7.5	mV
Input Offset Current	$V_{CM} = 0V$		2	25		2	100	nA
Input Bias Current	$V_{CM} = 0V$		50	100		50	250	nA
Supply Current (4 Op Amps)			1.7	2.2		1.7	2.5	mA

DC Electrical Characteristics (Continued) ($V_S = \pm 15V$, $I_{SET} = 10\ \mu A$, Note 4)

Parameter	Conditions	LM146			LM246/LM346			Units
		Min	Typ	Max	Min	Typ	Max	
Large Signal Voltage Gain	$R_L = 10\ k\Omega$, $\Delta V_{OUT} = \pm 10V$	50	1000		25	1000		V/mV
Input CM Range		± 13.5	± 14		± 13.5	± 14		V
CM Rejection Ratio	$R_S \leq 50\Omega$	70	100		70	100		dB
Power Supply Rejection Ratio	$R_S \leq 50\Omega$, $V_S = \pm 5V$ to $\pm 15V$	76	100		74	100		dB
Output Voltage Swing	$R_L \geq 10\ k\Omega$	± 12	± 14		± 12	± 14		V

DC Electrical Characteristic ($V_S = \pm 15V$, $I_{SET} = 1\ \mu A$)

Parameter	Conditions	LM146			LM246/LM346			Units
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	$V_{CM} = 0V$, $R_S \leq 50\Omega$, $T_A = 25°C$		0.5	5		0.5	7	mV
Input Bias Current	$V_{CM} = 0V$, $T_A = 25°C$		7.5	20		7.5	100	nA
Supply Current (4 Op Amps)	$T_A = 25°C$		140	250		140	300	μA
Gain Bandwidth Product	$T_A = 25°C$	80	100		50	100		kHz

DC Electrical Characteristics ($V_S = \pm 1.5V$, $I_{SET} = 10\ \mu A$)

Parameter	Conditions	LM146			LM246/LM346			Units
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	$V_{CM} = 0V$, $R_S \leq 50\Omega$, $T_A = 25°C$		0.5	5		0.5	7	mV
Input CM Range	$T_A = 25°C$	± 0.7			± 0.7			V
CM Rejection Ratio	$R_S \leq 50\Omega$, $T_A = 25°C$		80			80		dB
Output Voltage Swing	$R_L \geq 10\ k\Omega$, $T_A = 25°C$	± 0.6			± 0.6			V

Note 1: For supply voltages less than $\pm 15V$, the absolute maximum input voltage is equal to the supply voltage.

Note 2: The maximum power dissipation for these devices must be derated at elevated temperatures and is dictated by T_{jMAX}, θ_{jA}, and the ambient temperature, T_A. The maximum available power dissipation at any temperature is $P_d = (T_{jMAX} - T_A)/\theta_{jA}$ or the 25°C P_{dMAX}, whichever is less.

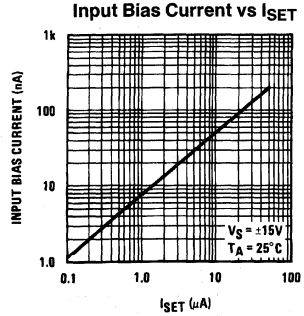
Note 3: Any of the amplifier outputs can be shorted to ground indefinitely; however, more than one should not be simultaneously shorted as the maximum junction temperature will be exceeded.

Note 4: These specifications apply over the absolute maximum operating temperature range unless otherwise noted.

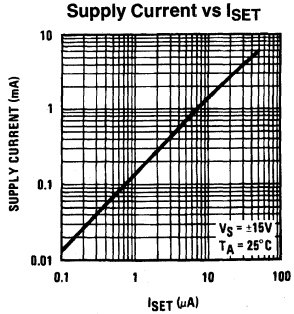
Note 5: Refer to RETS146X for LM146J military specifications.

Typical Performance Characteristics

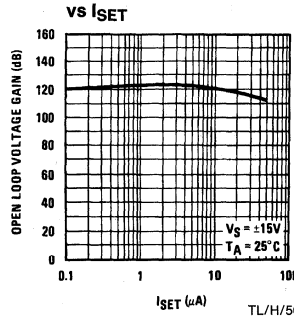
Input Bias Current vs I_{SET}



Supply Current vs I_{SET}



Open Loop Voltage Gain vs I_{SET}



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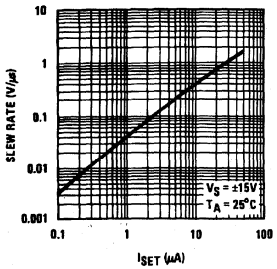
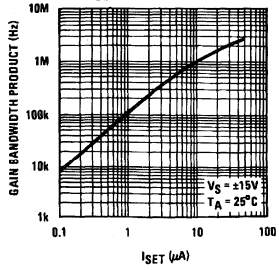
Typical Performance Characteristics

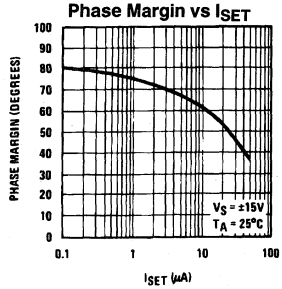
Slew Rate vs I_{SET}



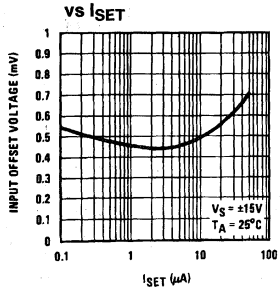
Gain Bandwidth Product vs I_{SET}



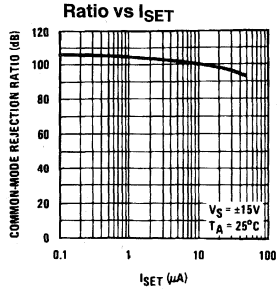
Phase Margin vs I_{SET}



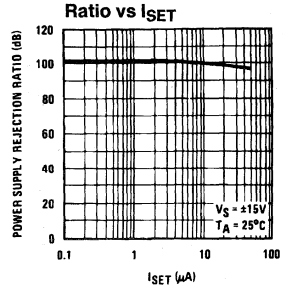
Input Offset Voltage vs I_{SET}



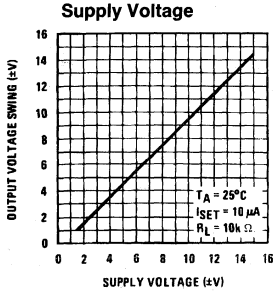
Common-Mode Rejection Ratio vs I_{SET}



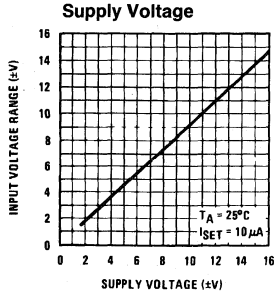
Power Supply Rejection Ratio vs I_{SET}



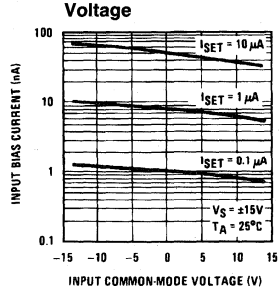
Output Voltage Swing vs Supply Voltage



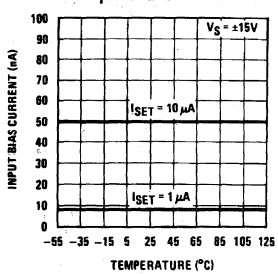
Input Voltage Range vs Supply Voltage



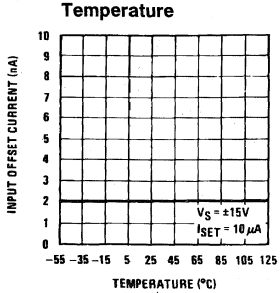
Input Bias Current vs Input Common-Mode Voltage



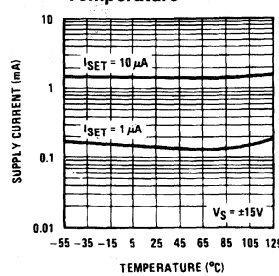
Input Bias Current vs Temperature



Input Offset Current vs Temperature



Supply Current vs Temperature



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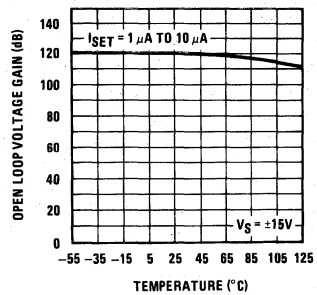
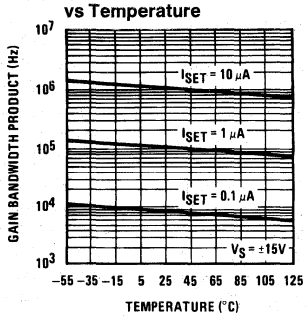
Typical Performance Characteristics (Continued)

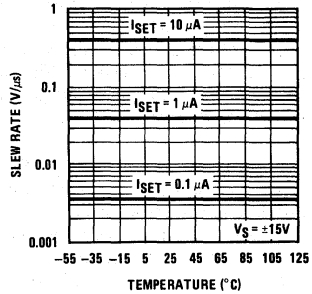
Open Loop Voltage Gain vs Temperature



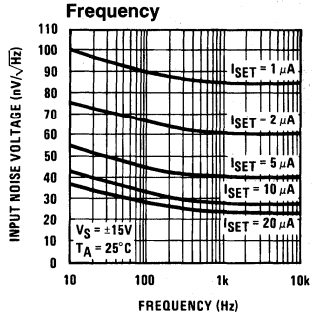
Gain Bandwidth Product vs Temperature



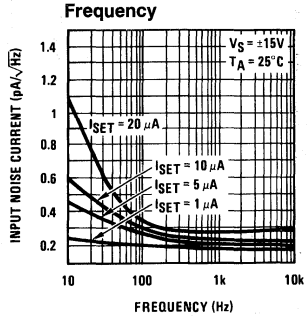
Slew Rate vs Temperature



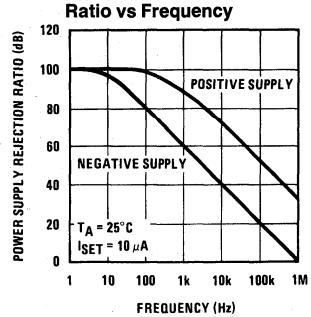
Input Noise Voltage vs Frequency



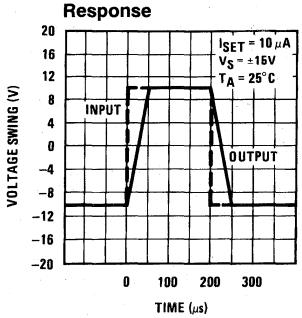
Input Noise Current vs Frequency



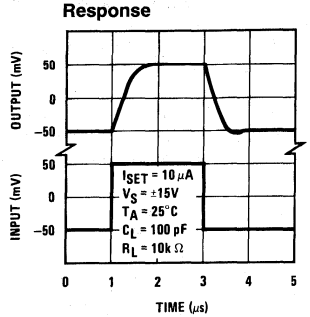
Power Supply Rejection Ratio vs Frequency



Voltage Follower Pulse Response



Voltage Follower Transient Response



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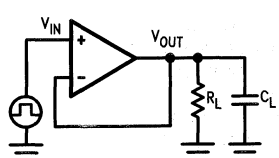
Transient Response Test Circuit



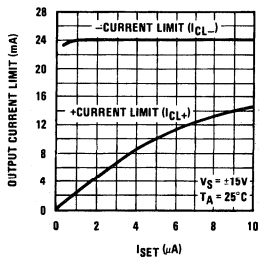
TL/H/5654–6

Application Hints

Avoid reversing the power supply polarity; the device will fail.

Common-Mode Input Voltage: The negative common-mode voltage limit is one diode drop above the negative supply voltage. Exceeding this limit on either input will result in an output phase reversal. The positive common-mode limit is typically 1V below the positive supply voltage. No output phase reversal will occur if this limit is exceeded by either input.

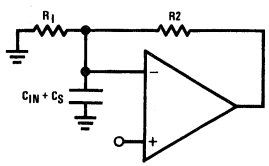
Output Voltage Swing vs I_{SET}: For a desired output voltage swing the value of the minimum load depends on the positive and negative output current capability of the op amp. The maximum available positive output current, (I_{CL+}), of the device increases with I_{SET} whereas the negative output current (I_{CL-}) is independent of I_{SET}. *Figure 1* illustrates the above.



TL/H/5654–7

FIGURE 1. Output Current Limit vs I_{SET}

Input Capacitance: The input capacitance, C_{IN}, of the LM146 is approximately 2 pF; any stray capacitance, C_S, (due to external circuit circuit layout) will add to C_{IN}. When resistive or active feedback is applied, an additional pole is added to the open loop frequency response of the device. For instance with resistive feedback (*Figure 2*), this pole occurs at $\frac{1}{2\pi}$ (R1||R2) (C_{IN} + C_S). Make sure that this pole occurs at least 2 octaves beyond the expected −3 dB frequency corner of the closed loop gain of the amplifier; if not, place a lead capacitor in the feedback such that the time constant of this capacitor and the resistance it parallels is equal to the $R_I(C_S + C_{IN})$, where R_I is the input resistance of the circuit.



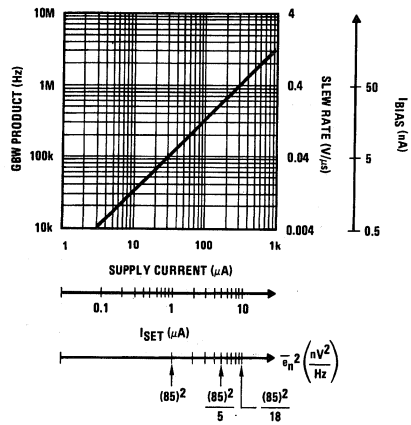
TL/H/5654–9

FIGURE 2

Temperature Effect on the GBW: The GBW (gain bandwidth product), of the LM146 is directly proportional to I_{SET} and inversely proportional to the absolute temperature. When using resistors to set the bias current, I_{SET}, of the device, the GBW product will decrease with increasing temperature. Compensation can be provided by creating an I_{SET} current directly proportional to temperature (see typical applications).

Isolation Between Amplifiers: The LM146 die is isothermally layed out such that crosstalk between *all 4* amplifiers is in excess of −105 dB (DC). Optimum isolation (better than −110 dB) occurs between amplifiers A and D, B and C; that is, if amplifier A dissipates power on its output stage, amplifier D is the one which will be affected the least, and vice versa. Same argument holds for amplifiers B and C.

LM146 Typical Performance Summary: The LM146 typical behaviour is shown in *Figure 3*. The device is fully predictable. As the set current, I_{SET}, increases, the speed, the bias current, and the supply current increase while the noise power decreases proportionally and the V_{OS} remains constant. The usable GBW range of the op amp is 10 kHz to 3.5−4 MHz.

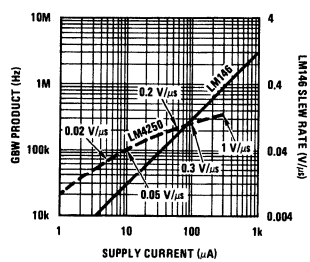


TL/H/5654–8

FIGURE 3. LM146 Typical Characteristics

Low Power Supply Operation: The quad op amp operates down to ±1.3V supply. Also, since the internal circuitry is biased through programmable current sources, no degradation of the device speed will occur.

Speed vs Power Consumption: LM146 vs LM4250 (single programmable). Through *Figure 4*, we observe that the LM146's power consumption has been optimized for GBW products above 200 kHz, whereas the LM4250 will reach a GBW of no more than 300 kHz. For GBW products below 200 kHz, the LM4250 will consume less power.

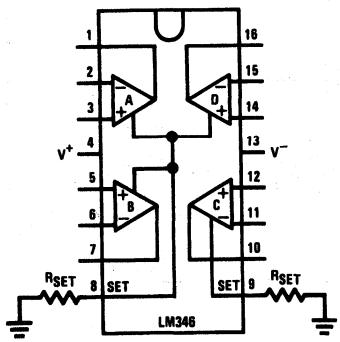


TL/H/5654–10

FIGURE 4. LM146 vs LM4250

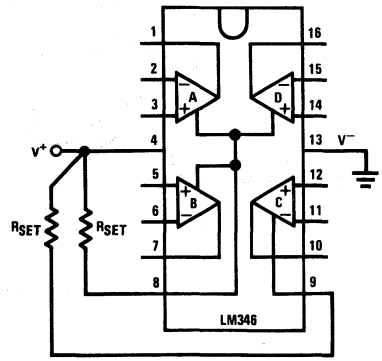
Typical Applications

Dual Supply or Negative Supply Biasing



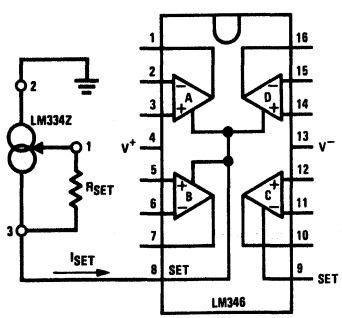
$$I_{SET} \cong \frac{|V-|-0.6V}{R_{SET}}$$

Single (Positive) Supply Biasing



$$I_{SET} \cong \frac{V+-0.6V}{R_{SET}}$$

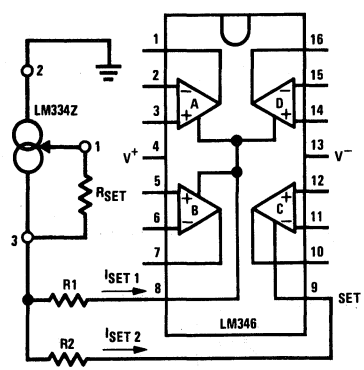
Current Source Biasing with Temperature Compensation



$$I_{SET} = \frac{67.7\ mV}{R_{SET}}$$

- The LM334 provides an I_{SET} directly proportional to absolute temperature. This cancels the slight GBW product Temperature coefficient of the LM346.

Biasing all 4 Amplifiers with Single Current Source



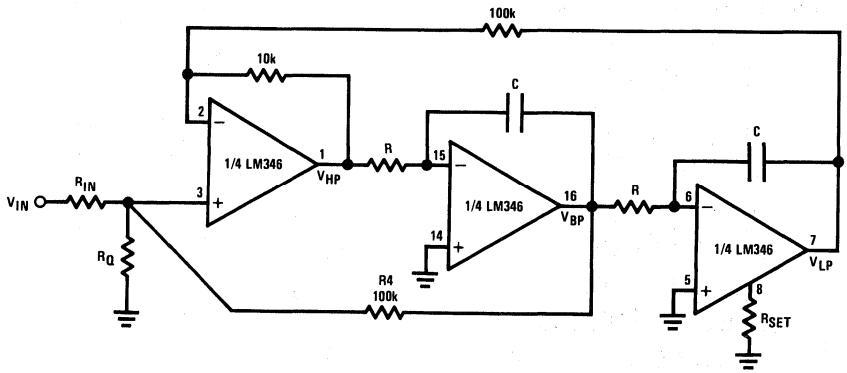
TL/H/5654–11

$$\frac{I_{SET1}}{I_{SET2}} = \frac{R2}{R1},\ I_{SET1} + I_{SET2} = \frac{67.7\ mV}{R_{SET}}$$

- For $I_{SET1} \cong I_{SET2}$ resistors R1 and R2 are not required if a slight error between the 2 set currents can be tolerated. If not, then use R1 = R2 to create a 100 mV drop across these resistors.

Active Filters Applications

Basic (Non-Inverting "State Variable") Active Filter Building Block



TL/H/5654–12

- The LM146 quad programmable op amp is especially suited for active filters because of their adequate GBW product and low power consumption.

Circuit synthesis equations (for circuit analysis equations, consult with the LM148 data sheet).

Need to know desired: f_o = center frequency measured at the BP output

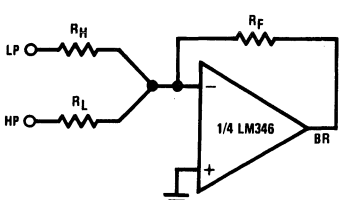
Q_o = quality factor measured at the BP output

H_o = gain at the output of interest (BP or HP or LP or all of them)

- Relation between different gains: $H_{o(BP)} = 0.316 \times Q_o \times H_{o(LP)}$; $H_{o(LP)} = 10 \times H_{o(HP)}$
- $R \times C = \dfrac{5.033 \times 10^{-2}}{f_o}$ (sec)
- For BP output: $R_Q = \left(\dfrac{3.478\,Q_o - H_{o(BP)}}{10^5} - \dfrac{H_{o(BP)}}{10^5 \times 3.748 \times Q_o}\right)^{-1}$; $R_{IN} = \dfrac{\left(\dfrac{3.478\,Q_o}{H_{o(BP)}} - 1\right)}{\dfrac{1}{RQ} + 10^{-5}}$
- For HP ouput: $R_Q = \dfrac{1.1 \times 10^5}{3.478\,Q_o\,(1.1 - H_{o(HP)}) - H_{o(HP)}}$; $R_{IN} = \dfrac{\dfrac{1.1}{H_{o(HP)}} - 1}{\dfrac{1}{RQ} + 10^{-5}}$

Note. All resistor values are given in ohms.

- For LP output: $R_Q = \dfrac{11 \times 10^5}{3.478\,Q_o\,(11 - H_{o(LP)}) - H_{o(LP)}}$; $R_{IN} = \dfrac{\dfrac{11}{H_{o(LP)}} - 1}{\dfrac{1}{RQ} + 10^{-5}}$
- For BR (notch) output: Use the 4th amplifier of the LM146 to sum the LP and HP outputs of the basic filter.



$$\sqrt{\frac{R_H}{R_L}} = 0.316\,\frac{f_{notch}}{f_o}$$

TL/H/5654–13

Determine R_F according to the desired gains: $H_{o(BR)}\Big|_{f<<f_{notch}} = \dfrac{R_F}{R_L} H_{o(LP)}$, $H_{o(BR)}\Big|_{f>>f_{notch}} = \dfrac{R_F}{R_H} H_{o(HP)}$

- **Where to use amplifier C:** Examine the above gain relations and determine the dynamics of the filter. Do not allow slew rate limiting in any output (V_{HP}, V_{BP}, V_{LP}), **that is:**

$$V_{IN(peak)} < 63.66 \times 10^3 \times \frac{I_{SET}}{10\ \mu A} \times \frac{1}{f_o \times H_o}\ (\text{Volts})$$

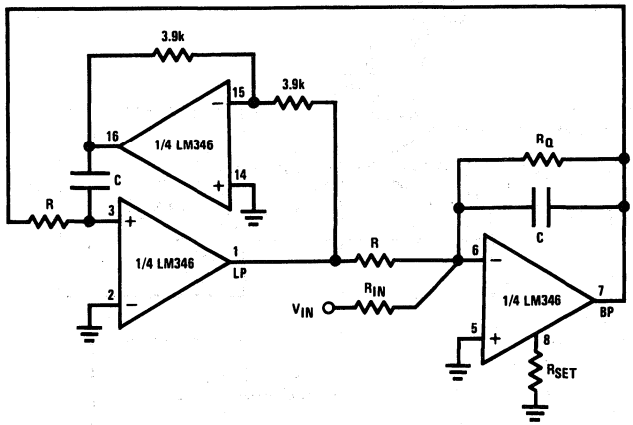
If necessary, use amplifier C, biased at higher I_{SET}, where you get the largest output swing.

Deviation from Theoretical Predictions: Due to the finite GBW products of the op amps the f_o, Q_o will be slightly different from the theoretical predictions.

$$f_{real} \cong \frac{f_o}{1 + \dfrac{2\,f_o}{GBW}},\quad Q_{real} \cong \frac{Q_o}{1 - \dfrac{3.2\,f_o \times Q_o}{GBW}}$$

Active Filters Applications (Continued)

A Simple-to-Design BP, LP Filter Building Block



TL/H/5654–14

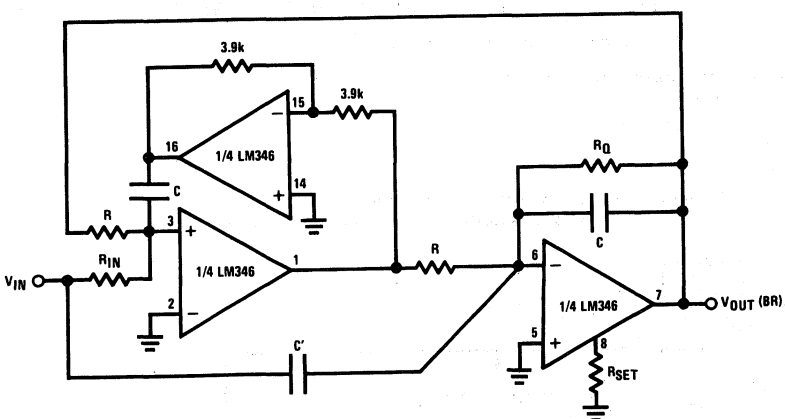
- If resistive biasing is used to set the LM346 performance, the Q_o of this filter building block is nearly insensitive to the op amp's GBW product temperature drift; it has also better noise performance than the state variable filter.

Circuit Synthesis Equations

$$H_{o(BP)} = Q_o H_{o(LP)};\ R \times C = \frac{0.159}{f_o};\ R_Q = Q_o \times R;\ R_{IN} = \frac{R_Q}{H_{o(BP)}} = \frac{R}{H_{o(LP)}}$$

- For the eventual use of amplifier C, see comments on the previous page.

A 3-Amplifier Notch Filter (or Elliptic Filter Building Block)



TL/H/5654–15

Circuit Synthesis Equations

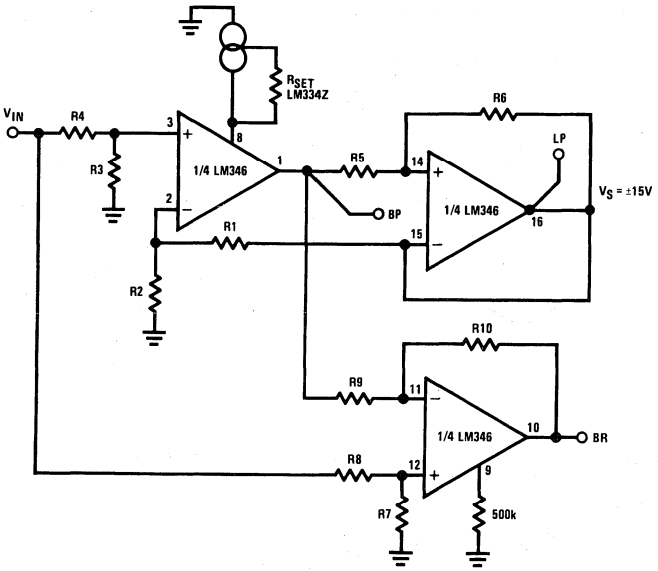
$$R \times C = \frac{0.159}{f_o};\ R_o = Q_o \times R;\ R_{IN} = \frac{0.159 \times f_o}{C' \times f^2_{notch}}$$

$$H_{o(BR)}\Big|_{f<<f_{notch}} = \frac{R}{R_{IN}} H_{o(BR)}\Big|_{f>>f_{notch}} = \frac{C'}{C}$$

- For nothing but a notch output: $R_{IN} = R$, $C' = C$.

Active Filters Applications (Continued)

Capacitorless Active Filters (Basic Circuit)



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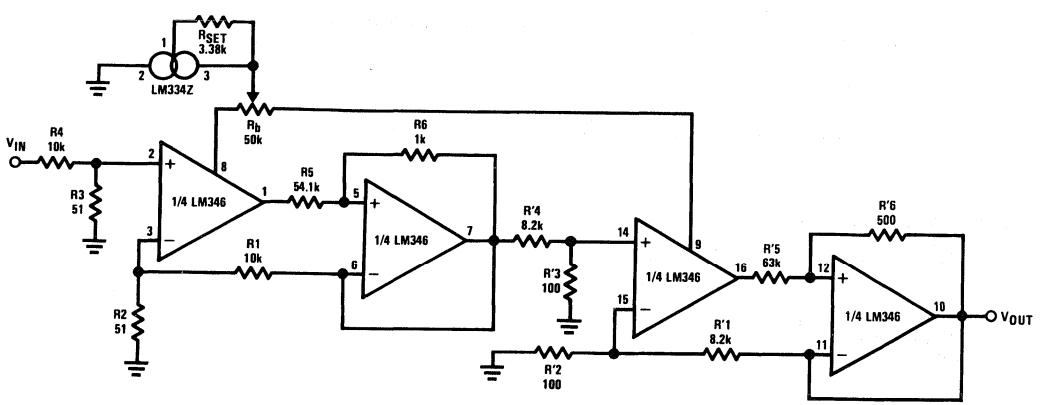
- This is a BP, LP, BR filter. The filter characteristics are created by using the tunable frequency response of the LM346.
- **Limitations:** $Q_o < 10$, $f_o \times Q_o < 1.5$ MHz, output voltage should not exceed Vpeak(out) $\leq \frac{63.66 \times 10^3}{f_o} \times \frac{I_{SET}(\mu A)}{10\ \mu A}$ (V)
- Design equations: $a = \frac{R6 + R5}{R6}$, $b = \frac{R2}{R1 + R2}$, $c = \frac{R3}{R3 + R4}$, $d = \frac{R7}{R8 + R7}$, $e = \frac{R10}{R(+ R10}$, $f_{o(BP)} = f_u\sqrt{\frac{b}{a}}$, $H_{o(BP)} = a \times c$, $H_{o(LP)} = \frac{c}{b}$, $Q_o = \sqrt{a \times b}$

  $f_{o(BR)} = f_{o(BP)}$, $\left(1 - \frac{c}{b}\right) \cong f_{o(BP)}$ $(C << 1)$ provided that $d = H_{o(BP)} \times e$, $H_{o(BR)} = \frac{R10}{R9}$.
- Advantage: f_oQ_o, H_o can be independently adjusted; that is, the filter is extremely easy to tune.
- Tuning procedure (ex. BP tuning)
  1. Pick up a convenient value for b; $(b < 1)$
  2. Adjust Q_o through R5
  3. Adjust $H_{o(BP)}$ through R4
  4. Adjust f_o through R_{SET}. This adjusts the unity gain frequency (f_u) of the op amp.

A 4th Order Butterworth Low Pass Capacitorless Filter



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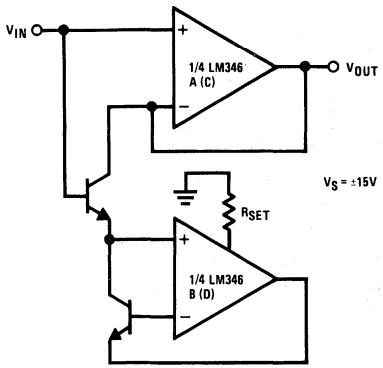
Ex: f_c = 20 kHz, H_o (gain of the filter) = 1, Q_{01} = 0.541, Q_{o2} = 1.306.

- Since for this filter the GBW product of all 4 amplifiers has been designed to be the same (~1 MHz) only one current source can be used to bias the circuit. Fine tuning can be further accomplished through R_b.

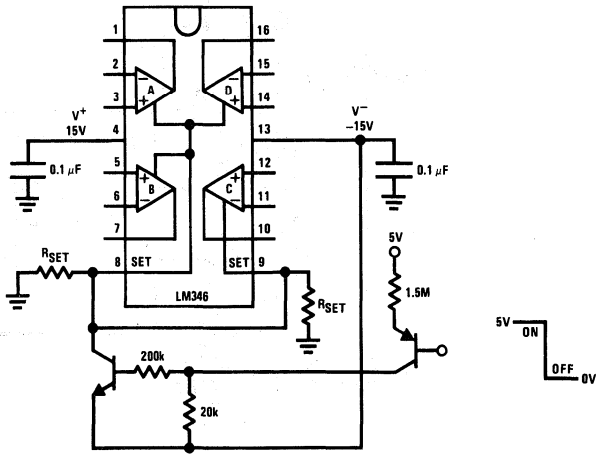
Miscellaneous Applications

A Unity Gain Follower with Bias Current Reduction



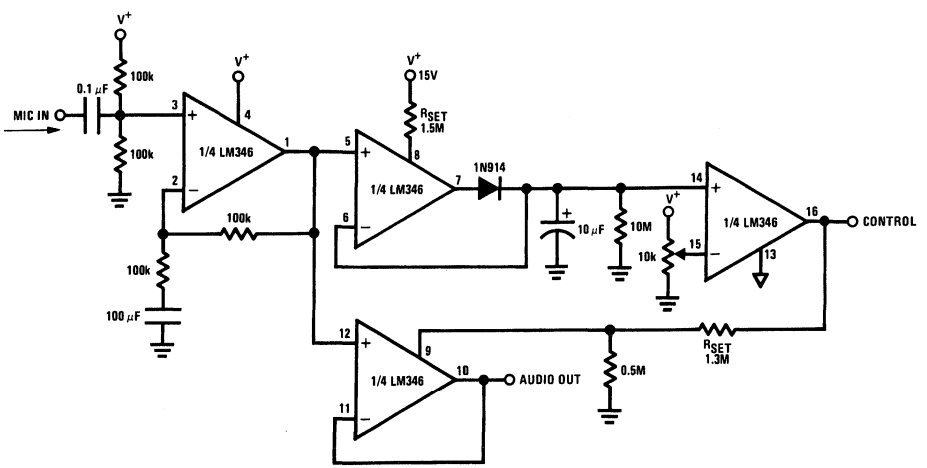
• For better performance, use a matched NPN pair.

Circuit Shutdown



• By pulling the SET pin(s) to V⁻ the op amp(s) shuts down and its output goes to a high impedance state. According to this property, the LM346 can be used as a very low speed analog switch.

Voice Activated Switch and Amplifier



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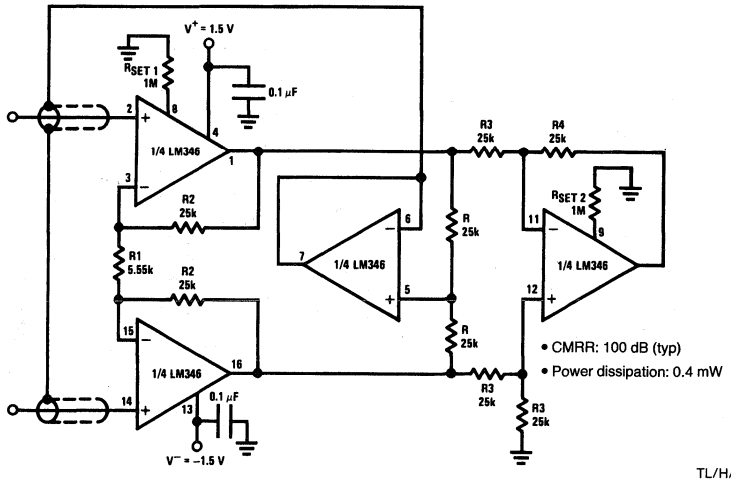
Miscellaneous Applications (Continued)

X10 Micropower Instrumentation Amplifier with Buffered Input Guarding



TL/H/5654–19

National Semiconductor

LM148/LM149 Series Quad 741 Op Amp

LM148/LM248/LM348 Quad 741 Op Amps
LM149/LM349 Wide Band Decompensated ($A_{V\,(MIN)} = 5$)

General Description

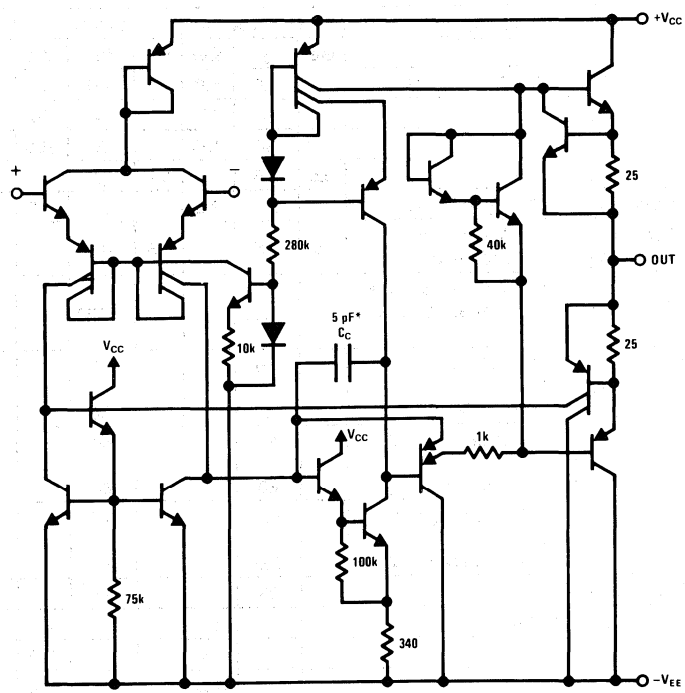
The LM148 series is a true quad 741. It consists of four independent, high gain, internally compensated, low power operational amplifiers which have been designed to provide functional characteristics identical to those of the familiar 741 operational amplifier. In addition the total supply current for all four amplifiers is comparable to the supply current of a single 741 type op amp. Other features include input offset currents and input bias current which are much less than those of a standard 741. Also, excellent isolation between amplifiers has been achieved by independently biasing each amplifier and using layout techniques which minimize thermal coupling. The LM149 series has the same features as the LM148 plus a gain bandwidth product of 4 MHz at a gain of 5 or greater.

The LM148 can be used anywhere multiple 741 or 1558 type amplifiers are being used and in applications where amplifier matching or high packing density is required.

Features

- 741 op amp operating characteristics
- Low supply current drain 0.6 mA/Amplifier
- Class AB output stage—no crossover distortion
- Pin compatible with the LM124
- Low input offset voltage 1 mV
- Low input offset current 4 nA
- Low input bias current 30 nA
- Gain bandwidth product
  - LM148 (unity gain) 1.0 MHz
  - LM149 ($A_V \geq 5$) 4 MHz
- High degree of isolation between amplifiers 120 dB
- Overload protection for inputs and outputs

Schematic Diagram



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*1 pF in the LM149

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.
(Note 4)

	LM148/LM149	LM248	LM348/LM349
Supply Voltage	±22V	±18V	±18V
Differential Input Voltage	±44V	±36V	±36V
Output Short Circuit Duration (Note 1)	Continuous	Continuous	Continuous
Power Dissipation (P_d at 25°C) and			
Thermal Resistance (θ_{jA}), (Note 2)			
Molded DIP (N) P_d	—	—	750 mW
θ_{jA}	—	—	100°C/W
Cavity DIP (J) P_d	1100 mW	800 mW	700 mW
θ_{JA}	110°C/W	110°C/W	110°C/W
Maximum Junction Temperature (T_{jMAX})	150°C	110°C	100°C
Operating Temperature Range	$-55°C \le T_A \le +125°C$	$-25°C \le T_A \le +85°C$	$0°C \le T_A \le +70°C$
Storage Temperature Range	−65°C to +150°C	−65°C to +150°C	−65°C to +150°C
Lead Temperature (Soldering, 10 sec.) Ceramic	300°C	300°C	300°C
Lead Temperature (Soldering, 10 sec.) Plastic			260°C
Soldering Information			
Dual-In-Line Package			
Soldering (10 seconds)	260°C	260°C	260°C
Small Outline Package			
Vapor Phase (60 seconds)	215°C	215°C	215°C
Infrared (15 seconds)	220°C	220°C	220°C
See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.			
ESD tolerance (Note 5)	500V	500V	500V

Electrical Characteristics (Note 3)

Parameter	Conditions	LM148/LM149			LM248			LM348/LM349			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	$T_A = 25°C$, $R_S \le 10\ k\Omega$		1.0	5.0		1.0	6.0		1.0	6.0	mV
Input Offset Current	$T_A = 25°C$		4	25		4	50		4	50	nA
Input Bias Current	$T_A = 25°C$		30	100		30	200		30	200	nA
Input Resistance	$T_A = 25°C$	0.8	2.5		0.8	2.5		0.8	2.5		MΩ
Supply Current All Amplifiers	$T_A = 25°C$, $V_S = \pm 15V$		2.4	3.6		2.4	4.5		2.4	4.5	mA
Large Signal Voltage Gain	$T_A = 25°C$, $V_S = \pm 15V$ $V_{OUT} = \pm 10V$, $R_L \ge 2\ k\Omega$	50	160		25	160		25	160		V/mV
Amplifier to Amplifier Coupling	$T_A = 25°C$, f = 1 Hz to 20 kHz (Input Referred) See Crosstalk Test Circuit		−120			−120			−120		dB
Small Signal Bandwidth	LM148 Series $T_A = 25°C$ LM149 Series		1.0 4.0			1.0 4.0			1.0 4.0		MHz MHz
Phase Margin	LM148 Series ($A_V = 1$) $T_A = 25°C$ LM149 Series ($A_V = 5$)		60 60			60 60			60 60		degrees degrees
Slew Rate	LM148 Series ($A_V = 1$) $T_A = 25°C$ LM149 Series ($A_V = 5$)		0.5 2.0			0.5 2.0			0.5 2.0		V/μs V/μs
Output Short Circuit Current	$T_A = 25°C$		25			25			25		mA
Input Offset Voltage	$R_S \le 10\ k\Omega$			6.0			7.5			7.5	mV
Input Offset Current				75			125			100	nA
Input Bias Current				325			500			400	nA

Electrical Characteristics (Note 3) (Continued)

Parameter	Conditions	LM148/LM149			LM248			LM348/LM349			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Large Signal Voltage Gain	$V_S = \pm 15V$, $V_{OUT} = \pm 10V$, $R_L > 2\ k\Omega$	25			15			15			V/mV
Output Voltage Swing	$V_S = \pm 15V$, $R_L = 10\ k\Omega$ $R_L = 2\ k\Omega$	± 12 ± 10	± 13 ± 12		± 12 ± 10	± 13 ± 12		± 12 ± 10	± 13 ± 12		V V
Input Voltage Range	$V_S = \pm 15V$	± 12			± 12			± 12			V
Common-Mode Rejection Ratio	$R_S \leq 10\ k\Omega$	70	90		70	90		70	90		dB
Supply Voltage Rejection	$R_S \leq 10\ k\Omega$, $\pm 5V \leq V_S \leq \pm 15V$	77	96		77	96		77	96		dB

Note 1: Any of the amplifier outputs can be shorted to ground indefinitely; however, more than one should not be simultaneously shorted as the maximum junction temperature will be exceeded.

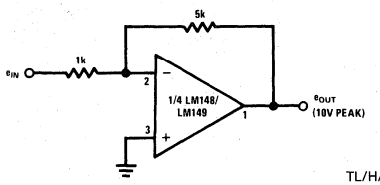
Note 2: The maximum power dissipation for these devices must be derated at elevated temperatures and is dicated by T_{jMAX}, θ_{jA}, and the ambient temperature, T_A. The maximum available power dissipation at any temperature is $P_d = (T_{jMAX} - T_A)/\theta_{jA}$ or the 25°C P_{dMAX}, whichever is less.

Note 3: These specifications apply for $V_S = \pm 15V$ and over the absolute maximum operating temperature range ($T_L \leq T_A \leq T_H$) unless otherwise noted.

Note 4: Refer to RETS 148X for LM148 military specifications and refer to RETS 149X for LM149 military specifications.

Note 5: Human body model, 1.5 kΩ in series with 100 pF.

Cross Talk Test Circuit



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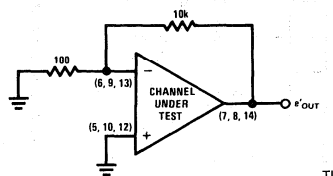

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$$\text{Crosstalk} = -20 \log \frac{e'_{OUT}}{101 \times e_{OUT}} \text{(dB)}$$

$V_S = \pm 15V$

Application Hints

The LM148 series are quad low power 741 op amps. In the proliferation of quad op amps, these are the first to offer the convenience of familiar, easy to use operating characteristics of the 741 op amp. In those applications where 741 op amps have been employed, the LM148 series op amps can be employed directly with no change in circuit performance.

The LM149 series has the same characteristics as the LM148 except it has been decompensated to provide a wider bandwidth. As a result the part requires a minimum gain of 5.

The package pin-outs are such that the inverting input of each amplifier is adjacent to its output. In addition, the amplifier outputs are located in the corners of the package which simplifies PC board layout and minimizes package related capacitive coupling between amplifiers.

The input characteristics of these amplifiers allow differential input voltages which can exceed the supply voltages. In addition, if either of the input voltages is within the operating common-mode range, the phase of the output remains correct. If the negative limit of the operating common-mode range is exceeded at both inputs, the output voltage will be positive. For input voltages which greatly exceed the maximum supply voltages, either differentially or common-mode, resistors should be placed in series with the inputs to limit the current.

Like the LM741, these amplifiers can easily drive a 100 pF capacitive load throughout the entire dynamic output voltage and current range. However, if very large capacitive loads must be driven by a non-inverting unity gain amplifier, a resistor should be placed between the output (and feedback connection) and the capacitance to reduce the phase shift resulting from the capacitive loading.

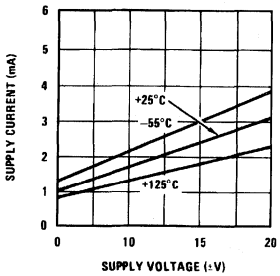
The output current of each amplifier in the package is limited. Short circuits from an output to either ground or the power supplies will not destroy the unit. However, if multiple output shorts occur simultaneously, the time duration should be short to prevent the unit from being destroyed as a result of excessive power dissipation in the IC chip.

As with most amplifiers, care should be taken lead dress, component placement and supply decoupling in order to ensure stability. For example, resistors from the output to an input should be placed with the body close to the input to minimize "pickup" and maximize the frequency of the feedback pole which capacitance from the input to ground creates.

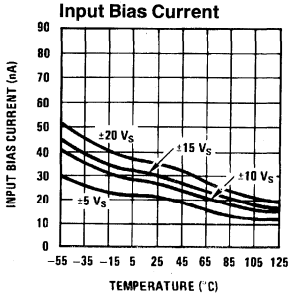
A feedback pole is created when the feedback around any amplifier is resistive. The parallel resistance and capacitance from the input of the device (usually the inverting input) to AC ground set the frequency of the pole. In many instances the frequency of this pole is much greater than the expected 3 dB frequency of the closed loop gain and consequently there is negligible effect on stability margin. However, if the feedback pole is less than approximately six times the expected 3 dB frequency a lead capacitor should be placed from the output to the input of the op amp. The value of the added capacitor should be such that the RC time constant of this capacitor and the resistance it parallels is greater than or equal to the original feedback pole time constant.

Typical Performance Characteristics

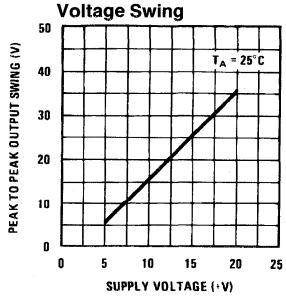
Supply Current



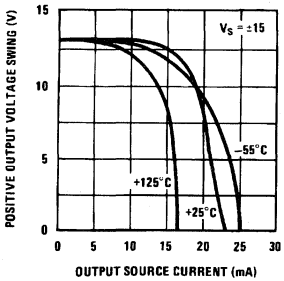
Input Bias Current



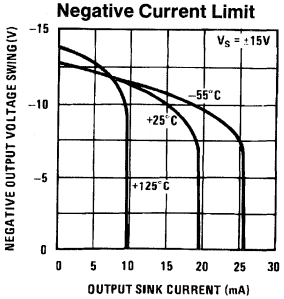
Voltage Swing



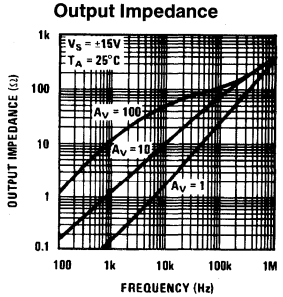
Positive Current Limit



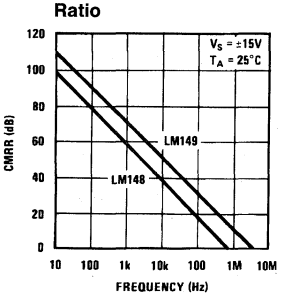
Negative Current Limit



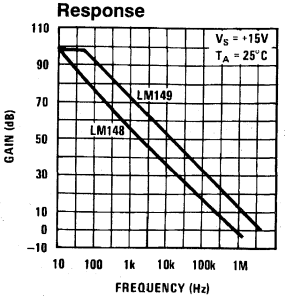
Output Impedance



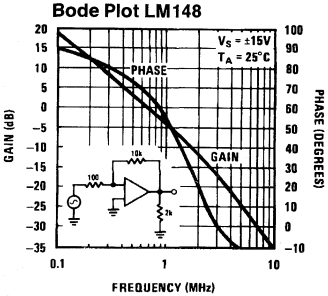
Common-Mode Rejection Ratio



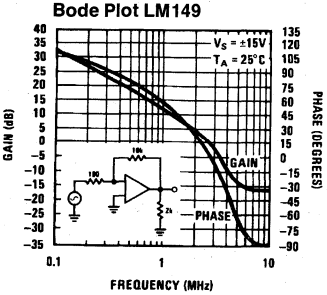
Open Loop Frequency Response



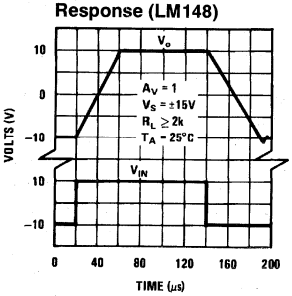
Bode Plot LM148



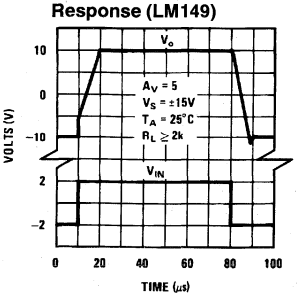
Bode Plot LM149



Large Signal Pulse Response (LM148)



Large Signal Pulse Response (LM149)



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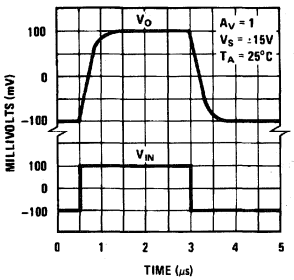
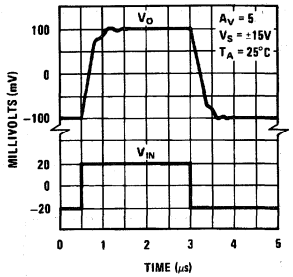
Typical Performance Characteristics (Continued)

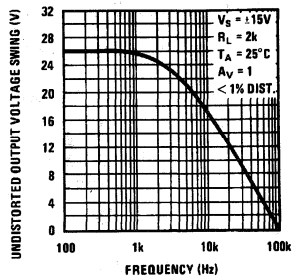
Small Signal Pulse Response (LM148)



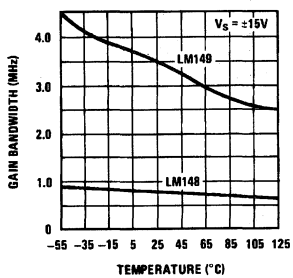
Small Signal Pulse Response (LM149)



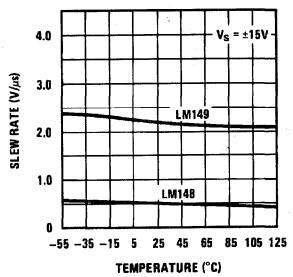
Undistorted Output Voltage Swing



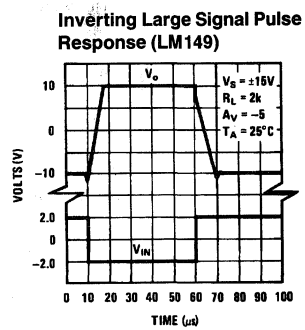
Gain Bandwidth



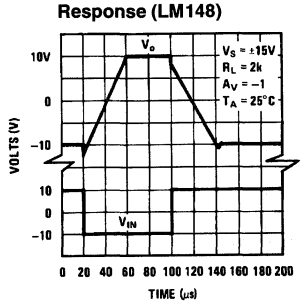
Slew Rate



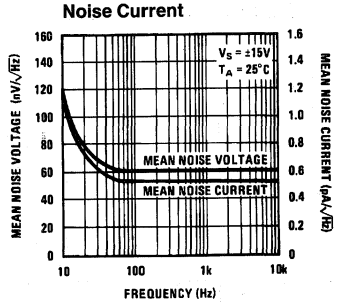
Inverting Large Signal Pulse Response (LM149)



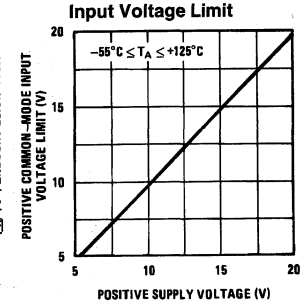
Inverting Large Signal Pulse Response (LM148)



Input Noise Voltage and Noise Current

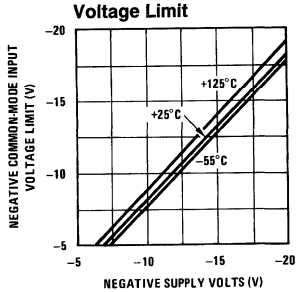


Positive Common-Mode Input Voltage Limit



TL/H/7786–4

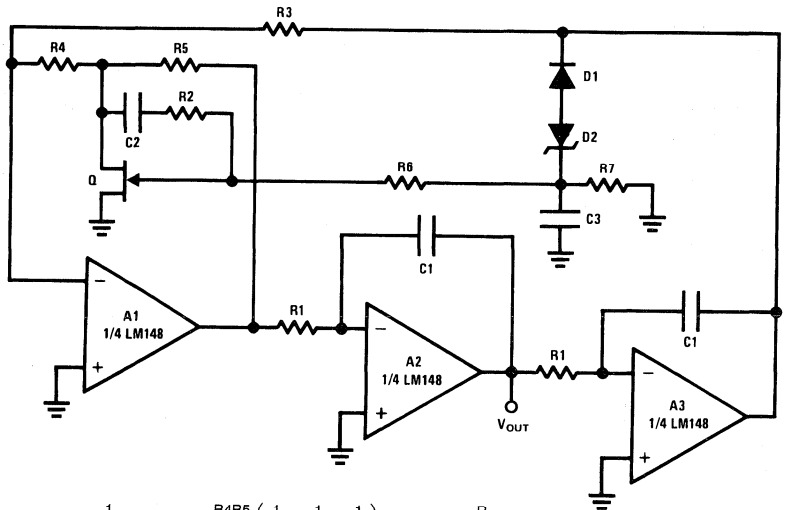
Negative Common-Mode Input Voltage Limit



TL/H/7786–5

Typical Applications—LM148

One Decade Low Distortion Sinewave Generator



$$f = \frac{1}{2\pi R1C1} \times \sqrt{K},\ K = \frac{R4R5}{R3}\left(\frac{1}{r_{DS}} + \frac{1}{R4} + \frac{1}{R5}\right),\quad r_{DS} \approx \frac{R_{ON}}{\left(1 - \frac{V_{GS}}{V_P}\right)^{1/2}}$$

TL/H/7786–8

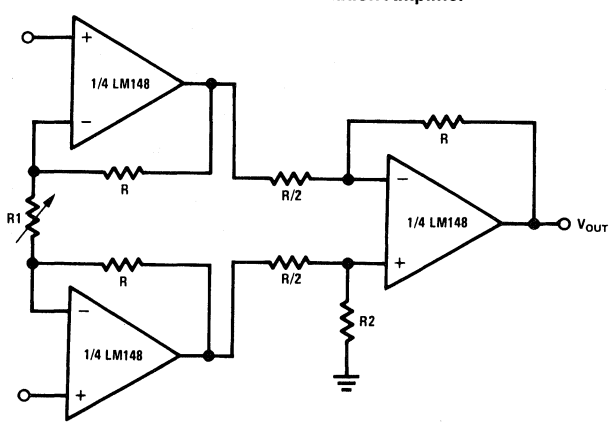
f_{MAX} = 5 kHz, THD ≤ 0.03%

R1 = 100k pot. C1 = 0.0047 μF, C2 = 0.01 μF, C3 = 0.1 μF, R2 = R6 = R7 = 1M,

R3 = 5.1k, R4 = 12Ω, R5 = 240Ω, Q = NS5102, D1 = 1N914, D2 = 3.6V avalanche diode (ex. LM103), V_S = ±15V

A simpler version with some distortion degradation at high frequencies can be made by using A1 as a simple inverting amplifier, and by putting back to back zeners in the feedback loop of A3.

Low Cost Instrumentation Amplifier



$$V_{OUT} = 2\left(\frac{2R}{R1} + 1\right),\ V_S - 3V \le V_{IN\,CM} \le V_S^+ - 3V,$$

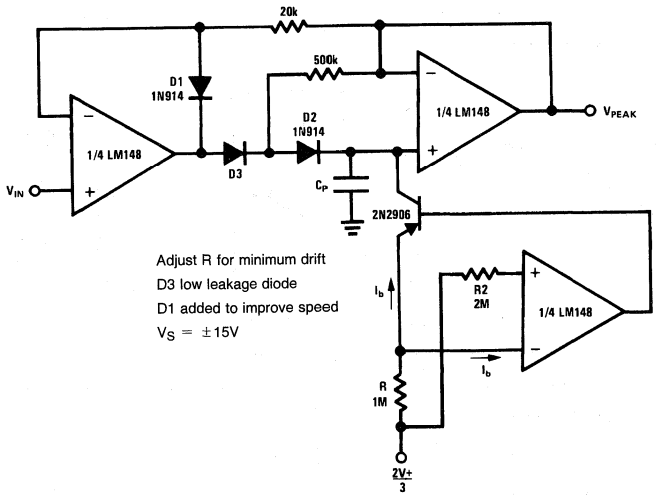
TL/H/7786–9

V_S = ±15V

R = R2, trim R2 to boost CMRR

Typical Applications—LM148 (Continued)

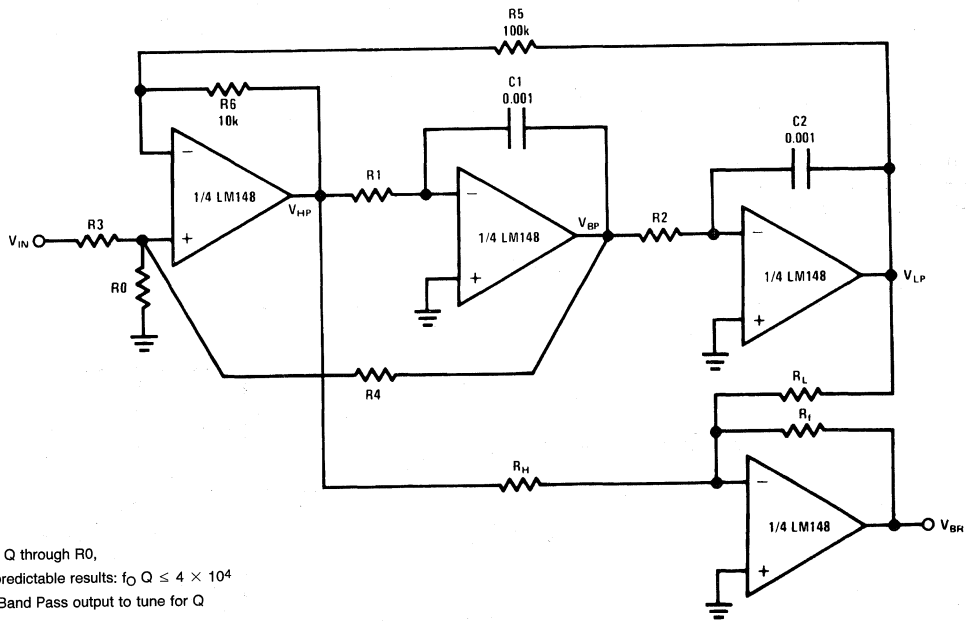
Low Drift Peak Detector with Bias Current Compensation



Adjust R for minimum drift
D3 low leakage diode
D1 added to improve speed
$V_S = \pm 15V$

TL/H/7786–10

Universal State-Variable Filter



Tune Q through R0,
For predictable results: $f_O\ Q \leq 4 \times 10^4$
Use Band Pass output to tune for Q

TL/H/7786–11

$$\frac{V_{(s)}}{V_{IN(s)}} = \frac{N_{(s)}}{D_{(s)}},\ D(s) = S^2 + \frac{S\omega_o}{Q} + \omega_o^2$$

$$N_{HP(s)} = S^2\,H_{OHP},\ N_{BP(s)} = \frac{-s\omega_O\,H_{OBP}}{Q}\quad N_{LP} = \omega_o^2\,H_{OLP}.$$

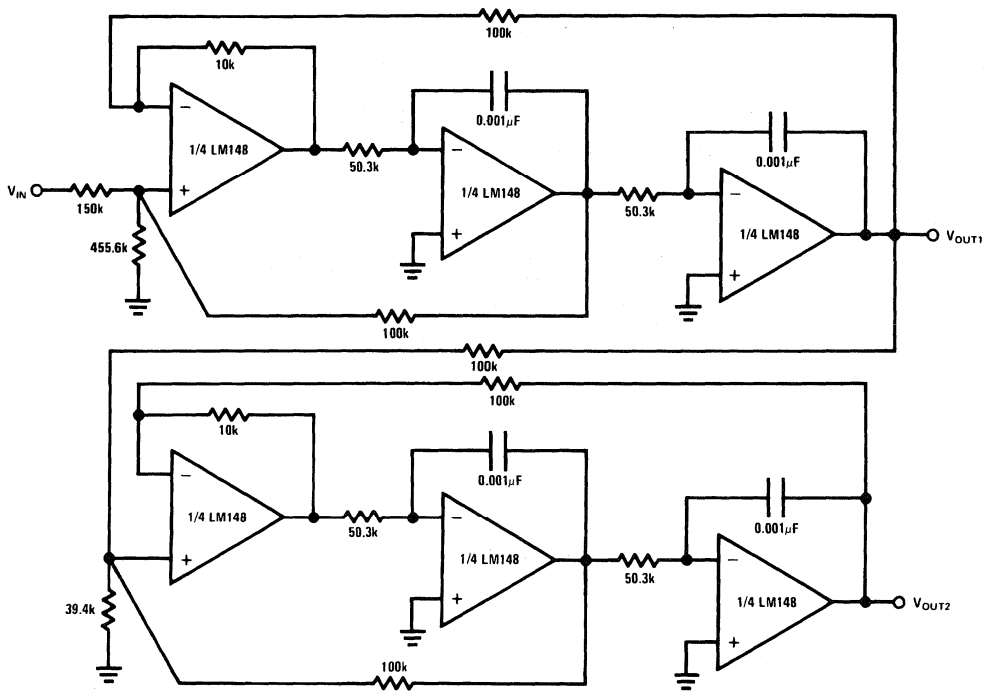
$$f_o = \frac{1}{2\pi}\sqrt{\frac{R6}{R5}}\sqrt{\frac{1}{t1t2}},\ t_i = R_iC_i,\ Q = \left(\frac{1 + R4|R3 + R4|R0}{1 + R6|R5}\right)\left(\frac{R6}{R5}\frac{t_1}{t_2}\right)^{1/2}$$

$$f_{NOTCH} = \frac{1}{2\pi}\left(\frac{R_H}{R_L\,t_1\,t_2}\right)^{1/2},\ H_{OHP} = \frac{1 + R6|R5}{1 + R3|R0 + R3|R4},\ H_{OBP} = \frac{1 + R4|R3 + R4|R0}{1 + R3|R0 + R3|R4}$$

$$H_{OLP} = \frac{1 + R5|R6}{1 + R3|R0 + R3|R4}$$

Typical Applications—LM148 (Continued)

A 1 kHz 4 Pole Butterworth



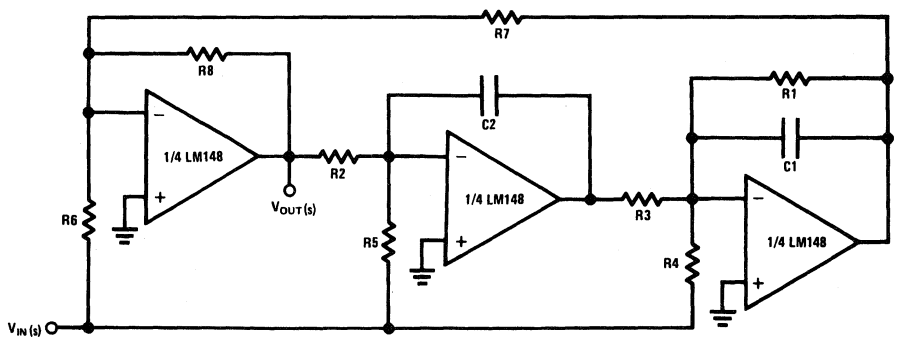
TL/H/7786–12

Use general equations, and tune each section separately

$Q_{1stSECTION} = 0.541$, $Q_{2ndSECTION} = 1.306$

The response should have 0 dB peaking

A 3 Amplifier Bi-Quad Notch Filter



TL/H/7786–13

$$Q = \sqrt{\frac{R8}{R7}} \times \frac{R1C1}{\sqrt{R3C2R2C1}},\quad f_o = \frac{1}{2\pi}\sqrt{\frac{R8}{R7}} \times \frac{1}{\sqrt{R2R3C1C2}},\quad f_{NOTCH} = \frac{1}{2\pi}\sqrt{\frac{R6}{R3R5R7C1C2}}$$

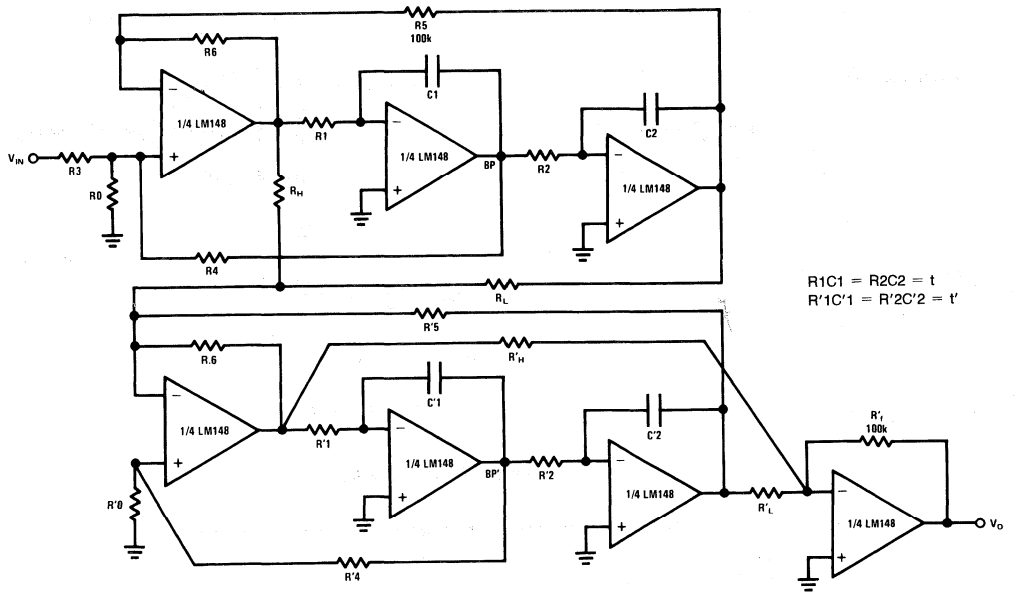
Necessary condition for notch: $\frac{1}{R6} = \frac{R1}{R4R7}$

Ex: f_{NOTCH} = 3 kHz, Q = 5, R1 = 270k, R2 = R3 = 20k, R4 = 27k, R5 = 20k, R6 = R8 = 10k, R7 = 100k, C1 = C2 = 0.001 μF

Better noise performance than the state-space approach.

Typical Applications—LM148 (Continued)

A 4th Order 1 kHz Elliptic Filter (4 Poles, 4 Zeros)



R1C1 = R2C2 = t
R'1C'1 = R'2C'2 = t'

TL/H/7786–14

f_C = 1 kHz, f_S = 2 kHz, f_p = 0.543, f_Z = 2.14, Q = 0.841, f'_P = 0.987, f'_Z = 4.92, Q' = 4.403, normalized to ripple BW

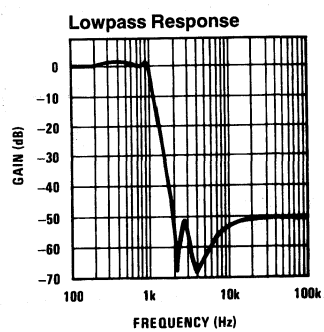
$$f_P = \frac{1}{2\pi}\sqrt{\frac{R6}{R5}} \times \frac{1}{t},\ f_Z = \frac{1}{2\pi}\sqrt{\frac{R_H}{R_L}} \times \frac{1}{t},\ Q = \left(\frac{1 + R4|R3 + R4|R0}{1 + R6|R5}\right) \times \sqrt{\frac{R6}{R5}},\ Q' = \sqrt{\frac{R'6}{R5}}\ \frac{1 + R'4|R'0}{1 + R'6|R'5 + R'6|R_P}$$

$$R_P = \frac{R_H R_L}{R_H + R_L}$$

Use the BP outputs to tune Q, Q', tune the 2 sections separately

R1 = R2 = 92.6k, R3 = R4 = R5 = 100k, R6 = 10k, R0 = 107.8k, R_L = 100k, R_H = 155.1k,

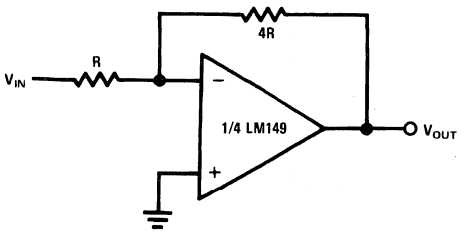
R'1 = R'2 = 50.9k, R'4 = R'5 = 100k, R'6 = 10k, R'0 = 5.78k, R'_L = 100k, R'_H = 248.12k, R'f = 100k. All capacitors are 0.001 μF.



TL/H/7786–15

Typical Applications—LM149

Minimum Gain to Insure LM149 Stability



TL/H/7786–16

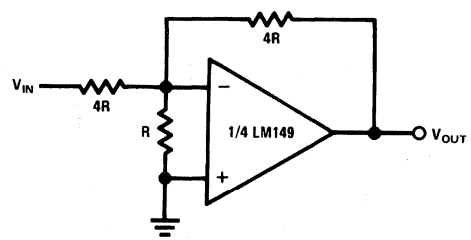
$$A_{CL(S)} = \frac{V_{OUT}}{V_{IN}} = \frac{-4}{\left(1 + \frac{5}{A_{OL(s)}}\right)} \cong -4$$

$V_O\Big|_{V_{IN}=0} \cong \pm 5\, V_{OS}$

Power BW = 40 kHz

Small Signal BW = G BW/5

The LM149 as a Unity Gain Inverter



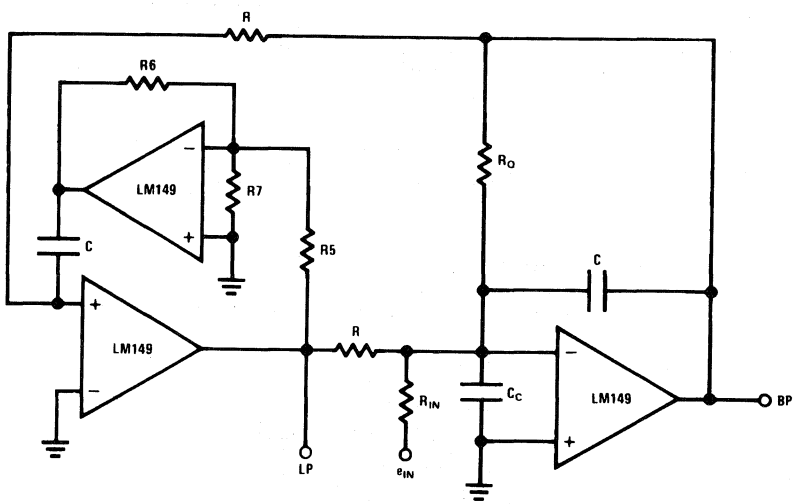
TL/H/7786–17

$$A_{CL(s)} = \frac{V_{OUT}}{V_{IN}} = \left(\frac{-1}{1 + \frac{6}{A_{OL(s)}}}\right) \cong -1$$

$V_O\Big|_{V_{IN}=0} \cong \pm 5\, V_{OS}$

Small Signal BW = G BW/5

Non-inverting-Integrator Bandpass Filter



TL/H/7786–18

For stability purposes: R7 = R6/4, 10R6 = R5, C_C = 10C

$f_O = \frac{1}{2\pi}\sqrt{\frac{R5}{R6}} \times \frac{1}{RC}$, $Q = \frac{R_Q}{R}\sqrt{\frac{R5}{R6}}$, $Ho_{BP} = \frac{R_Q}{R_{IN}}$

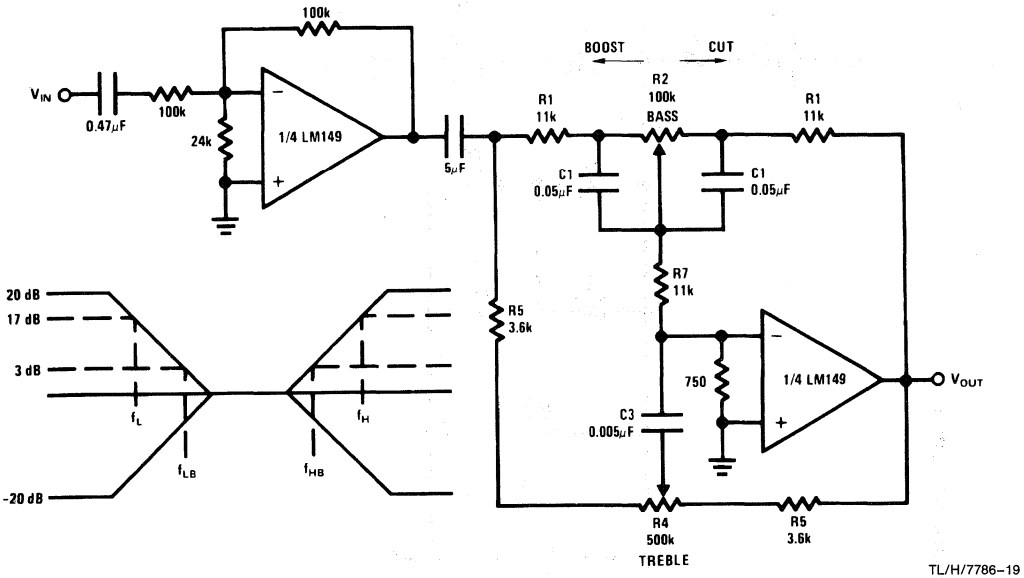
$f_{O(MAX)}$, Q_{MAX} = 20 kHz, 10

Better Q sensitivity with respect to open loop gain variations than the state variable filter.

R7, C_C added for compensation

Typical Applications—LM149 (Continued)

Active Tone Control with Full Output Swing (No Slew Limiting at 20 kHz)



TL/H/7786–19

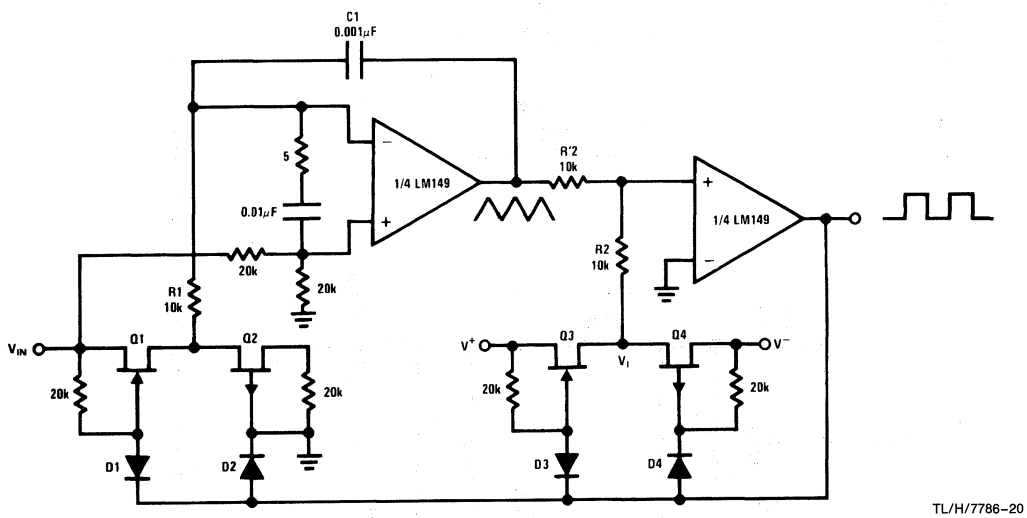
$V_S = \pm 15V$, $V_{OUT(MAX)} = 9.1\ V_{RMS}$,
$f_{MAX} = 20$ kHz, THD ≤ 1%
Duplicate the above circuit for stereo

$$f_L = \frac{1}{2\pi R2C1},\ f_{LB} = \frac{1}{2\pi R1C1}$$

$$f_H = \frac{1}{2\pi R5C3},\ f_{HB} = \frac{1}{2\pi(R1 + 2R7)\,C3}$$

Max Bass Gain ≅ (R1 + R2)/R1
Max Treble Gain ≅ (R1 + 2R7)/R5
as shown: $f_L \cong 32$ Hz, $f_{LB} \cong 320$ Hz
$f_H \cong 11$ kHz, $f_{HB} \cong 1.1$ Hz

Triangular Squarewave Generator



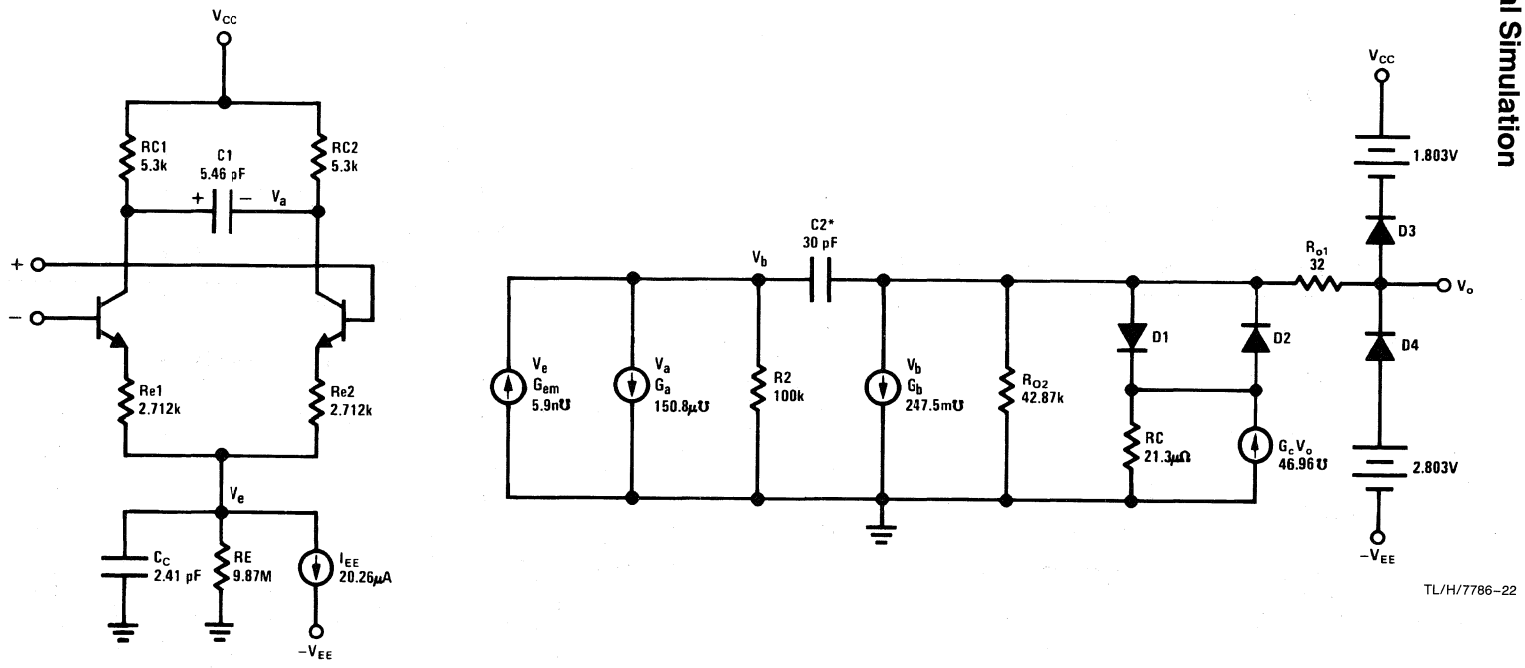
TL/H/7786–20

$$f = \frac{K \times V_{IN}}{8V^+C1R1},\ K = R2/R'2,\ \frac{2V_I}{K} \le 25V,\ V^+ = V^-,\ V_S = \pm 15V$$

Use LM125 for ±15V supply
The circuit can be used as a low frequency V/F for process control.
Q1, Q3: KE4393, Q2, Q4: P1087E, D1–D4 = 1N914

Typical Simulation

LM148, LM149, LM741 Macromodel for Computer Simulation



TL/H/7786–22

TL/H/7786–21

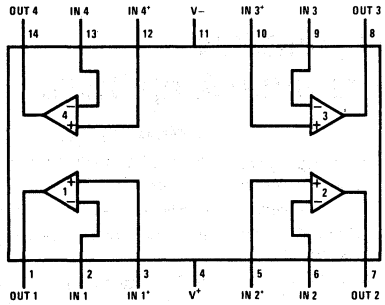
$\beta_{o1} = 112$ $I_S = 8 \times 10^{-16}$

$\beta_{o2} = 144$ *C2 = 6 pF for LM149

For more details, see IEEE Journal of Solid-State Circuits, Vol. SC-9, No. 6, December 1974

Connection Diagram

Dual-In-Line Package



TL/H/7786–2

Top View

Order Number LM148J, LM148J/883, LM149J, LM149J/883, LM248J, LM348J, LM348M, LM348N or LM349N
See NS Package Number J14A, M14A or N14A
LM148J is available per JM38510/11001

National Semiconductor

LM158/LM258/LM358, LM2904
Low Power Dual Operational Amplifiers

General Description

The LM158 series consists of two independent, high gain, internally frequency compensated operational amplifiers which were designed specifically to operate from a single power supply over a wide range of voltages. Operation from split power supplies is also possible and the low power supply current drain is independent of the magnitude of the power supply voltage.

Application areas include transducer amplifiers, dc gain blocks and all the conventional op amp circuits which now can be more easily implemented in single power supply systems. For example, the LM158 series can be directly operated off of the standard +5 V_{DC} power supply voltage which is used in digital systems and will easily provide the required interface electronics without requiring the additional ±15 V_{DC} power supplies.

Unique Characteristics

- In the linear mode the input common-mode voltage range includes ground and the output voltage can also swing to ground, even though operated from only a single power supply voltage.
- The unity gain cross frequency is temperature compensated.
- The input bias current is also temperature compensated.

Advantages

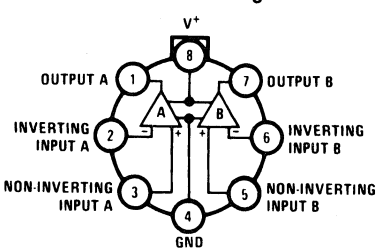
- Two internally compensated op amps in a single package
- Eliminates need for dual supplies
- Allows directly sensing near GND and V_{OUT} also goes to GND
- Compatible with all forms of logic
- Power drain suitable for battery operation
- Pin-out same as LM1558/LM1458 dual operational amplifier

Features

- Internally frequency compensated for unity gain
- Large dc voltage gain 100 dB
- Wide bandwidth (unity gain) 1 MHz
  (temperature compensated)
- Wide power supply range:
  Single supply 3 V_{DC} to 32 V_{DC}
  or dual supplies ±1.5 V_{DC} to ±16 V_{DC}
- Very low supply current drain (500 μA)—essentially independent of supply voltage
- Low input offset voltage 2 mV_{DC}
- Input common-mode voltage range includes ground
- Differential input voltage range equal to the power supply voltage
- Large output voltage swing 0 V_{DC} to V^+ − 1.5 V_{DC}

Connection Diagrams (Top Views)

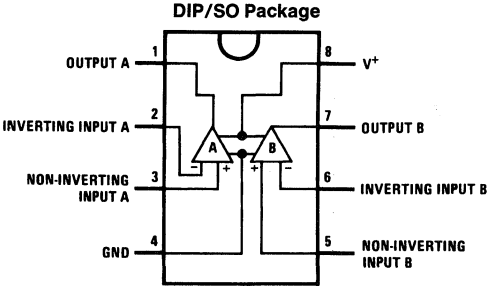
Metal Can Package



TL/H/7787–1

Order Number LM158AH, LM158AH/883*, LM158H, LM158H/883*, LM258AH, LM258H, LM358AH or LM358H
See NS Package Number H08C

DIP/SO Package



TL/H/7787–2

Order Number LM158J, LM158J/883*, LM158AJ, LM158AJ/883* or LM358J
See NS Package Number J08A
Order Number LM358M, LM358AM or LM2904M
See NS Package Number M08A
Order Number LM358AN, LM358N or LM2904N
See NS Package Number N08E

*LM158 is available per SMD #5962-8771001
LM158A is available per SMD #5962-8771002

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications. (Note 9)

	LM158/LM258/LM358 LM158A/LM258A/LM358A	LM2904
Supply Voltage, V^+	32 V_{DC}	26 V_{DC}
Differential Input Voltage	32 V_{DC}	26 V_{DC}
Input Voltage	−0.3 V_{DC} to +32 V_{DC}	−0.3 V_{DC} to +26 V_{DC}
Power Dissipation (Note 1)		
Molded DIP	830 mW	830 mW
Metal Can	550 mW	
Small Outline Package (M)	530 mW	530 mW
Output Short-Circuit to GND (One Amplifier) (Note 2) $V^+ \leq 15\ V_{DC}$ and $T_A = 25°C$	Continuous	Continuous
Input Current ($V_{IN} < -0.3\ V_{DC}$) (Note 3)	50 mA	50 mA

	LM158/LM258/LM358 LM158A/LM258A/LM358A	LM2904
Operating Temperature Range		
LM358	0°C to +70°C	−40°C to +85°C
LM258	−25°C to +85°C	
LM158	−55°C to +125°C	
Storage Temperature Range	−65°C to +150°C	−65°C to +150°C
Lead Temperature, DIP (Soldering, 10 seconds)	260°C	260°C
Lead Temperature, Metal Can (Soldering, 10 seconds)	300°C	300°C
Soldering Information		
Dual-In-Line Package		
Soldering (10 seconds)	260°C	260°C
Small Outline Package		
Vapor Phase (60 seconds)	215°C	215°C
Infrared (15 seconds)	220°C	220°C
See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.		
ESD Tolerance (Note 10)	250V	250V

Electrical Characteristics $V^+ = +5.0\ V_{DC}$, unless otherwise stated

Parameter	Conditions	LM158A		LM258A		LM358A		LM158/LM258		LM358		LM2904		Units
		Min Typ	Max	Min Typ	Max	Min Typ	Max	Min Typ	Max	Min Typ	Max	Min Typ	Max	
Input Offset Voltage	(Note 5), $T_A = 25°C$	±1	±2	±1	±3	±2	±3	±2	±5	±2	±7	±2	±7	mV_{DC}
Input Bias Current	$I_{IN(+)}$ or $I_{IN(-)}$, $T_A = 25°C$, $V_{CM} = 0V$, (Note 6)	20	50	40	80	45	100	45	150	45	250	45	250	nA_{DC}
Input Offset Current	$I_{IN(+)} - I_{IN(-)}$, $V_{CM} = 0V$, $T_A = 25°C$	±2	±10	±2	±15	±5	±30	±3	±30	±5	±50	±5	±50	nA_{DC}
Input Common-Mode Voltage Range	$V^+ = 30\ V_{DC}$, (Note 7) (LM2904, $V^+ = 26V$), $T_A = 25°C$	0 $V^+ - 1.5$		0 $V^+ - 1.5$		0 $V^+ - 1.5$		0 $V^+ - 1.5$		0 $V^+ - 1.5$		0 $V^+ - 1.5$		V_{DC}
Supply Current	Over Full Temperature Range $R_L = \infty$ on All Op Amps													
	$V^+ = 30V$ (LM2904 $V^+ = 26V$)	1	2	1	2	1	2	1	2	1	2	1	2	mA_{DC}
	$V^+ = 5V$	0.5	1.2	0.5	1.2	0.5	1.2	0.5	1.2	0.5	1.2	0.5	1.2	mA_{DC}

Electrical Characteristics (Continued) $V^+ = +5.0\ V_{DC}$, Note 4, unless otherwise stated

Parameter	Conditions	LM158A			LM258A			LM358A			LM158/LM258			LM358			LM2904			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Large Signal Voltage Gain	$V^+ = 15\ V_{DC}$, $T_A = 25°C$, $R_L \geq 2\ k\Omega$, (For $V_O = 1\ V_{DC}$ to $11\ V_{DC}$)	50	100		50	100		25	100		50	100		25	100		25	100		V/mV
Common-Mode Rejection Ratio	DC, $T_A = 25°C$, $V_{CM} = 0V$ to $V^+ - 1.5\ V_{DC}$	70	85		70	85		65	85		70	85		65	85		50	70		dB
Power Supply Rejection Ratio	DC, $V^+ = 5\ V_{DC}$ to $30\ V_{DC}$ (LM2904, $V^+ = 5\ V_{DC}$ to $26\ V_{DC}$), $T_A = 25°C$	65	100		65	100		65	100		65	100		65	100		50	100		dB
Amplifier-to-Amplifier Coupling	$f = 1$ kHz to 20 kHz, $T_A = 25°C$ (Input Referred), (Note 8)		−120			−120			−120			−120			−120			−120		dB
Output Current Source	$V_{IN}^+ = 1\ V_{DC}$, $V_{IN}^- = 0\ V_{DC}$, $V^+ = 15\ V_{DC}$, $V_O = 2\ V_{DC}$, $T_A = 25°C$	20	40		20	40		20	40		20	40		20	40		20	40		mA_{DC}
Sink	$V_{IN}^- = 1\ V_{DC}$, $V_{IN}^+ = 0\ V_{DC}$ $V^+ = 15\ V_{DC}$, $T_A = 25°C$, $V_O = 2\ V_{DC}$	10	20		10	20		10	20		10	20		10	20		10	20		mA_{DC}
	$V_{IN}^- = 1\ V_{DC}$, $V_{IN}^+ = 0\ V_{DC}$ $T_A = 25°C$, $V_O = 200\ mV_{DC}$, $V^+ = 15\ V_{DC}$	12	50		12	50		12	50		12	50		12	50		12	50		μA_{DC}
Short Circuit to Ground	$T_A = 25°C$, (Note 2), $V^+ = 15\ V_{DC}$		40	60		40	60		40	60		40	60		40	60		40	60	mA_{DC}
Input Offset Voltage	(Note 5)			±4			±4			±5			±7			±9			±10	mV_{DC}
Input Offset Voltage Drift	$R_S = 0\Omega$		7	15		7	15		7	20		7			7			7		$\mu V/°C$
Input Offset Current	$I_{IN(+)} - I_{IN(-)}$			±30			±30			±75			±100			±150		±45	±200	nA_{DC}
Input Offset Current Drift	$R_S = 0\Omega$		10	200		10	200		10	300		10			10			10		$pA_{DC}/°C$
Input Bias Current	$I_{IN(+)}$ or $I_{IN(-)}$		40	100		40	100		40	200		40	300		40	500		40	500	nA_{DC}

Electrical Characteristics (Continued) $V^+ = +5.0\ V_{DC}$, Note 4, unless otherwise stated

Parameter	Conditions	LM158A			LM258A			LM358A			LM158/LM258			LM358			LM2904			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input Common-Mode Voltage Range	$V^+ = 30\ V_{DC}$, (Note 7) (LM2904, $V^+ = 26\ V_{DC}$)	0		$V^+ -2$	0		$V^+ -2$	0		$V^+ -2$	0		$V^+ -2$	0		$V^+ -2$	0		$V^+ -2$	V_{DC}
Large Signal Voltage Gain	$V^+ = +15\ V_{DC}$ ($V_O = 1\ V_{DC}$ to $11\ V_{DC}$) $R_L \geq 2\ k\Omega$	25			25			15			25			15			15			V/mV
Output Voltage Swing V_{OH}	$V^+ = +30\ V_{DC}$, $R_L = 2\ k\Omega$	26			26			26			26			26			22			V_{DC}
	$R_L \geq 10\ k\Omega$ (LM2904, $V^+ = 26\ V_{DC}$)	27	28		27	28		27	28		27	28		27	28		23	24		V_{DC}
V_{OL}	$V^+ = 5\ V_{DC}$, $R_L \geq 10\ k\Omega$		5	20		5	20		5	20		5	20		5	20		5	100	mV_{DC}
Output Current Source	$V_O = 2\ V_{DC}$ $V_{IN}^+ = +1\ V_{DC}$, $V_{IN}^- = 0\ V_{DC}$, $V^+ = 15\ V_{DC}$	10	20		10	20		10	20		10	20		10	20		10	20		mA_{DC}
Sink	$V_{IN}^- = +1\ V_{DC}$, $V_{IN}^+ = 0\ V_{DC}$, $V^+ = 15\ V_{DC}$	10	15		5	8		5	8		5	8		5	8		5	8		mA_{DC}

Note 1: For operating at high temperatures, the LM358/LM358A, LM2904 must be derated based on a +125°C maximum junction temperature and a thermal resistance of 120°C/W which applies for the device soldered in a printed circuit board, operating in a still air ambient. The LM258/LM258A and LM158/LM158A can be derated based on a +150°C maximum junction temperature. The dissipation is the total of both amplifiers—use external resistors, where possible, to allow the amplifier to saturate or to reduce the power which is dissipated in the integrated circuit.

Note 2: Short circuits from the output to V^+ can cause excessive heating and eventual destruction. When considering short cirucits to ground, the maximum output current is approximately 40 mA independent of the magnitude of V^+. At values of supply voltage in excess of $+15\ V_{DC}$, continuous short-circuits can exceed the power dissipation ratings and cause eventual destruction. Destructive dissipation can result from simultaneous shorts on all amplifiers.

Note 3: This input current will only exist when the voltage at any of the input leads is driven negative. It is due to the collector-base junction of the input PNP transistors becoming forward biased and thereby acting as input diode clamps. In addition to this diode action, there is also lateral NPN parasitic transistor action on the IC chip. This transistor action can cause the output voltages of the op amps to go to the V^+ voltage level (or to ground for a large overdrive) for the time duration that an input is driven negative. This is not destructive and normal output states will re-establish when the input voltage, which was negative, again returns to a value greater than $-0.3\ V_{DC}$ (at 25°C).

Note 4: These specifications are limited to $-55°C \leq T_A \leq +125°C$ for the LM158/LM158A. With the LM258/LM258A, all temperature specifications are limited to $-25°C \leq T_A \leq +85°C$, the LM358/LM358A temperature specifications are limited to $0°C \leq T_A \leq +70°C$, and the LM2904 specifications are limited to $-40°C \leq T_A \leq +85°C$.

Note 5: $V_O \cong 1.4\ V_{DC}$, $R_S = 0\Omega$ with V^+ from $5\ V_{DC}$ to $30\ V_{DC}$; and over the full input common-mode range ($0\ V_{DC}$ to $V^+ -1.5\ V_{DC}$) at 25°C. For LM2904, V^+ from $5\ V_{DC}$ to $26\ V_{DC}$.

Note 6: The direction of the input current is out of the IC due to the PNP input stage. This current is essentially constant, independent of the state of the output so no loading change exists on the input lines.

Note 7: The input common-mode voltage of either input signal voltage should not be allowed to go negative by more than 0.3V (at 25°C). The upper end of the common-mode voltage range is $V^+ -1.5V$ (at 25°C), but either or both inputs can go to $+32\ V_{DC}$ without damage ($+26\ V_{DC}$ for LM2904), independent of the magnitude of V^+.

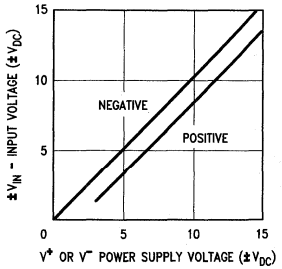
Note 8: Due to proximity of external components, insure that coupling is not originating via stray capacitance between these external parts. This typically can be detected as this type of capacitance increases at higher frequencies.

Note 9: Refer to RETS158AX for LM158A military specifications and to RETS158X for LM158 military specifications.

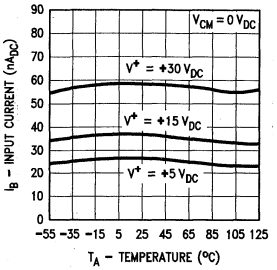
Note 10: Human body model, 1.5 kΩ in series with 100 pF.

Typical Performance Characteristics

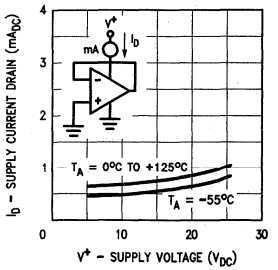
Input Voltage Range



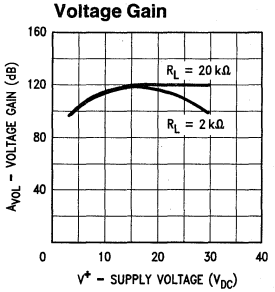
Input Current



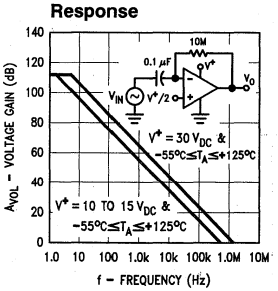
Supply Current



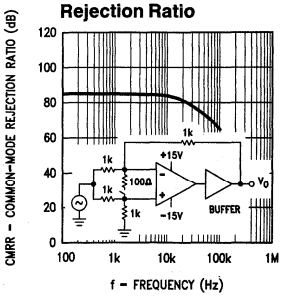
Voltage Gain



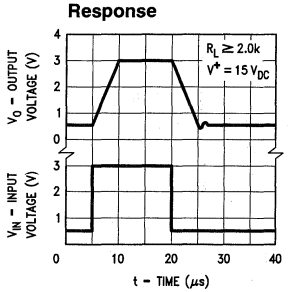
Open Loop Frequency Response



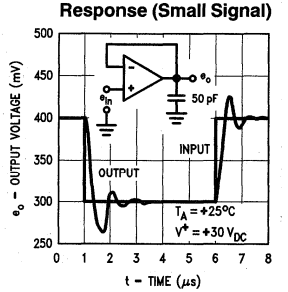
Common-Mode Rejection Ratio



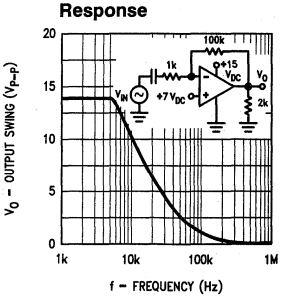
Voltage Follower Pulse Response



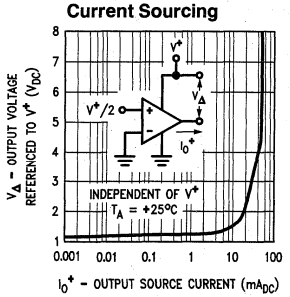
Voltage Follower Pulse Response (Small Signal)



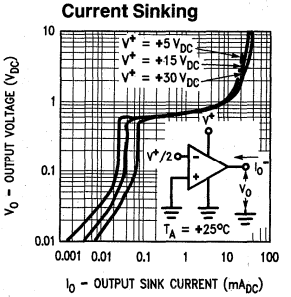
Large Signal Frequency Response



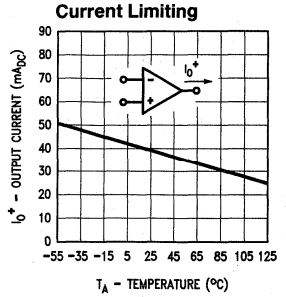
Output Characteristics Current Sourcing



Output Characteristics Current Sinking



Current Limiting



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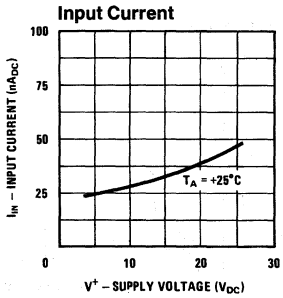
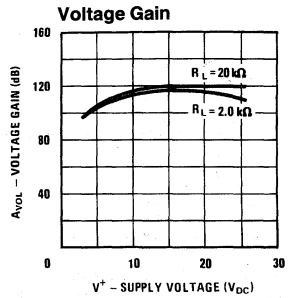
Typical Performance Characteristics (Continued) (LM2902 only)





TL/H/7787–5

Application Hints

The LM158 series are op amps which operate with only a single power supply voltage, have true-differential inputs, and remain in the linear mode with an input common-mode voltage of 0 V_{DC}. These amplifiers operate over a wide range of power supply voltage with little change in performance characteristics. At 25°C amplifier operation is possible down to a minimum supply voltage of 2.3 V_{DC}.

Precautions should be taken to insure that the power supply for the integrated circuit never becomes reversed in polarity or that the unit is not inadvertently installed backwards in a test socket as an unlimited current surge through the resulting forward diode within the IC could cause fusing of the internal conductors and result in a destroyed unit.

Large differential input voltages can be easily accomodated and, as input differential voltage protection diodes are not needed, no large input currents result from large differential input voltages. The differential input voltage may be larger than V^+ without damaging the device. Protection should be provided to prevent the input voltages from going negative more than -0.3 V_{DC} (at 25°C). An input clamp diode with a resistor to the IC input terminal can be used.

To reduce the power supply current drain, the amplifiers have a class A output stage for small signal levels which converts to class B in a large signal mode. This allows the amplifiers to both source and sink large output currents. Therefore both NPN and PNP external current boost transistors can be used to extend the power capability of the basic amplifiers. The output voltage needs to raise approximately 1 diode drop above ground to bias the on-chip vertical PNP transistor for output current sinking applications.

For ac applications, where the load is capacitively coupled to the output of the amplifier, a resistor should be used, from the output of the amplifier to ground to increase the class A bias current and prevent crossover distortion. Where the load is directly coupled, as in dc applications, there is no crossover distortion.

Capacitive loads which are applied directly to the output of the amplifier reduce the loop stability margin. Values of 50 pF can be accomodated using the worst-case non-inverting unity gain connection. Large closed loop gains or resistive isolation should be used if larger load capacitance must be driven by the amplifier.

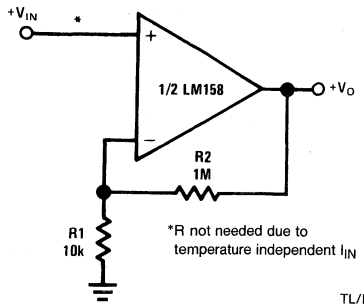
The bias network of the LM158 establishes a drain current which is independent of the magnitude of the power supply voltage over the range of 3 V_{DC} to 30 V_{DC}.

Output short circuits either to ground or to the positive power supply should be of short time duration. Units can be destroyed, not as a result of the short circuit current causing metal fusing, but rather due to the large increase in IC chip dissipation which will cause eventual failure due to excessive function temperatures. Putting direct short-circuits on more than one amplifier at a time will increase the total IC power dissipation to destructive levels, if not properly protected with external dissipation limiting resistors in series with the output leads of the amplifiers. The larger value of output source current which is available at 25°C provides a larger output current capability at elevated temperatures (see typical performance characteristics) than a standard IC op amp.

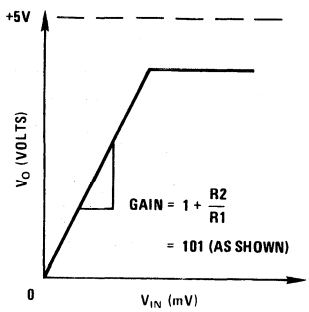
The circuits presented in the section on typical applications emphasize operation on only a single power supply voltage. If complementary power supplies are available, all of the standard op amp circuits can be used. In general, introducing a pseudo-ground (a bias voltage reference of $V^+/2$) will allow operation above and below this value in single power supply systems. Many application circuits are shown which take advantage of the wide input common-mode voltage range which includes ground. In most cases, input biasing is not required and input voltages which range to ground can easily be accommodated.

Typical Single-Supply Applications ($V^+ = 5.0\ V_{DC}$)

Non-Inverting DC Gain (0V Input = 0V Output)

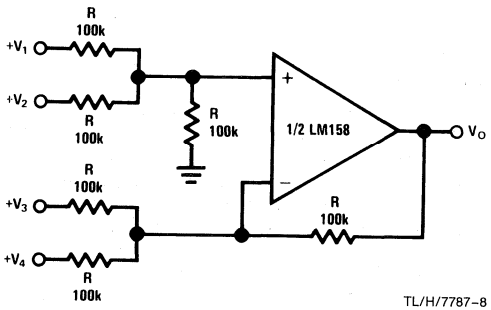


TL/H/7787–6



TL/H/7787–7

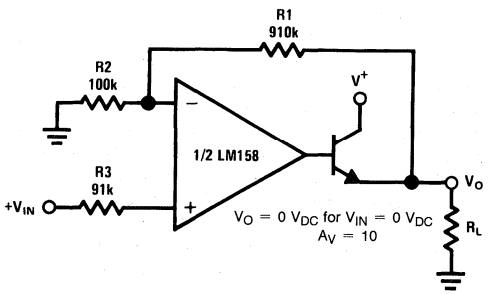
DC Summing Amplifier
(V_{IN}'S ≥ 0 V_{DC} and V_O ≥ 0 V_{DC})



TL/H/7787–8

Where: $V_O = V_1 + V_2 + V_3 + V_4$
$(V_1 + V_2) \geq (V_3 + V_4)$ to keep $V_O > 0\ V_{DC}$

Power Amplifier



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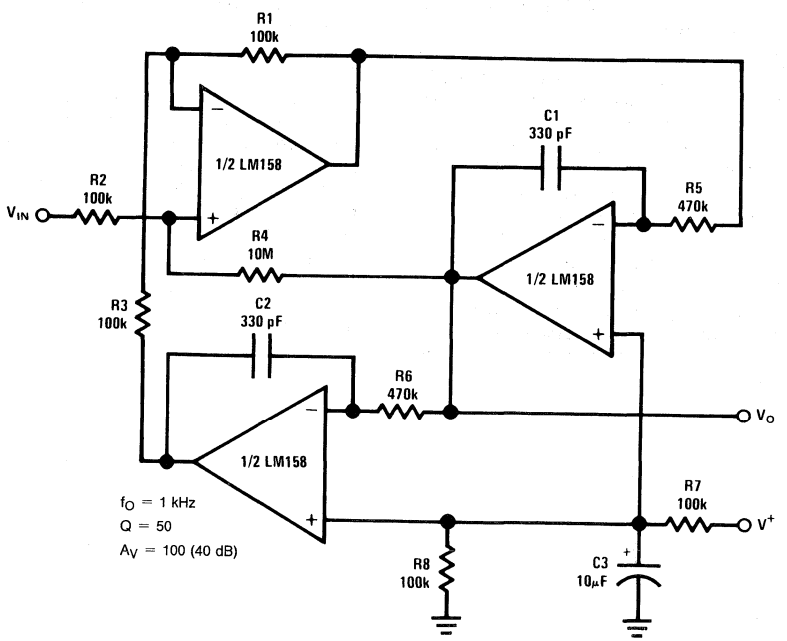
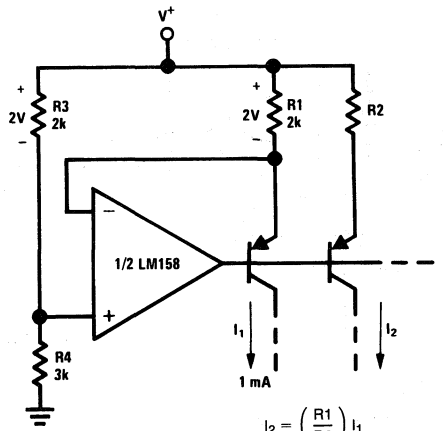
"BI-QUAD" RC Active Bandpass Filter



TL/H/7787–10

Typical Single-Supply Applications (V^+ = 5.0 V_{DC}) (Continued)

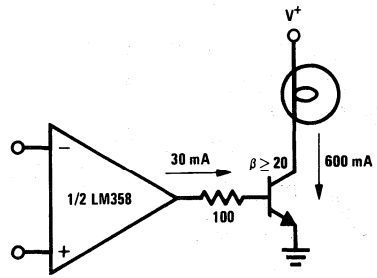
Fixed Current Sources



$$I_2 = \left(\frac{R1}{R2}\right) I_1$$

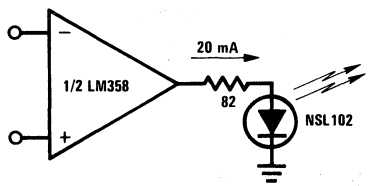
TL/H/7787–11

Lamp Driver



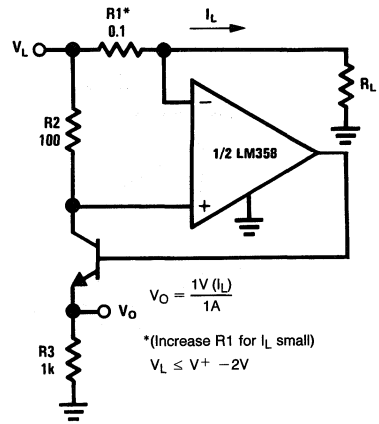
TL/H/7787–12

LED Driver



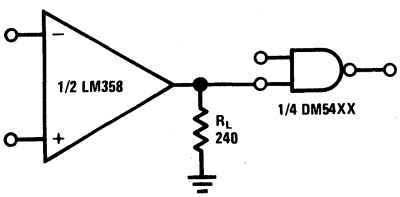
TL/H/7787–13

Current Monitor



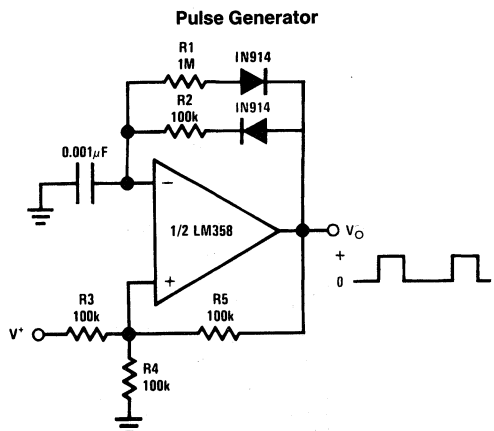
TL/H/7787–14

Driving TTL



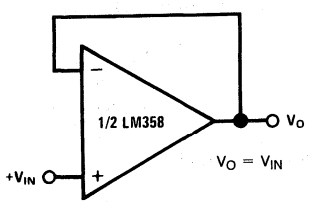
TL/H/7787–15

Pulse Generator



TL/H/7787–16

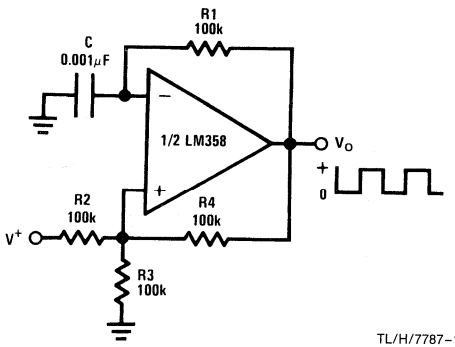
Voltage Follower



TL/H/7787–17

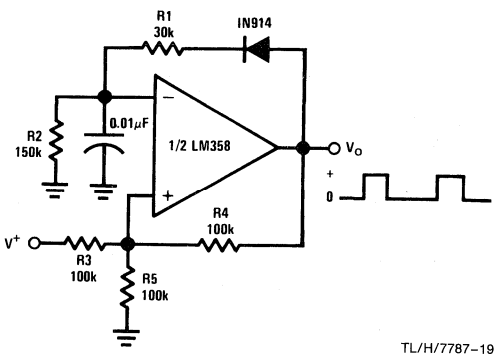
Typical Single-Supply Applications (V^+ = 5.0 V_{DC}) (Continued)

Squarewave Oscillator



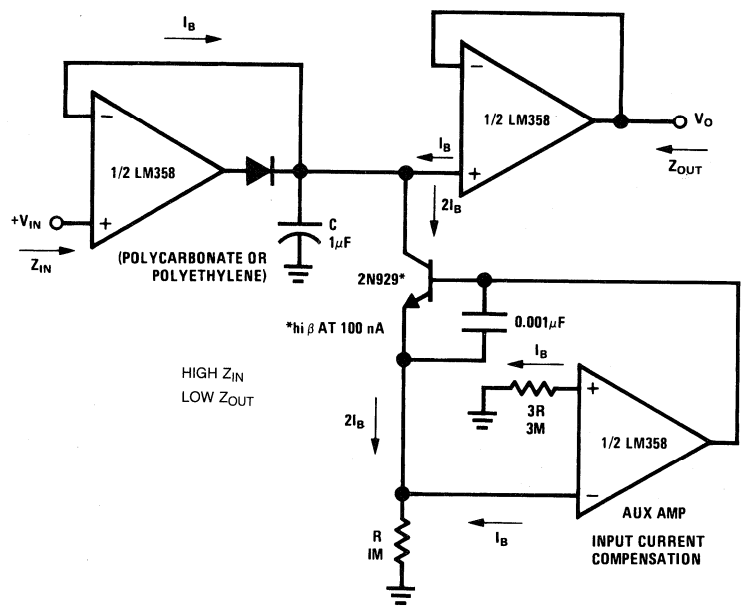
TL/H/7787–18

Pulse Generator



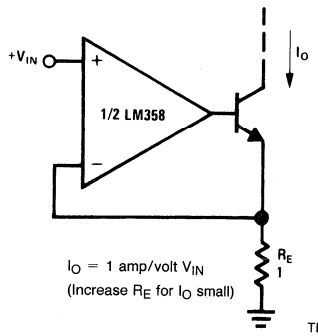
TL/H/7787–19

Low Drift Peak Detector



TL/H/7787–20

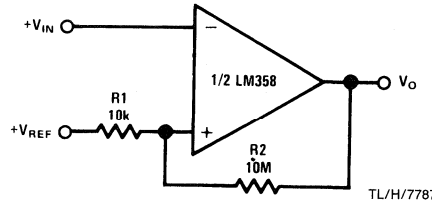
High Compliance Current Sink



I_O = 1 amp/volt V_{IN}
(Increase R_E for I_O small)

TL/H/7787–21

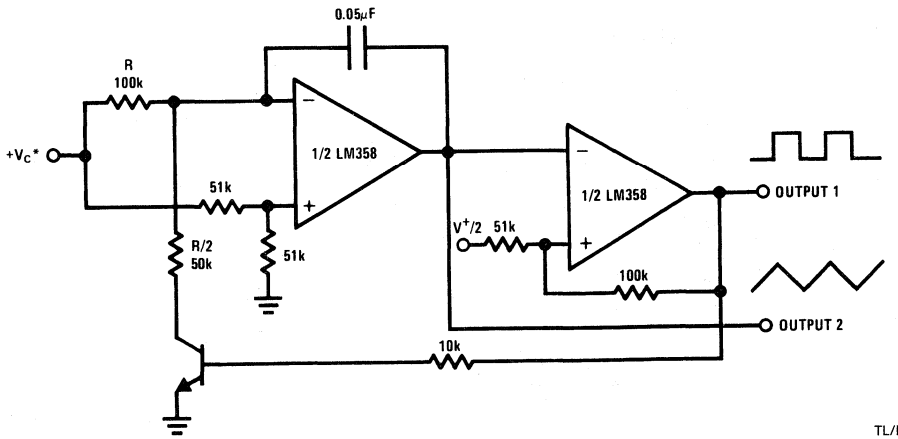
Comparator with Hysteresis



TL/H/7787–22

Typical Single-Supply Applications ($V^+ = 5.0\ V_{DC}$) (Continued)

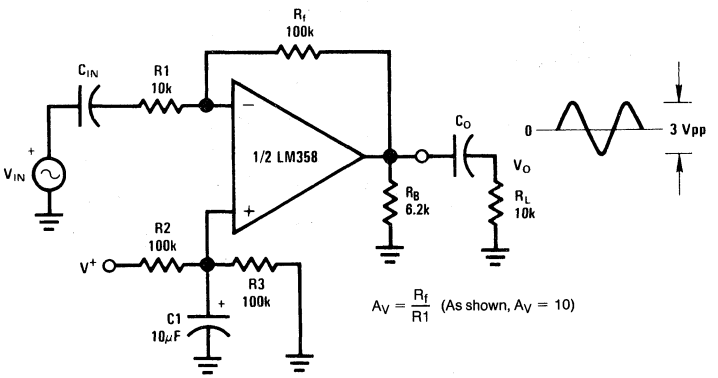
Voltage Controlled Oscillator (VCO)



TL/H/7787–23

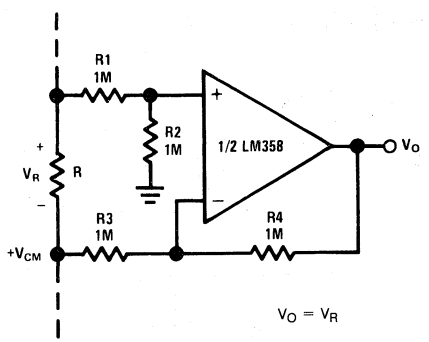
*WIDE CONTROL VOLTAGE RANGE: $0\ V_{DC} \leq V_C \leq 2\ (V^+ - 1.5V_{DC})$

AC Coupled Inverting Amplifier



TL/H/7787–24

Ground Referencing a Differential Input Signal

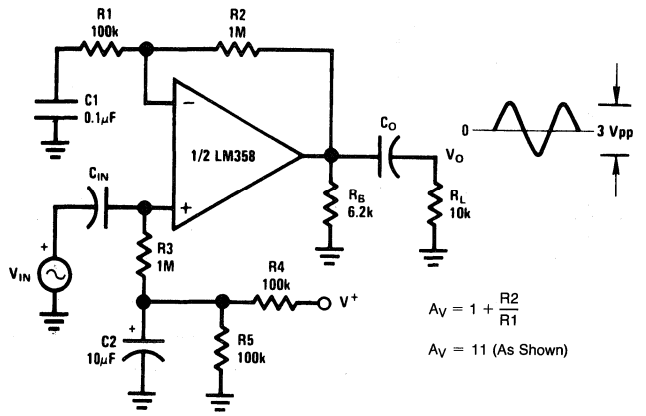


$V_O = V_R$

TL/H/7787–25

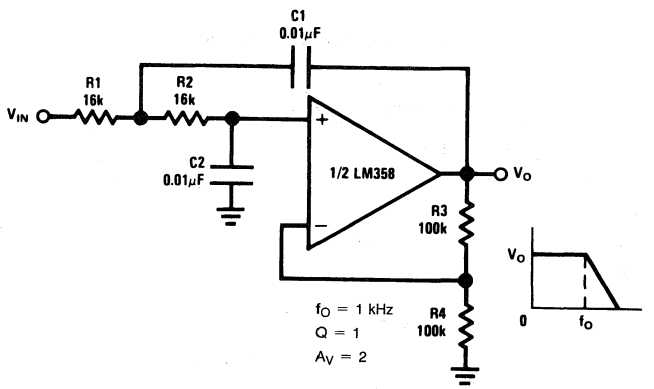
Typical Single-Supply Applications (V^+ = 5.0 V_{DC}) (Continued)

AC Coupled Non-Inverting Amplifier



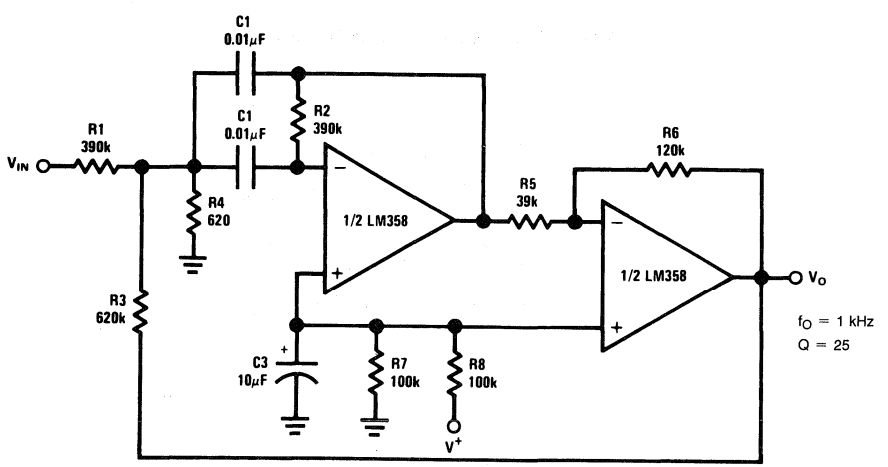
TL/H/7787–26

DC Coupled Low-Pass RC Active Filter



TL/H/7787–27

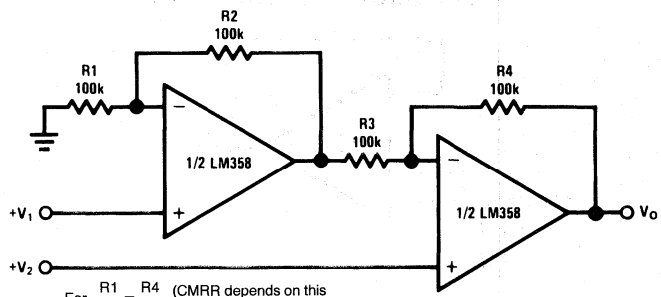
Bandpass Active Filter



TL/H/7787–28

Typical Single-Supply Applications ($V^+ = 5.0\ V_{DC}$) (Continued)

High Input Z, DC Differential Amplifier



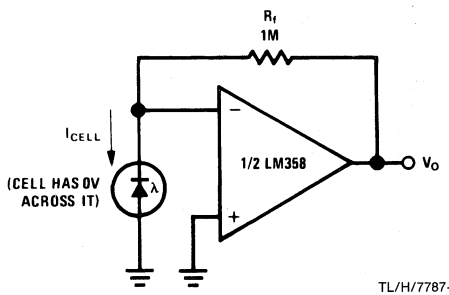
TL/H/7787–29

For $\frac{R1}{R2} = \frac{R4}{R3}$ (CMRR depends on this resistor ratio match)

$V_O = 1 + \frac{R4}{R3}(V_2 - V_1)$

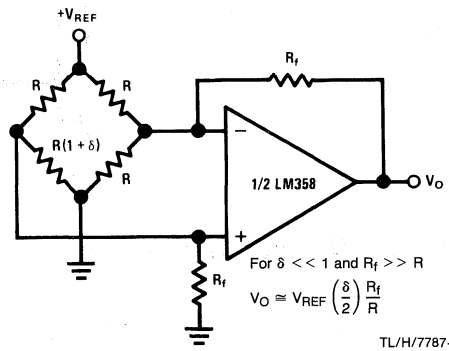
As Shown: $V_O = 2(V_2 - V_1)$

Photo Voltaic-Cell Amplifier



TL/H/7787–30

Bridge Current Amplifier

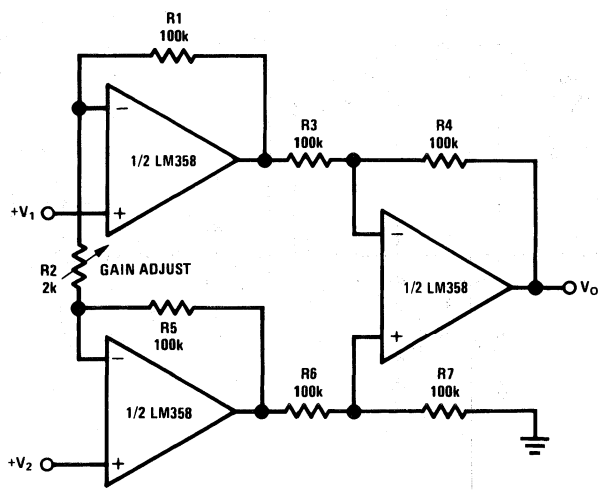


For $\delta << 1$ and $R_f >> R$

$V_O \cong V_{REF}\left(\frac{\delta}{2}\right)\frac{R_f}{R}$

TL/H/7787–33

High Input Z Adjustable-Gain DC Instrumentation Amplifier



TL/H/7787–31

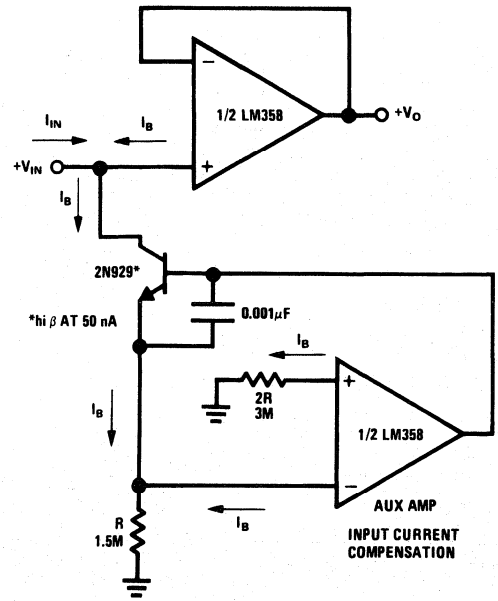
If R1 = R5 & R3 = R4 = R6 = R7 (CMRR depends on match)

$V_O = 1 + \frac{2R1}{R2}(V_2 - V_1)$

As shown $V_O = 101(V_2 - V_1)$

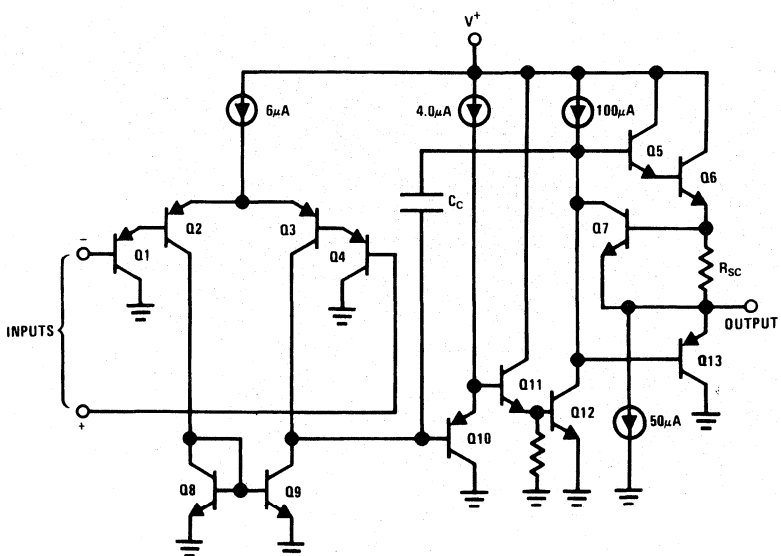
Typical Single-Supply Applications (V^+ = 5.0 V_{DC}) (Continued)

Using Symmetrical Amplifiers to Reduce Input Current (General Concept)



TL/H/7787–32

Schematic Diagram (Each Amplifier)



TL/H/7787–3

National Semiconductor

LM194/LM394 Supermatch Pair

General Description

The LM194 and LM394 are junction isolated ultra well-matched monolithic NPN transistor pairs with an order of magnitude improvement in matching over conventional transistor pairs. This was accomplished by advanced linear processing and a unique new device structure.

Electrical characteristics of these devices such as drift versus initial offset voltage, noise, and the exponential relationship of base-emitter voltage to collector current closely approach those of a theoretical transistor. Extrinsic emitter and base resistances are much lower than presently available pairs, either monolithic or discrete, giving extremely low noise and theoretical operation over a wide current range. Most parameters are guaranteed over a current range of 1 μA to 1 mA and 0V up to 40V collector-base voltage, ensuring superior performance in nearly all applications.

To guarantee long term stability of matching parameters, internal clamp diodes have been added across the emitter-base junction of each transistor. These prevent degradation due to reverse biased emitter current—the most common cause of field failures in matched devices. The parasitic isolation junction formed by the diodes also clamps the substrate region to the most negative emitter to ensure complete isolation between devices.

The LM194 and LM394 will provide a considerable improvement in performance in most applications requiring a closely matched transistor pair. In many cases, trimming can be eliminated entirely, improving reliability and decreasing costs. Additionally, the low noise and high gain make this device attractive even where matching is not critical.

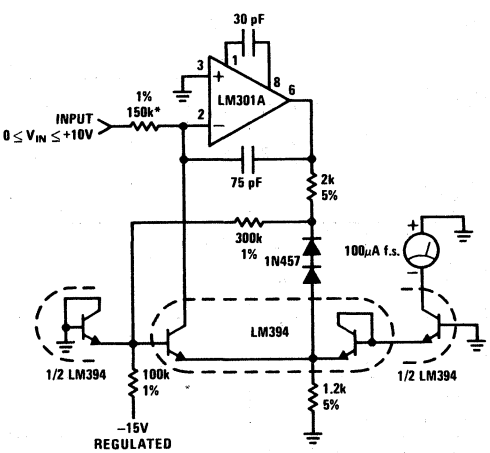
The LM194 and LM394/LM394B/LM394C are available in an isolated header 6-lead TO-5 metal can package. The LM394/LM394B/LM394C are available in an 8-pin plastic dual-in-line package. The LM194 is identical to the LM394 except for tighter electrical specifications and wider temperature range.

Features

- Emitter-base voltage matched to 50 μV
- Offset voltage drift less than 0.1 μV/°C
- Current gain (h_{FE}) matched to 2%
- Common-mode rejection ratio greater than 120 dB
- Parameters guaranteed over 1 μA to 1 mA collector current
- Extremely low noise
- Superior logging characteristics compared to conventional pairs
- Plug-in replacement for presently available devices

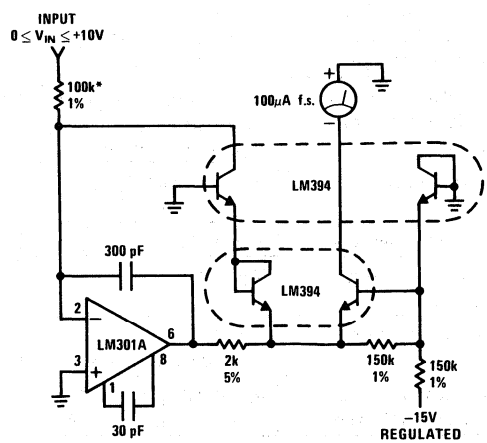
Typical Applications

Low Cost Accurate Square Root Circuit
$I_{OUT} = 10^{-5}.\sqrt{10\,V_{IN}}$



TL/H/9241–1

Low Cost Accurate Squaring Circuit
$I_{OUT} = 10^{-6}\,(V_{IN})^2$



TL/H/9241–2

*Trim for full scale accuracy

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications. (Note 4)

Collector Current	20 mA
Collector-Emitter Voltage	V_{MAX}
Collector-Emitter Voltage	35V
LM394C	20V
Collector-Base Voltage	35V
LM394C	20V
Collector-Substrate Voltage	35V
LM394C	20V
Collector-Collector Voltage	35V
LM394C	20V
Base-Emitter Current	±10 mA
Power Dissipation	500 mW
Junction Temperature	
LM194	−55°C to +125°C
LM394/LM394B/LM394C	−25°C to +85°C
Storage Temperature Range	−65°C to +150°C
Soldering Information	
Metal Can Package (10 sec.)	260°C
Dual-In-Line Package (10 sec.)	260°C
Small Outline Package	
Vapor Phase (60 sec.)	215°C
Infrared (15 sec.)	220°C

See AN-450 "Surface Mounting and their Effects on Product Reliability" for other methods of soldering surface mount devices.

Electrical Characteristics (T_J = 25°C)

Parameter	Conditions	LM194			LM394			LM394B/394C			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Current Gain (h_{FE})	V_{CB} = 0V to V_{MAX} (Note 1)										
	I_C = 1 mA	350	700		300	700		225	500		
	I_C = 100 μA	350	550		250	550		200	400		
	I_C = 10 μA	300	450		200	450		150	300		
	I_C = 1 μA	200	300		150	300		100	200		
Current Gain Match, (h_{FE} Match) $= \frac{100\ [\Delta I_B]\ [h_{FE(MIN)}]}{I_C}$	V_{CB} = 0V to V_{MAX}										
	I_C = 10 μA to 1 mA		0.5	2		0.5	4		1.0	5	%
	I_C = 1 μA		1.0			1.0			2.0		%
Emitter-Base Offset Voltage	V_{CB} = 0										
	I_C = 1 μA to 1 mA		25	100		25	150		50	200	μV
Change in Emitter-Base Offset Voltage vs Collector-Base Voltage (CMRR)	(Note 1) I_C = 1 μA to 1 mA, V_{CB} = 0V to V_{MAX}		10	25		10	50		10	100	μV
Change in Emitter-Base Offset Voltage vs Collector Current	V_{CB} = 0V, I_C = 1 μA to 0.3 mA		5	25		5	50		5	50	μV
Emitter-Base Offset Voltage Temperature Drift	I_C = 10 μA to 1 mA (Note 2) $I_{C1} = I_{C2}$		0.08	0.3		0.08	1.0		0.2	1.5	μV/°C
	V_{OS} Trimmed to 0 at 25°C		0.03	0.1		0.03	0.3		0.03	0.5	μV/°C
Logging Conformity	I_C = 3 nA to 300 μA, V_{CB} = 0, (Note 3)		150			150			150		μV
Collector-Base Leakage	$V_{CB} = V_{MAX}$		0.05	0.25		0.05	0.5		0.05	0.5	nA
Collector-Collector Leakage	$V_{CC} = V_{MAX}$		0.1	2.0		0.1	5.0		0.1	5.0	nA
Input Voltage Noise	I_C = 100 μA, V_{CB} = 0V, f = 100 Hz to 100 kHz		1.8			1.8			1.8		nV/$\sqrt{Hz}$
Collector to Emitter Saturation Voltage	I_C = 1 mA, I_B = 10 μA		0.2			0.2			0.2		V
	I_C = 1 mA, I_B = 100 μA		0.1			0.1			0.1		V

Note 1: Collector-base voltage is swept from 0 to V_{MAX} at a collector current of 1 μA, 10 μA, 100 μA, and 1 mA.

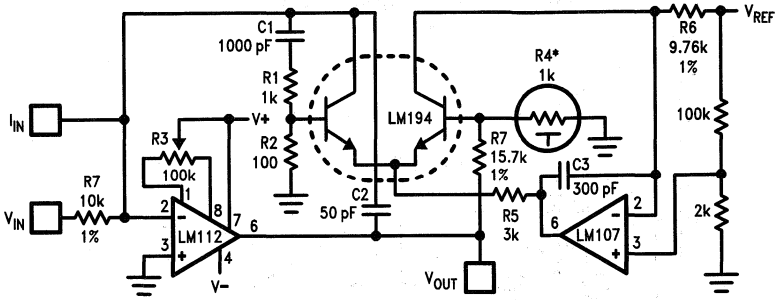
Note 2: Offset voltage drift with V_{OS} = 0 at T_A = 25°C is valid only when the ratio of I_{C1} to I_{C2} is adjusted to give the initial zero offset. This ratio must be held to within 0.003% over the entire temperature range. Measurements taken at +25°C and temperature extremes.

Note 3: Logging conformity is measured by computing the best fit to a true exponential and expressing the error as a base-emitter voltage deviation.

Note 4: Refer to RETS194X drawing of military LM194H version for specifications.

Typical Applications (Continued)

Fast, Accurate Logging Amplifier, V_{IN} = 10V to 0.1 mV or I_{IN} = 1 mA to 10 nA

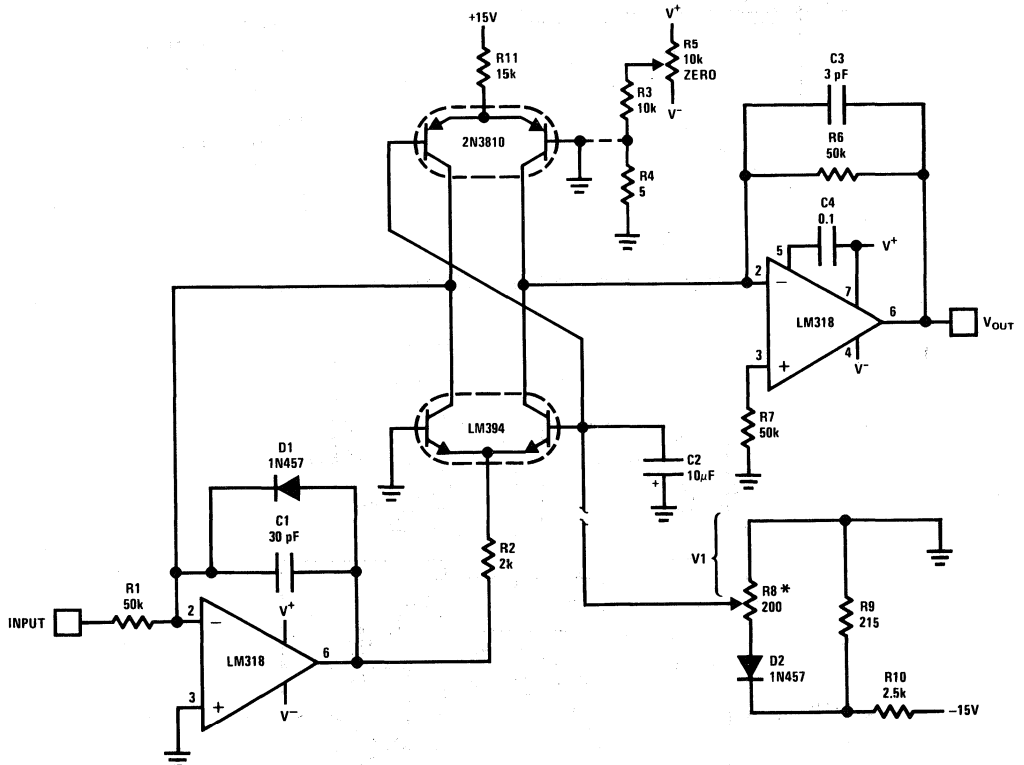


TL/H/9241–3

*1 kΩ (±1%) at 25°C, +3500 ppm/°C. Available from Vishay Ultronix, Grand Junction, CO, Q81 Series.

$$V_{OUT} = -\log_{10}\left(\frac{V_{IN}}{V_{REF}}\right)$$

Voltage Controlled Variable Gain Amplifier



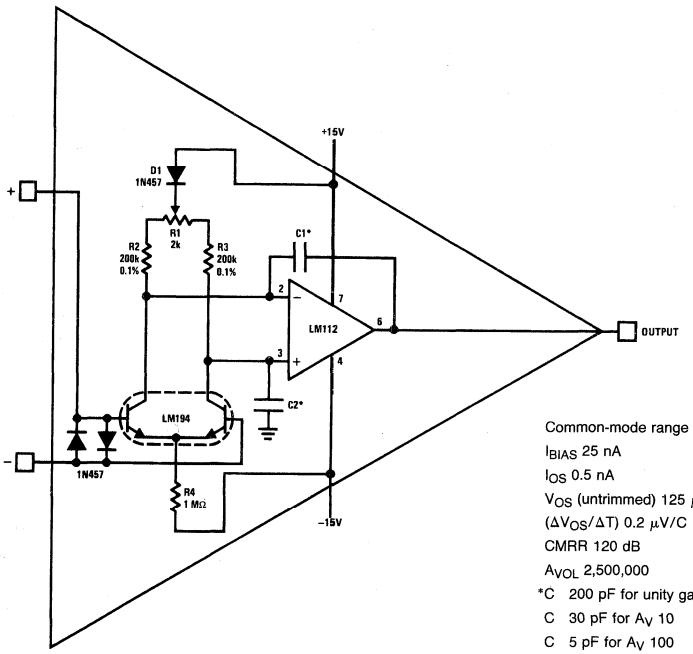
TL/H/9241–4

*R8–R10 and D2 provide a temperature independent gain control.
G = −336 V1 (dB)

Distortion < 0.1%
Bandwidth > 1 MHz
100 dB gain range

Typical Applications (Continued)

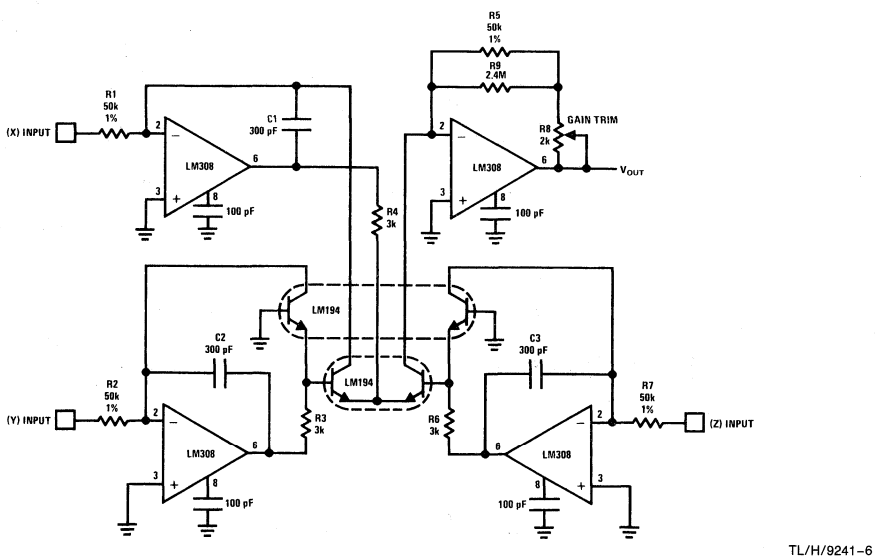
Precision Low Drift Operational Amplifier



Common-mode range 10V
I_{BIAS} 25 nA
I_{OS} 0.5 nA
V_{OS} (untrimmed) 125 μV
$(\Delta V_{OS}/\Delta T)$ 0.2 μV/C
CMRR 120 dB
A_{VOL} 2,500,000
*C 200 pF for unity gain
C 30 pF for A_V 10
C 5 pF for A_V 100
C 0 pF for A_V 1000

TL/H/9241–5

High Accuracy One Quadrant Multiplier/Divider



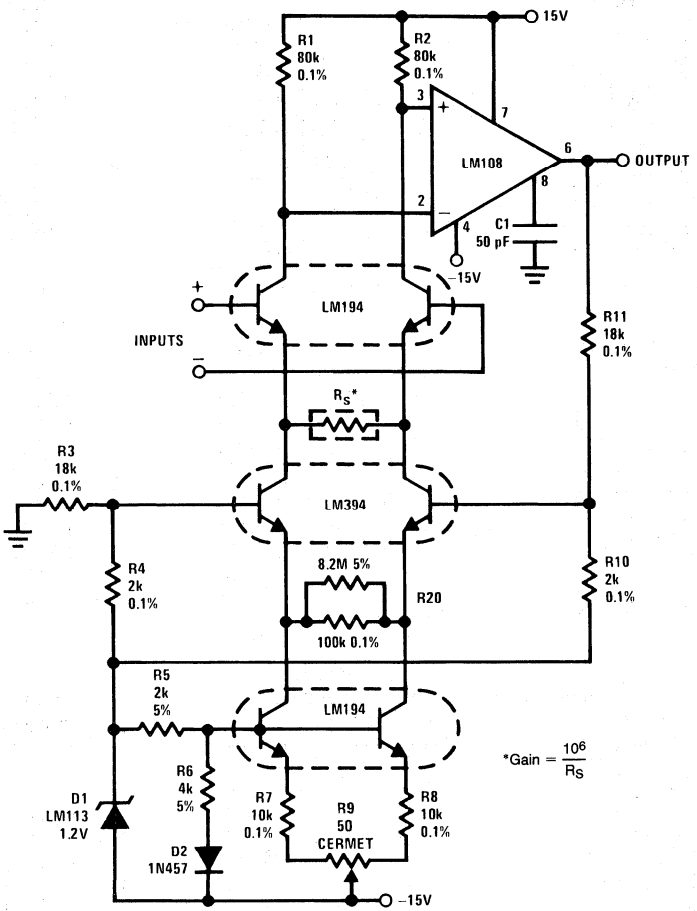
TL/H/9241–6

$V_{OUT} = \frac{(X)(Y)}{(Z)}$; positive inputs only.

*Typical linearity 0.1%

Typical Applications (Continued)

High Performance Instrumentation Amplifier



TL/H/9241–7

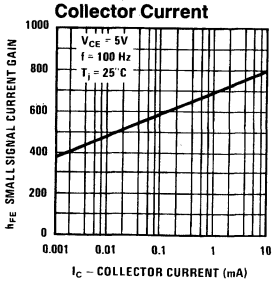
Performance Characteristics

	G = 10,000	G = 1,000	G = 100	G = 10	
Linearity of Gain (±10V Output)	≤0.01	≤0.01	≤0.02	≤0.05	%
Common-Mode Rejection Ratio (60 Hz)	≥120	≥120	≥110	≥90	dB
Common-Mode Rejection Ratio (1 kHz)	≥110	≥110	≥90	≥70	dB
Power Supply Rejection Ratio					
+Supply	>110	>110	>110	>110	dB
−Supply	>110	>110	>90	>70	dB
Bandwidth (−3 dB)	50	50	50	50	kHz
Slew Rate	0.3	0.3	0.3	0.3	V/μs
Offset Voltage Drift**	≤0.25	≤0.4	2	≤10	μV/°C
Common-Mode Input Resistance	$>10^9$	$>10^9$	$>10^9$	$>10^9$	Ω
Differential Input Resistance	$>3 \times 10^8$	$>3 \times 10^8$	$>3 \times 10^8$	$>3 \times 10^8$	Ω
Input Referred Noise (100 Hz ≤ f ≤ 10 kHz)	5	6	12	70	$\frac{nV}{\sqrt{Hz}}$
Input Bias Current	75	75	75	75	nA
Input Offset Current	1.5	1.5	1.5	1.5	nA
Common-Mode Range	±11	±11	±11	±10	V
Output Swing (R_L = 10 kΩ)	±13	±13	±13	±13	V

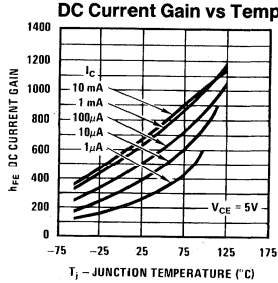
**Assumes ≤ 5 ppm/°C tracking of resistors

Typical Performance Characteristics

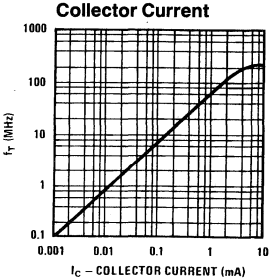
Small Signal Current Gain vs Collector Current



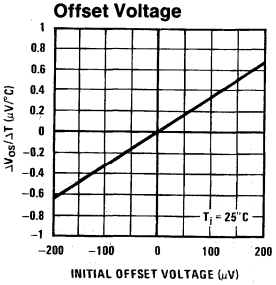
DC Current Gain vs Temperature



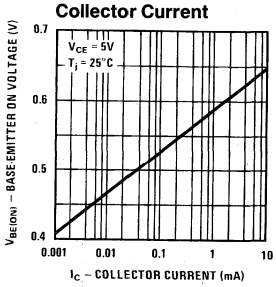
Unity Gain Frequency (f_t) vs Collector Current



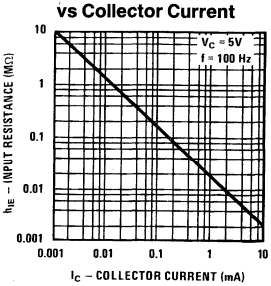
Offset Voltage Drift vs Initial Offset Voltage



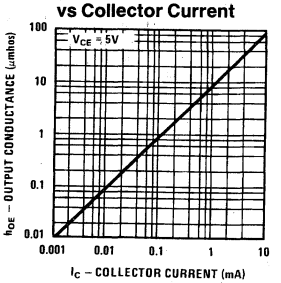
Base-Emitter On Voltage vs Collector Current



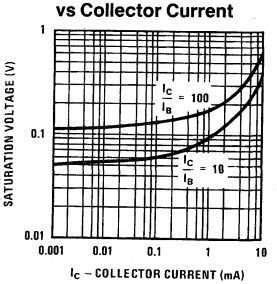
Small Signal Input Resistance (h_{ie}) vs Collector Current



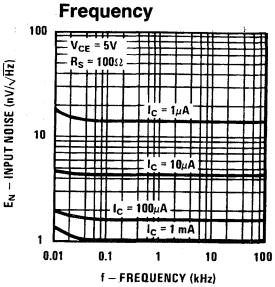
Small Signal Output Conductance vs Collector Current



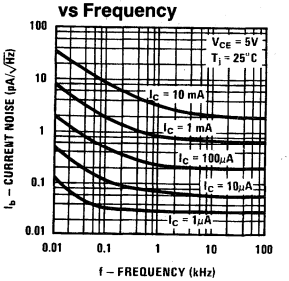
Collector-Emitter Saturation Voltage vs Collector Current



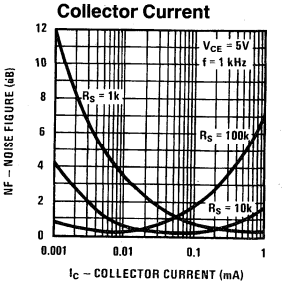
Input Voltage Noise vs Frequency



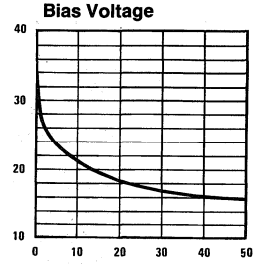
Base Current Noise vs Frequency



Noise Figure vs Collector Current



Collector to Collector Capacitance vs Reverse Bias Voltage



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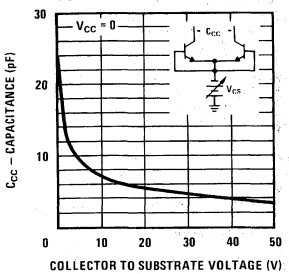
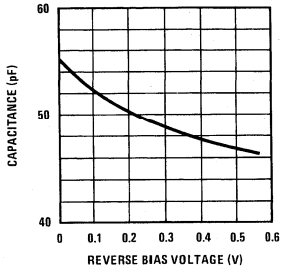
Typical Performance Characteristics (Continued)

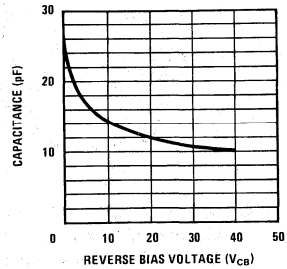
Collector to Collector Capacitance vs Collector-Substrate Voltage



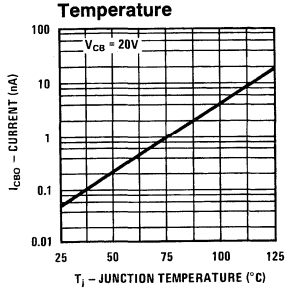
Emitter-Base Capacitance vs Reverse Bias Voltage



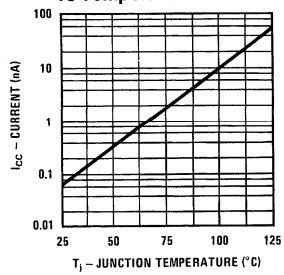
Collector-Base Capacitance vs Reverse Bias Voltage



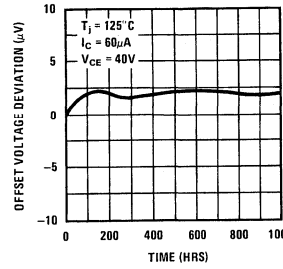
Collector-Base Leakage vs Temperature



Collector to Collector Leakage vs Temperature



Offset Voltage Long Term Stability at High Temperature



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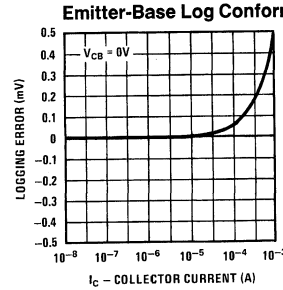
Emitter-Base Log Conformity



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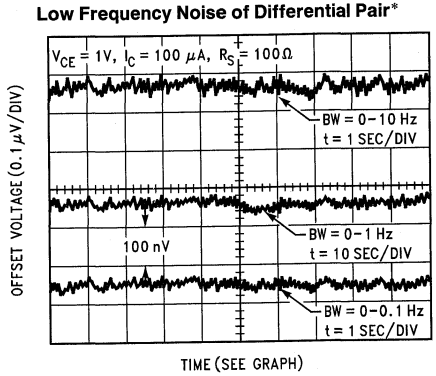
Low Frequency Noise of Differential Pair*



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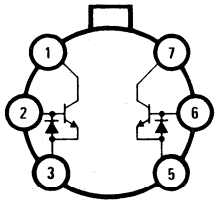
*Unit must be in still air environment so that differential lead temperature is held to less than 0.0003°C.

Connection Diagrams

Metal Can Package



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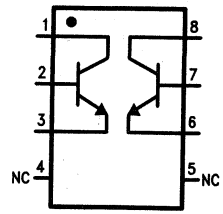
Top View

Order Number LM194H, LM194H/883*, LM394H, LM394BH or LM394CH
See NS Package Number H06C

Dual-In-Line and Small Outline Packages



TL/H/9241–13

Top View

Order Number LM394N or LM394CN
See NS Package Number N08E

*Available per SMD #5962-8777701

National Semiconductor

LM359 Dual, High Speed, Programmable, Current Mode (Norton) Amplifiers

General Description

The LM359 consists of two current differencing (Norton) input amplifiers. Design emphasis has been placed on obtaining high frequency performance and providing user programmable amplifier operating characteristics. Each amplifier is broadbanded to provide a high gain bandwidth product, fast slew rate and stable operation for an inverting closed loop gain of 10 or greater. Pins for additional external frequency compensation are provided. The amplifiers are designed to operate from a single supply and can accommodate input common-mode voltages greater than the supply.

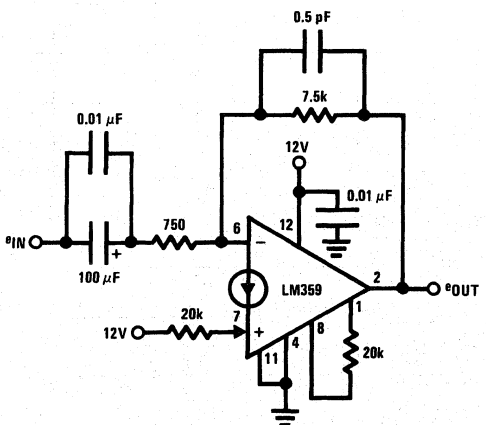
Applications

- General purpose video amplifiers
- High frequency, high Q active filters
- Photo-diode amplifiers
- Wide frequency range waveform generation circuits
- All LM3900 AC applications work to much higher frequencies

Features

- User programmable gain bandwidth product, slew rate, input bias current, output stage biasing current and total device power dissipation
- High gain bandwidth product (I_{SET} = 0.5 mA)
  400 MHz for A_V = 10 to 100
  30 MHz for A_V = 1
- High slew rate (I_{SET} = 0.5 mA)
  60 V/μs for A_V = 10 to 100
  30 V/μs for A_V = 1
- Current differencing inputs allow high common-mode input voltages
- Operates from a single 5V to 22V supply
- Large inverting amplifier output swing, 2 mV to V_{CC} − 2V
- Low spot noise, 6 nV/$\sqrt{Hz}$, for f > 1 kHz

Typical Application



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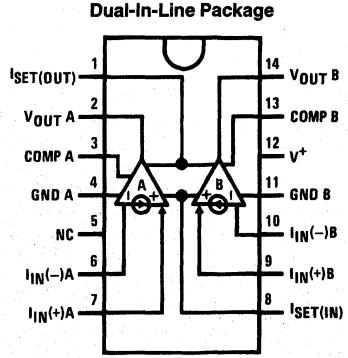
- A_V = 20 dB
- −3 dB bandwidth = 2.5 Hz to 25 MHz
- Differential phase error < 1° at 3.58 MHz
- Differential gain error < 0.5% at 3.58 MHz

Connection Diagram

Dual-In-Line Package



TL/H/7788–2

Top View

Order Number LM359J, LM359M or LM359N
See NS Package Number J14A, M14A or N14A

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage — 22 V_{DC} or ±11 V_{DC}

Power Dissipation (Note 1)
- J Package — 1W
- N Package — 750 mW

Maximum T_J
- J Package — +150°C
- N Package — +125°C

Thermal Resistance

J Package

θ_{jA} 147°C/W still air
110°C/W with 400 linear feet/min air flow

N Package

θ_{jA} 100°C/W still air
75°C/W with 400 linear feet/min air flow

Input Currents, $I_{IN}(+)$ or $I_{IN}(-)$ — 10 mA_{DC}

Set Currents, $I_{SET(IN)}$ or $I_{SET(OUT)}$ — 2 mA_{DC}

Operating Temperature Range
- LM359 — 0°C to +70°C

Storage Temperature Range — −65°C to +150°C

Lead Temperature (Soldering, 10 sec.) — 260°C

Soldering Information
- Dual-In-Line Package
  - Soldering (10 sec.) — 260°C
- Small Outline Package
  - Vapor Phase (60 sec.) — 215°C
  - Infrared (15 sec.) — 220°C

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

ESD rating to be determined.

Electrical Characteristics $I_{SET(IN)} = I_{SET(OUT)} = 0.5$ mA, $V_{supply} = 12V$, $T_A = 25°C$ unless otherwise noted

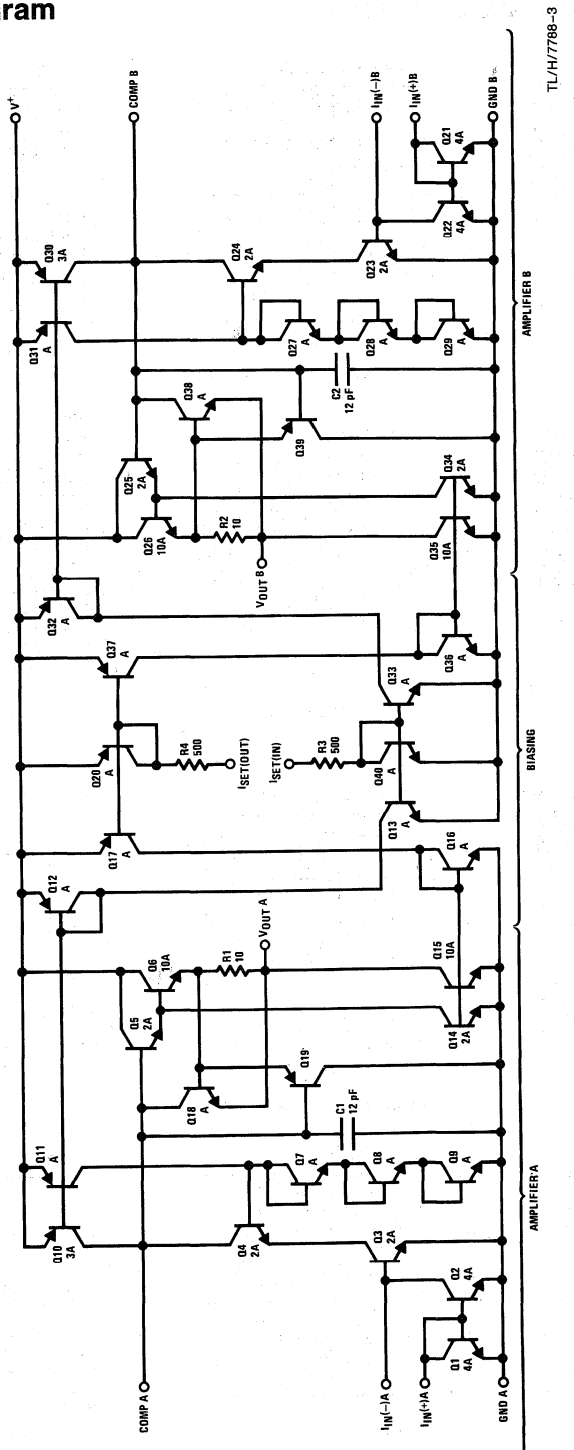
Parameter	Conditions	LM359 Min	LM359 Typ	LM359 Max	Units
Open Loop Voltage Gain	$V_{supply} = 12V$, $R_L = 1k$, $f = 100$ Hz $T_A = 125°C$	62	72 68		dB dB
Bandwidth Unity Gain	$R_{IN} = 1$ kΩ, $C_{comp} = 10$ pF	15	30		MHz
Gain Bandwidth Product Gain of 10 to 100	$R_{IN} = 50Ω$ to $200Ω$	200	400		MHz
Slew Rate Unity Gain Gain of 10 to 100	 $R_{IN} = 1$ kΩ, $C_{comp} = 10$ pF $R_{IN} < 200Ω$		 30 60		 V/μs V/μs
Amplifier to Amplifier Coupling	$f = 100$ Hz to 100 kHz, $R_L = 1k$		−80		dB
Mirror Gain (Note 2)	at 2 mA $I_{IN}(+)$, $I_{SET} = 5$ μA, $T_A = 25°C$ at 0.2 mA $I_{IN}(+)$, $I_{SET} = 5$ μA Over Temp. at 20 μA $I_{IN}(+)$, $I_{SET} = 5$ μA Over Temp.	0.9 0.9 0.9	1.0 1.0 1.0	1.1 1.1 1.1	μA/μA μA/μA μA/μA
ΔMirror Gain (Note 2)	at 20 μA to 0.2 mA $I_{IN}(+)$ Over Temp, $I_{SET} = 5$ μA		3	5	%
Input Bias Current	Inverting Input, $T_A = 25°C$ Over Temp.		8	15 30	μA μA
Input Resistance (βre)	Inverting Input		2.5		kΩ
Output Resistance	$I_{OUT} = 15$ mA rms, $f = 1$ MHz		3.5		Ω
Output Voltage Swing V_{OUT} High V_{OUT} Low	$R_L = 600Ω$ $I_{IN}(-)$ and $I_{IN}(+)$ Grounded $I_{IN}(-) = 100$ μA, $I_{IN}(+) = 0$	 9.5	 10.3 2	 50	 V mV
Output Currents Source Sink (Linear Region) Sink (Overdriven)	 $I_{IN}(-)$ and $I_{IN}(+)$ Grounded, $R_L = 100Ω$ $V_{comp} - 0.5V = V_{OUT} = 1V$, $I_{IN}(+) = 0$ $I_{IN}(-) = 100$ μA, $I_{IN}(+) = 0$, V_{OUT} Force = 1V	 16 1.5	 40 4.7 3	 	 mA mA mA
Supply Current	Non-Inverting Input Grounded, $R_L = \infty$		18.5	22	mA
Power Supply Rejection (Note 3)	$f = 120$ Hz, $I_{IN}(+)$ Grounded	40	50		dB

Note 1: See Maximum Power Dissipation graph.

Note 2: Mirror gain is the current gain of the current mirror which is used as the non-inverting input. $\left(A_I = \frac{I_{IN}(-)}{I_{IN}(+)}\right)$ ΔMirror Gain is the % change in A_I for two different mirror currents at any given temperature.

Note 3: See Supply Rejection graphs.

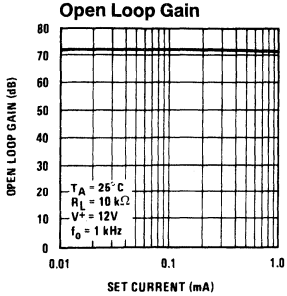
Schematic Diagram



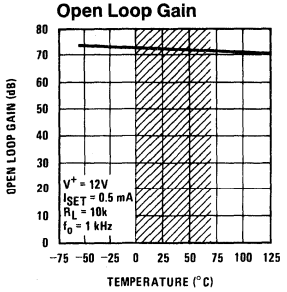
TL/H/7788–3

Typical Performance Characteristics

Open Loop Gain

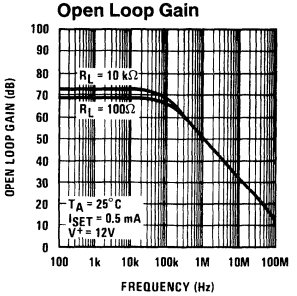


Open Loop Gain

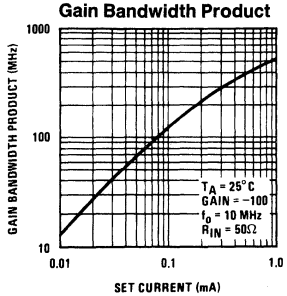


Note: Shaded area refers to LM359

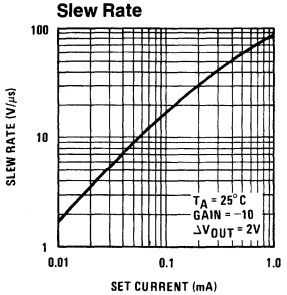
Open Loop Gain



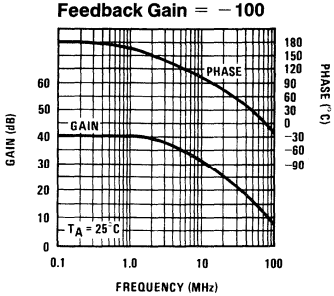
Gain Bandwidth Product



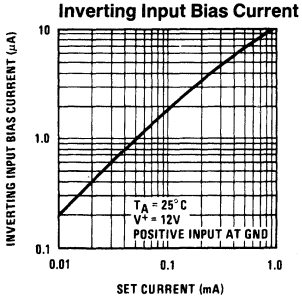
Slew Rate



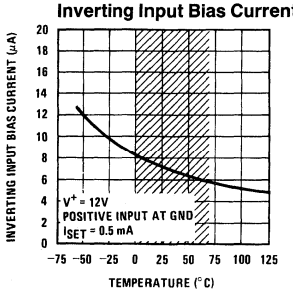
Gain and Phase
Feedback Gain = −100



Inverting Input Bias Current

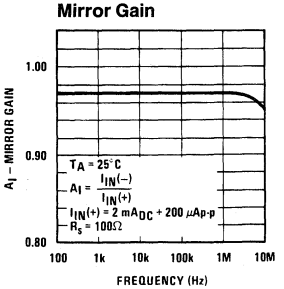


Inverting Input Bias Current

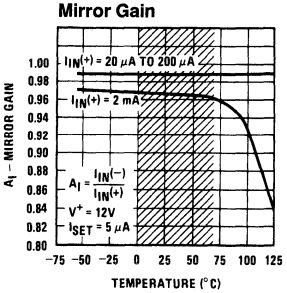


Note: Shaded area refers to LM359

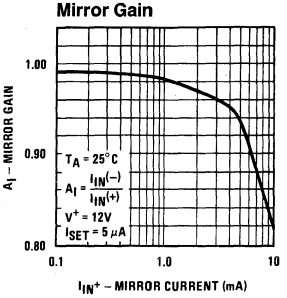
Mirror Gain



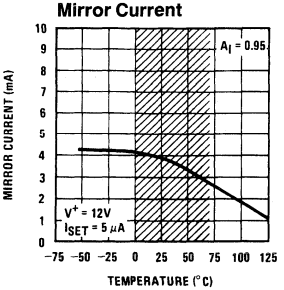
Mirror Gain



Mirror Gain



Mirror Current



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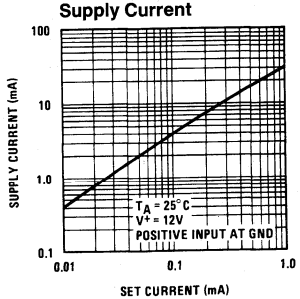
Note: Shaded area refers to LM359

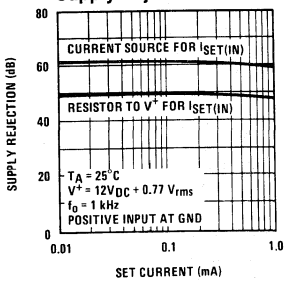
Note: Shaded area refers to LM359

Typical Performance Characteristics (Continued)

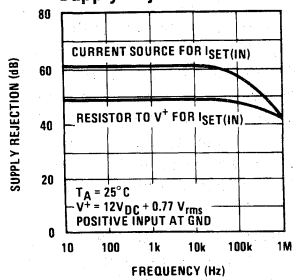
Supply Current



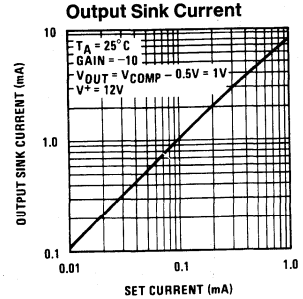
Supply Rejection



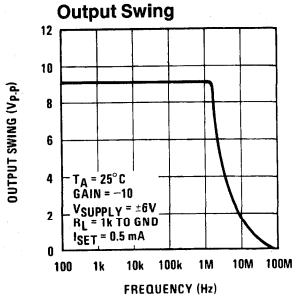
Supply Rejection



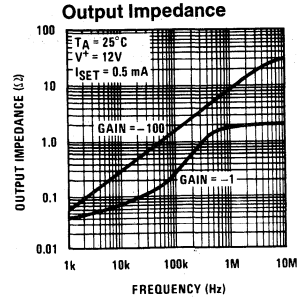
Output Sink Current



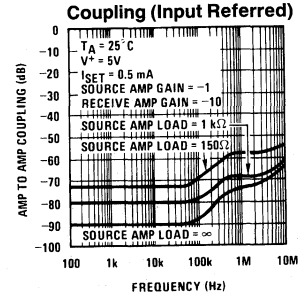
Output Swing



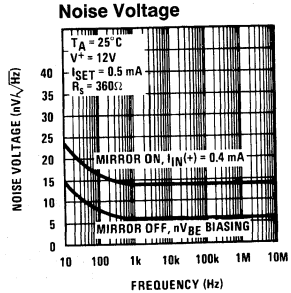
Output Impedance



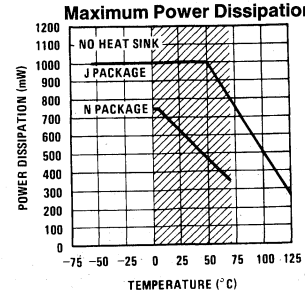
Amplifier to Amplifier Coupling (Input Referred)



Noise Voltage



Maximum Power Dissipation



Note: Shaded area refers to LM359J/LM359N

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Application Hints

The LM359 consists of two wide bandwidth, decompensated current differencing (Norton) amplifiers. Although similar in operation to the original LM3900, design emphasis for these amplifiers has been placed on obtaining much higher frequency performance as illustrated in *Figure 1*.

This significant improvement in frequency response is the result of using a common-emitter/common-base (cascode) gain stage which is typical in many discrete and integrated video and RF circuit designs. Another versatile aspect of these amplifiers is the ability to externally program many internal amplifier parameters to suit the requirements of a wide variety of applications in which this type of amplifier can be used.

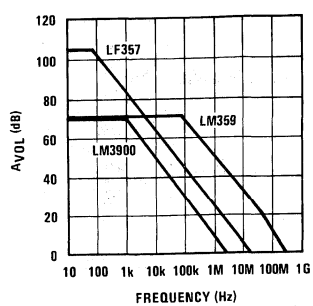

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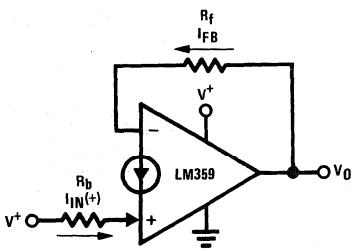
FIGURE 1

Application Hints (Continued)

DC BIASING

The LM359 is intended for single supply voltage operation which requires DC biasing of the output. The current mirror circuitry which provides the non-inverting input for the amplifier also facilitates DC biasing the output. The basic operation of this current mirror is that *the current (both DC and AC) flowing into the non-inverting input will force an equal amount of current to flow into the inverting input.* The mirror gain (A_I) specification is the measure of how closely these two currents match. For more details see National Application Note AN-72.

DC biasing of the output is accomplished by establishing a reference DC current into the (+) input, $I_{IN}(+)$, and requiring the output to provide the (−) input current. This forces the output DC level to be whatever value necessary (within the output voltage swing of the amplifier) to provide this DC reference current, *Figure 2*.



$$V_{o(DC)} = V_{BE}(-) + I_{FB}\,R_f$$

$$I_{FB} = I_{IN}(+)\,A_I + I_b(-)$$

$$I_{IN}(+) = \frac{V^+ - V_{BE}(+)}{R_b}$$

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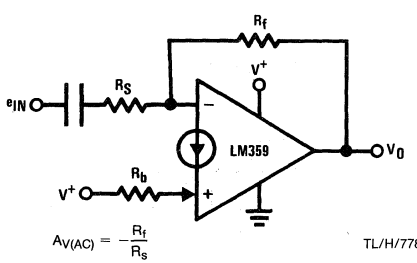
$I_b(-)$ is the inverting input bias current

FIGURE 2

The DC input voltage at each input is a transistor V_{BE} ($\cong$ 0.6 V_{DC}) and must be considered for DC biasing. For most applications, the supply voltage, V^+, is suitable and convenient for establishing $I_{IN}(+)$. The inverting input bias current, $I_b(-)$, is a direct function of the programmable input stage current (see current programmability section) and to obtain predictable output DC biasing set $I_{IN}(+) \geq 10I_b(-)$.

The following figures illustrate typical biasing schemes for AC amplifiers using the LM359:



$$A_{V(AC)} = -\frac{R_f}{R_s}$$

$$V_{o(DC)} = V_{BE}(-) + R_f\left[\frac{V^+ - V_{BE}(+)}{R_b} + I_b(-)\right]$$

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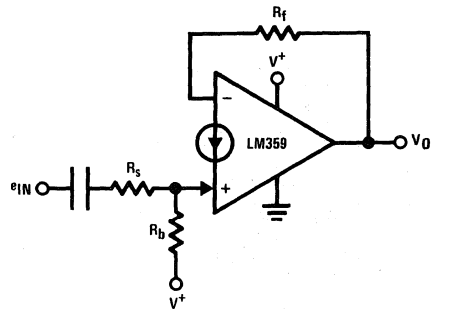
FIGURE 3. Biasing an Inverting AC Amplifier



$$A_{V(AC)} = +\frac{R_f}{R_s + r_e}$$

$$V_{o(DC)} = V_{BE}(-) + R_f\left[\frac{V^+ - V_{BE}(+)}{R_b} + I_b(-)\right]$$

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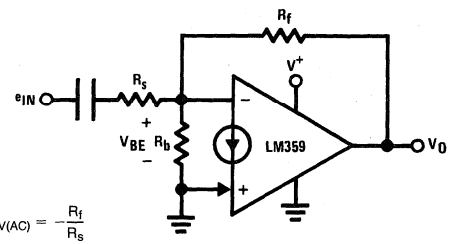
FIGURE 4. Biasing a Non-Inverting AC Amplifier



$$A_{V(AC)} = -\frac{R_f}{R_s}$$

$$V_{o(DC)} = V_{BE}(-)\left(1 + \frac{R_f}{R_B}\right) + I_b(-)R_f$$

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FIGURE 5. nV_{BE} Biasing

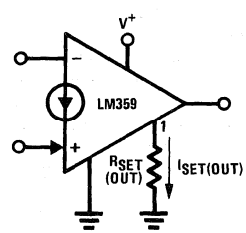
The nV_{BE} biasing configuration is most useful for low noise applications where a reduced input impedance can be accommodated (see typical applications section).

OPERATING CURRENT PROGRAMMABILITY (I_{SET})

The input bias current, slew rate, gain bandwidth product, output drive capability and total device power consumption of both amplifiers can be simultaneously controlled and optimized via the two programming pins $I_{SET(OUT)}$ and $I_{SET(IN)}$.

$I_{SET(OUT)}$

The output set current ($I_{SET(OUT)}$) is equal to the amount of current sourced from pin 1 and establishes the class A biasing current for the Darlington emitter follower output stage. Using a single resistor from pin 1 to ground, as shown in *Figure 6*, this current is equal to:



$$I_{SET(OUT)} = \frac{V^+ - V_{BE}}{R_{SET(OUT)} + 500\Omega}$$

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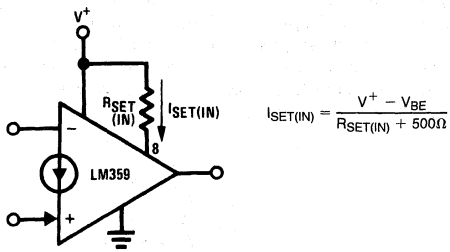
FIGURE 6. Establishing the Output Set Current

Application Hints (Continued)

The output set current can be adjusted to optimize the amount of current the output of the amplifier can sink to drive load capacitance and for loads connected to V^+. *The maximum output sinking current is approximately 10 times $I_{SET(OUT)}$.* This set current is best used to reduce the total device supply current if the amplifiers are not required to drive small load impedances.

$I_{SET(IN)}$

The input set current $I_{SET(IN)}$ is equal to the current flowing into pin 8. A resistor from pin 8 to V^+ sets this current to be:



$$I_{SET(IN)} = \frac{V^+ - V_{BE}}{R_{SET(IN)} + 500\Omega}$$

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FIGURE 7. Establishing the Input Set Current

$I_{SET(IN)}$ is most significant in controlling the AC characteristics of the LM359 as it directly sets the total input stage current of the amplifiers which determines the maximum slew rate, the frequency of the open loop dominant pole, the input resistance of the (−) input and the biasing current $I_b(-)$. All of these parameters are significant in wide band amplifier design. The input stage current is approximately 3 times $I_{SET(IN)}$ and by using this relationship the following first order approximations for these AC parameters are:

$$S_{r(MAX)} = \text{max slew rate} \cong \frac{3\, I_{SET(IN)}\, (10^{-6})}{C_{comp}} \; (V/\mu s)$$

$$\text{frequency of dominant pole} \cong \frac{3\, I_{SET(IN)}}{2\pi\, C_{comp}\, A_{VOL}\, (0.026V)} \; (Hz)$$

$$\text{input resistance} = \beta re \cong \frac{150\, (0.026V)}{3 I_{SET(IN)}} \; (\Omega)$$

where C_{comp} is the total capacitance from the compensation pin (pin 3 or pin 13) to ground, A_{VOL} is the low frequency open loop voltage gain in V/V and an ambient temperature of 25°C is assumed (KT/q = 26 mV and β_{typ} = 150). $I_{SET(IN)}$ also controls the DC input bias current by the expression:

$$I_b(-) = \frac{3 I_{SET}}{\beta} \cong \frac{I_{SET}}{50} \text{ for NPN } \beta = 150$$

which is important for DC biasing considerations.

The total device supply current (for both amplifiers) is also a direct function of the set currents and can be approximated by:

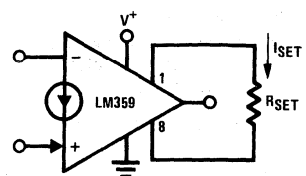
$$I_{supply} \cong 27 \times I_{SET(OUT)} + 11 \times I_{SET(IN)}$$

with each set current programmed by individual resistors.

PROGRAMMING WITH A SINGLE RESISTOR

Operating current programming may also be accomplished using only one resistor by letting $I_{SET(IN)}$ equal $I_{SET(OUT)}$. The programming current is now referred to as I_{SET} and it is created by connecting a resistor from pin 1 to pin 8 *(Figure 8)*.

$$I_{SET} = \frac{V^+ - 2\, V_{BE}}{R_{SET} + 1\ k\Omega} \text{ where } V_{BE} \cong 0.6V$$



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$I_{SET(IN)} = I_{SET(OUT)} = I_{SET}$

FIGURE 8. Single Resistor Programming of I_{SET}

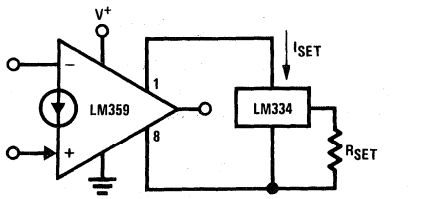
This configuration does not affect any of the internal set current dependent parameters differently than previously discussed except the total supply current which is now equal to:

$$I_{supply} \cong 37 \times I_{SET}$$

Care must be taken when using resistors to program the set current to prevent significantly increasing the supply voltage above the value used to determine the set current. This would cause an increase in total supply current due to the resulting increase in set current and the maximum device power dissipation could be exceeded. The set resistor value(s) should be adjusted for the new supply voltage.

Application Hints (Continued)

One method to avoid this is to use an adjustable current source which has voltage compliance to generate the set current as shown in *Figure 9*.



$$I_{SET} = \frac{67.7\ mV}{R_{SET}} @ 25°C$$

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FIGURE 9. Current Source Programming of I_{SET}

This circuit allows I_{SET} to remain constant over the entire supply voltage range of the LM359 which also improves power supply ripple rejection as illustrated in the Typical Performance Characteristics. It should be noted, however, that the current through the LM334 as shown will change linearly with temperature but this can be compensated for (see LM334 data sheet).

Pin 1 must never be shorted to ground or pin 8 never shorted to V^+ without limiting the current to 2 mA or less to prevent catastrophic device failure.

CONSIDERATIONS FOR HIGH FREQUENCY OPERATION

The LM359 is intended for use in relatively high frequency applications and many factors external to the amplifier itself must be considered. Minimization of stray capacitances and their effect on circuit operation are the primary requirements. The following list contains some general guidelines to help accomplish this end:

1. Keep the leads of all external components as short as possible.
2. Place components conducting signal current from the output of an amplifier away from that amplifier's non-inverting input.
3. Use reasonably low value resistances for gain setting and biasing.
4. Use of a ground plane is helpful in providing a shielding effect between the inputs and from input to output. Avoid using vector boards.
5. Use a single-point ground and single-point supply distribution to minimize crosstalk. Always connect the two grounds (one from each amplifier) together.
6. Avoid use of long wires (> 2 ") but if necessary, use shielded wire.
7. Bypass the supply close to the device with a low inductance, low value capacitor (typically a 0.01 μF ceramic) to create a good high frequency ground. If long supply leads are unavoidable, a small resistor (~10Ω) in series with the bypass capacitor may be needed and using shielded wire for the supply leads is also recommended.

COMPENSATION

The LM359 is internally compensated for stability with closed loop inverting gains of 10 or more. For an inverting gain of less than 10 and all non-inverting amplifiers (the amplifier always has 100% negative current feedback regardless of the gain in the non-inverting configuration) some external frequency compensation is required because the stray capacitance to ground from the (−) input and the feedback resistor add additional lagging phase within the feedback loop. The value of the input capacitance will typically be in the range of 6 pF to 10 pF for a reasonably constructed circuit board. When using a feedback resistance of 30 kΩ or less, the best method of compensation, without sacrificing slew rate, is to add a lead capacitor in parallel with the feedback resistor with a value on the order of 1 pF to 5 pF as shown in *Figure 10*.

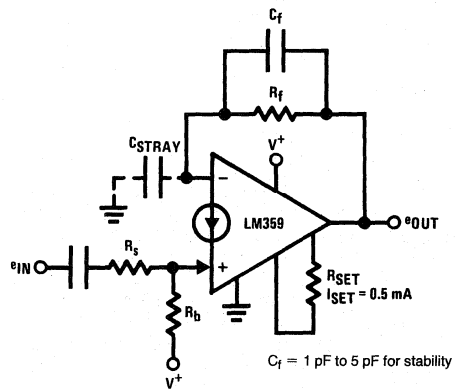

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FIGURE 10. Best Method of Compensation

Another method of compensation is to increase the effective value of the internal compensation capacitor by adding capacitance from the COMP pin of an amplifier to ground. An external 20 pF capacitor will generally compensate for all gain settings but will also reduce the gain bandwidth product and the slew rate. These same results can also be obtained by reducing $I_{SET(IN)}$ if the full capabilities of the amplifier are not required. This method is termed over-compensation.

Another area of concern from a stability standpoint is that of capacitive loading. The amplifier will generally drive capacitive loads up to 100 pF without oscillation problems. Any larger C loads can be isolated from the output as shown in *Figure 11*. Over-compensation of the amplifier can also be used if the corresponding reduction of the GBW product can be afforded.

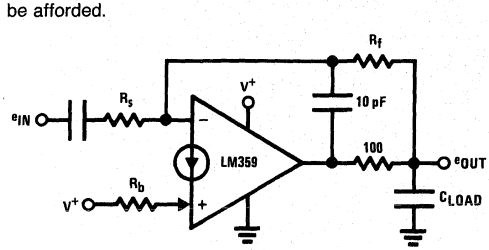

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FIGURE 11. Isolating Large Capacitive Loads

Application Hints (Continued)

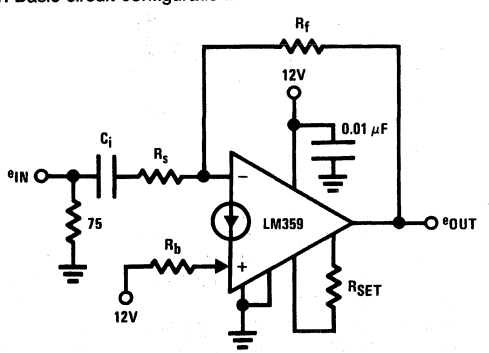
In most applications using the LM359, the input signal will be AC coupled so as not to affect the DC biasing of the amplifier. This gives rise to another subtlety of high frequency circuits which is the effective series inductance (ESL) of the coupling capacitor which creates an increase in the impedance of the capacitor at high frequencies and can cause an unexpected gain reduction. Low ESL capacitors like solid tantalum for large values of C and ceramic for smaller values are recommended. A parallel combination of the two types is even better for gain accuracy over a wide frequency range.

AMPLIFIER DESIGN EXAMPLES

The ability of the LM359 to provide gain at frequencies higher than most monolithic amplifiers can provide makes it most useful as a basic broadband amplification stage. The design of standard inverting and non-inverting amplifiers, though different than standard op amp design due to the current differencing inputs, also entail subtle design differences between the two types of amplifiers. These differences will be best illustrated by design examples. For these examples a practical video amplifier with a passband of 8 Hz to 10 MHz and a gain of 20 dB will be used. It will be assumed that the input will come from a 75Ω source and proper signal termination will be considered. The supply voltage is 12 V_{DC} and single resistor programming of the operating current, I_{SET}, will be used for simplicity.

AN INVERTING VIDEO AMPLIFIER

1. Basic circuit configuration:



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2. Determine the required I_{SET} from the characteristic curves for gain bandwidth product.

$$GBW_{MIN} = 10 \times 10\ MHz = 100\ MHz$$

For a flat response to 10 MHz a closed loop response to two octaves above 10 MHz (40 MHz) will be sufficient.

Actual GBW = 10 × 40 MHz = 400 MHz

I_{SET} required = 0.5 mA

$$R_{SET} = \frac{V^+ - 2\,V_{BE}}{I_{SET}} - 1\,k\Omega = \frac{10.8V}{0.5\,mA} - 1\,k\Omega = 20.6\,k\Omega$$

3. Determine maximum value for R_f to provide stable DC biasing

$$I_{f(MIN)} \geq 10 \times \frac{3\,I_{SET}}{\beta} = 100\,\mu A \text{ minimum DC feedback current}$$

Optimum output DC level for maximum symmetrical swing without clipping is:

$$V_{oDC(opt)} = \frac{V_{o(MAX)} - V_{o(MIN)}}{2} + V_{o(MIN)}$$

$$\approx \frac{(V^+ - 3\,V_{BE}) - 2\,mV}{2}$$

$$V_{oDC(opt)} \cong \frac{12 - 1.8V}{2} = \frac{10.2V}{2} = 5.1\,V_{DC}$$

$R_{f(MAX)}$ can now be found:

$$R_{f(MAX)} = \frac{V_{oDC(opt)} - V_{BE(-)}}{I_{f(MIN)}} = \frac{5.1V - 0.6V}{100\,\mu A} = 45\,k\Omega$$

This value should not be exceeded for predictable DC biasing.

4. Select R_s to be large enough so as not to appreciably load the input termination resistance:

$$R_s \geq 750\Omega \text{ Let } R_s = 750\Omega$$

5. Select R_f for appropriate gain:

$$A_V = -\frac{R_f}{R_s} \text{ so; } R_f = 10\,R_s = 7.5\,k\Omega$$

7.5 kΩ is less than the calculated $R_{f(MAX)}$ so DC predictability is insured.

6. Since R_f = 7.5k, for the output to be biased to 5.1 V_{DC}, the reference current $I_{IN}(+)$ must be:

$$I_{IN}(+) = \frac{5.1V - V_{BE(-)}}{R_f} = \frac{5.1V - 0.6V}{7.5\,k\Omega} = 600\,\mu A$$

Now R_b can be found by:

$$R_b = \frac{V^+ - V_{BE(+)}}{I_{IN}(+)} = \frac{12 - 0.6}{600\,\mu A} = 19\,k\Omega$$

7. Select C_i to provide the proper gain for the 8 Hz minimum input frequency:

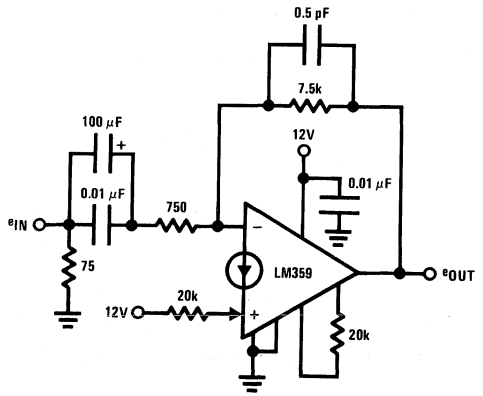
$$C_i \geq \frac{1}{2\pi\,R_s\,(f_{low})} = \frac{1}{2\pi\,(750\Omega)\,(8\,Hz)} = 26\,\mu F$$

A larger value of C_i will allow a flat frequency response down to 8 Hz and a 0.01 µF ceramic capacitor in parallel with C_i will maintain high frequency gain accuracy.

8. Test for peaking of the frequency response and add a feedback "lead" capacitor to compensate if necessary.

Application Hints (Continued)

Final Circuit Using Standard 5% Tolerance Resistor Values:



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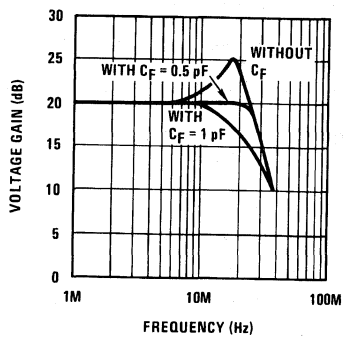
Circuit Performance:



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$V_{o(DC)}$ = 5.1V

Differential phase error < 1° for 3.58 MHz f_{IN}

Differential gain error < 0.5% for 3.58 MHz f_{IN}

$f_{-3\ dB}$ low = 2.5 Hz

A NON-INVERTING VIDEO AMPLIFIER

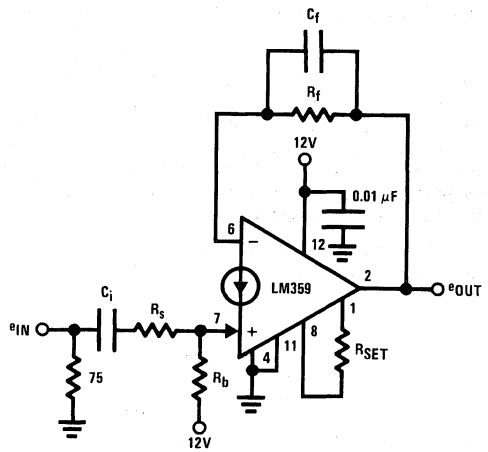
For this case several design considerations must be dealt with.

- The output voltage (AC and DC) is strictly a function of the size of the feedback resistor and the sum of AC and DC "mirror current" flowing into the (+) input.
- The amplifier always has 100% current feedback so external compensation is required. Add a small (1 pF–5 pF) feedback capacitance to leave the amplifier's open loop response and slew rate unaffected.
- To prevent saturating the mirror stage the total AC and DC current flowing into the amplifier's (+) input should be less than 2 mA.
- The output's maximum negative swing is one diode above ground due to the V_{BE} diode clamp at the (−) input.

DESIGN EXAMPLE:

e_{IN} = 50 mV (MAX), f_{IN} = 10 MHz (MAX), desired circuit BW = 20 MHz, A_V = 20 dB, driving source impedance = 75Ω, V^+ = 12V.

1. Basic circuit configuration:



TL/H/7788–20

2. Select I_{SET} to provide adequate amplifier bandwidth so that the closed loop bandwidth will be determined by R_f and C_f. To do this, the set current should program an amplifier open loop gain of at least 20 dB at the desired closed loop bandwidth of the circuit. For this example, an I_{SET} of 0.5 mA will provide 26 dB of open loop gain at 20 MHz which will be sufficient. Using single resistor programming for I_{SET}:

$$R_{SET} = \frac{V^+ - 2\,V_{BE}}{I_{SET}} - 1\ k\Omega = 20.6\ k\Omega$$

3. Since the closed loop bandwidth will be determined by

$$R_f \text{ and } C_f \left(f_{-3\,dB} = \frac{1}{2\pi\, R_f\, C_f} \right)$$

Application Hints (Continued)

to obtain a 20 MHz bandwidth, both R_f and C_f should be kept small. It can be assumed that C_f can be in the range of 1 pF to 5 pF for carefully constructed circuit boards to insure stability and allow a flat frequency response. This will limit the value of R_f to be within the range of:

$$\frac{1}{2\pi\ 5\ \text{pF}\ 20\ \text{MHz}} \leq R_f \leq \frac{1}{2\pi\ 1\ \text{pF}\ 20\ \text{MHz}}$$

$$\text{or } 1.6\ \text{k}\Omega \leq R_f \leq 7.96\ \text{k}\Omega$$

Also, for a closed loop gain of +10, R_f must be 10 times $R_s + r_e$ where r_e is the mirror diode resistance.

4. So as not to appreciably load the 75Ω input termination resistance the value of $(R_s + r_e)$ is set to 750Ω.
5. For $A_v = 10$; R_f is set to 7.5 kΩ.
6. The optimum output DC level for symmetrical AC swing is:

$$V_{oDC(opt)} = \frac{V_{o(MAX)} - V_{o(MIN)}}{2} + V_{o(MIN)}$$

$$= \frac{(12 - 1.8)V - 0.6V}{2} + 0.6V = 5.4\ V_{DC}$$

7. The DC feedback current must be:

$$I_{FB} = \frac{V_{oDC(opt)} - V_{BE(-)}}{R_f} = \frac{5.4V - 0.6V}{7.5k}$$

$$= 640\ \mu A = I_{IN(+)}$$

DC biasing predictability will be insured because 640 μA is greater than the minimum of $I_{SET}/5$ or 100 μA.

For gain accuracy the total AC and DC mirror current should be less than 2 mA. For this example the maximum AC mirror current will be;

$$\frac{\pm e_{in\ peak}}{R_s + r_e} = \frac{\pm 50\ \text{mV}}{750\Omega} = \pm 66\ \mu A$$

therefore the total mirror current range will be 574 μA to 706 μA which will insure gain accuracy.

8. R_b can now be found:

$$R_b = \frac{V^+ - V_{BE(+)}}{I_{IN(+)}} = \frac{12 - 0.6}{640\ \mu A} = 17.8\ \text{k}\Omega$$

9. Since $R_s + r_e$ will be 750Ω and r_e is fixed by the DC mirror current to be:

$$r_e = \frac{KT}{q\ I_{IN(+)}} = \frac{26\ \text{mV}}{640\ \mu A} \cong 40\Omega \text{ at } 25°C$$

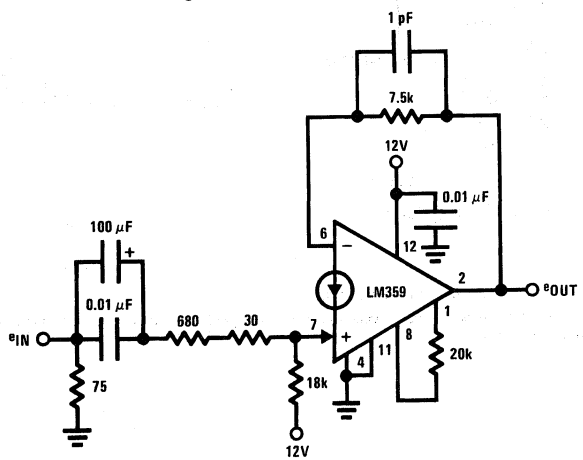
R_s must be 750Ω−40Ω or 710Ω which can be a 680Ω resistor in series with a 30Ω resistor which are standard 5% tolerance resistor values.

10. As a final design step, C_i must be selected to pass the lower passband frequency corner of 8 Hz for this example.

$$C_i = \frac{1}{2\pi\ (R_s + r_e)\ f_{low}} = \frac{1}{2\pi\ (750\Omega)\ (8\ \text{Hz})} = 26.5\ \mu F$$

A larger value may be used and a 0.01 μF ceramic capacitor in parallel with C_i will maintain high frequency gain accuracy.

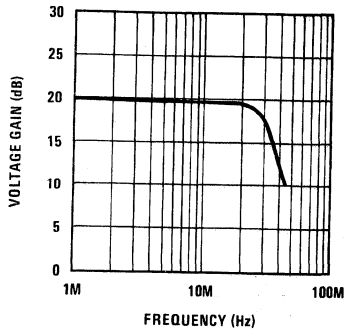
Final Circuit Using Standard 5% Tolerance Resistor Values



TL/H/7788–21

Application Hints (Continued)

Circuit Performance



TL/H/7788–22

$V_{o(DC)}$ = 5.4V
Differential phase error < 0.5°
Differential gain error < 2%
$f_{-3\ dB}$ low = 2.5 Hz

GENERAL PRECAUTIONS

The LM359 is designed primarily for single supply operation but split supplies may be used if the negative supply voltage is well regulated as the amplifiers have no negative supply rejection.

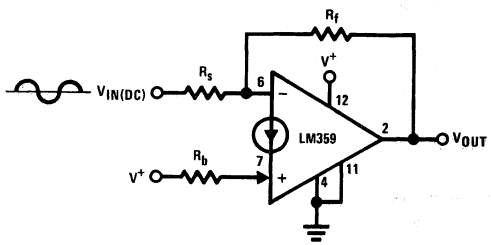
The total device power dissipation must always be kept in mind when selecting an operating supply voltage, the programming current, I_{SET}, and the load resistance, particularly when DC coupling the output to a succeeding stage. To prevent damaging the current mirror input diode, the mirror current should always be limited to 10 mA, or less, which is important if the input is susceptible to high voltage transients. The voltage at any of the inputs must not be forced more negative than −0.7V without limiting the current to 10 mA.

The supply voltage must never be reversed to the device; however, plugging the device into a socket backwards would then connect the positive supply voltage to the pin that has no internal connection (pin 5) which may prevent inadvertent device failure.

Typical Applications

DC Coupled Inputs

Inverting

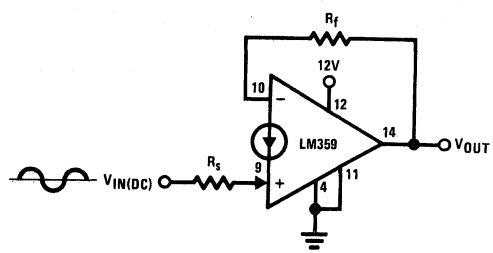


TL/H/7788–23

$$V_{o(DC)} = \left[\frac{V^+ - V_{BE(+)}}{R_b} - \frac{V_{IN(DC)} - V_{BE(-)}}{R_s}\right] R_f + V_{BE(-)}$$

$$A_{V(AC)} = \frac{R_f}{R_s}$$

Non-Inverting



TL/H/7788–24

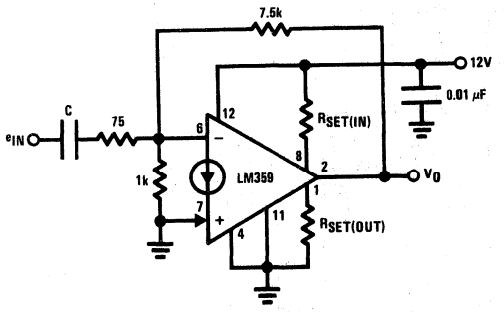
$$V_{o(DC)} = V_{BE(-)} + \frac{(V_{IN(DC)} - V_{BE(+)})\, R_f}{R_s}$$

$$A_{V(AC)} = +\frac{R_f}{R_s + r_{e(+)}}$$

- Eliminates the need for an input coupling capacitor
- Input DC level must be stable and can exceed the supply voltage of the LM359 provided that maximum input currents are not exceeded.

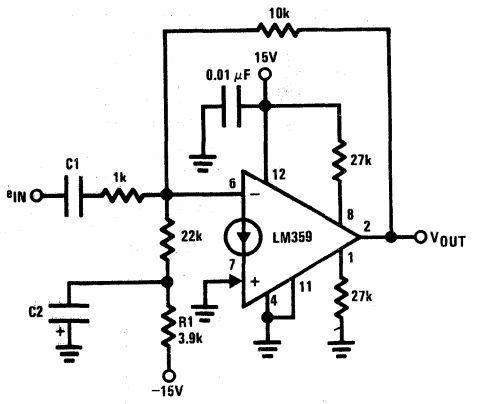
Application Hints (Continued)

Noise Reduction using nV_{BE} Biasing



TL/H/7788–25

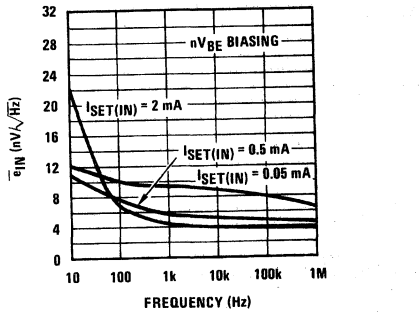
nV_{BE} Biasing with a Negative Supply



TL/H/7788–26

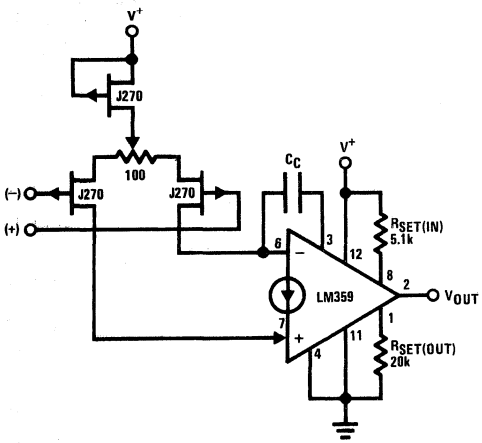
- R1 and C2 provide additional filtering of the negative biasing supply

Typical Input Referred Noise Performance



TL/H/7788–27

Adding a JFET Input Stage

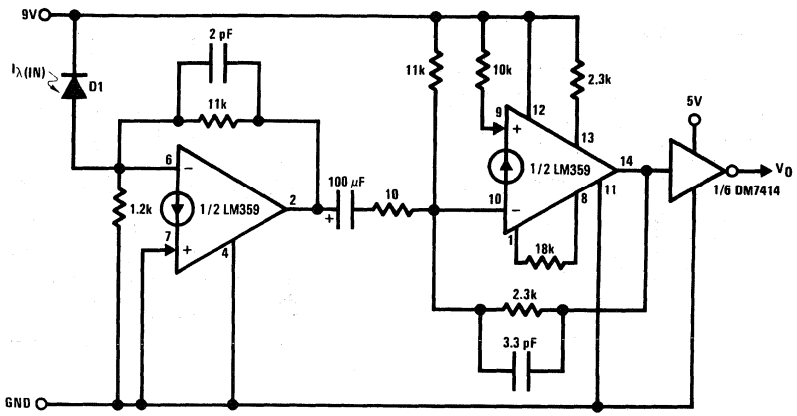


TL/H/7788–28

- FET input voltage mode op amp
- For $A_V = +1$; BW = 40 MHz, S_r = 60 V/μs; C_C = 51 pF
- For $A_V = +11$; BW = 24 MHz, S_r = 130 V/μs; C_C = 5 pF
- For $A_V = +100$; BW = 4.5 MHz, S_r = 150 V/μs; C_C = 2 pF
- V_{OS} is typically <25 mV; 100Ω potentiometer allows a V_{OS} adjust range of ≈ ±200 mV
- Inputs must be DC biased for single supply operation

Typical Applications (Continued)

Photo Diode Amplifier

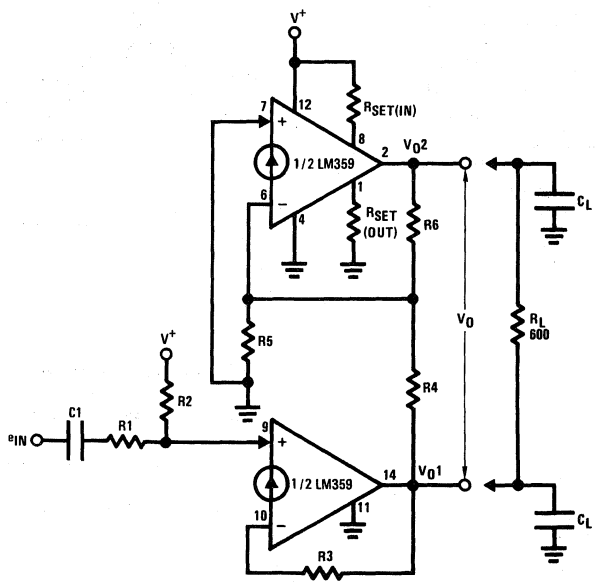


TL/H/7788–29

D1 ~ RCA N-Type Silicon P-I-N Photodiode

- Frequency response of greater than 10 MHz
- If slow rise and fall times can be tolerated the gate on the output can be removed. In this case the rise and the fall time of the LM359 is 40 ns.
- T_{PDL} = 45 ns, T_{PDH} = 50 ns — T^2L output

Balanced Line Driver



TL/H/7788–30

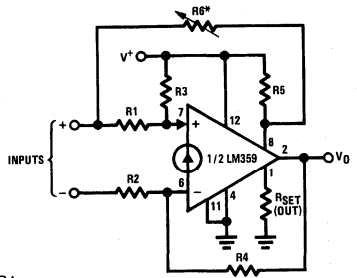
For $V_O1 = V_O2 = \frac{V^+}{2}$, $\frac{R3}{R2} = \frac{V^+ - 2\phi}{2(V^+ - \phi)}$, $\frac{R6}{R5} = \frac{V^+ - 2\phi}{\phi}$ where $\phi \approx 0.6V$

$$A_V = \frac{R3}{R1}\left(\frac{R6}{R4} + 1\right)$$

- 1 MHz—3 dB bandwidth with gain of 10 and 0 dbm into 600Ω
- 0.3% distortion at full bandwidth; reduced to 0.05% with bandwidth of 10 kHz
- Will drive C_L = 1500 pF with no additional compensation, ±0.01 μF with C_{comp} = 180 pF
- 70 dB signal to noise ratio at 0 dbm into 600Ω, 10 kHz bandwidth

Typical Applications (Continued)

Difference Amplifier



$$V_{o(DC)} = \frac{R4}{R3}(V^+ - \phi) \text{ where } \phi = 0.6V$$

TL/H/7788–31

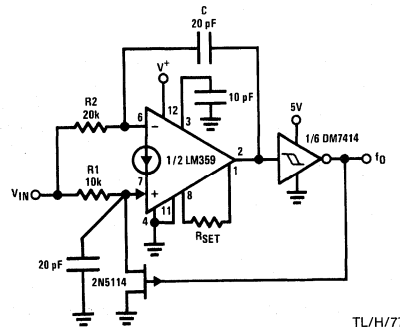
$$A_V = \frac{R4}{R1} \text{ for } R1 = R2$$

*CMRR is adjusted for max at expected CM input signal

$$R6 \approx \frac{R5}{5}, \text{ for } R5 = 100\ k\Omega$$

- Wide bandwidth
- 70 dB CMRR typ
- Wide CM input voltage range

Voltage Controlled Oscillator



TL/H/7788–32

$$f_o = \frac{V_{IN} - \phi}{4\,C\Delta V\,R1}$$

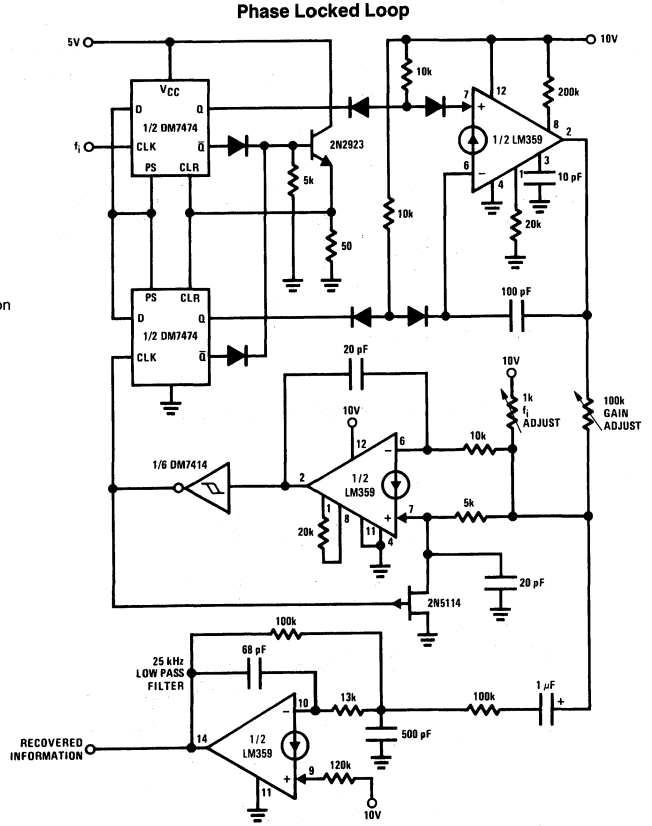
where: R2 = 2R1

ϕ = amplifier input voltage = 0.6V

ΔV = DM7414 hysteresis, typ 1V

- 5 MHz operation
- T^2L output

Phase Locked Loop



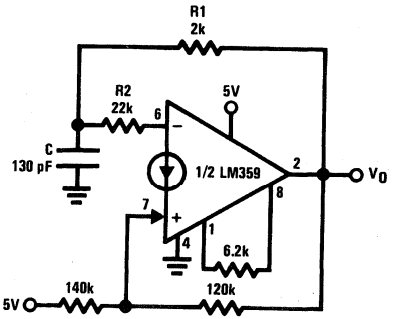
- Up to 5 MHz operation
- T^2L compatible input

All diodes = 1N914

TL/H/7788–33

Typical Applications (Continued)

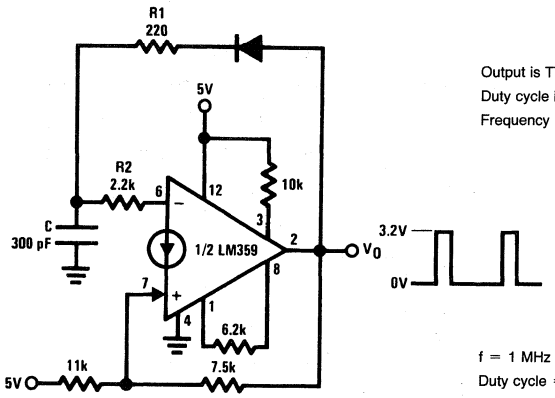
Squarewave Generator



TL/H/7788–34

f = 1 MHz
Output is TTL compatible
Frequency is adjusted by R1 & C (R1 ≪ R2)

Pulse Generator

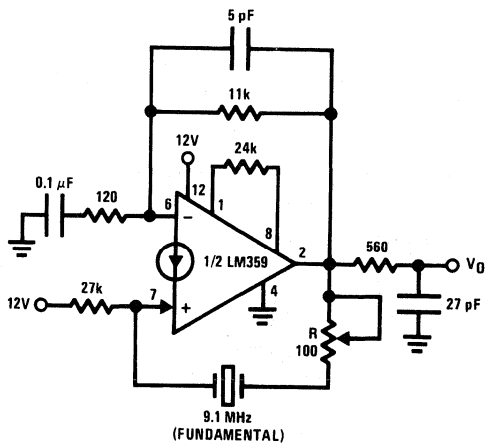


Output is TTL compatible
Duty cycle is adjusted by R1
Frequency is adjusted by C

f = 1 MHz
Duty cycle = 20%

TL/H/7788–36

Crystal Controlled Sinewave Oscillator

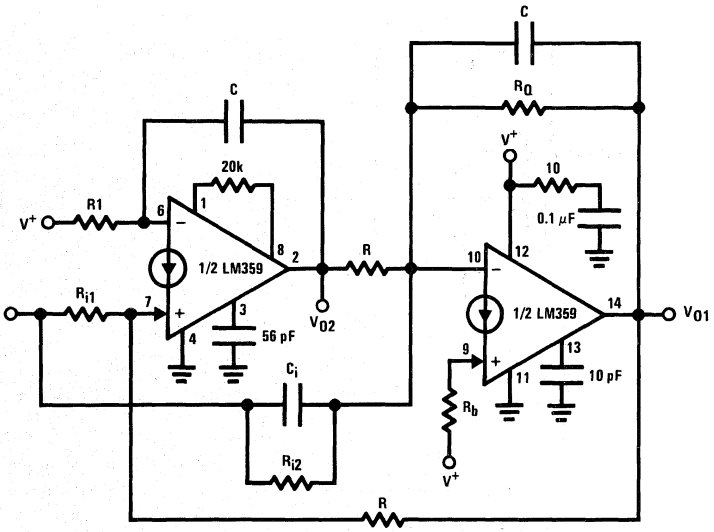


V_o = 500 mVp-p
f = 9.1 MHz
THD < 2.5%

TL/H/7788–37

Typical Applications (Continued)

High Performance 2 Amplifier Biquad Filter(s)



TL/H/7788–35

- The high speed of the LM359 allows the center frequency Q_o product of the filter to be: $f_o \times Q_o \leq 5$ MHz
- The above filter(s) maintains performance over wide temperature range
- One half of LM359 acts as a true non-inverting integrator so only 2 amplifiers (instead of 3 or 4) are needed for the biquad filter structure

DC Biasing Equations for $V_{O1(DC)} \cong V_{O2(DC)} \cong V^+/2$

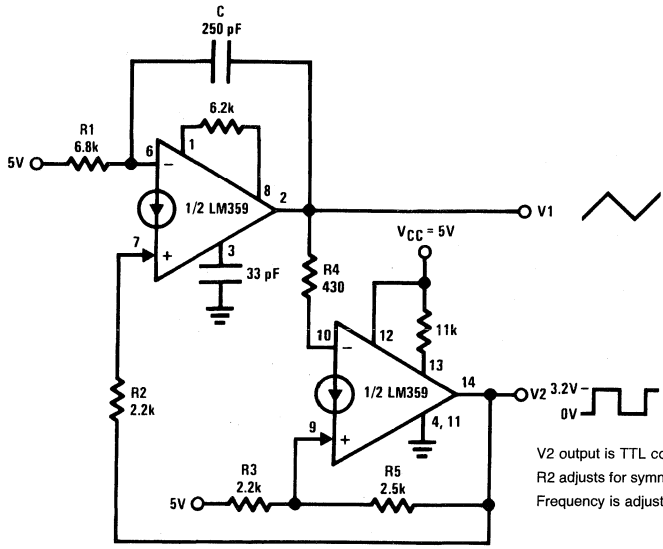
Type I	$\frac{2\,V_{IN(DC)}}{V^+\,(R_{i2})} + \frac{1}{R} + \frac{1}{R_Q} = \frac{2}{R_b}$; R1 = 2R
Type II	$\frac{1}{R} + \frac{1}{R_Q} = \frac{2}{R_b}$; R1 = 2R
Type III	$\frac{1}{R} + \frac{1}{R_Q} = \frac{2}{R_b}; \frac{1}{R1} = \frac{V_{IN(DC)}}{V^+\,(R_{i1})} + \frac{1}{2R}$

Analysis and Design Equations

Type	V_{O1}	V_{O2}	C_i	R_{i2}	R_{i1}	f_o	Q_o	$f_{Z(notch)}$	$H_{O(LP)}$	$H_{O(BP)}$	$H_{O(HP)}$	$H_{O(BR)}$
I	BP	LP	O	R_{i2}	∞	$\frac{1}{2}\pi RC$	R_Q/R	—	R/R_{i2}	R_Q/R_{i2}	—	—
II	HP	BP	C_i	∞	∞	$\frac{1}{2}\pi RC$	R_Q/R	—	—	R_QC_i/RC	C_i/C	—
III	Notch/ BR	—	C_i	∞	R_{i1}	$\frac{1}{2}\pi RC$	R_Q/R	$\frac{1}{2}\pi\sqrt{RR_iCC_i}$	—	—	—	$H_o\Big\vert_{f\to\infty} = C_i/C$ $H_o\Big\vert_{f\to 0} = C/R_i$

Typical Applications (Continued)

Triangle Waveform Generator



V2 output is TTL compatible
R2 adjusts for symmetry of the triangle waveform
Frequency is adjusted with R5 and C

TL/H/7788–38

National Semiconductor

LM392/LM2924
Low Power Operational Amplifier/Voltage Comparator

General Description

The LM392 series consists of 2 independent building block circuits. One is a high gain, internally frequency compensated operational amplifier, and the other is a precision voltage comparator. Both the operational amplifier and the voltage comparator have been specifically designed to operate from a single power supply over a wide range of voltages. Both circuits have input stages which will common-mode input down to ground when operating from a single power supply. Operation from split power supplies is also possible and the low power supply current is independent of the magnitude of the supply voltage.

Application areas include transducer amplifier with pulse shaper, DC gain block with level detector, VCO, as well as all conventional operational amplifier or voltage comparator circuits. Both circuits can be operated directly from the standard 5 V_{DC} power supply voltage used in digital systems, and the output of the comparator will interface directly with either TTL or CMOS logic. In addition, the low power drain makes the LM392 extremely useful in the design of portable equipment.

Advantages

- Eliminates need for dual power supplies
- An internally compensated op amp and a precision comparator in the same package
- Allows sensing at or near ground
- Power drain suitable for battery operation
- Pin-out is the same as both the LM358 dual op amp and the LM393 dual comparator

Features

- Wide power supply voltage range
  - Single supply 3V to 32V
  - Dual supply ±1.5V to ±16V
- Low supply current drain—essentially independent of supply voltage 600 μA
- Low input biasing current 50 nA
- Low input offset voltage 2 mV
- Low input offset current 5 nA
- Input common-mode voltage range includes ground
- Differential input voltage range equal to the power supply voltage

ADDITIONAL OP AMP FEATURES

- Internally frequency compensated for unity gain
- Large DC voltage gain 100 dB
- Wide bandwidth (unity gain) 1 MHz
- Large output voltage swing 0V to $V^+ - 1.5V$

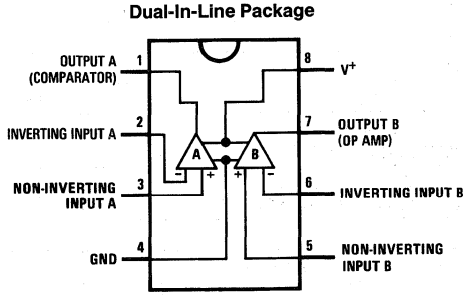
ADDITIONAL COMPARATOR FEATURES

- Low output saturation voltage 250 mV at 4 mA
- Output voltage compatible with all types of logic systems

Connection Diagram (Top View)

(Amplifier A = Comparator)
(Amplifier B = Operational Amplifier)

Dual-In-Line Package



TL/H/7793–1

Order Number LM392M or LM2924M
See NS Package Number M08A
Order Number LM392N or LM2924N
See NS Package Number N08E

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

	LM392	LM2924
Supply Voltage, V^+	32V or ±16V	26V or ±13V
Differential Input Voltage	32V	26V
Input Voltage	−0.3V to +32V	−0.3V to +26V
Power Dissipation (Note 1)		
Molded DIP (LM392N, LM2924N)	820 mW	820 mW
Small Outline Package (LM392M, LM2924M)	530 mW	530 mW
Output Short-Circuit to Ground (Note 2)	Continuous	Continuous
Input Current ($V_{IN} < -0.3\ V_{DC}$) (Note 3)	50 mA	50 mA
Operating Temperature Range	0°C to +70°C	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	260°C	260°C
ESD rating to be determined.		
Soldering Information		
Dual-in-Line Package		
Soldering (10 seconds)	260°C	260°C
Small Outline Package		
Vapor Phase (60 seconds)	215°C	215°C
Infrared (15 seconds)	220°C	220°C

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

Electrical Characteristics ($V^+ = 5\ V_{DC}$; specifications apply to both amplifiers unless otherwise stated) (Note 4)

Parameter	Conditions	LM392			LM2924			Units
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	$T_A = 25°C$, (Note 5)		±2	±5		±2	±7	mV
Input Bias Current	IN(+) or IN(−), $T_A = 25°C$, (Note 6), $V_{CM} = 0V$		50	250		50	250	nA
Input Offset Current	IN(+) − IN(−), $T_A = 25°C$		±5	±50		±5	±50	nA
Input Common-Mode Voltage Range	$V^+ = 30\ V_{DC}$, $T_A = 25°C$, (Note 7) (LM2924, $V^+ = 26\ V_{DC}$)	0		$V^+ - 1.5$	0		$V^+ - 1.5$	V
Supply Current	$R_L = \infty$, $V^+ = 30V$, (LM2924, $V^+ = 26V$)		1	2		1	2	mA
Supply Current	$R_L = \infty$, $V^+ = 5V$		0.5	1		0.5	1	mA
Amplifier-to-Amplifier Coupling	f = 1 kHz to 20 kHz, $T_A = 25°C$, Input Referred, (Note 8)		−100			−100		dB
Input Offset Voltage	(Note 5)			±7			±10	mV
Input Bias Current	IN(+) or IN(−)			400			500	nA
Input Offset Current	IN(+) − IN(−)			150			200	nA
Input Common-Mode Voltage Range	$V^+ = 30\ V_{DC}$, (Note 7) (LM2924, $V^+ = 26\ V_{DC}$)	0		$V^+ - 2$	0		$V^+ - 2$	V
Differential Input Voltage	Keep All V_{IN}'s ≥ 0 V_{DC} (or V^-, if Used), (Note 9)			32			26	V
OP AMP ONLY								
Large Signal Voltage Gain	$V^+ = 15\ V_{DC}$, V_o swing = 1 V_{DC} to 11 V_{DC}, $R_L = 2\ k\Omega$, $T_A = 25°C$	25	100		25	100		V/mV

Electrical Characteristics ($V^+ = 5\ V_{DC}$; specifications apply to both amplifiers unless otherwise stated)

(Note 4) (Continued)

Parameter	Conditions	LM392			LM2924			Units
		Min	Typ	Max	Min	Typ	Max	
OP AMP ONLY								
Output Voltage Swing	$R_L = 2\ k\Omega$, $T_A = 25°C$, (LM2924, $R_L \geq 10\ k\Omega$)	0		$V^+ - 1.5$	0		$V^+ - 1.5$	V
Common-Mode Rejection Ratio	DC, $T_A = 25°C$, $V_{CM} = 0\ V_{DC}$ to $V^+ - 1.5\ V_{DC}$	65	70		50	70		dB
Power Supply Rejection Ratio	DC, $T_A = 25°C$	65	100		50	100		dB
Output Current Source	$V_{IN(+)} = 1\ V_{DC}$, $V_{IN(-)} = 0\ V_{DC}$, $V^+ = 15\ V_{DC}$, $V_o = 2\ V_{DC}$, $T_A = 25°C$	20	40		20	40		mA
Output Current Sink	$V_{IN(-)} = 1\ V_{DC}$, $V_{IN(+)} = 0\ V_{DC}$, $V^+ = 15\ V_{DC}$, $V_o = 2\ V_{DC}$, $T_A = 25°C$	10	20		10	20		mA
	$V_{IN(-)} = 1\ V_{DC}$, $V_{IN(+)} = 0\ V_{DC}$, $V^+ = 15\ V_{DC}$, $V_o = 200\ mV$, $T_A = 25°C$	12	50		12	50		μA
Input Offset Voltage Drift	$R_S = 0\Omega$		7			7		μV/°C
Input Offset Current Drift	$R_S = 0\Omega$		10			10		pA_{DC}/°C
COMPARATOR ONLY								
Voltage Gain	$R_L \geq 15\ k\Omega$, $V^+ = 15\ V_{DC}$, $T_A = 25°C$	50	200		25	100		V/mV
Large Signal Response Time	V_{IN} = TTL Logic Swing, $V_{REF} = 1.4\ V_{DC}$ $V_{RL} = 5\ V_{DC}$, $R_L = 5.1\ k\Omega$, $T_A = 25°C$		300			300		ns
Response Time	$V_{RL} = 5\ V_{DC}$, $R_L = 5.1\ k\Omega$, $T_A = 25°C$, (Note 10)		1.3			1.5		μs
Output Sink Current	$V_{IN(-)} = 1\ V_{DC}$, $V_{IN(+)} = 0\ V_{DC}$, $V_o \geq 1.5\ V_{DC}$, $T_A = 25°C$	6	16		6	16		mA
Saturation Voltage	$V_{IN(-)} \geq 1\ V_{DC}$, $V_{IN(+)} = 0$, $I_{SINK} \leq 4\ mA$, $T_A = 25°C$		250	400			400	mV
	$V_{IN(-)} \geq 1\ V_{DC}$, $V_{IN(+)} = 0$, $I_{SINK} \leq 4\ mA$			700			700	mV
Output Leakage Current	$V_{IN(-)} = 0$, $V_{IN(+)} \geq 1\ V_{DC}$, $V_o = 5\ V_{DC}$, $T_A = 25°C$		0.1			0.1		nA
	$V_{IN(-)} = 0$, $V_{IN(+)} \geq 1\ V_{DC}$, $V_o = 30\ V_{DC}$			1.0			1.0	μA

Note 1: For operating at temperatures above 25°C, the LM392 and the LM2924 must be derated based on a 125°C maximum junction temperature and a thermal resistance of 122°C/W which applies for the device soldered in a printed circuit board, operating in still air ambient. The dissipation is the total of both amplifiers—use external resistors, where possible, to allow the amplifier to saturate or to reduce the power which is dissipated in the integrated circuit.

Note 2: Short circuits from the output to V^+ can cause excessive heating and eventual destruction. When considering short circuits to ground, the maximum output current is approximately 40 mA for the op amp and 30 mA for the comparator independent of the magnitude of V^+. At values of supply voltage in excess of 15V, continuous short circuits can exceed the power dissipation ratings and cause eventual destruction.

Note 3: This input current will only exist when the voltage at any of the input leads is driven negative. It is due to the collector-base junction of the input PNP transistors becoming forward biased and thereby acting as input diode clamps. In addition to this diode action, there is also lateral NPN parasitic transistor action on the IC chip. This transistor action can cause the output voltages of the amplifiers to go to the V^+ voltage level (or to ground for a large overdrive) for the time duration that an input is driven negative. This is not destructive and normal output states will re-establish when the input voltage, which was negative, again returns to a value greater than −0.3V (at 25°C).

Note 4: These specifications apply for $V^+ = 5V$, unless otherwise stated. For the LM392, temperature specifications are limited to $0°C \leq T_A \leq +70°C$ and the LM2924 temperature specifications are limited to $-40°C \leq T_A \leq +85°C$.

Note 5: At output switch point, $V_O \cong 1.4V$, $R_S = 0\Omega$ with V^+ from 5V to 30V; and over the full input common-mode range (0V to $V^+ - 1.5V$).

Note 6: The direction of the input current is out of the IC due to the PNP input stage. This current is essentially constant, independent of the state of the output so no loading change exists on the input lines.

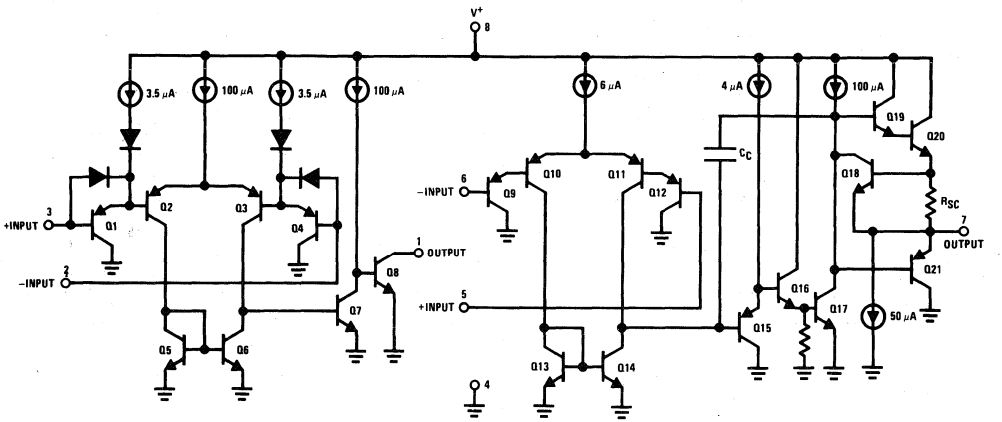
Note 7: The input common-mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3V. The upper end of the common-mode voltage range is $V^+ - 1.5V$, but either or both inputs can go to 32V without damage (26V for LM2924).

Note 8: Due to proximity of external components, insure that coupling is not originating via the stray capacitance between these external parts. This typically can be detected as this type of capacitive increases at higher frequencies.

Note 9: Positive excursions of input voltage may exceed the power supply level. As long as the other input voltage remains within the common-mode range, the comparator will provide a proper output state. The input voltage to the op amp should not exceed the power supply level. The input voltage state must not be less than $-0.3V$ (or 0.3V below the magnitude of the negative power supply, if used) on either amplifier.

Note 10: The response time specified is for a 100 mV input step with 5 mV overdrive. For larger overdrive signals 300 ns can be obtained.

Schematic Diagram



Comparator A **Amplifier B**

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Application Hints

Please refer to the application hints section of the LM193 and the LM158 datasheets.

National Semiconductor

LM604 4 Channel Mux-Amp

General Description

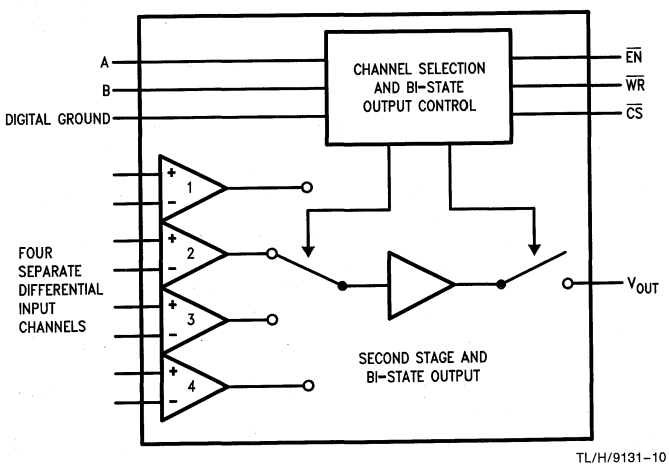
The LM604 Mux-Amp is an op-amp with four selectable differential inputs, combining the functions of a multiplexer with an op-amp. The LM604 can select, buffer, and amplify one of four different input signals, providing a complete system for multiplexing analog signals. It also has the unique Bi-State output which allows two or more Mux-Amps to be connected together at their outputs to increase the number of multiplexed channels. Channel selection and the Bi-State output are controlled by internal logic that interfaces directly to a microprocessor. Besides these unique features, the LM604 has excellent AC and DC op-amp specifications and is internally compensated.

Applications include signal multiplexing and linear circuits that are controlled by digital signals (i.e., programmable gain blocks, filters, and other op-amp circuits).

Features

- Multiplexes four differential input channels to a single op-amp
- Easy to interface to microprocessor, or operates "stand alone"
- Bi-State output: Operates in two states, Active and Disabled. When disabled, it becomes a high impedance.
- Wide operating voltage range
  - single supply: 4V to 32V
  - split supply: ±2V to ±16V
- Wide input common mode range: V^- to $V^+ - 1V$
- Fast channel to channel switching time: 5 μs
- Output will drive a 600Ω load

Block Diagram



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Channel Selection

A	B	$\overline{WR}$	$\overline{CS}$	Channel
0	0	0	0	1
0	1	0	0	2
1	0	0	0	3
1	1	0	0	4
X	X	X	1	Unchanged
X	X	1	X	Unchanged

Bi-State Output Control

$\overline{EN}$	$\overline{WR}$	$\overline{CS}$	Output State
0	0	0	Enabled
1	0	0	Disabled, High Z
X	X	1	Unchanged
X	1	X	Unchanged

Order Number LM604AMJ, LM604IJ, LM604IN, LM604ACN, LM604CN, LM604ACM, or LM604CM
See NS Package Number J18A, N18A or M20B

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	36V or ±18V
Differential Input Voltage	±Supply Voltage
Input Voltage Range	±Supply Voltage
Output Short Circuit to Gnd	Continuous (Note 1)
ESD Tolerance (C_{ZAP} = 120 pF, R_{ZAP} = 1500Ω)	2,000V
Lead Temperature (Soldering, 5 sec.)	300°C
Storage Temperature Range	−65°C to 150°C

Operating Ambient Temperature Range	
LM604AM	$-55°C \le T_A \le 125°C$
LM604I	$-40°C \le T_A \le 85°C$
LM604AC, LM604C	$0°C \le T_A \le 70°C$

	J Pkg.	M Pkg.	N Pkg.
Power Dissipation (Note 2)	1,600 mW	1,500 mW	1,900 mW
T_{JMAX}	150°C	150°C	150°C
θ_{JA} (Typical, Board Mounted)	75°C/W	83°C/W	65°C/W

DC Electrical Characteristics V_{SUPPLY} = ±15V (Note 3)

Parameter	Conditions		Typical	LM604AM		LM604I		LM604AC LM604C		Units (Limit)
				Tested Limit (Note 4)	Design Limit (Note 5)	Tested Limit (Note 4)	Design Limit (Note 5)	Tested Limit (Note 4)	Design Limit (Note 5)	
Input Offset Voltage (V_{OS})	R_S = 10 kΩ	LM604	1.0			3.0	**5.0**	3.0	**5.0**	mV
		LM604A	0.5	1.0				1.0	**3.0**	(Max)
				3.0						
V_{OS} Temperature Drift			5.5							µV/°C
Input Offset Current (I_{OS})			2	10		10	**12**	10	**12**	nA
				12						(Max)
I_{OS} Temperature Drift			10							pA/°C
Input Bias Current (I_B)		LM604	50			80	**100**	80	**100**	nA
		LM604A	30	50				50	**60**	(Max)
				60						
I_B Temperature Drift			55							pA/°C
Input Common Mode Voltage Range		Upper Limit	14.0	13.5		13.5	**13.0**	13.5	**13.0**	V
				13.0						(Min)
		Lower Limit	−15.0	−15.0		−15.0	**−15.0**	−15.0	**−15.0**	V
				−15.0						(Max)
Input Resistance			1.0							Meg Ω
Output Voltage Swing	R_L = 10 kΩ	Upper Limit	13.4	13.0		13.0	**12.5**	13.0	**12.5**	V
				12.5						(Min)
		Lower Limit	−14.2	−13.8		−13.8	**−13.3**	−13.8	**−13.3**	V
				−13.3						(Max)
	R_L = 600Ω	Upper Limit	12.7	12.3		12.3	**10.0**	12.3	**10.0**	V
				10.0						(Min)
		Lower Limit	−12.6	−12.2		−12.2	**−11.7**	−12.2	**−11.7**	V
				−11.7						(Max)
Large Signal Voltage Gain	V_{OUT} = ±10V	R_L = 2 kΩ	200	50		50	**25**	50	**25**	V/mV
				25						(Min)
		R_L = 600Ω	200	50		50	**25**	50	**25**	
				25						
Common Mode Rejection Ratio	V_{CM} = −15.0V to 13.5V		100	80		80	**70**	80	**70**	dB
				70						(Min)

DC Electrical Characteristics $V_{SUPPLY} = \pm 15V$ (Note 3)

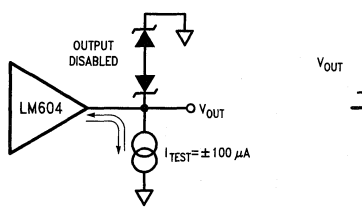
Parameter	Conditions	Typical	LM604AM		LM604I		LM604AC LM604C		Units (Limit)
			Tested Limit (Note 4)	Design Limit (Note 5)	Tested Limit (Note 4)	Design Limit (Note 5)	Tested Limit (Note 4)	Design Limit (Note 5)	
Power Supply Rejection Ratio	$V_{SUPPLY} = \pm 5.0V$ to $\pm 16.0V$	100	80 **70**		80	**70**	80	**70**	dB (Min)
Output Short Circuit Current		±35	±50 **±60**		±50	**±60**	±50	**±60**	mA (Max)
Output Leakage Current	$V_{OUT} = -13.5V$ to 13.0V Bi-State Output Disabled	4.0	10.0 **20.0**		10.0	**20.0**	10.0	**20.0**	µA (Max)
Output Capacitance	Bi-State Output Disabled See *Figure 1*	10							pF
Supply Current		7.0	9.0 **10.0**		9.0	**10.0**	9.0	**10.0**	mA (Max)

AC Electrical Characteristics $V_{SUPPLY} = \pm 15V$ (Note 3)

Parameter	Conditions	Typical	LM604AM		LM604I		LM604AC LM604C		Units (Limit)
			Tested Limit (Note 4)	Design Limit (Note 5)	Tested Limit (Note 4)	Design Limit (Note 5)	Tested Limit (Note 4)	Design Limit (Note 5)	
Slew Rate	$A_V = 1, R_L = 2 k\Omega$	3.0	2.0 **1.5**		2.0	**1.5**	2.0	**1.5**	V/µs (Min)
Gain Bandwidth Product	f = 100 kHz	7.0	6.0 **3.0**		6.0	**3.0**	6.0	**3.0**	MHz (Min)
Unity Gain Frequency		3.0		2.5		2.5		2.5	MHz (Min)
Phase Margin	$R_L = 2 k\Omega, C_L = 200$ pF	50							Degrees
Settling Time to 0.1% of Final Value	$A_V = -1, V_{OUT} = -5.0V$ to 5.0V $R_L = 2 k\Omega$	4.0							µs
Channel Switching Time	See *Figure 2* t_{SW1}	4.0	5.5 **6.5**		5.5	**6.5**	5.5	**6.5**	µs (Max)
	t_{SW2}	5.0		6.5		6.5		6.5	
Channel to Channel Isolation	$R_S = 10 k\Omega$, f = 10 kHz $V_{IN} = 10.0V_{p-p}$	100							dB
Input Noise Voltage	$R_S = 100 \Omega$, f = 1 kHz	20							nV/√Hz
Input Noise Current	f = 1 kHz	0.3							pA/√Hz
Mux-Amp Enable Time	See *Figure 3* t_{EN1}	3.0	4.0 **5.0**		4.0	**5.0**	4.0	**5.0**	µs (Max)
	t_{EN2}	4.0		5.5		5.5		5.5	
Mux-Amp Disable Time (t_{DIS})	See *Figure 3*	1.0	2.0 **3.0**		2.0	**3.0**	2.0	**3.0**	µs (Max)

DC Electrical Characteristics V_{SUPPLY} = 5V (Note 3)

Parameter	Conditions		Typical	LM604AM		LM604I		LM604AC LM604C		Units (Limit)
				Tested Limit (Note 4)	Design Limit (Note 5)	Tested Limit (Note 4)	Design Limit (Note 5)	Tested Limit (Note 4)	Design Limit (Note 5)	
Input Offset Voltage	R_S = 10 kΩ V_{OUT} = 2.0V	LM604 LM604A	1.0 0.5	 1.0 **3.0**		3.0	**5.0**	3.0 1.0	**5.0** **3.0**	mV (Max)
Input Offset Current	V_{OUT} = 2.0V		3.0	10 **18**		10	**18**	10	**18**	nA (Max)
Input Bias Current	V_{OUT} = 2.0V	LM604 LM604A	70 50	 80 **110**		130	**150**	130 80	**150** **110**	nA (Max)
Input Common Mode Voltage Range	V_{OUT} = 2.0V	Upper Limit	4.0	3.5 **3.0**		3.5	**3.0**	3.5	**3.0**	V (Min)
		Lower Limit	0	0 **0**		0	**0**	0	**0**	
Output Voltage Swing	R_L = 10 kΩ	Upper Limit	3.5	3.2 **3.0**		3.2	**3.0**	3.2	**3.0**	V (Min)
		Lower Limit	0.5	0.7 **0.8**		0.7	**0.8**	0.7	**0.8**	V (Max)
	R_L = 600Ω	Upper Limit	3.3	3.0 **2.8**		3.0	**2.8**	3.0	**2.8**	V (Min)
		Lower Limit	0.4	0.6 **0.7**		0.6	**0.7**	0.6	**0.7**	V (Max)
Large Signal Voltage Gain	V_{OUT} = 0.8V to 2.8V	R_L = 2 kΩ	200		50 **25**		50 **25**		50 **25**	V/mV (Min)
		R_L 600Ω	200		50 **25**		50 **25**		50 **25**	
Common Mode Rejection Ratio	V_{CM} = 0V to 3.5V V_{OUT} = 2.0V		100	80 **70**		80	**70**	80	**70**	dB (Min)
Power Supply Rejection Ratio	V^+ = 4.0V to 5.0V V_{OUT} = 2.0V		100	80 **70**		80	**70**	80	**70**	dB (Min)



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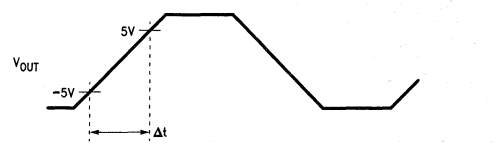

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$$C_{OUT} = \frac{\Delta t}{10V} \times 100\ \mu A$$

FIGURE 1. Output Capacitance Test

Digital Input Electrical Characteristics $V_{SUPPLY} = \pm 15V$ (Note 6)

Parameter	Conditions	Typical	LM604AM		LM604I		LM604AC LM604C		Units (Limit)
			Tested Limit (Note 4)	Design Limit (Note 5)	Tested Limit (Note 4)	Design Limit (Note 5)	Tested Limit (Note 4)	Design Limit (Note 5)	
V_{INHI}			1.8 **2.0**		1.8	**2.0**	1.8	**2.0**	V (Min)
V_{INLO}			1.0 **0.8**		1.0	**0.8**	1.0	**0.8**	V (Max)
I_{INHI}			5.0 **10.0**		5.0	**10.0**	5.0	**10.0**	μA (Max)
I_{INLO}			5.0 **10.0**		5.0	**10.0**	5.0	**10.0**	μA (Max)
Minimum Pulse Width for WR & CS				**100**		**100**		**100**	ns (Min)
Minimum Set-Up Time (t_S)	See *Figures 3* and *5*			**100**		**100**		**100**	ns (Min)
Minimum Hold Time (t_H)	See *Figures 3* and *5*			**50**		**50**		**50**	ns (Min)
Input Capacitance		5							pF

Note 1: Applies to both single and split supply operation. Continuous short circuit operation can result in exceeding the maximum allowed junction temperature.

Note 2: When operating at $T_A > 25°C$, the maximum power dissipation must be derated based on θ_{JA}.

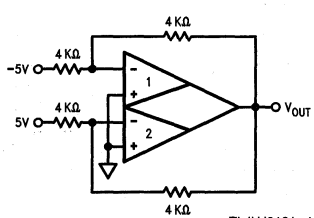
Note 3: Unless specified otherwise, all limits are guaranteed for $T_A = T_J = 25°C$, $V_{CM} = 0V$, $V_{OUT} = 0V$, and $R_L > 1Meg\Omega$. **Boldface** limits apply at $0°C \leq T_J \leq 70°C$ for LM604AC and LM604C, $-40°C \leq T_J \leq 85°C$ for LM604I, and $-55°C \leq T_J$ 125°C for LM604AM.

Note 4: Guaranteed and 100% production tested.

Note 5: Guaranteed but not 100% production tested. These numbers are not used to calculate outgoing quality levels.

Note 6: Unless specified otherwise, all units are guaranteed at $T_A = T_J = 25°C$. **Boldface** limits apply at the junction temperature extremes specified in note 3. Input voltage levels are with respect to digital ground (pin 4) which must be at least 4.0V below V^+.

Switching from Channel 1 to 2 with Channel Select preset to $\overline{AB}$ before $\overline{WR}$ = 0. This test applies to all channels.



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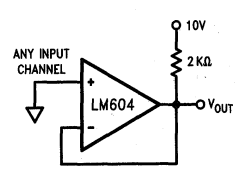

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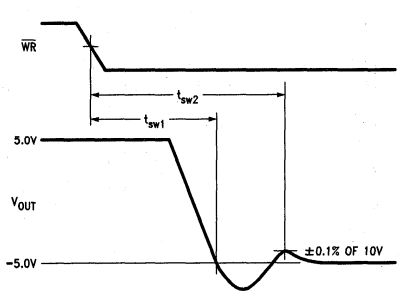

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FIGURE 2. Channel Switching Time Test

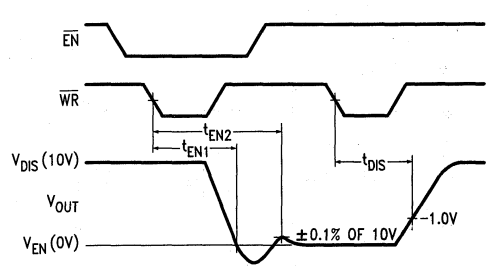

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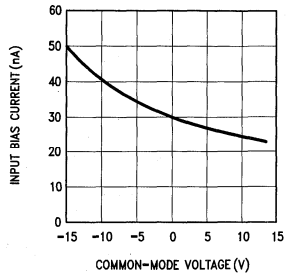
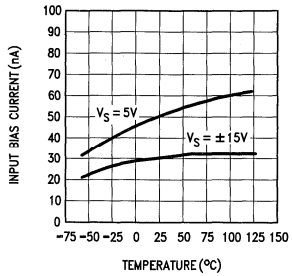
FIGURE 3. Bi-State Output Enable and Disable Time Test

Typical Performance Characteristics (Note 7)

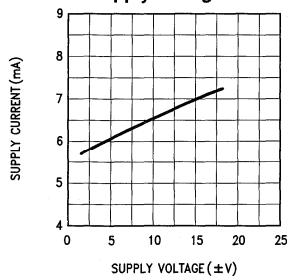
Input Bias Current vs Input Common-Mode Voltage



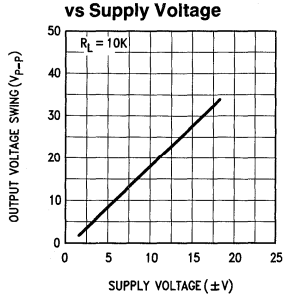
Input Bias Current vs Temperature



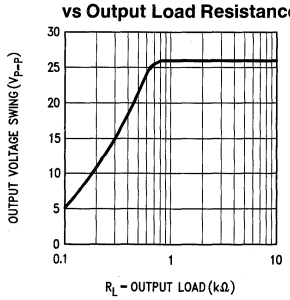
Supply Current vs Supply Voltage



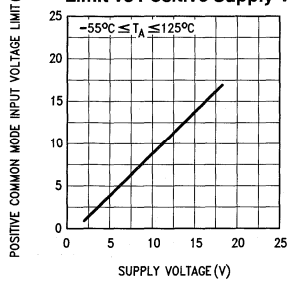
Output Voltage Swing vs Supply Voltage



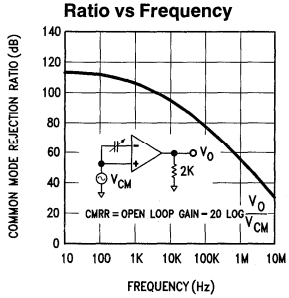
Output Voltage Swing vs Output Load Resistance



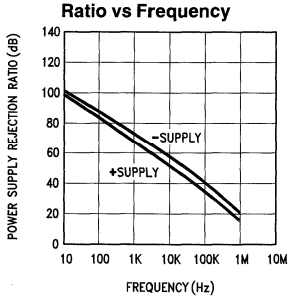
Upper Common-Mode Voltage Limit vs Positive Supply Voltage



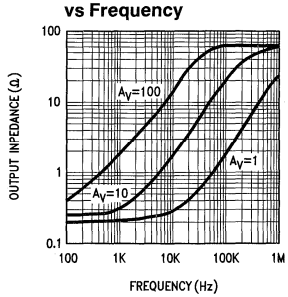
Common-Mode Rejection Ratio vs Frequency



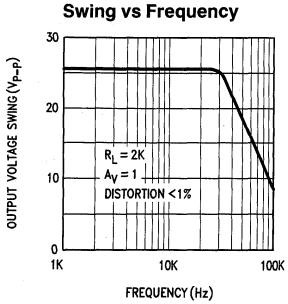
Power Supply Rejection Ratio vs Frequency



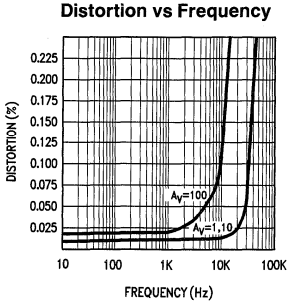
Output Impedance vs Frequency



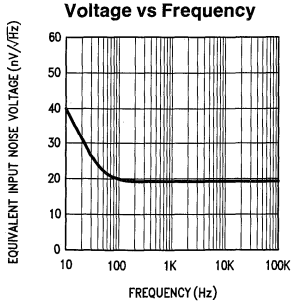
Undistorted Output Voltage Swing vs Frequency



Distortion vs Frequency



Equivalent Input Noise Voltage vs Frequency



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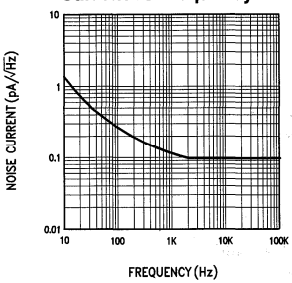
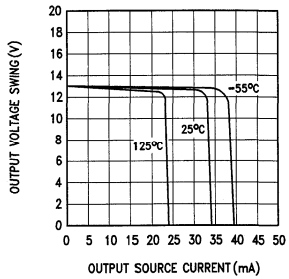
Typical Performance Characteristics (Note 7)

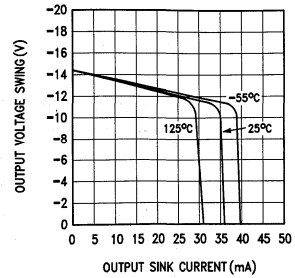
Equivalent Input Noise Current vs Frequency



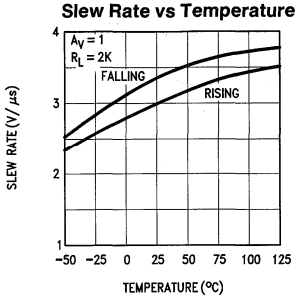
Positive Current Limit



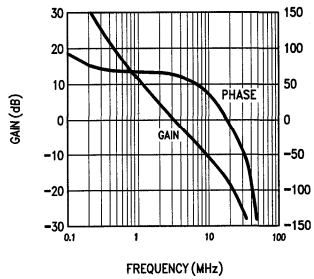
Negative Current Limit



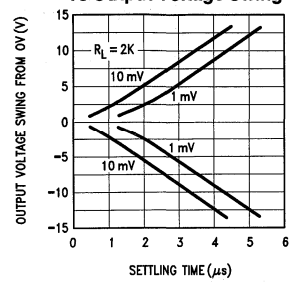
Slew Rate vs Temperature



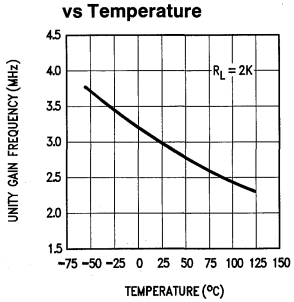
Bode Plot



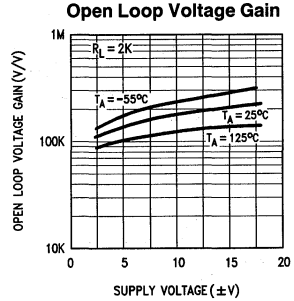
Inverter Settling Time vs Output Voltage Swing



Unity Gain Frequency vs Temperature



Open Loop Voltage Gain



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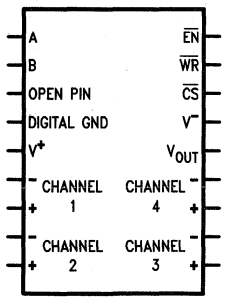
Note 7: Unless specified otherwise, $T_A = T_J = 25°C$, $V_S = \pm 15V$, $V_{CM} = 0V$, $V_{OUT} = 0V$, and $R_L > 1$ Meg.

Connection Diagrams

18 Pin Dual-In-Line Package



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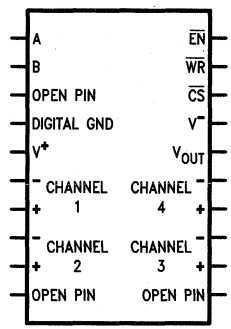
20 Pin Small Outline Package



TL/H/9131–26

FIGURE 4

Timing Diagrams

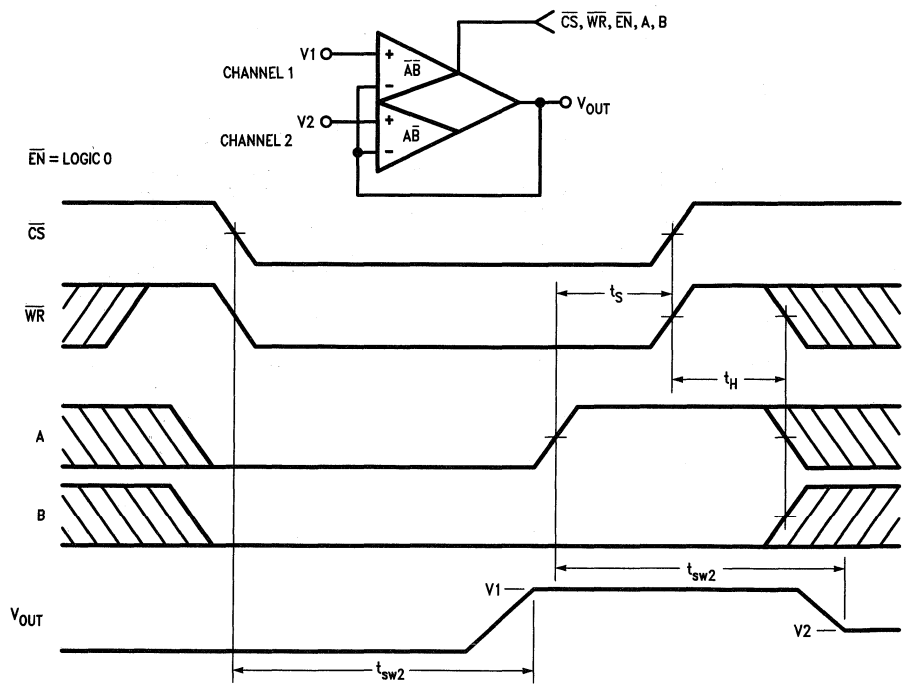


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FIGURE 5. Channel Switching Timing Diagram

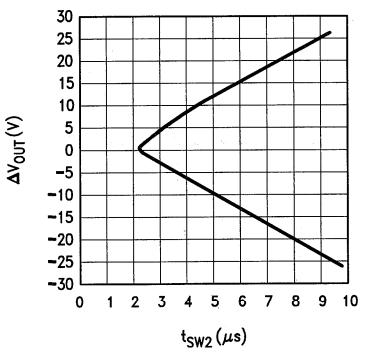
Functional Description

INPUT CHANNEL SELECTION

The LM604 contains four differential input channels that are selected one at a time. An input is selected by writing its binary code to pins A and B when $\overline{CS}$ and $\overline{WR}$ are a logic 0, see block diagram. The LM604 always has one of its inputs selected. In order to isolate all four channels from the output, the Bi-State output can be disabled.

Figure 5 illustrates how the LM604 switches from one channel to another. The switching begins on the falling edge of $\overline{WR}$ if A and B are valid before $\overline{WR}$ is a logic 0, or when A and B become valid while $\overline{WR}$ is a logic 0. In either case, the channel switching time (t_{SW2}) remains the same. If a channel is to remain selected, its binary code must be valid during the rising edge of $\overline{WR}$ as specified by t_S and t_H.

Channel switching time is specified by t_{SW1} and t_{SW2} as shown in *Figure 2*. t_{SW1} is the time it takes the output to first reach its new value, and t_{SW2} is the time it takes the output to settle to within 0.1% of its new value. Clearly, t_{SW2} is a more useful parameter for specifying switching time, but it is difficult to test on a production basis. Therefore, t_{SW1} is tested and this allows t_{SW2} to be guaranteed. Channel switching time will vary as a function of how far the output swings to reach its new value. This is shown in *Figure 6* where t_{SW2} is plotted as a function of output voltage swing (ΔV_{OUT}).



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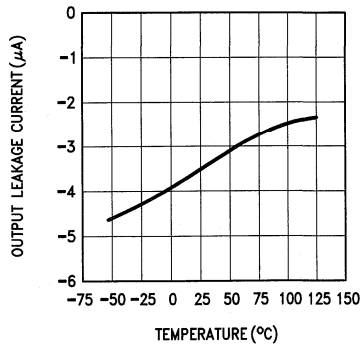
ΔV_{OUT} = V_{OUT} (Selected Channel) − V_{OUT} (Previous Channel)

FIGURE 6. t_{SW2} vs ΔV_{OUT}

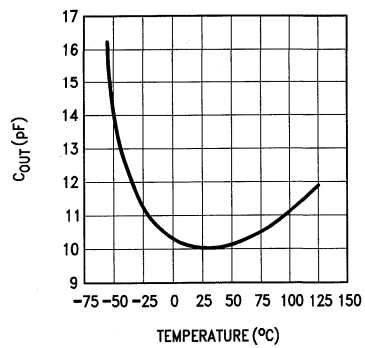
BI-STATE OUTPUT

The Bi-State output can be either enabled (on) or disabled (off). When disabled, the output becomes a high impedance load that can be driven by another output stage. This allows several Mux-Amps to be connected together at their outputs by having only one output enabled at one time. Thus, several Mux-Amps can be in parallel to the same output to increase the number of multiplexed channels. The Bi-State output is controlled by $\overline{EN}$ when $\overline{CS}$ and $\overline{WR}$ are a logic 0, see block diagram.

When the output is disabled and driven by another output, it behaves like a small capacitive load with a few microamps of leakage current. The data sheet specifies this with the parameters "Output Capacitance" and "Output Leakage Current". Both parameters vary with temperature, as shown in *Figure 7*.



TL/H/9131–13



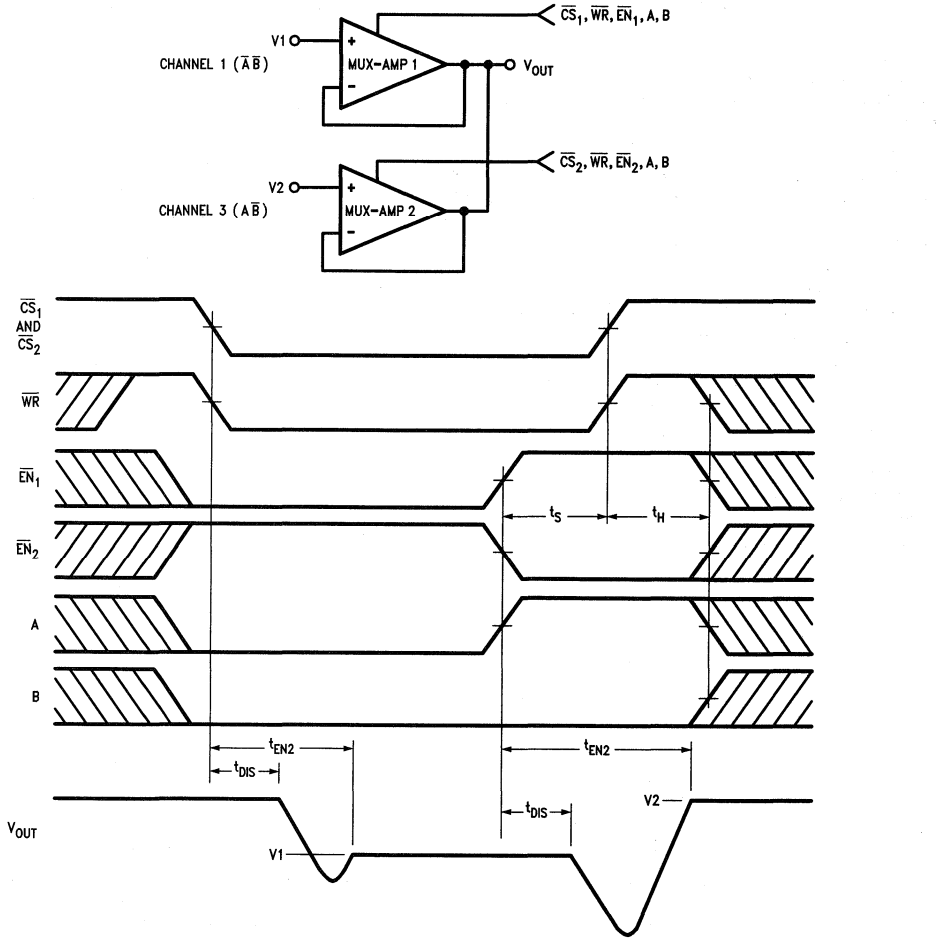
TL/H/9131–14

FIGURE 7. $I_{LEAKAGE}$ and C_{OUT} vs Temperature

Figure 8 illustrates switching between two Mux-Amps that are connected in parallel to the same output. Switching begins on the falling edge of $\overline{WR}$ if the $\overline{EN}$ signals are correctly set before $\overline{WR}$ is a logic 0, or when the $\overline{EN}$ signals become valid while $\overline{WR}$ is a logic 0. The Bi-State output takes less time to become disabled than it does to become enabled, and this insures the outputs are switched in a "break before make" method. If an in output is to remain enabled or disabled after $\overline{WR}$ becomes a logic 1, $\overline{EN}$ must be valid during the rising edge of $\overline{WR}$ as specified by t_S and t_H. Note that when a Mux-Amp has its output enabled, the binary code for the selected input channel must also be written.

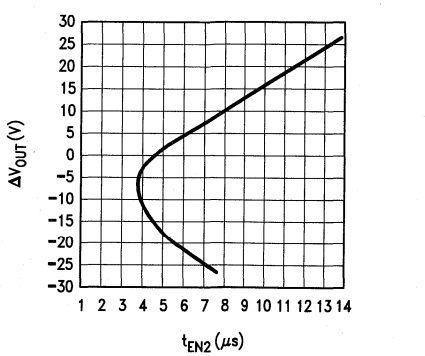
Bi-State output enable time (t_{EN1} and t_{EN2}) and disable time (t_{DIS}) are defined in *Figure 3*. t_{EN1} is the time it takes the output to first reach its enabled value (V_{EN}), and t_{EN2} is the time it takes the output to settle to within 0.1% of V_{EN}. As with channel switching time, t_{EN1} is a tested parameter that allows t_{EN2} to be guaranteed. t_{DIS} is the time it takes the output to become a high impedance. Output enable time will vary according to how far the output swings from V_{DIS} to V_{EN}, and this is plotted in *Figure 9*.

Functional Description (Continued)



TL/H/9131–15

FIGURE 8. Timing Diagram for Switching Bi-State Outputs



TL/H/9131–16

$\Delta V_{OUT} = V_{EN} - V_{DIS}$

FIGURE 9. t_{EN2} vs ΔV_{OUT}

DIGITAL CONTROL

As mentioned in the previous sections, the input channels and Bi-State output are controlled by logic levels on pins A, B, and $\overline{EN}$. There are two ways to apply logic levels to these pins. 1) Hardwire $\overline{WR}$ and $\overline{CS}$ directly to digital ground so that the LM604 operates in a "stand alone" mode. This allows input logic levels to directly control the LM604. 2) Write digital signals to A, B, and $\overline{EN}$ as shown in the timing diagrams of *Figures 5* and *8*. This method is used when the LM604 interfaces to a microprocessor. Note that $\overline{CS}$ and $\overline{WR}$ can occur simultaneously, so set-up and hold times are not required for $\overline{CS}$. Also, notice that $\overline{WR}$ must remain a logic 1 during the hold time period.

Input logic levels are referenced to a 1.4V threshold voltage, making the LM604 compatible with TTL and CMOS logic. This threshold voltage is referenced to digital ground. The voltage level of digital ground can be as low as V^- (pin 15) and as high as 4V below V^+ (pin 5).

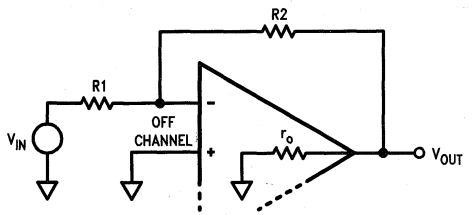
Application Hints

USING MULTIPLE FEEDBACK LOOPS

Each input channel of the LM604 is used as a single op-amp with its own feedback loop. Two examples of this are circuits with multiple inverting gain channels and non-inverting gain channels (*Figure 10*). These circuits have multiple feedback loops connected to the same output with one feedback loop connected to a selected channel and the others connected to "off" channels. The feedback loop of the selected channel determines the gain of these circuits. The off channel feedback loops affect these circuits in two ways. 1) They create an additional load at the output. 2) Feedback loops for inverting gain channels provide feedthrough paths from the inputs of the off channels to the output.

In *Figure 10*, the loading affect of multiple feedback loops is given in terms of current flowing through the feedback loops (I_F). In circuits with non-inverting gain channels, I_F is a function of V_{OUT} and the resistance of the feedback loops. In circuits with inverting gain channels, I_F is different for each channel selected because it is also a function of the off channel input voltages. This additional loading must be accounted for when designing Mux-Amp circuits. Otherwise, the output load resistance will be less than anticipated.

Figure 11 illustrates feedthrough in an off inverting gain channel. Feedthrough occurs because the feedback resistors and the Mux-Amp output impedance (r_o) form a voltage divider. This divider allows a portion of the off channel's input signal to appear at the output. The amount of signal that feeds through depends on the ratio of output impedance to feedback loop resistance. Output impedance varies according to Mux-Amp gain (gain of the selected channel) and the frequency of the feedthrough signal. This variation must be considered when calculating feedthrough, and it is plotted in the "Typical Device Characteristics" section.



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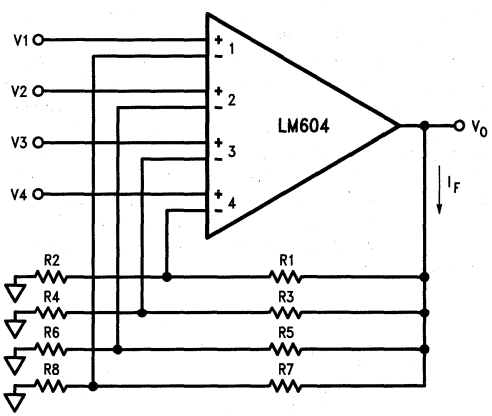
$$V_{OUT} = V_{IN}\left(\frac{r_o}{R1 + R2 + r_o}\right)$$

FIGURE 11. Inverting Gain Channel Feedthrough



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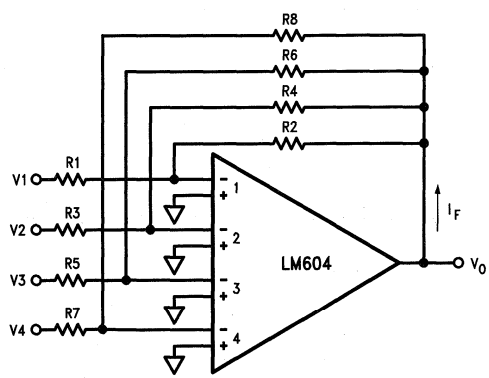
Channel	V_o
1	$V1\left(1 + \frac{R7}{R8}\right)$
2	$V2\left(1 + \frac{R5}{R6}\right)$
3	$V3\left(1 + \frac{R3}{R4}\right)$
4	$V4\left(1 + \frac{R1}{R2}\right)$

$$I_F = V_o\left(\frac{1}{R1 + R2} + \frac{1}{R3 + R4} + \frac{1}{R5 + R6} + \frac{1}{R7 + R8}\right)$$

Multiple Non-Inverting Gain Channels



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Channel	V_o	I_F
1	$-V1\left(\frac{R2}{R1}\right)$	$\frac{V_o}{R2} + \frac{V_o - V2}{R3 + R4} + \frac{V_o - V3}{R5 + R6} + \frac{V_o - V4}{R7 + R8}$
2	$-V2\left(\frac{R4}{R3}\right)$	$\frac{V_o}{R4} + \frac{V_o - V1}{R1 + R2} + \frac{V_o - V3}{R5 + R6} + \frac{V_o - V4}{R7 + R8}$
3	$-V3\left(\frac{R6}{R5}\right)$	$\frac{V_o}{R6} + \frac{V_o - V1}{R1 + R2} + \frac{V_o - V2}{R3 + R4} + \frac{V_o - V4}{R7 + R8}$
4	$-V4\left(\frac{R8}{R7}\right)$	$\frac{V_o}{R8} + \frac{V_o - V1}{R1 + R2} + \frac{V_o - V2}{R3 + R4} + \frac{V_o - V3}{R5 + R6}$

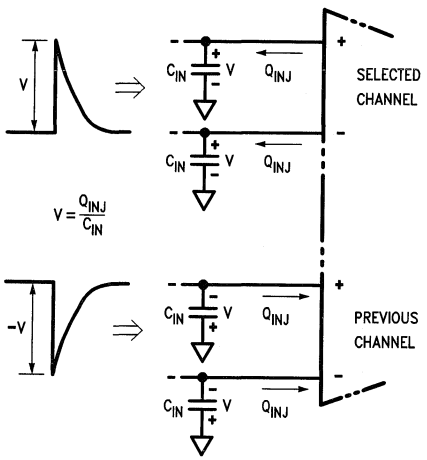
Multiple Inverting Gain Channels

FIGURE 10. Circuits Using Multiple Inverting and Non-Inverting Gain Channels

Application Hints (Continued)

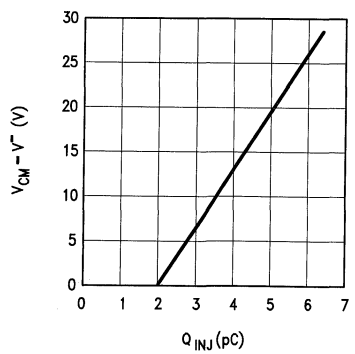
INPUT CHARGE INJECTION

When the Mux-Amp switches channels, charge is injected from the inputs of the selected and previous channels, see *Figure 12*. This causes a positive error voltage at the input of the selected channel and a negative voltage at the previous channel. The amplitude of this error voltage equals Q_{INJ}/C_{IN}, where C_{IN} is the total capacitance at the input and Q_{INJ} is the charge injected. As plotted in *Figure 13*, Q_{INJ} increases proportionally with the difference in voltage between a channel's input common mode voltage and the negative supply. The RC time constant of C_{IN} times resistance seen from the input will determine how long the error voltage remains at the input.



TL/H/9131–20

FIGURE 12. Error Voltage From Input Charge Injection



TL/H/9131–21

FIGURE 13. Q_{INJ} vs $V_{CM} - V^-$

MAXIMUM OUTPUT LOAD CONDITIONS

The Mux-Amp is guaranteed to drive a 600Ω load as specified over its entire operating range. Reducing the load resistance below this value may cause the output to current limit. It may also cause the junction temperature limit to be exceeded when operating the part near its maximum ambient temperature.

The Mux-Amp is unconditionally stable with as much as 500 pF connected from the output to ground. If the output is required to drive a larger capacitive load, the Mux-Amp may need to operate with at least a gain of 10. Otherwise, it may become unstable when sinking current.

DIGITAL FEEDTHROUGH

When interfacing the Mux-Amp to a microprocessor, pins A, B, $\overline{EN}$, and $\overline{WR}$ are connected to an address bus where high frequency digital signals are present. The fast edges of these signals can propagate into the Mux-Amp's analog signal path, causing fast transients to appear at the output. To avoid this problem, the following precautions should be taken.

1) Analog and digital ground must be kept separate. They can only be connected together back at the power supply or supply bus.

2) Bypass capacitors should have low inductance to prevent noise spikes on the voltage supply pins. A ceramic disc capacitor of 0.1 μF is usually sufficient.

3) All lead lengths should be kept short to prevent them from picking up digital signals.

By using these rules, digital signals can be attenuated at the input channels by typically 100 dB.

Lab measurements have shown a minimum digital feedthrough signal of 2 mV occurs at the output even when the best layout precautions are taken. This is fine for many applications, but to completely eliminate digital feedthrough, any signals coming directly from the bus must be sent to the Mux-Amp via a Tri-State buffer, see *Figure 14*. This isolates the Mux-Amp's digital pins from the address bus to prevent pin to pin feedthrough. CS can be used to enable the Tri-State buffers when signals are sent to the Mux-Amp from the address bus.

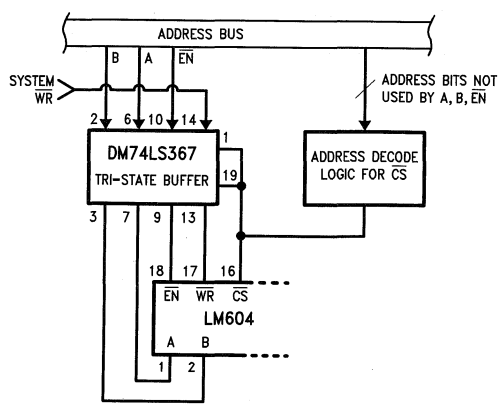


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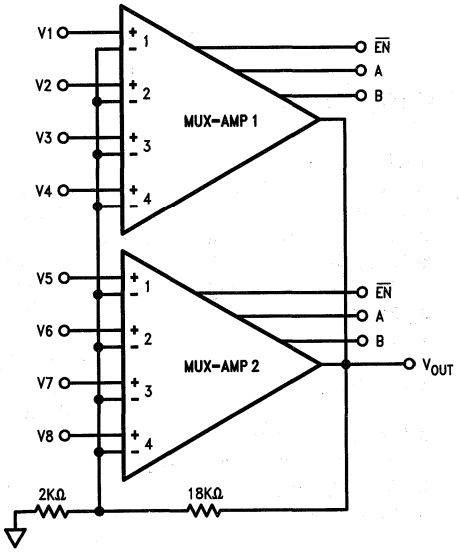
FIGURE 14. Isolating Mux-Amp from Address Bus by Using a Tri-State Buffer

Typical Applications



Mux-Amp 1			Mux-Amp 2			Input
A	B	$\overline{EN}$	A	B	$\overline{EN}$	
0	0	0	X	X	1	V1
0	1	0	X	X	1	V2
1	0	0	X	X	1	V3
1	1	0	X	X	1	V4
X	X	1	0	0	0	V5
X	X	1	0	1	0	V6
X	X	1	1	0	0	V7
X	X	1	1	1	0	V8

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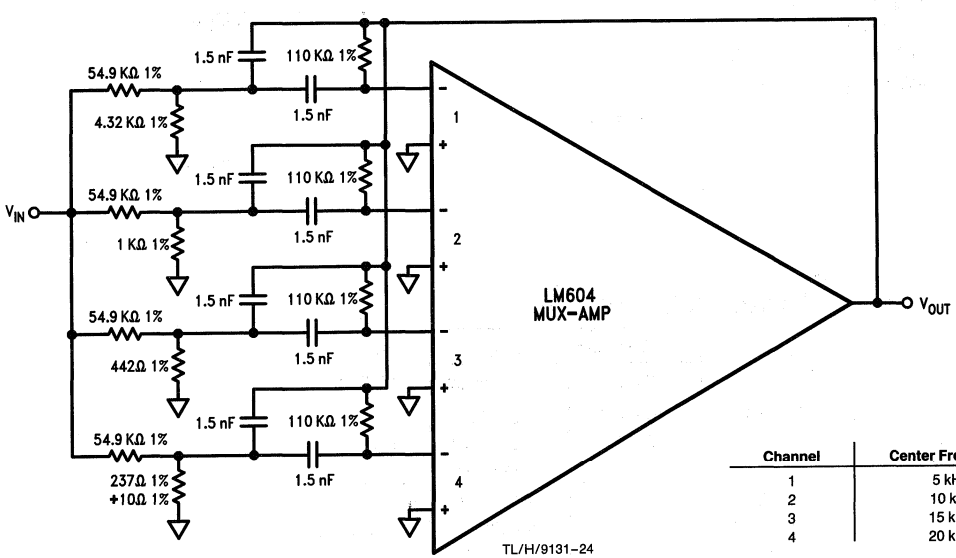
Eight Channel Multiplexer and Amplifier with a Gain of 10



Channel	Center Frequency
1	5 kHz
2	10 khz
3	15 kHz
4	20 kHz

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Programmable Bandpass Filter: Each channel has a 2 kHz bandwidth and a gain of 1 at the center frequency

National Semiconductor

LM607 Precision Operational Amplifier

General Description

The LM607 series of precision operational amplifiers are trimmed at wafer sort to extremely low values of offset voltage. Advanced circuit design and testing techniques allow guaranteed drift specifications as low as 0.3 μV/°C with offsets as low as 25 μV.

Other input parameters are equally impressive. The typical open loop voltage gain of 5 Million yields extremely low error in high-gain applications. CMRR and PSRR are typically 140 dB.

Using Super-Beta transistors in the front end enables the LM607 to operate at high input stage current while maintaining low values of input bias current (1 nA typ.) This gives the part its low input voltage noise: 6.5 nV/$\sqrt{\text{Hz}}$.

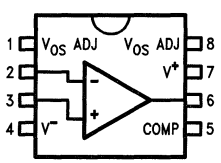
High operating currents also help give the LM607 its high gain-bandwidth product of 1.8 MHz and slew rate of 0.7V/μs. Despite its higher speed, the LM607 draws less supply current than OP-07 and OP-77 types: only 1 mA at ±15V supplies.

Features

- Low V_{OS} LM607A: 25 μV max
- Low drift LM607A: 0.3 μV/°C max
- Drift *100% tested:* A and B grades
- High gain LM607A: 5 million min
- High CMRR LM607A: 124 dB min
- High PSRR LM607A: 120 dB min
- Low noise 6.5 nV/$\sqrt{\text{Hz}}$ @ 1 kHz; 7.2 nV/$\sqrt{\text{Hz}}$ @ 10 Hz
- High speed 1.8 MHz gain-bandwidth; 0.7V/μs slew rate
- Low supply current 1 mA
- Wide input common mode range ±13.5V
- Wide supply range ±3V to ±18V
- Overcompensation Allows driving high C_L

Connection Diagrams

Cerdip and Molded DIP



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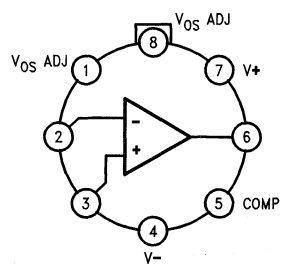
Top View

TO-99 Metal Package



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Top View

Ordering Information

Package	Temperature Range		NSC Drawing
	Military	Commercial	
TO-99	LM607AMH LM607BMH	LM607ACH LM607BCH LM607CH	H08C
8-Pin Molded DIP		LM607ACN LM607BCN LM607CN	N08E

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Differential Input Overdrive Current (Note 7)	±25 mA
Supply Voltage	44V
Input Voltage	Supply Voltage
Output Short Circuit to Gnd	Continuous
Power Dissipation (Note 9)	500 mW
Maximum Junction Temperture	150°C
Storage Temperature Range	−65°C to 150°C
Lead Temperature (Soldering, 10 sec.)	260°C
ESD Tolerance	
C_{ZAP} = 100 pF	2000V
R_{ZAP} = 1.5 kΩ	

Operating Rating

Temperature Range (Note 9)	
LM607AM/LM607BM	$-55°C \le T_J \le +125°C$
LM607C/LM607AC/LM607BC	$0°C \le T_J \le +70°C$

Electrical Characteristics

All limits guaranteed for T_J = 25°C, V_{CM} = 0, V_O = 0, and ±15V supplies unless otherwise specified. **Boldface limits apply at operating temperature extremes.**

Parameter	Conditions	Typ	LM607AM		LM607BM		Units
			Tested Limit (Note 5)	Design Limit (Note 6)	Tested Limit (Note 5)	Design Limit (Note 6)	
Input Offset Voltage	(Note 2)	15	25 **80**		60 **120**		μV Max
Input Offset Voltage Drift	(Note 3)	0.2	**0.3**		**0.6**		μV/°C Max
Input Offset Voltage Long Term Stability	(Note 4)	0.2					μV/mo Max
Input Bias Current		1	2 **4**		3 **6**		nA Max
Input Offset Current		0.5	2 **4**		2.8 **5.6**		nA Max
Input Noise Voltage	0.1 to 10 Hz	0.2		0.5		0.5	μV p-p Max
Input Noise Voltage Density	f = 10 Hz f = 100 Hz f = 1 kHz	7.2 6.6 6.5	18 8	 10 	18 8	 10 	nV/√Hz Max
Input Noise Current	0.1 to 10 Hz	14					pA p-p Max
Input Noise Current Density	f = 10 Hz f = 100 Hz f = 1 kHz	0.32 0.14 0.12					pA/√Hz Max
Input Resistance	Differential Mode Common Mode	2 100					MΩ GΩ
Input Voltage Range		±13.5	±13 **±12.5**		±13 **±12.5**		V Min
Common-Mode Rejection Ratio	V_{CM} = ±13V **V_{CM} = ±12.5V**	140	124 **120**		116 **112**		dB Min
Power Supply Rejection Ratio	V_S = ±3V to ±18V (Note 8)	140	120 **117**		114 **112**		dB Min
Large-Signal Voltage Gain	V_O = ±10V $R_L \ge 2$ kΩ $R_L \ge 1$ kΩ	10000 5000	5000 **2000** 1500		2000 **1500** 1000		V/mV Min

Electrical Characteristics (Continued)

Parameter	Conditions	Typ	LM607AM		LM607BM		Units
			Tested Limit (Note 5)	Design Limit (Note 6)	Tested Limit (Note 5)	Design Limit (Note 6)	
Output Voltage Swing	$R_L \geq 2\,k\Omega$ $R_L \geq 1\,k\Omega$	±13.8	±13 **±12.5** ±12.5		±13 **±12.5** ±12.5		V Min
Slew Rate		0.7		0.4		0.4	V/μs Min
Gain-Bandwidth Product	f = 100 kHz	1.8		1.0		1.0	MHz Min
Open-Loop Output Resistance		50					Ω
Supply Current		1	1.5 **2.0**		1.5 **2.0**		mA Max
Offset Adjust Range		1.5					mV

Electrical Characteristics

All limits guaranteed for T_J = 25°C, V_{CM} = 0, V_O = 0, and ±15V supplies unless otherwise specified. **Boldface limits apply at operating temperature extremes.**

Parameter	Conditions	Typ	LM607AC		LM607BC		LM607C		Units
			Tested Limit (Note 5)	Design Limit (Note 6)	Tested Limit (Note 5)	Design Limit (Note 6)	Tested Limit (Note 5)	Design Limit (Note 6)	
Input Offset Voltage	(Note 2)	15	25 **40**		60 **90**		150	**250**	μV Max
Input Offset Voltage Drift	(Note 3)	0.2	**0.3**		**0.6**			**2.5**	μV/°C Max
Input Offset Voltage Long Term Stability	(Note 4)	0.2							μV/mo Max
Input Bias Current		1	2	**4**	3	**6**	10	**14**	nA Max
Input Offset Current		0.5	2	**4**	2.8	**5.6**	6	**10**	nA Max
Input Noise Voltage	0.1 to 10 Hz	0.2		0.5		0.5		0.5	μV p-p Max
Input Voltage Noise Density	f = 10 Hz f = 100 Hz f = 1 kHz	7.2 6.6 6.5	18 8	10	18 8	10	20 11.5	13.5	nV/√Hz Max
Input Noise Current	0.1 to 10 Hz	14							pA p-p Max
Input Noise Current Density	f = 10 Hz f = 100 Hz f = 1 kHz	0.32 0.14 0.12							pA/√Hz Max
Input Resistance	Differential Mode Common Mode	2 100							MΩ GΩ
Input Voltage Range		±13.5	±13	**±12.5**	±13	**±12.5**	±13	**±12.5**	V Min
Common-Mode Rejection Ratio	V_{CM} = ±13V **V_{CM} = ±12.5 V**	140	124	**120**	116	**112**	110	**108**	dB Min
Power Supply Rejection Ratio	V_S = ±3V to ±18V (Note 8)	140	120	**117**	114	**112**	110	**108**	dB Min

Electrical Characteristics (Continued)

Parameter	Conditions	Typ	LM607AC		LM607BC		LM607C		Units
			Tested Limit (Note 5)	Design Limit (Note 6)	Tested Limit (Note 5)	Design Limit (Note 6)	Tested Limit (Note 5)	Design Limit (Note 6)	
Large-Signal Voltage Gain	$V_O = \pm 10V$ $R_L \geq 2\ k\Omega$ $R_L \geq 1\ k\Omega$	10000 5000	5000 1500	**2000**	2000 1000	**1500**	1500 1000	**1000**	V/mV Min
Output Voltage Swing	$R_L \geq 2\ k\Omega$ $R_L \geq 1\ k\Omega$	± 13.8	± 13 ± 12.5	$\pm$ **12.5**	± 13 ± 12.5	$\pm$ **12.5**	± 12.5 ± 12	$\pm$ **12**	V Min
Slew Rate		0.7		0.4		0.4		0.4	V/μs Min
Gain-Bandwidth Product	f = 100 kHz	1.8		1.0		1.0		1.0	MHz Min
Open-Loop Output Resistance		50							Ω
Supply Current		1	1.5	**2.0**	1.5	**2.0**	1.8	**2.2**	mA Max
Offset Adjust Range		1.5							mV

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed.

Note 2: Input offset voltage for A and B grades is tested and guaranteed with the device fully warmed up. See *Figure 1* in the Application Hints for test circuit. Warmup drift is typically 3 μV settling out in 5 minutes. The LM607C offset voltage is measured by automated test equipment within 200 ms of applying power.

Note 3: Input offset voltage drift is defined as $[V_{OS}(70°C) - V_{OS}(-5°C)]/75°C$ for the commercial temperature range. For the military temperature range, the input offset voltage drift is measured from room temperature to both extremes: both $[V_{OS}(25°C) - V_{OS}(-55°C)]/80°C$ and $[V_{OS}(125°C) - V_{OS}(25°C)]/100°C$.

Note 4: Input offset voltage long term stability refers to the average trend line of V_{OS} vs. time over extended periods of time after the first 30 days of operation. Excluding the initial hour of operation, changes in V_{OS} during the first 30 days are typically 2 μV.

Note 5: Guaranteed and 100% production tested.

Note 6: Limits at temperature extremes are guaranteed via correlation using Standard Statistical Quality Control (SQC) Methods. All limits are to be used to calculate Average Outgoing Quality Level (AOQL).

Note 7: Inputs are protected by back-to-back diodes to prevent zener breakdown of the input transistors. Series limiting resistors have not been included since they degrade noise performance. Excessive current may flow if a differential voltage in excess of 0.7V is applied.

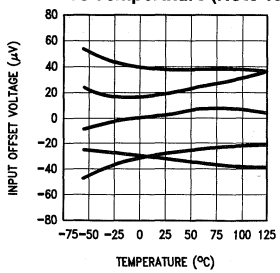
Note 8: Power Supply Rejection Ratio is tested by moving both power supplies together from their minimum to maximum values.

Note 9: Typical thermal resistance of the molded package is 95°C/W junction-to-ambient. Typical thermal resistance of the metal can package is 150°C/W junction-to-ambient and 17°C/W junction-to-case.

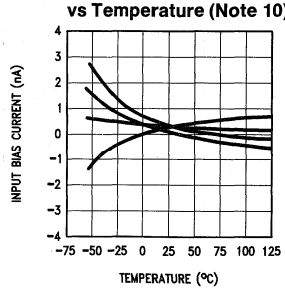
Note 10: These units selected to illustrate the type of variations that may be encountered. (This note refers to particular curves within the Typical Performance Characteristics.)

Typical Performance Characteristics $V_S = \pm 15V$, $T_A = 25°C$, $R_L = 2k$ unless otherwise indicated

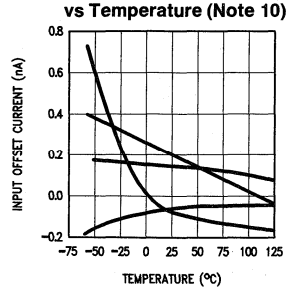
Input Offset Voltage of 5 Representative Units vs Temperature (Note 10)



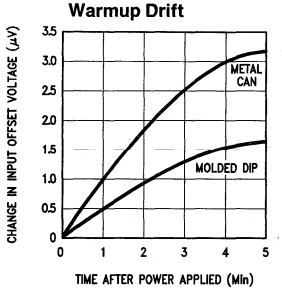
Input Bias Current of 4 Representative Units vs Temperature (Note 10)



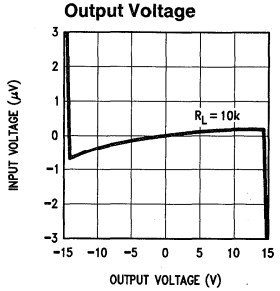
Input Offset Current of 4 Representative Units vs Temperature (Note 10)



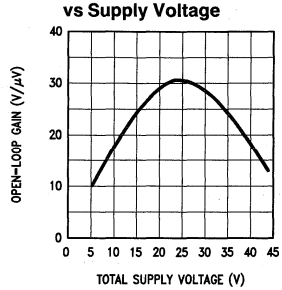
Warmup Drift



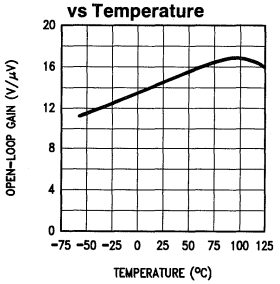
Input Voltage vs Output Voltage



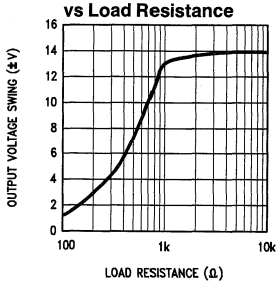
Open-Loop Gain vs Supply Voltage



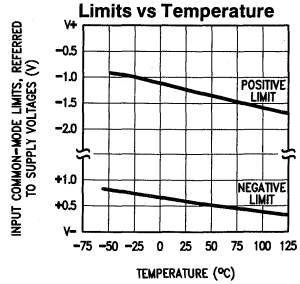
Open-Loop Gain vs Temperature



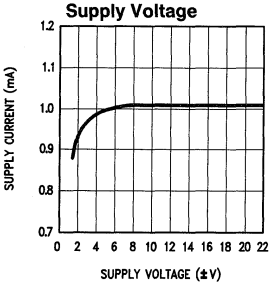
Output Voltage Swing vs Load Resistance



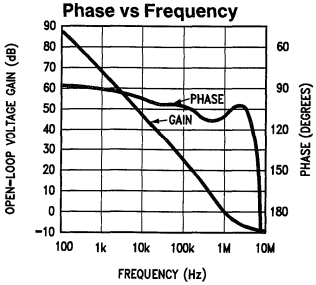
Input Common-Mode Limits vs Temperature



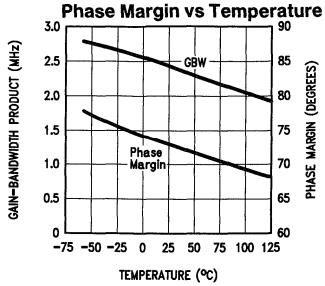
Supply Current vs Supply Voltage



Open Loop Gain and Phase vs Frequency



Gain-Bandwidth Product, Phase Margin vs Temperature



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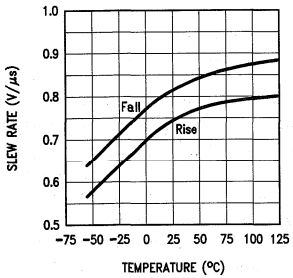
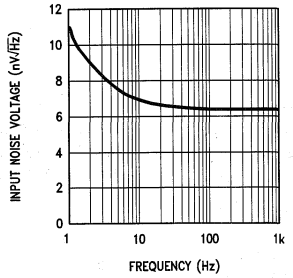
Typical Performance Characteristics (Continued)

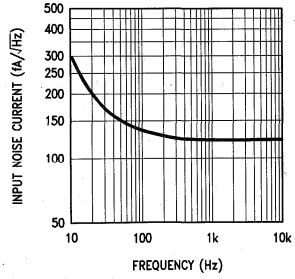
Slew Rate vs Temperature



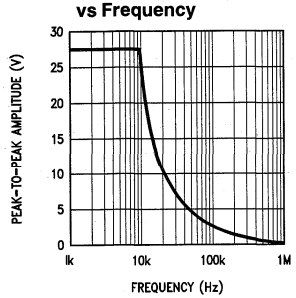
Noise Voltage vs Frequency



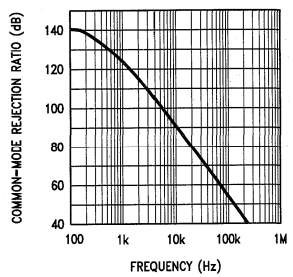
Noise Current vs Frequency



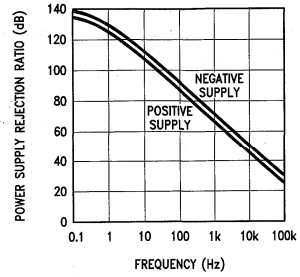
Maximum Output Swing vs Frequency



Common-Mode Rejection Ratio vs Frequency

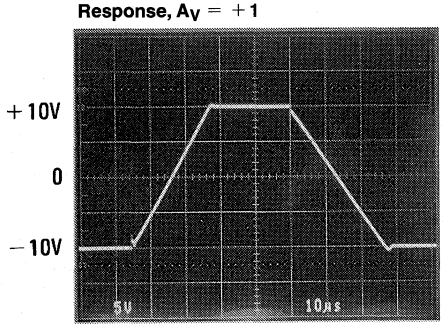


Power Supply Rejection Ratio vs Frequency



TL/H/8787–13

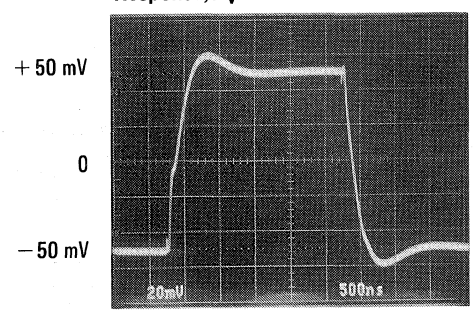
Large-Signal Pulse Response, $A_V = +1$



TIME (10 μs/DIV)

TL/H/8787–14

Small-Signal Pulse Response, $A_V = +1$



TIME (500 ns/DIV)

TL/H/8787–15

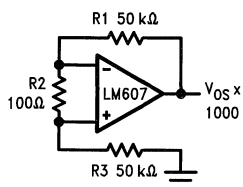
Application Hints

OFFSET VOLTAGE

Offset voltage of the LM607 is internally trimmed to a very low value. The data sheet V_{OS} specification applies at T_J = 25°C, V_{CM} = 0 and ±15V supplies. For other conditions, temperature drift, common-mode rejection and power-supply rejection errors must be taken into account.

Although the LM607C is specified as T_J = 25°C, the 3 μV typical warmup drift is a small fraction of its 100 μV max offset. For the 25 μV LM607A and 50 μV LM607B grades, the offset voltage is measured fully warmed up with the circuit of *Figure 1* approximately 5 minutes after applying power.

To measure V_{OS} with high accuracy, gain must be taken right at the device as shown, otherwise the offset voltage would get swamped out by noise and thermoelectric voltages. Thermocouples occur in the devices, the IC socket and the resistor across the device inputs (R2), all of which must be held isothermal. Usually best results are obtained by placing the circuit in a box or chamber to minimized airflow and employing a long thermal soak time. R2 should be mounted symmetrically with respect to potential thermal gradients: e.g. *not* perpendicular to the board but instead parallel to the board and the device socket. In addition, R2 should have low thermal EMF. Cermet or nichrome metal film types are acceptable; avoid tin-oxide resistors.

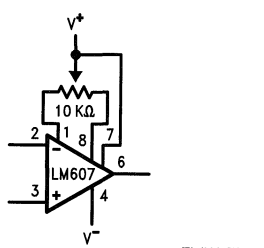


TL/H/8787–3

FIGURE 1. Offset Voltage Test Circuit

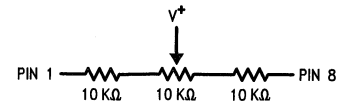
OFFSET NULLING

This is usually not required on the LM607 family since its offset voltage is internally trimmed. An offset adjust range of approximately ±1.5 mV is available using a single 10 or 20 kΩ potentiometer as shown in *Figure 2*. With these values, the adjustment is relatively linear over the entire range. If a 100 kΩ potentiometer is used, the adjustment becomes very coarse at the extremes (above 700 μV) but fine in the center, which makes it easier to precisely null the offset. For even more sensitivity, employ a pot in conjunction with two fixed resistors. For example the circuit of *Figure 3* has an adjustment range of ±150 μV.



TL/H/8787–4

FIGURE 2. Offset Adjust Circuit



TL/H/8787–5

FIGURE 3. Improved Sensitivity Offset Adjust

Because adjusting the offset voltage of an LM607 will alter its offset voltage temperature drift, caution is advised. Every 100 μV of offset will produce a 0.33 μV/°C drift component. For this reason the offset adjust potentiometer should not be used to null out a sensor offset if system temperature drift is important; rather a stable voltage reference must be added to the sensor voltage. Offset voltage drift is guaranteed by design for the LM607C either with or without external nulling. The higher precision A and B grades are 100% drift tested and guaranteed without nulling only.

OVERCOMPENSATION

Without any external compensation, the LM607 is stable at unity gain and up to 750 pF load capacitance. It has a slew rate of 0.7V/μs and a gain-bandwidth product of 1.8 MHz. If desired, the amplifier may be overcompensated by adding external components as shown in *Figure 4*. This increases maximum capacitive loading to 0.01 μF while decreasing slew rate to 0.13V/μs and bandwidth to 200 kHz. If overcompensation is not desired, pin 5 should be left open.

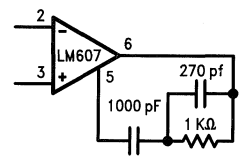


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FIGURE 4. Overcompensation

NOISE

The LM607 achieves lower voltage noise than the OP-07 primarily by operating at higher input stage current. Its superbeta input transistors and trimmed bias-current compensation prevent the bias current from increasing. When measuring spot noise, a circuit as shown in *Figure 5* is recommended. The DUT runs at a gain of 100 will not roll off until approximately 15 kHz. Another gain of 100 amplifier following brings total DUT-input-referred gain up to 10,000 to minimize sensitivity to EMI in the environment. When measuring spot noise at 100 Hz, it is recommended that the bandwidth be 20 Hz or less to minimize pickup of 120 Hz, the second harmonic of line frequency.

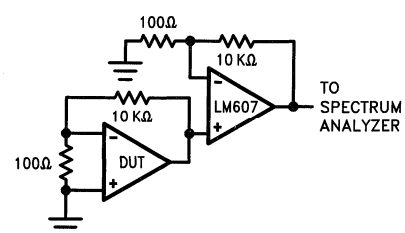

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FIGURE 5. Spot Noise Test Circuit

Application Hints (Continued)

The circuit used to measure peak-to-peak noise in the 0.1 to 10 Hz range is shown in *Figure 6*. The device should be warmed up for about 2 minutes and shielded from air currents to minimize warmup drift and thermoelectric voltages. The test time should be limited to only 10 seconds, as this limits noise contributions below 0.1 Hz, in addition to the single zero rolloff. The measuring equipment must be flat beyond this bandwidth. DC coupling must be employed to ensure this. Certain types of X-Y plotters may not be usable because of severe rolloff above a few Hz.

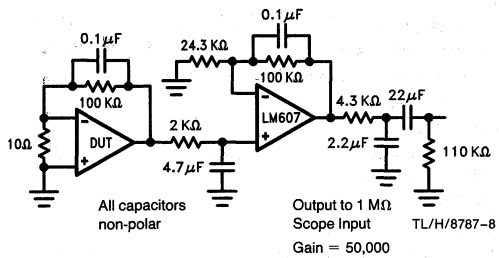


FIGURE 6. 0.1 to 10 Hz Noise Test Circuit

Input Overdrive

The LM607's input-protection diodes prevent zener breakdown of the input transistors and the ensuing degradation of input DC parameters. Current limiting resistors have not been included as they would degrade input noise voltage. Input current should be limited to ±25 mA to avoid potential damage to the IC metallization.

In voltage follower applications, large input voltage steps may be coupled directly to the op amp's output via the protection diodes. If the input and feedback resistances are low in value, the output stage may be driven temporarily into current limit. The resulting output waveform exhibits an initial fast step when the diodes are conducting followed by a slight glitch as the amplifier comes out of current limit before true slewing is observed. For best results, use input and feedback resistors of 2 kΩ each in parallel with 30 pF capacitors. The capacitors eliminate input and feedback poles which respectively cause signal rolloff and instabilities.

National Semiconductor

LM611
Operational Amplifier and Adjustable Reference

General Description

The LM611 consists of a single-supply op-amp and a programmable voltage reference in one space saving 8-pin package. The op-amp out-performs most single-supply op-amps by providing higher speed and bandwidth along with low supply current. This device was specifically designed to lower cost and board space requirements in transducer, test, measurement and data acquisition systems.

Combining a stable voltage reference with a wide output swing op-amp makes the LM611 ideal for single supply transducers, signal conditioning and bridge driving where large common-mode-signals are common. The voltage reference consists of a reliable band-gap design that maintains low dynamic output impedance (1Ω typical), excellent initial tolerance (0.6%), and the ability to be programmed from 1.2V to 6.3V via two external resistors. The voltage reference is very stable even when driving large capacitive loads, as are commonly encountered in CMOS data acquisition systems.

As a member of National's Super-Block™ family, the LM611 is a space-saving monolithic alternative to a multi-chip solution, offering a high level of integration without sacrificing performance.

Features

OP AMP

- Low operating current — 300 μA (op amp)
- Wide supply voltage range — 4V to 36V
- Wide common-mode range — V^- to ($V^+ - 1.8V$)
- Wide differential input voltage — ±36V
- Available in low cost 8-pin DIP
- Available in plastic package rated for Military Temperature Range Operation

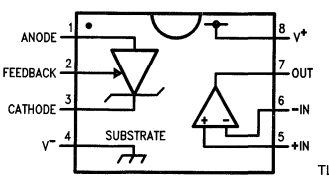
REFERENCE

- Adjustable output voltage — 1.2V to 6.3V
- Tight initial tolerance available — ±0.6%
- Wide operating current range — 17 μA to 20 mA
- Reference floats above ground
- Tolerant of load capacitance

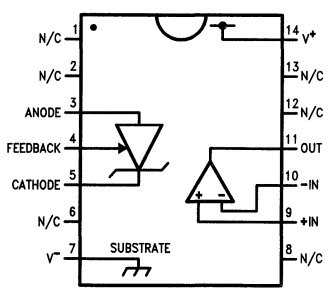
Applications

- Transducer bridge driver
- Process and Mass Flow Control systems
- Power supply voltage monitor
- Buffered voltage references for A/D's

Connection Diagrams



TL/H/9221-1



TL/H/9221-2

Ordering Information

Reference Tolerance & V_{OS}	Temperature Range			Package	NSC Drawing
	Military $-55°C \le T_A \le +125°C$	Industrial $-40°C \le T_A \le +85°C$	Commercial $0°C \le T_A \le +70°C$		
±0.6% @ 80 ppm/°C max V_{OS} = 3.5 mV max	LM611AMN	LM611AIN	—	8-pin molded DIP	N08E
	LM611AMJ/883 (Note 12)	—	—	8-pin ceramic DIP	J08A
±2.0% @ 150 ppm/°C max V_{OS} = 5 mV max	LM611MN	LM611BIN	LM611CN	8-pin molded DIP	N08E
	—	LM611IM	LM611CM	14-pin Narrow Surface Mount	M14A

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Voltage on Any Pins Except V_R (referred to V^- pin) 36V (Max)
(Note 2) −0.3V (Min)

Current through Any Input Pin and V_R Pin ±20 mA

Differential Input Voltage
Military and Industrial ±36V
Commercial ±32V

Storage Temperature Range $-65°C \le T_J \le +150°C$

Maximum Junction Temperature 150°C

Thermal Resistance, Junction-to-Ambient (Note 3)
N Package 100°C/W
M Package 150°C/W

Soldering Information Soldering (10 seconds)
N Package 260°C
M Package 220°C

ESD Tolerance (Note 4) ±1 kV

Operating Temperature Range

LM611AI, LM611I, LM611BI $-40°C \le T_J \le +85°C$
LM611AM, LM611M $-55°C \le T_J \le +125°C$
LM611C $0°C \le T_J \le 70°C$

Electrical Characteristics

These specifications apply for $V^- = GND = 0V$, $V^+ = 5V$, $V_{CM} = V_{OUT} = 2.5V$, $I_R = 100\ \mu A$, FEEDBACK pin shorted to GND, unless otherwise specified. Limits in standard typeface are for $T_J = 25°C$; limits in **boldface type** apply over the **Operating Temperature Range.**

Symbol	Parameter	Conditions	Typical (Note 5)	LM611AM LM611AI Limits (Note 6)	LM611M LM611BI LM611I LM611C Limits (Note 6)	Units
I_S	Total Supply Current	$R_{LOAD} = \infty$, $4V \le V^+ \le 36V$ (32V for LM611C)	210 **221**	300 **320**	350 **370**	µA max µA max
V_S	Supply Voltage Range		2.2 **2.9**	2.8 **3**	2.8 **3**	V min V min
			46 **43**	36 **36**	32 **32**	V max V max
OPERATIONAL AMPLIFIER						
V_{OS1}	V_{OS} Over Supply	$4V \le V^+ \le 36V$ $(4V \le V^+ \le 32V$ for LM611C)	1.5 **2.0**	3.5 **6.0**	5.0 **7.0**	mV max mV max
V_{OS2}	V_{OS} Over V_{CM}	V_{CM} = 0V through V_{CM} = $(V^+ - 1.8V)$, $V^+ = 30V$, $V^- = 0V$	1.0 **1.5**	3.5 **6.0**	5.0 **7.0**	mV max mV max
$\frac{V_{OS3}}{\Delta T}$	Average V_{OS} Drift	(Note 6)	**15**			µV/°C max
I_B	Input Bias Current		10 **11**	25 **30**	35 **40**	nA max nA max
I_{OS}	Input Offset Current		0.2 **0.3**	4 **5**	4 **5**	nA max nA max
$\frac{I_{OS1}}{\Delta T}$	Average Offset Drift Current		**4**			pA/°C
R_{IN}	Input Resistance	Differential	1800			MΩ
		Common-Mode	3800			MΩ
C_{IN}	Input Capacitance	Common-Mode	5.7			pF
e_n	Voltage Noise	f = 100 Hz, Input Referred	74			$nV/\sqrt{Hz}$
I_n	Current Noise	f = 100 Hz, Input Referred	58			$fA/\sqrt{Hz}$
CMRR	Common-Mode Rejection-Ratio	$V^+ = 30V$, $0V \le V_{CM} \le (V^+ - 1.8V)$ $CMRR = 20 \log (\Delta V_{CM}/\Delta V_{OS})$	95 **90**	80 **75**	75 **70**	dB min dB min
PSRR	Power Supply Rejection-Ratio	$4V \le V^+ \le 30V$, $V_{CM} = V^+/2$, $PSRR = 20 \log (\Delta V^+/\Delta V_{OS})$	110 **100**	80 **75**	75 **70**	dB min dB min
A_V	Open Loop Voltage Gain	$R_L = 10\ k\Omega$ to GND, $V^+ = 30V$, $5V \le V_{OUT} \le 25V$	500 **50**	100 **40**	94 **40**	V/mV min
SR	Slew Rate	$V^+ = 30V$ (Note 7)	0.70 **0.65**	0.55 **0.45**	0.50 **0.45**	V/µs

Electrical Characteristics (Continued)

These specifications apply for V^- = GND = 0V, V^+ = 5V, V_{CM} = V_{OUT} = 2.5V, I_R = 100 μA, FEEDBACK pin shorted to GND, unless otherwise specified. Limits in standard typeface are for T_J = 25°C; limits in **boldface type** apply over the **Operating Temperature Range.**

Symbol	Parameter	Conditions	Typical (Note 5)	LM611AM LM611AI Limits (Note 6)	LM611M LM611BI LM611I LM611C Limits (Note 6)	Units
OPERATIONAL AMPLIFIER (Continued)						
GBW	Gain Bandwidth	C_L = 50 pF	0.80 **0.50**			MHz
V_{O1}	Output Voltage Swing High	R_L = 10 kΩ to GND V^+ = 36V (32V for LM611C)	$V^+ - 1.4$ **$V^+ - 1.6$**	$V^+ - 1.7$ **$V^+ - 1.9$**	$V^+ - 1.8$ **$V^+ - 1.9$**	V min V min
V_{O2}	Output Voltage Swing Low	R_L = 10 kΩ to V^+ V^+ = 36V (32V for LM611C)	$V^- + 0.8$ **$V^- + 0.9$**	$V^- + 0.9$ **$V^- + 1.0$**	$V^- + 0.95$ **$V^- + 1.0$**	V max V max
I_{OUT}	Output Source Current	V_{OUT} = 2.5V, V_{+IN} = 0V, V_{-IN} = −0.3V	25 **15**	20 **13**	16 **13**	mA min mA min
I_{SINK}	Output Sink Current	V_{OUT} = 1.6V, V_{+IN} = 0V, V_{-IN} = 0.3V	17 **9**	14 **8**	13 **8**	mA min mA min
I_{SHORT}	Short Circuit Current	V_{OUT} = 0V, V_{+IN} = 3V, V_{-IN} = 2V, Source	30 **40**	50 **60**	50 **60**	mA max mA max
		V_{OUT} = 5V, V_{+IN} = 2V, V_{-IN} = 3V, Sink	30 **32**	60 **80**	70 **90**	mA max mA max
VOLTAGE REFERENCE						
V_R	Reference Voltage	(Note 8)	1.244	1.2365 1.2515 (±0.6%)	1.2191 1.2689 (±2.0%)	V min V max
$\frac{\Delta V_R}{\Delta T}$	Average Temperature Drift	(Note 9)	**10**	**80**	**150**	PPM/°C max
$\frac{\Delta V_R}{\Delta T_J}$	Hysteresis	Hyst = (Vro′ − Vro)/ΔT_J (Note 10)	**3.2**			μV/°C
$\frac{\Delta V_R}{\Delta I_R}$	V_R Change with Current	$V_{R(100\ \mu A)} - V_{R(17\ \mu A)}$	0.05 **0.1**	1 **1.1**	1 **1.1**	mV max mV max
		$V_{R(10\ mA)} - V_{R(100\ \mu A)}$ (Note 11)	1.5 **2.0**	5 **5.5**	5 **5.5**	mV max mV max
R	Resistance	$\Delta V_{R(10 \rightarrow 0.1\ mA)}$/9.9 mA $\Delta V_{R(100 \rightarrow 17\ \mu A)}$/83 μA	**0.2** **0.6**	**0.56** **13**	**0.56** **13**	Ω max Ω max
$\frac{\Delta V_R}{V_{RO}}$	V_R Change with High V_{RO}	$V_{R(Vro\ =\ Vr)} - V_{R(Vro\ =\ 6.3V)}$ (5.06V between Anode and FEEDBACK)	2.5 **2.8**	7 **10**	7 **10**	mV max mV max
$\frac{\Delta V_R}{\Delta V^+}$	V_R Change with V^+ Change	$V_{R(V^+\ =\ 5V)} - V_{R(V^+\ =\ 36V)}$ (V^+ = 32V for LM611C)	0.1 **0.1**	1.2 **1.3**	1.2 **1.3**	mV max mV max
		$V_{R(V^+\ =\ 5V)} - V_{R(V^+\ =\ 3V)}$	0.01 **0.01**	1 **1.5**	1 **1.5**	mV max mV max
$\frac{\Delta V_R}{\Delta V_{ANODE}}$	V_R Change with V_{ANODE} Change	$V^+ = V^+$ max, $\Delta V_R = V_R$ (@ $V_{ANODE} = V^- =$ GND) − V_R (@ $V_{ANODE} = V^+ - 1.0V$)	0.7 **3.3**	1.5 **3.0**	1.6 **3.0**	mV max mV max
I_{FB}	FEEDBACK Bias Current	I_{FB}; $V_{ANODE} \leq V_{FB} \leq 5.06V$	22 **29**	35 **40**	50 **55**	nA max nA max
e_n	V_R Noise	10 Hz to 10,000 Hz, $V_{RO} = V_R$	30			μV_{RMS}

Electrical Characteristics (Continued)

Note 1: Absolute maximum ratings indicate limits beyond which damage to the component may occur. Electrical specifications do not apply when operating the device beyond its rated operating conditions.

Note 2: More accurately, it is excessive current flow, with resulting excess heating, that limits the voltages on all pins. When any pin is pulled a diode drop below V^-, a parasitic NPN transistor turns ON. No latch-up will occur as long as the current through that pin remains below the Maximum Rating. Operation is undefined and unpredictable when any parasitic diode or transistor is conducting.

Note 3: Junction temperature may be calculated using $T_J = T_A + P_D \theta_{JA}$. The given thermal resistance is worst-case for packages in sockets in still air. For packages soldered to copper-clad board with dissipation from one op amp or reference output transistor, nominal θ_{JA} is 90°C/W for the N package amd 135°C/W for the M package

Note 4: Human body model, 100 pF discharged through a 1.5 kΩ resistor.

Note 5: Typical values in standard typeface are for $T_J = 25°C$; values in **boldface type** apply for the full operating temperature range. These values represent the most likely parametric norm.

Note 6: All limits are guaranteed at room temperature (standard type face) or at operating temperature extremes **(bold face type)**.

Note 7: Slew rate is measured with op amp in a voltage follower configuration. For rising slew rate, the input voltage is driven from 5V to 25V, and the output voltage transition is sampled at 10V and 20V. For falling slew rate, the input voltage is driven from 25V to 5V, and output voltage transition is sampled at 20V and 10V.

Note 8: V_R is the cathode-feedback voltage, nominally 1.244V.

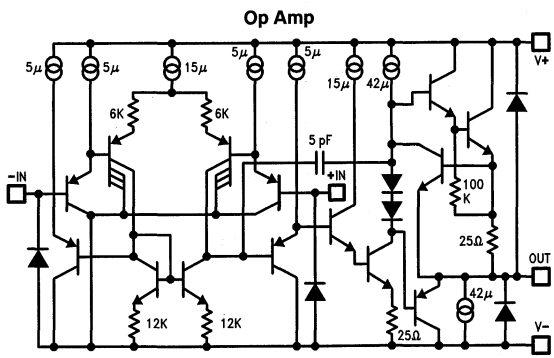
Note 9: Average reference drift is calculated from the measurement of the reference voltage at 25°C and at the temperature extremes. The drift, in ppm/°C, is $10^6 \bullet \Delta V_R / (V_{R[25°C]} \bullet \Delta T_J)$, where ΔV_R is the lowest value subtracted from the highest, $V_{R[25°C]}$ is the value at 25°C, and ΔT_J is the temperature range. This parameter is guaranteed by design and sample testing.

Note 10: Hysteresis is the change in V_R caused by a change in T_J, after the reference has been "dehysterized". To dehysterize the reference; that is minimize the hysteresis to the typical value, its junction temperature should be cycled in the following pattern, spiraling in toward 25°C: 25°C, 85°C, −40°C, 70°C, 0°C, 25°C.

Note 11: Low contact resistance is required for accurate measurement.

Note 12: Military RETS 611AMX electrical test specification is available on request. The LM611AMJ/883 can also be procured as a Standard Military Drawing.

Simplified Schematic Diagrams



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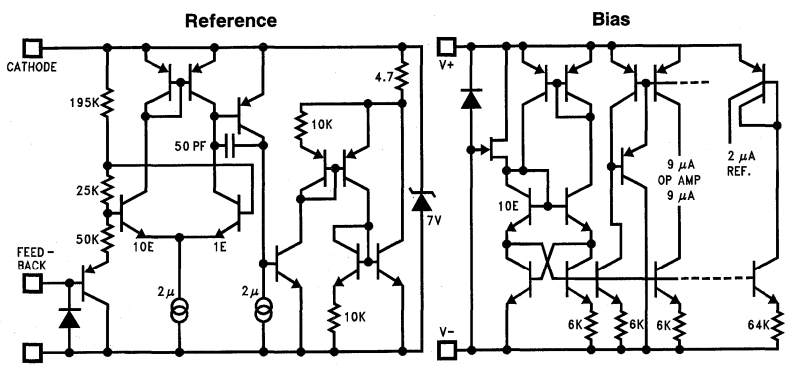

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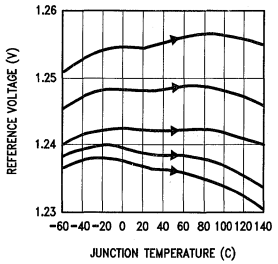
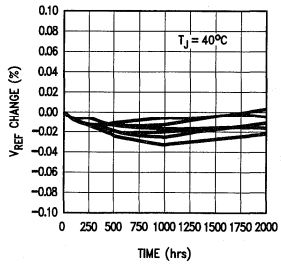
Typical Performance Characteristics (Reference)

T_J = 25°C, FEEDBACK pin shorted to V^- = 0V, unless otherwise noted

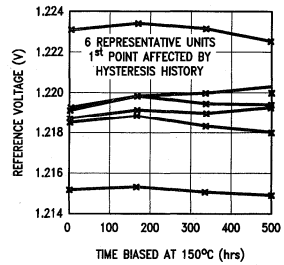
Reference Voltage vs Temp on 5 Representative Units



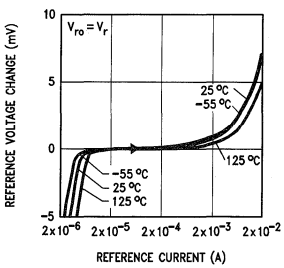
Reference Voltage Drift



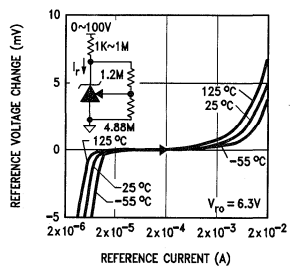
Accelerated Reference Voltage Drift vs Time



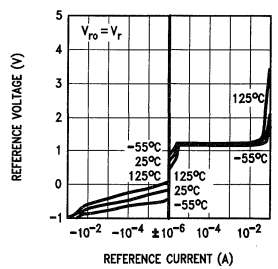
Reference Voltage vs Current and Temperature



Reference Voltage vs Current and Temperature

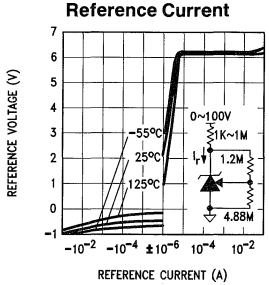


Reference Voltage vs Reference Current

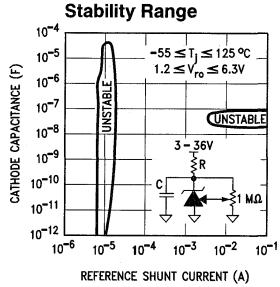


TL/H/9221–5

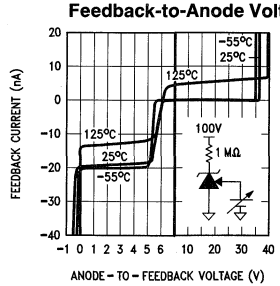
Reference Voltage vs Reference Current



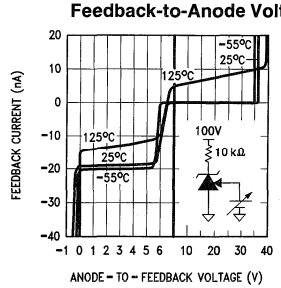
Reference AC Stability Range



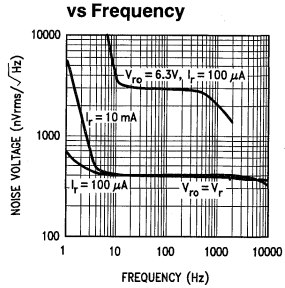
Feedback Current vs Feedback-to-Anode Voltage



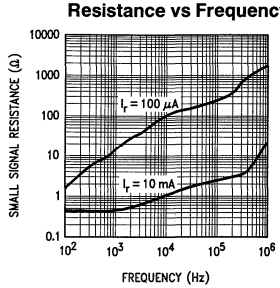
Feedback Current vs Feedback-to-Anode Voltage



Reference Noise Voltage vs Frequency



Reference Small-Signal Resistance vs Frequency

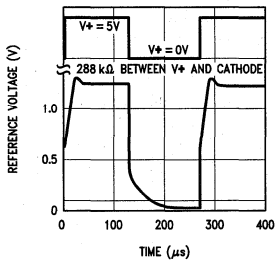


TL/H/9221–6

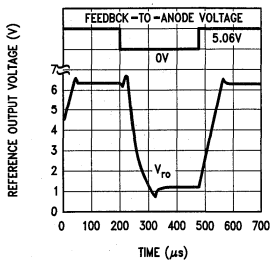
Typical Performance Characteristics (Reference) (Continued)

T_J = 25°C, FEEDBACK pin shorted to V^- = 0V, unless otherwise noted

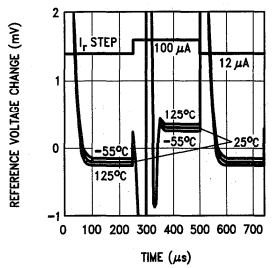
Reference Power-Up Time



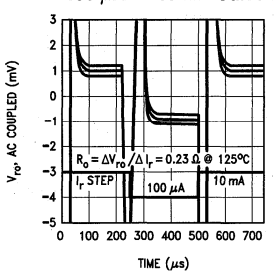
Reference Voltage with Feedback Voltage Step



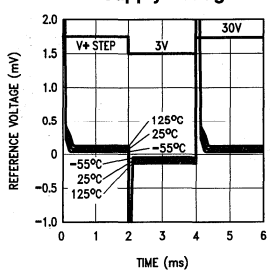
Reference Voltage with 100 ~ 12 μA Current Step



Reference Step Response for 100 μA ~ 10 mA Current Step



Reference Voltage Change with Supply Voltage Step

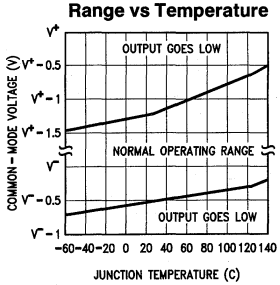


TL/H/9221-7

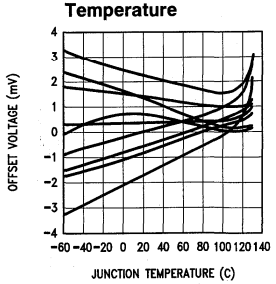
Typical Performance Characteristics (Op Amps)

V^+ = 5V, V^- = GND = 0V, $V_{CM} = V^+/2$, $V_{OUT} = V^+/2$, T_J = 25°C, unless otherwise noted

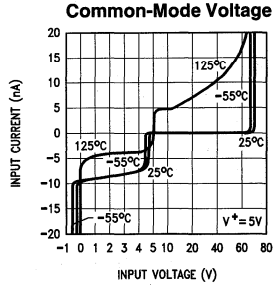
Input Common-Mode Voltage Range vs Temperature



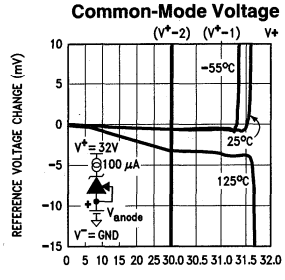
V_{OS} vs Junction Temperature



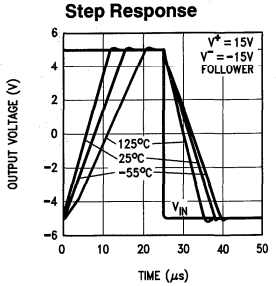
Input Bias Current vs Common-Mode Voltage



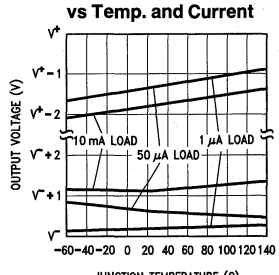
Reference Change vs Common-Mode Voltage



Large-Signal Step Response



Output Voltage Swing vs Temp. and Current



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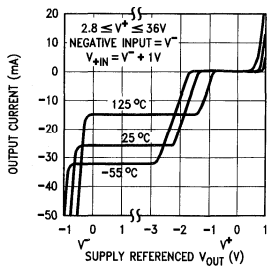
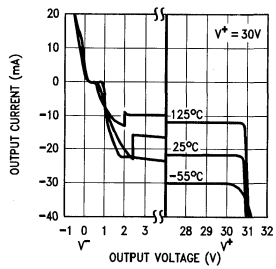
Typical Performance Characteristics (Op Amps) (Continued)

$V^+ = 5V$, $V^- = GND = 0V$, $V_{CM} = V^+/2$, $V_{OUT} = V^+/2$, $T_J = 25°C$, unless otherwise noted

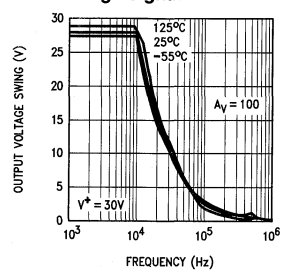
Output Source Current vs Output Voltage and Temp.



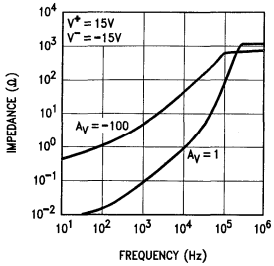
Output Sink Current vs Output Voltage



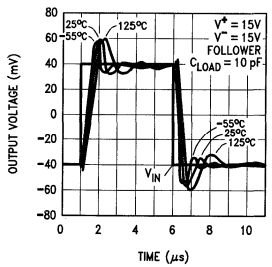
Output Swing, Large Signal



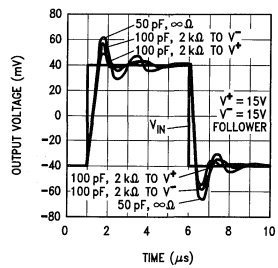
Output Impedance vs Frequency and Gain



Small Signal Pulse Response vs Temp.



Small-Signal Pulse Response vs Load



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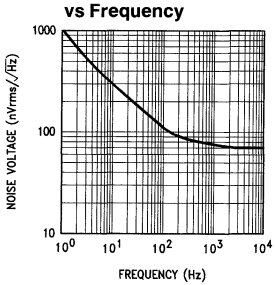
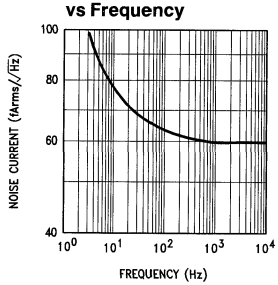
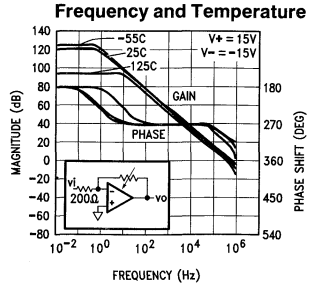
Op Amp Voltage Noise vs Frequency



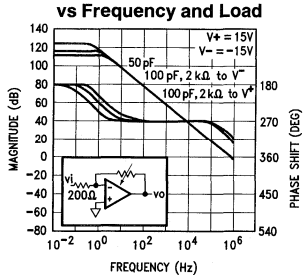
Op Amp Current Noise vs Frequency



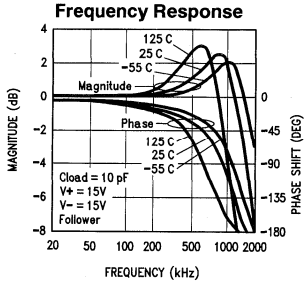
Small-Signal Voltage Gain vs Frequency and Temperature



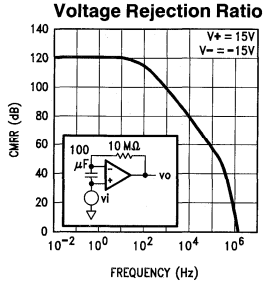
Small-Signal Voltage Gain vs Frequency and Load



Follower Small-Signal Frequency Response



Common-Mode Input Voltage Rejection Ratio



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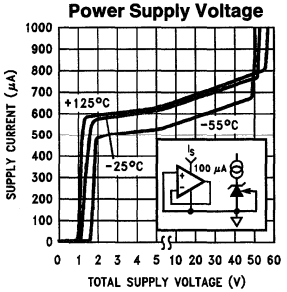
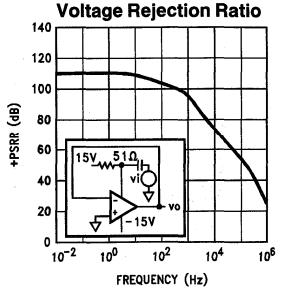
Typical Performance Characteristics (Op Amps) (Continued)

$V^+ = 5V$, V^- Q GND $= 0V$, $V_{CM} = V^+/2$, $V_{OUT} = V^+/2$, $T_J = 25°C$, unless otherwise noted

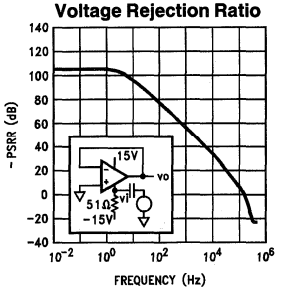
Power Supply Current vs Power Supply Voltage



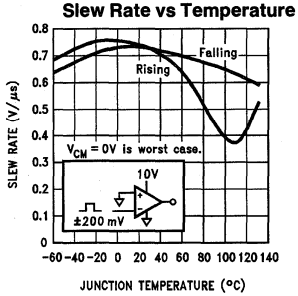
Positive Power Supply Voltage Rejection Ratio



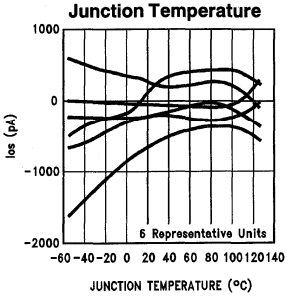
Negative Power Supply Voltage Rejection Ratio



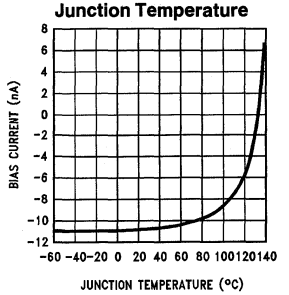
Slew Rate vs Temperature



Input Offset Current vs Junction Temperature



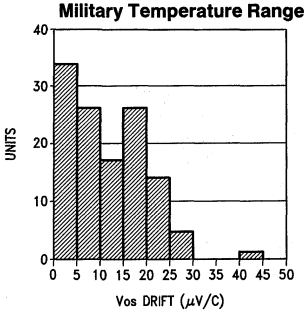
Input Bias Current vs Junction Temperature



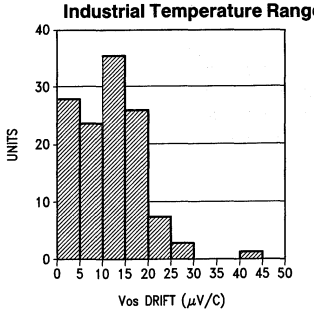
TL/H/9221–11

Typical Performance Distributions

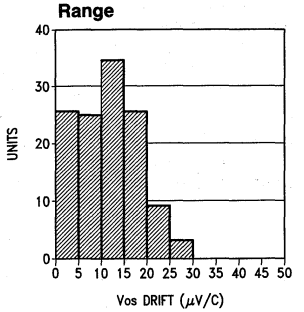
Average V_{OS} Drift Military Temperature Range



Average V_{OS} Drift Industrial Temperature Range



Average V_{OS} Drift Commercial Temperature Range



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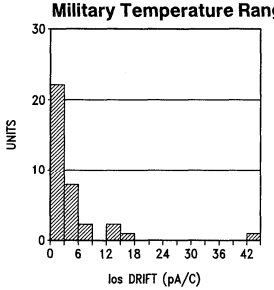
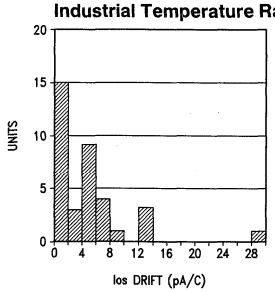
Typical Performance Distributions (Continued)

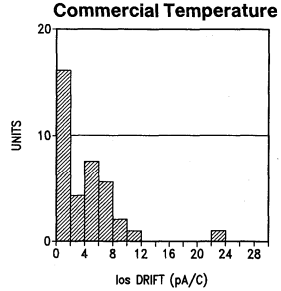
Average I_{OS} Drift Military Temperature Range



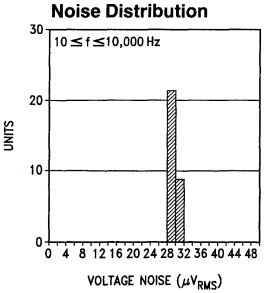
Average I_{OS} Drift Industrial Temperature Range



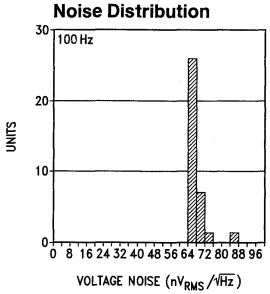
Average I_{OS} Drift Commercial Temperature Range



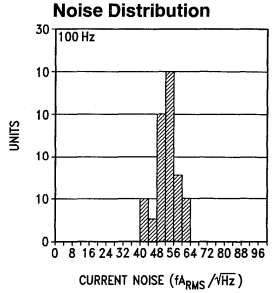
Voltage Reference Broad-Band Noise Distribution



Op Amp Voltage Noise Distribution



Op Amp Current Noise Distribution



TL/H/9221–13

Application Information

VOLTAGE REFERENCE

Reference Biasing

The voltage reference is of a shunt regulator topology that models as a simple zener diode. With current I_r flowing in the 'forward' direction there is the familiar diode transfer function. I_r flowing in the reverse direction forces the reference voltage to be developed from cathode to anode. The applied voltage to the cathode may range from a diode drop below V^- to the reference voltage or to the avalanche voltage of the parallel protection diode, nominally 7V. A 6.3V reference with $V^+ = 3V$ is allowed.

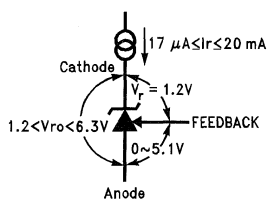


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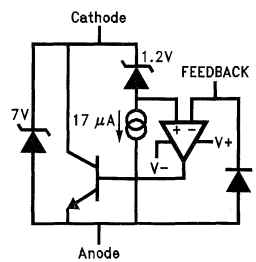
FIGURE 1. Voltages Associated with Reference (Current Source I_r is External)

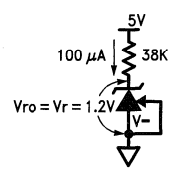
The reference equivalent circuit reveals how V_r is held at the constant 1.2V by feedback, and how the FEEDBACK pin passes little current.

To generate the required reverse current, typically a resistor is connected from a supply voltage higher than the reference voltage. Varying that voltage, and so varying I_r, has small effect with the equivalent series resistance of less than an ohm at the higher currents. Alternatively, an active current source, such as the LM134 series, may generate I_r.



TL/H/9221–15

FIGURE 2. Reference Equivalent Circuit



TL/H/9221–16

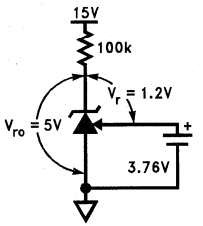
FIGURE 3. 1.2V Reference

Application Information (Continued)

Capacitors in parallel with the reference are allowed. See the Reference AC Stability Range curve for capacitance values—from 20 μA to 3 mA any capacitor value is stable. With the reference's wide stability range with resistive and capacitive loads, a wide range of RC filter values will perform noise filtering.

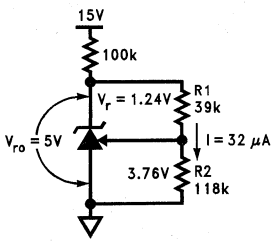
Adjustable Reference

The FEEDBACK pin allows the reference output voltage, V_{ro}, to vary from 1.24V to 6.3V. The reference attempts to hold V_r at 1.24V. If V_r is above 1.24V, the reference will conduct current from Cathode to Anode; FEEDBACK current always remains low. If FEEDBACK is connected to Anode, then $V_{ro} = V_r = 1.24V$. For higher voltages FEEDBACK is held at a constant voltage above Anode—say 3.76V for $V_{ro} = 5V$. Connecting a resistor across the constant V_r generates a current $I = R1/V_r$ flowing from Cathode into FEEDBACK node. A Thevenin equivalent 3.76V is generated from FEEDBACK to Anode with $R2 = 3.76/I$. Keep I greater than one thousand times larger than FEEDBACK bias current for <0.1% error—I≥32 μA for the military grade over the military temperature range (I≥5.5 μA for a 1% untrimmed error for a commercial part.)



TL/H/9221–17

FIGURE 4. Thevenin Equivalent of Reference with 5V Output



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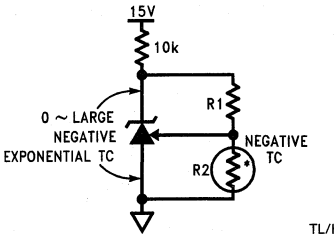
$$R1 = Vr/I = 1.24/32\mu = 39k$$

$$R2 = R1\{(Vro/Vr) - 1\} = 39k\{(5/1.24) - 1)\} = 118k$$

FIGURE 5. Resistors R1 and R2 Program Reference Output Voltage to be 5V

Understanding that V_r is fixed and that voltage sources, resistors, and capacitors may be tied to the FEEDBACK pin, a range of V_r temperature coefficients may be synthesized.



TL/H/9221–19

FIGURE 6. Output Voltage has Negative Temperature Coefficient (TC) if R2 has Negative TC

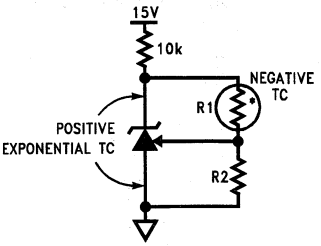


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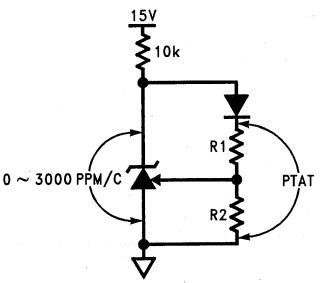
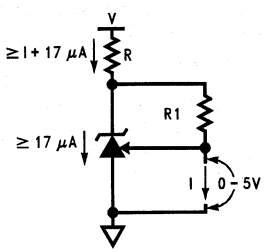
FIGURE 7. Output Voltage has Positive TC if R1 has Negative TC



TL/H/9221–21

FIGURE 8. Diode in Series with R1 Causes Voltage Across R1 and R2 to be Proportional to Absolute Temperature (PTAT)

Connecting a resistor across Cathode-to-FEEDBACK creates a 0 TC current source, but a range of TCs may be synthesized.

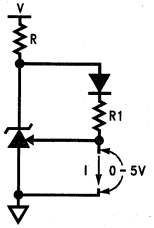


TL/H/9221–22

$$I = Vr/R1 = 1.24/R1$$

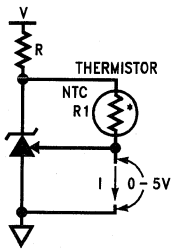
FIGURE 9. Current Source is Programmed by R1

Application Information (Continued)



TL/H/9221–23

FIGURE 10. Proportional-to-Absolute-Temperature Current Source



TL/H/9221–24

FIGURE 11. Negative −TC Current Source

Hysteresis

The reference voltage depends, slightly, on the thermal history of the die. Competitive micro-power products vary—always check the data sheet for any given device. Do not assume that no specification means no hysteresis.

OPERATIONAL AMPLIFIER

The amp or the reference may be biased in any way with no effect on the other, except when a substrate diode conducts (see Guaranteed Electrical Characteristics Note 1). The amp may have inputs outside the common-mode range, may be operated as a comparator, or have all terminals floating with no effect on the reference (tying inverting input to output and non-inverting input to V^- on unused amp is preferred). Choosing operating points that cause oscillation, such as driving too large a capacitive load, is best avoided.

Op Amp Output Stage

The op amp, like the LM124 series, has a flexible and relatively wide-swing output stage. There are simple rules to optimize output swing, reduce cross-over distortion, and optimize capacitive drive capability:

1) Output Swing: Unloaded, the 42 μA pull-down will bring the output within 300 mV of V^- over the military temperature range. If more than 42 μA is required, a resistor from output to V^- will help. Swing across any load may be improved slightly if the load can be tied to V^+, at the cost of poorer sinking open-loop voltage gain.

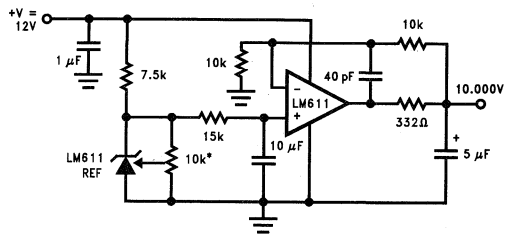
2) Cross-over Distortion: The LM611 has lower cross-over distortion (a 1 V_{BE} deadband versus 3 V_{BE} for the LM124), and increased slew rate as shown in the characteristic curves. A resistor pull-up or pull-down will force class-A operation with only the PNP or NPN output transistor conducting, eliminating cross-over distortion.

3) Capacitive Drive: Limited by the output pole caused by the output resistance driving capacitive loads, a pull-down resistor conducting 1 mA or more reduces the output stage NPN r_e until the output resistance is that of the current limit 25Ω. 200 pF may then be driven without oscillation.

Op Amp Input Stage

The lateral PNP input transistors, unlike those of most op amps, have BV_{EBO} equal to the absolute maximum supply voltage. Also, they have no diode clamps to the positive supply nor across the inputs. These features make the inputs look like high impedances to input sources producing large differential and common-mode voltages.

Typical Applications



*10k must be low t.c. trim pot.

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FIGURE 12. Ultra Low Noise 10.00V Reference. Total Output Noise is Typically 14 μV_{RMS}. Adjust the 10k pot for 10.000V.

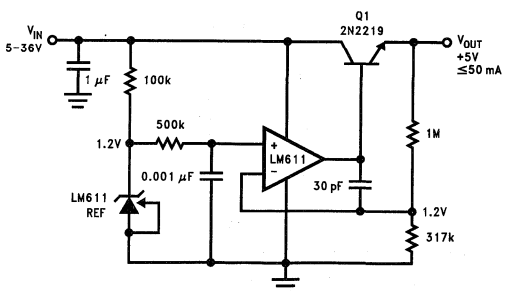

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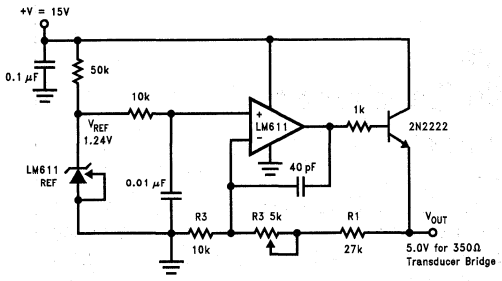
FIGURE 13. Simple Low Quiescent Drain Voltage Regulator. Total Supply Current is approximately 320 μA when V_{IN} = 5V, and output has no load.

Typical Applications (Continued)



$V_{OUT} = (R1/R2 + 1)\ V_{REF}$.
R1, R2 should be 1% metal film.
R3 should be low t.c. trim pot.

FIGURE 14. Slow Rise-Time Upon Power-Up, Adjustable Transducer Bridge Driver. Rise-time is approximately 0.5 ms.

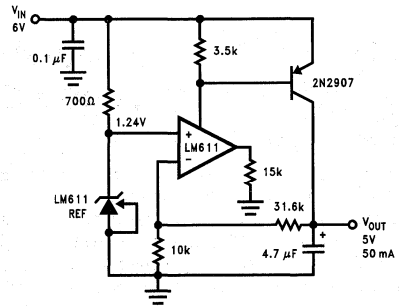


FIGURE 15. Low Drop-Out Voltage Regulator Circuit. Drop out voltage is typically 0.2V.

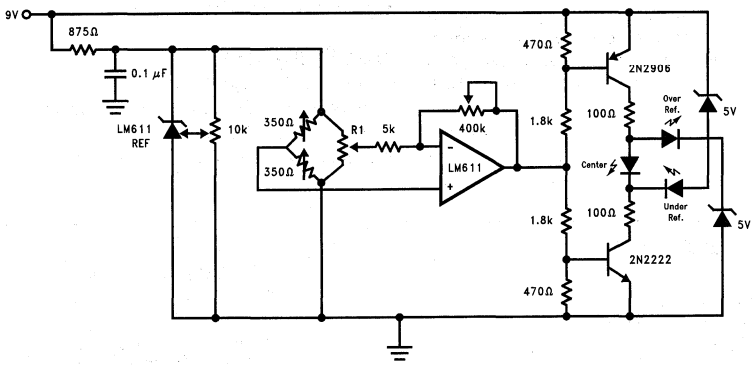


FIGURE 16. Nulling Bridge Detection System. Adjust sensitivity via 400 kΩ pot. Null offset with R1, and bridge drive with the 10k pot.

National Semiconductor

LM613 Dual Operational Amplifiers, Dual Comparators, and Adjustable Reference

General Description

The LM613 consists of dual op-amps, dual comparators, and a programmable voltage reference in a 16-pin package. The op-amps out-performs most single-supply op-amps by providing higher speed and bandwidth along with low supply current. This device was specifically designed to lower cost and board space requirements in transducer, test, measurement, and data acquisition systems.

Combining a stable voltage reference with wide output swing op-amps makes the LM613 ideal for single supply transducers, signal conditioning and bridge driving where large common-mode-signals are common. The voltage reference consists of a reliable band-gap design that maintains low dynamic output impedance (1Ω typical), excellent initial tolerance (0.6%), and the ability to be programmed from 1.2V to 6.3V via two external resistors. The voltage reference is very stable even when driving large capacitive loads, as are commonly encountered in CMOS data acquisition systems.

As a member of National's Super-Block™ family, the LM613 is a space-saving monolithic alternative to a multichip solution, offering a high level of integration without sacrificing performance.

Features

OP AMP

- Low operating current (Op Amp) 300 μA
- Wide supply voltage range 4V to 36V
- Wide common-mode range V^- to (V^+ − 1.8V)
- Wide differential input voltage ±36V
- Available in plastic package rated for Military Temp. Range Operation

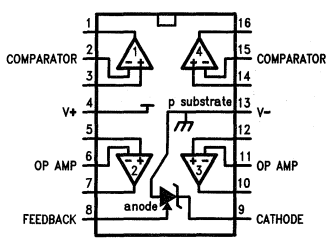
REFERENCE

- Adjustable output voltage 1.2V to 6.3V
- Tight initial tolerance available ±0.6%
- Wide operating current range 17 μA to 20 mA
- Tolerant of load capacitance

Applications

- Transducer bridge driver
- Process and mass flow control systems
- Power supply voltage monitor
- Buffered voltage references for A/D's

Connection Diagrams



Top View

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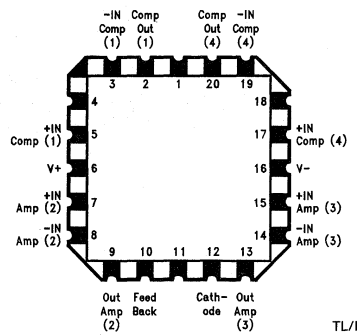
E Package Pinout



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Ordering Information

Reference Tolerance & V_{OS}	Temperature Range			Package	NSC Drawing
	Military $-55°C \le T_A \le +125°C$	Industrial $-40°C \le T_A \le +85°C$	Commercial $0°C \le T_A \le +70°C$		
±0.6% 80 ppm/°C Max. $V_{OS} \le 3.5$ mV	LM613AMN	LM613AIN	—	16-Pin Molded DIP	N16E
	LM613AMJ/883 (Note 14)	—	—	16-Pin Ceramic DIP	J16A
	LM613AME/883 (Note 14)	—	—	20-Pin LCC	E20A
±2.0% 150 ppm/°C Max. $V_{OS} \le 5.0$ mV Max.	LM613MN	LM613IN	LM613CN	16-Pin Molded DIP	N16E
	—	LM613IWM		16-Pin Wide Surface Mount	M16B

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Voltage on Any Pin Except V_R (referred to V^- pin)
(Note 2) 36V (Max)
(Note 3) −0.3V (Min)

Current through Any Input Pin & V_R Pin ±20 mA

Differential Input Voltage
Military and Industrial ±36V
Commercial ±32V

Storage Temperature Range $-65°C \le T_J \le +150°C$

Maximum Junction Temperature (Note 4) 150°C

Thermal Resistance, Junction-to-Ambient (Note 5)
N Package 100°C/W
WM Package 150°C/W

Soldering Information (10 Seconds)
N Package 260°C
WM Package 220°C

ESD Tolerance (Note 6) ±1 kV

Operating Temperature Range

LM613AI, LM613BI $-40°C$ to $+85°C$
LM613AM, LM613M $-55°C$ to $+125°C$
LM613C $0°C \le T_J \le +70°C$

Electrical Characteristics

These specifications apply for $V^- = GND = 0V$, $V^+ = 5V$, $V_{CM} = V_{OUT} = 2.5V$, $I_R = 100\ \mu A$, FEEDBACK pin shorted to GND, unless otherwise specified. Limits in standard typeface are for $T_J = 25°C$; limits in **boldface type** apply over the **Operating Temperature Range**.

Symbol	Parameter	Conditions	Typical (Note 7)	LM613AM LM613AI Limits (Note 8)	LM613M LM613I LM613C Limits (Note 8)	Units
I_S	Total Supply Current	$R_{LOAD} = \infty$, $4V \le V^+ \le 36V$ (32V for LM613C)	450 **550**	940 **1000**	1000 **1070**	µA (Max) µA (Max)
V_S	Supply Voltage Range		2.2 **2.9**	2.8 **3**	2.8 **3**	V (Min) V (Min)
			46 **43**	36 **36**	32 **32**	V (Max) V (Max)
OPERATIONAL AMPLIFIERS						
V_{OS1}	V_{OS} Over Supply	$4V \le V^+ \le 36V$ ($4V \le V^+ \le 32V$ for LM613C)	1.5 **2.0**	3.5 **6.0**	5.0 **7.0**	mV (Max) mV (Max)
V_{OS2}	V_{OS} Over V_{CM}	V_{CM} = 0V through V_{CM} = ($V^+ - 1.8V$), $V^+ = 30V$, $V^- = 0V$	1.0 **1.5**	3.5 **6.0**	5.0 **7.0**	mV (Max) mV (Max)
$\frac{V_{OS3}}{\Delta T}$	Average V_{OS} Drift	(Note 8)	**15**			µV/°C (Max)
I_B	Input Bias Current		10 **11**	25 **30**	35 **40**	nA (Max) nA (Max)
I_{OS}	Input Offset Current		0.2 **0.3**	4 **5**	4 **5**	nA (Max) nA (Max)
$\frac{I_{OS1}}{\Delta T}$	Average Offset Current		**4**			pA/°C
R_{IN}	Input Resistance	Differential	1000			MΩ
C_{IN}	Input Capacitance	Common-Mode	6			pF
e_n	Voltage Noise	f = 100 Hz, Input Referred	74			$nV/\sqrt{Hz}$
I_n	Current Noise	f = 100 Hz, Input Referred	58			$fA/\sqrt{Hz}$
CMRR	Common-Mode Rejection Ratio	$V^+ = 30V$, $0V \le V_{CM} \le (V^+ - 1.8V)$ $CMRR = 20 \log (\Delta V_{CM}/\Delta V_{OS})$	95 **90**	80 **75**	75 **70**	dB (Min) dB (Min)
PSRR	Power Supply Rejection Ratio	$4V \le V^+ \le 30V$, $V_{CM} = V^+/2$, $PSRR = 20 \log (\Delta V^+/V_{OS})$	110 **100**	80 **75**	75 **70**	dB (Min) dB (Min)
A_V	Open Loop Voltage Gain	$R_L = 10\ k\Omega$ to GND, $V^+ = 30V$, $5V \le V_{OUT} \le 25V$	500 **50**	100 **40**	94 **40**	V/mV (Min)

Electrical Characteristics These specifications apply for V^- = GND = 0V, V^+ = 5V, V_{CM} = V_{OUT} = 2.5V, I_R = 100 μA, FEEDBACK pin shorted to GND, unless otherwise specified. Limits in standard typeface are for T_J = 25°C; limits in **boldface type** apply over **Operating Temperature Range**. (Continued)

Symbol	Parameter	Conditions	Typical (Note 7)	LM613AM LM613AI Limits (Note 8)	LM613M LM613I LM613C Limits (Note 8)	Units
OPERATIONAL AMPLIFIERS (Continued)						
SR	Slew Rate	V^+ = 30V (Note 9)	0.70 **0.65**	0.55 **0.45**	0.50 **0.45**	V/μs
GBW	Gain Bandwidth	C_L = 50 pF	0.8 **0.5**			MHz MHz
V_{O1}	Output Voltage Swing High	R_L = 10 kΩ to GND, V^+ = 36V (32V for LM613C)	$V^+ - 1.4$ **$V^+ - 1.6$**	$V^+ - 1.7$ **$V^+ - 1.9$**	$V^+ - 1.8$ **$V^+ - 1.9$**	V (Min) V (Min)
V_{O2}	Output Voltage Swing Low	R_L = 10 kΩ to V^+, V^+ = 36V (32V for LM613C)	$V^- + 0.8$ **$V^- + 0.9$**	$V^- + 0.9$ **$V^- + 1.0$**	$V^- + 0.95$ **$V^- + 1.0$**	V (Max) V (Max)
I_{OUT}	Output Source Current	V_{OUT} = 2.5V, V^+_{IN} = 0V, V^-_{IN} = −0.3V	25 **15**	20 **13**	16 **13**	mA (Min) mA (Min)
I_{SINK}	Output Sink Current	V_{OUT} = 1.6V, V^+_{IN} = 0V, V^-_{IN} = 0.3V	17 **9**	14 **8**	13 **8**	mA (Min) mA (Min)
I_{SHORT}	Short Circuit Current	V_{OUT} = 0V, V^+_{IN} = 3V, V^-_{IN} = 2V	30 **40**	50 **60**	50 **60**	mA (Max) mA (Max)
		V_{OUT} = 5V, V^+_{IN} = 2V, V^-_{IN} = 3V	30 **32**	60 **80**	70 **90**	mA (Max) mA (Max)
COMPARATORS						
V_{OS}	Offset Voltage	4V ≤ V^+ ≤ 36V (32V for LM613C), R_L = 15 kΩ	1.0 **2.0**	3.0 **6.0**	5.0 **7.0**	mV (Max) mV (Max)
$\frac{V_{OS}}{V_{CM}}$	Offset Voltage over V_{CM}	0V ≤ V_{CM} ≤ 36V V^+ = 36V, (32V for LM613C)	1.0 **1.5**	3.0 **6.0**	5.0 **7.0**	mV (Max) mV (Max)
$\frac{V_{OS}}{\Delta T}$	Average Offset Voltage Drift		**15**			μV/°C (Max)
I_B	Input Bias Current		5 **8**	25 **30**	35 **40**	nA (Max) nA (Max)
I_{OS}	Input Offset Current		0.2 **0.3**	4 **5**	4 **5**	nA (Max) nA (Max)
A_V	Voltage Gain	R_L = 10 kΩ to 36V (32V for LM613C) 2V ≤ V_{OUT} ≤ 27V	500 **100**			V/mV V/mV
t_r	Large Signal Response Time	V^+_{IN} = 1.4V, V^-_{IN} = TTL Swing, R_L = 5.1 kΩ	1.5 **2.0**			μs μs
I_{SINK}	Output Sink Current	V^+_{IN} = 0V, V^-_{IN} = 1V, V_{OUT} = 1.5V	20 **13**	10 **8**	10 **8**	mA (Min) mA (Min)
		V_{OUT} = 0.4V	2.8 **2.4**	1.0 **0.5**	0.8 **0.5**	mA (Min) mA (Min)
I_{LEAK}	Output Leakage Current	V^+_{IN} = 1V, V^-_{IN} = 0V, V_{OUT} = 36V (32V for LM613C)	0.1 **0.2**	10	10	μA (Max) μA (Max)

Electrical Characteristics These specifications apply for V^- = GND = 0V, V^+ = 5V, V_{CM} = V_{OUT} = 2.5V, I_R = 100 μA, FEEDBACK pin shorted to GND, unless otherwise specified. Limits in standard typeface are for T_J = 25°C; limits in **boldface type** apply over **Operating Temperature Range.** (Continued)

Symbol	Parameter	Conditions	Typical (Note 7)	LM613AM LM613AI Limits (Note 8)	LM613M LM613I LM613C Limits (Note 8)	Units
VOLTAGE REFERENCE						
V_R	Voltage Reference	(Note 10)	1.244	1.2365 1.2515 (±0.6%)	1.2191 1.2689 (±2%)	V (Min) V (Max)
$\frac{\Delta V_R}{\Delta T}$	Average Temp. Drift	(Note 11)	**10**	**80**	**150**	ppm/°C (Max)
$\frac{\Delta V_R}{\Delta T_J}$	Hysteresis	(Note 12)	**3.2**			μV/°C
$\frac{\Delta V_R}{\Delta I_R}$	V_R Change with Current	$V_{R(100\ \mu A)} - V_{R(17\ \mu A)}$	0.05 **0.1**	1 **1.1**	1 **1.1**	mV (Max) mV (Max)
		$V_{R(10\ mA)} - V_{R(100\ \mu A)}$ (Note 13)	1.5 **2.0**	5 **5.5**	5 **5.5**	mV (Max) mV (Max)
R	Resistance	$\Delta V_{R(10 \rightarrow 0.1\ mA)}/9.9\ mA$ $\Delta V_{R(100 \rightarrow 17\ \mu A)}/83\ \mu A$	**0.2** **0.6**	**0.56** **13**	**0.56** **13**	Ω (Max) Ω (Max)
$\frac{V_R}{\Delta V_{RO}}$	V_R Change with High V_{RO}	$V_{R(Vro = Vr)} - V_{R(Vro = 6.3V)}$ (5.06V between Anode and FEEDBACK)	2.5 **2.8**	7 **10**	7 **10**	mV (Max) mV (Max)
$\frac{V_R}{\Delta V^+}$	V_R Change with V_{ANODE} Change	$V_{R(V^+ = 5V)} - V_{R(V^+ = 36V)}$ (V^+ = 32V for LM613C)	0.1 **0.1**	1.2 **1.3**	1.2 **1.3**	mV (Max) mV (Max)
		$V_{R(V^+ = 5V)} - V_{R(V^+ = 3V)}$	0.01 **0.01**	1 **1.5**	1 **1.5**	mV (Max) mV (Max)
I_{FB}	FEEDBACK Bias Current	$V_{ANODE} \leq V_{FB} \leq 5.06V$	22 **29**	35 **40**	50 **55**	nA (Max) nA (Max)
e_n	V_R Noise	10 Hz to 10 kHz, $V_{RO} = V_R$	30			μV_{RMS}

Note 1: Absolute maximum ratings indicate limits beyond which damage to the component may occur. Electrical specifications do not apply when operating the device beyond its rated operating conditions.

Note 2: Input voltage above V^+ is allowed. As long as one input pin voltage remains inside the common-mode range, the comparator will deliver the correct output.

Note 3: More accurately, it is excessive current flow, with resulting excess heating, that limits the voltages on all pins. When any pin is pulled a diode drop below V^-, a parasitic NPN transistor turns ON. No latch-up will occur as long as the current through that pin remains below the Maximum Rating. Operation is undefined and unpredictable when any parasitic diode or transistor is conducting.

Note 4: Simultaneous short-circuit of multiple comparators while using high supply voltages may force junction temperature above maximum, and thus should not be continuous.

Note 5: Junction temperature may be calculated using $T_J = T_A + P_D \theta_{JA}$. The given thermal resistance is worst-case for packages in sockets in still air. For packages soldered to copper-clad board with dissipation from one comparator or reference output transistor, nominal θ_{JA} is 90°C/W for the N package, and 135°C/W for the WM package.

Note 6: Human body model, 100 pF discharged through a 1.5 kΩ resistor.

Note 7: Typical values in standard typeface are for T_J = 25°C; values in **bold face type** apply for the full operating temperature range. These values represent the most likely parametric norm.

Note 8: All limits are guaranteed at room temperature (standard type face) or at operating temperature extremes **(bold type face).**

Note 9: Slew rate is measured with the op amp in a voltage follower configuration. For rising slew rate, the input voltage is driven from 5V to 25V, and the output voltage transition is sampled at 10V and @ 20V. For falling slew rate, the input voltage is driven from 25V to 5V, and the output voltage transition is sampled at 20V and 10V.

Note 10: V_R is the Cathode-to-feedback voltage, nominally 1.244V.

Note 11: Average reference drift is calculated from the measurement of the reference voltage at 25°C and at the temperature extremes. The drift, in ppm/°C, is $10^6 \bullet \Delta V_R / (V_{R[25°C]} \bullet \Delta T_J)$, where ΔV_R is the lowest value subtracted from the highest, $V_{R[25°C]}$ is the value at 25°C, and ΔT_J is the temperature range. This parameter is guaranteed by design and sample testing.

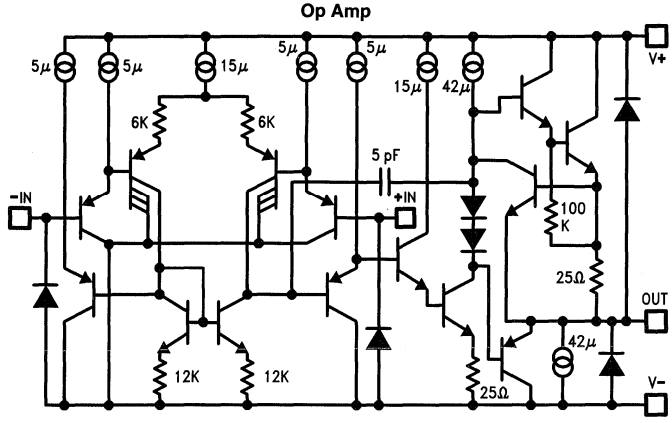
Note 12: Hysteresis is the change in V_R caused by a change in T_J, after the reference has been "dehysterized". To dehysterize the reference; that is minimize the hysteresis to the typical value, its junction temperature should be cycled in the following pattern, spiraling in toward 25°C: 25°C, 85°C, −40°C, 70°C, 0°C, 25°C.

Note 13: Low contact resistance is required for accurate measurement.

Note 14: A military RETS 613AMX electrical test specification is available on request. The Military screened parts can also be procured as a Standard Military Drawing.

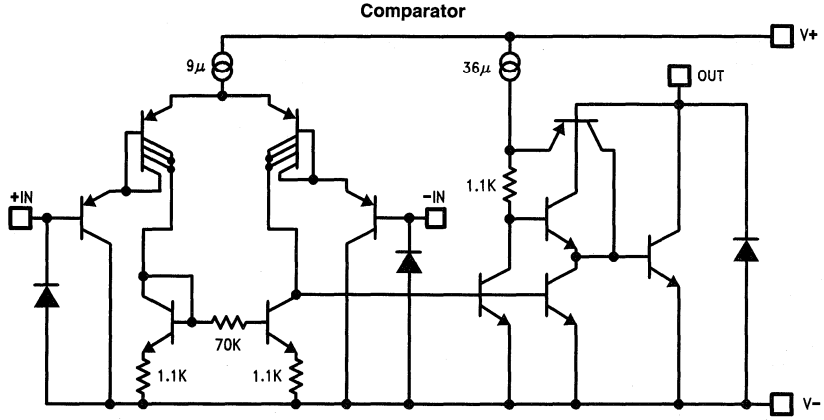
Simplified Schematic Diagrams

Op Amp



TL/H/9226-2

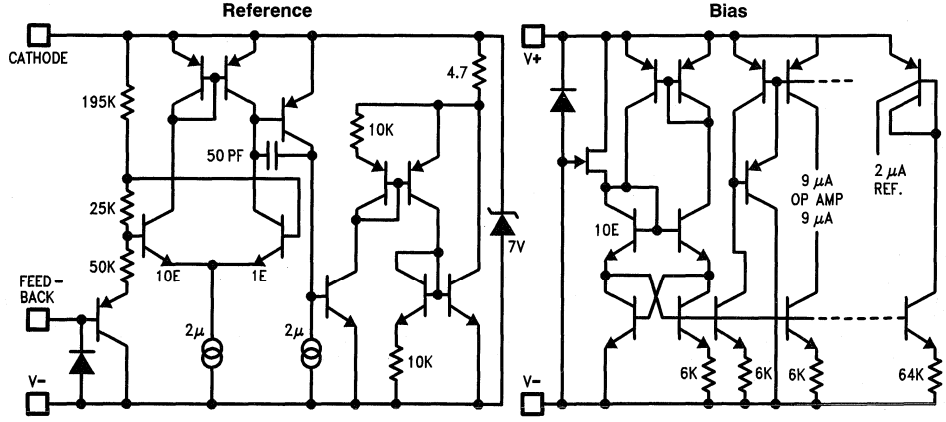
Comparator



TL/H/9226-3

Reference

Bias

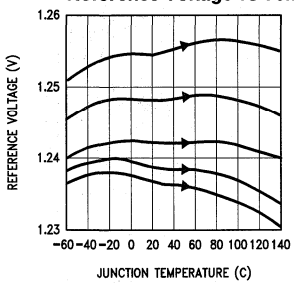


TL/H/9226-4

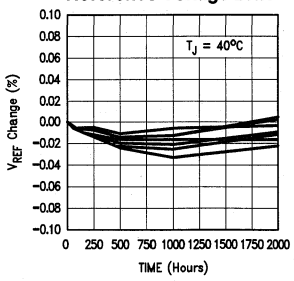
Typical Performance Characteristics (Reference)

T_J = 25°C, FEEDBACK pin shorted to V^- = 0V, unless otherwise noted

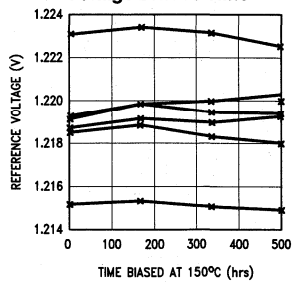
Reference Voltage vs Temp.



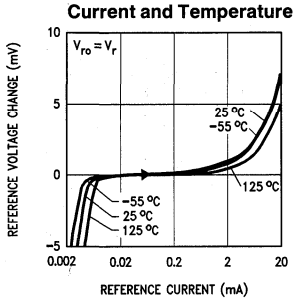
Reference Voltage Drift



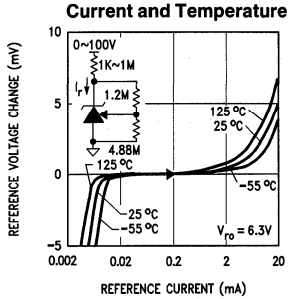
Accelerated Reference Voltage Drift vs Time



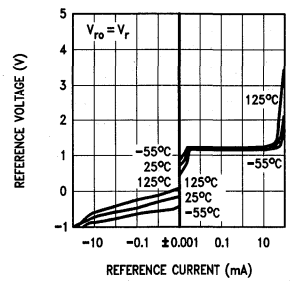
Reference Voltage vs Current and Temperature



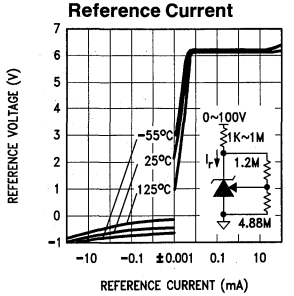
Reference Voltage vs Current and Temperature



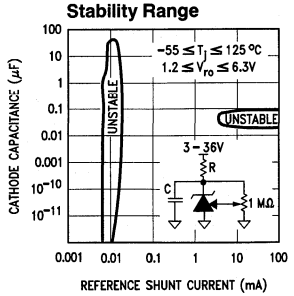
Reference Voltage vs Reference Current



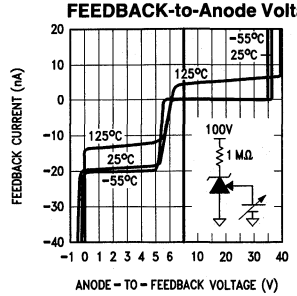
Reference Voltage vs Reference Current



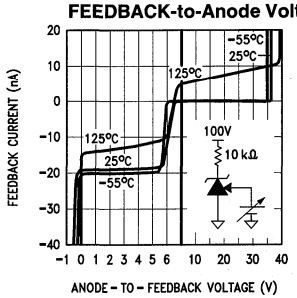
Reference AC Stability Range



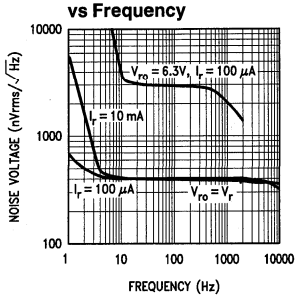
FEEDBACK Current vs FEEDBACK-to-Anode Voltage



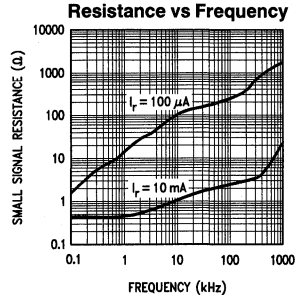
FEEDBACK Current vs FEEDBACK-to-Anode Voltage



Reference Noise Voltage vs Frequency



Reference Small-Signal Resistance vs Frequency

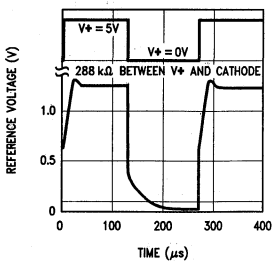


TL/H/9226–5

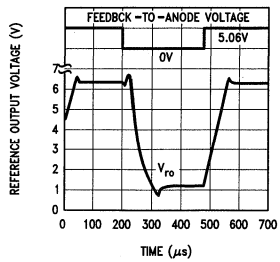
Typical Performance Characteristics (Reference) (Continued)

T_J = 25°C, FEEDBACK pin shorted to V^- = 0V, unless otherwise noted

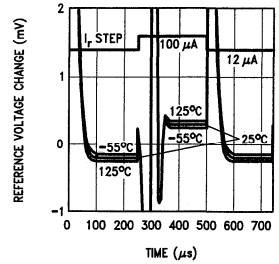
Reference Power-Up Time



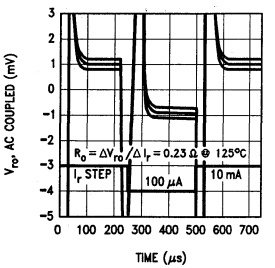
Reference Voltage with FEEDBACK Voltage Step



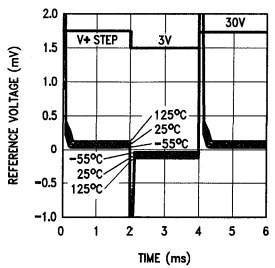
Reference Voltage with 100 ~ 12 μA Current Step



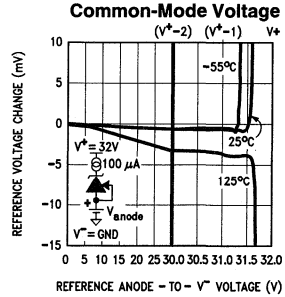
Reference Step Response for 100 μA ~ 10 mA Current Step



Reference Voltage Change with Supply Voltage Step



Reference Change vs Common-Mode Voltage

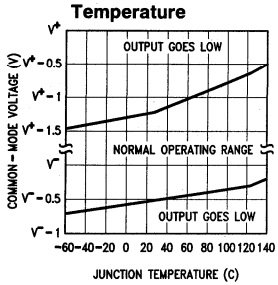


TL/H/9226–6

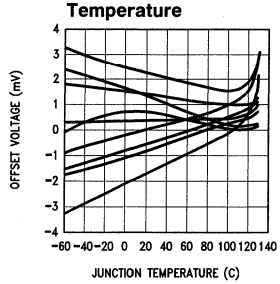
Typical Performance Characteristics (Op Amps)

V^+ = 5V, V^- = GND = 0V, V_{CM} = $V^+/2$, V_{OUT} = $V^+/2$, T_J = 25°C, unless otherwise noted

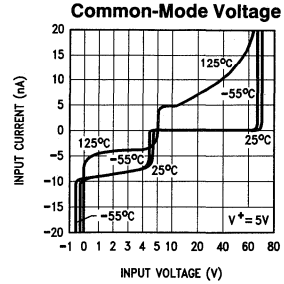
Input Common-Mode Voltage Range vs Temperature



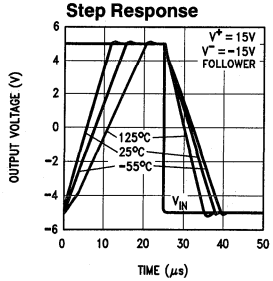
V_{OS} vs Junction Temperature



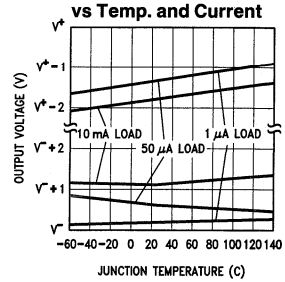
Input Bias Current vs Common-Mode Voltage



Large-Signal Step Response



Output Voltage Swing vs Temp. and Current

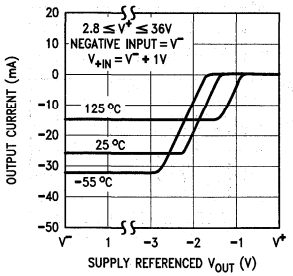


TL/H/9226–7

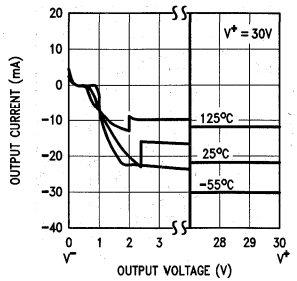
Typical Performance Characteristics (Op Amps) (Continued)

$V^+ = 5V$, $V^- = GND = 0V$, $V_{CM} = V^+/2$, $V_{OUT} = V^+/2$, $T_J = 25°C$, unless otherwise noted

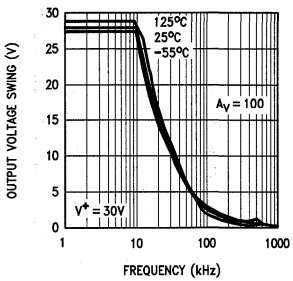
Output Source Current vs Output Voltage and Temp.



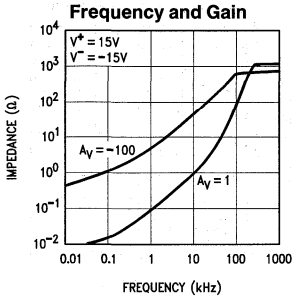
Output Sink Current vs Output Voltage



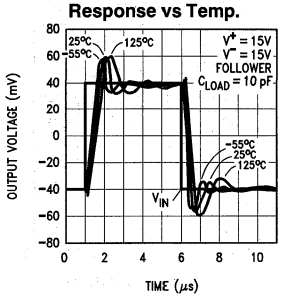
Output Swing, Large Signal



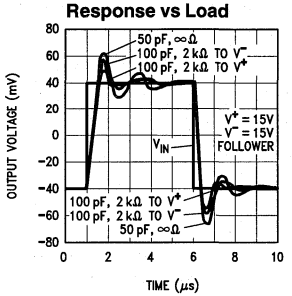
Output Impedance vs Frequency and Gain



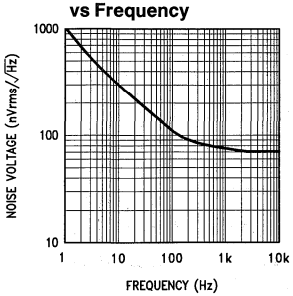
Small Signal Pulse Response vs Temp.



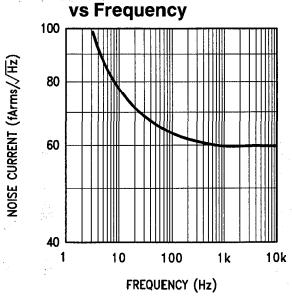
Small-Signal Pulse Response vs Load



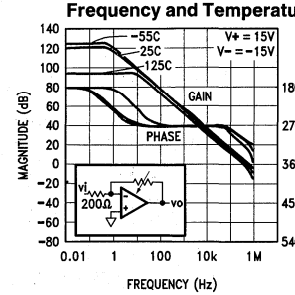
Op Amp Voltage Noise vs Frequency



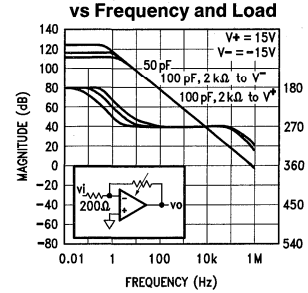
Op Amp Current Noise vs Frequency



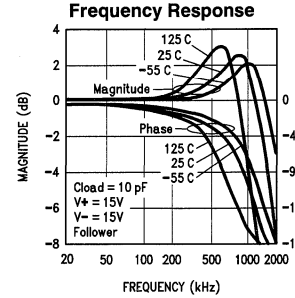
Small-Signal Voltage Gain vs Frequency and Temperature



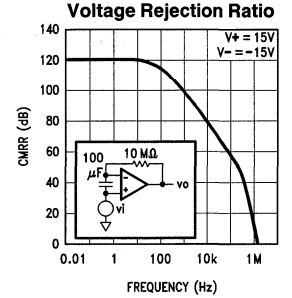
Small-Signal Voltage Gain vs Frequency and Load



Follower Small-Signal Frequency Response



Common-Mode Input Voltage Rejection Ratio

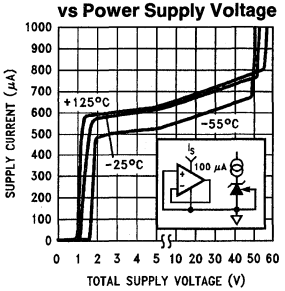


TL/H/9226–8

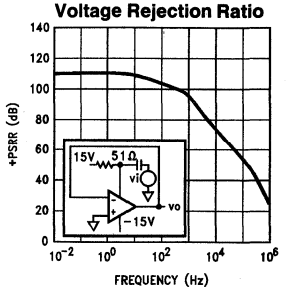
Typical Performance Characteristics (Op Amps) (Continued)

$V^+ = 5V$, $V^- = GND = 0V$, $V_{CM} = V^+/2$, $V_{OUT} = V^+/2$, $T_J = 25°C$, unless otherwise noted

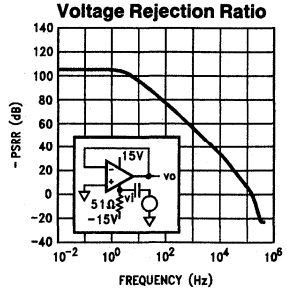
Power Supply Current vs Power Supply Voltage



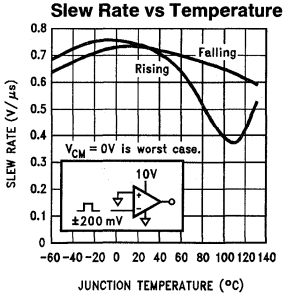
Positive Power Supply Voltage Rejection Ratio



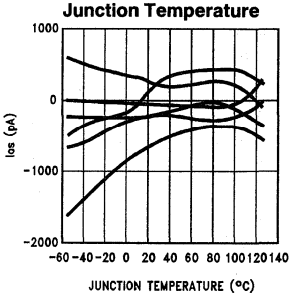
Negative Power Supply Voltage Rejection Ratio



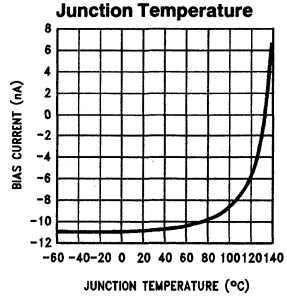
Slew Rate vs Temperature



Input Offset Current vs Junction Temperature



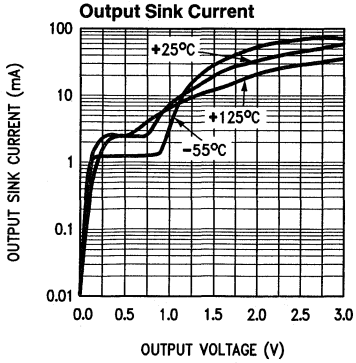
Input Bias Current vs Junction Temperature



TL/H/9226-9

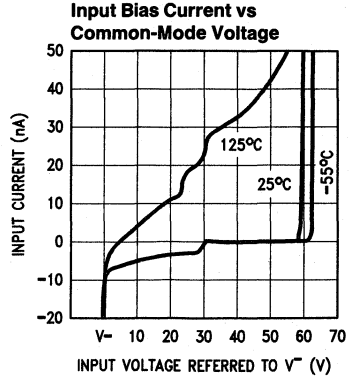
Typical Performance Characteristics (Comparators)

Output Sink Current



TL/H/9226-10

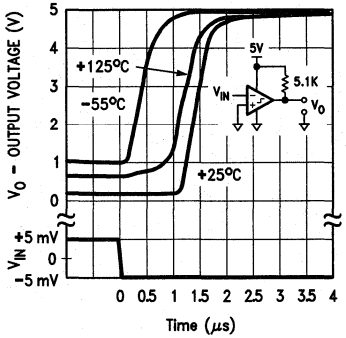
Input Bias Current vs Common-Mode Voltage



TL/H/9226-11

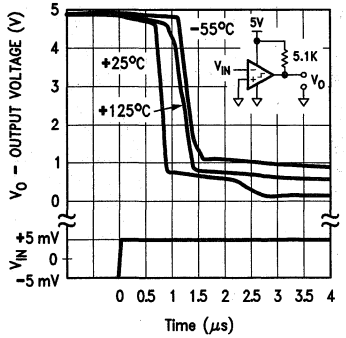
Typical Performance Characteristics (Comparators) (Continued)

Comparator Response Times—Inverting Input, Positive Transition



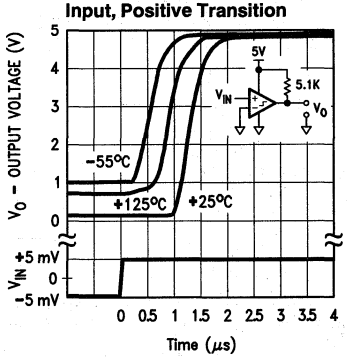
TL/H/9226–12

Comparator Response Times—Inverting Input, Negative Transition



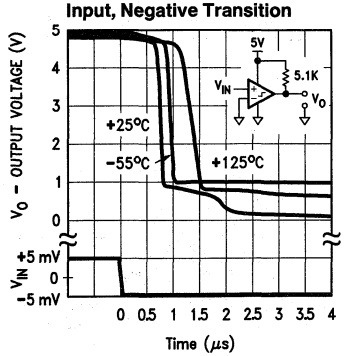
TL/H/9226–13

Comparator Response Times—Non-Inverting Input, Positive Transition



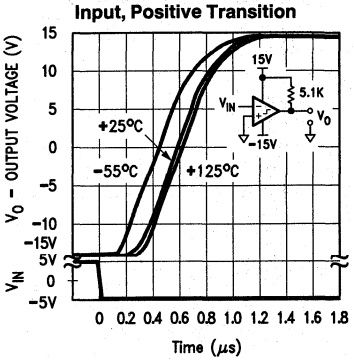
TL/H/9226–14

Comparator Response Times—Non-Inverting Input, Negative Transition



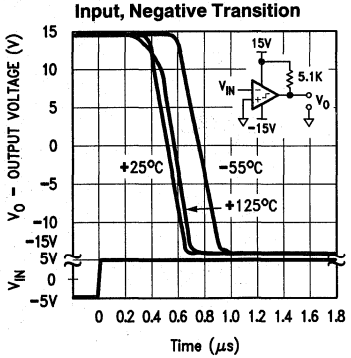
TL/H/9226–15

Comparator Response Times—Inverting Input, Positive Transition



TL/H/9226–16

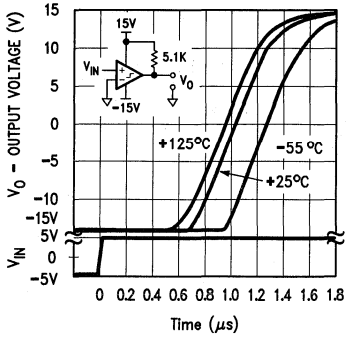
Comparator Response Times—Inverting Input, Negative Transition



TL/H/9226–17

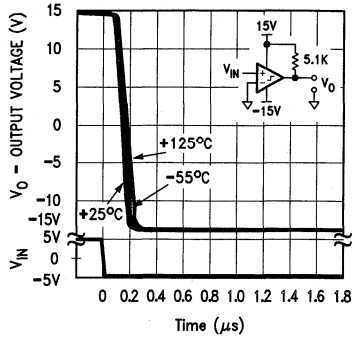
Typical Performance Characteristics (Comparators) (Continued)

Comparator Response Times—Non-Inverting Input, Positive Transition



TL/H/9226–18

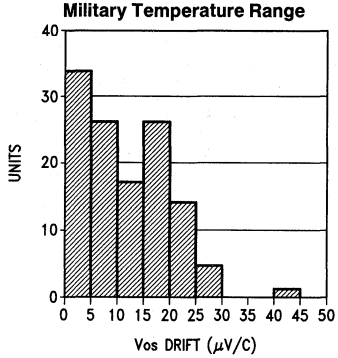
Comparator Response Times—Non-Inverting Input, Negative Transition



TL/H/9226–19

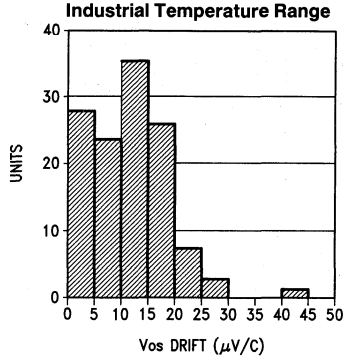
Typical Performance Distributions

Average V_{OS} Drift Military Temperature Range



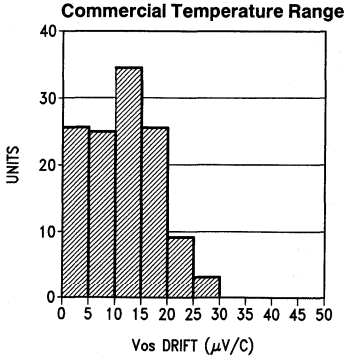
TL/H/9226–20

Average V_{OS} Drift Industrial Temperature Range



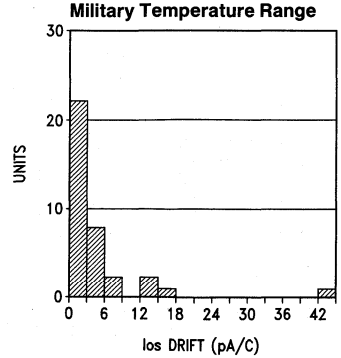
TL/H/9226–21

Average V_{OS} Drift Commercial Temperature Range



TL/H/9226–22

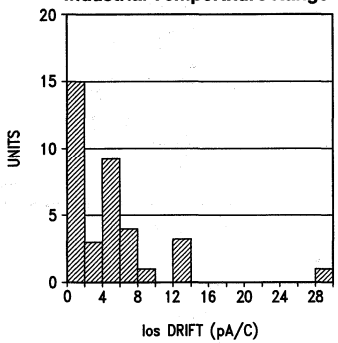
Average I_{OS} Drift Military Temperature Range



TL/H/9226–23

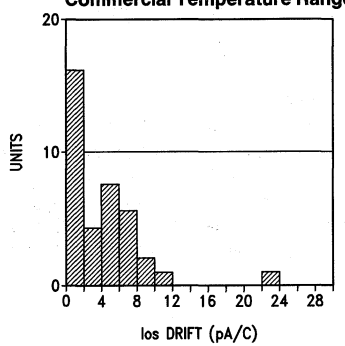
Typical Performance Distributions (Continued)

Average I_{OS} Drift Industrial Temperature Range



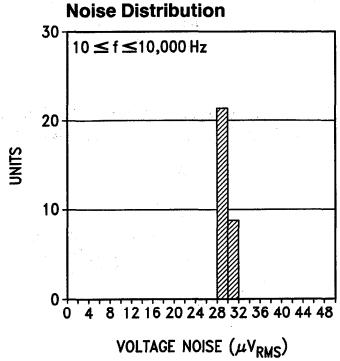
TL/H/9226-24

Average I_{OS} Drift Commercial Temperature Range



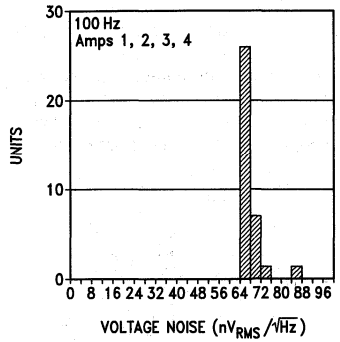
TL/H/9226-25

Voltage Reference Broad-Band Noise Distribution



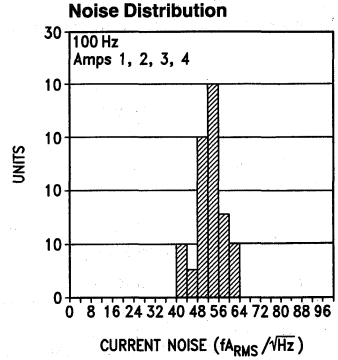
TL/H/9226-26

Op Amp Voltage Noise Distribution



TL/H/9226-27

Op Amp Current Noise Distribution



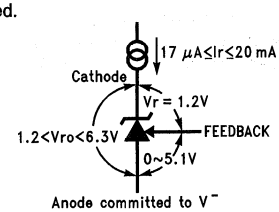
TL/H/9226-28

Application Information

VOLTAGE REFERENCE

Reference Biasing

The voltage reference is of a shunt regulator topology that models as a simple zener diode. With current I_r flowing in the "forward" direction there is the familiar diode transfer function. I_r flowing in the reverse direction forces the reference voltage to be developed from cathode to anode. The cathode may swing from a diode drop below V^- to the reference voltage or to the avalanche voltage of the parallel protection diode, nominally 7V. A 6.3V reference with $V^+ = 3V$ is allowed.



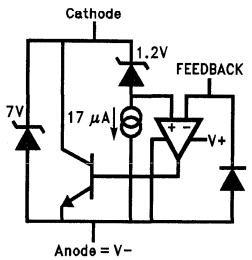
TL/H/9226-29

FIGURE 1. Voltage Associated with Reference (current source I_r is external)

Application Information (Continued)

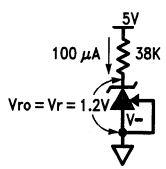
The reference equivalent circuit reveals how V_r is held at the constant 1.2V by feedback, and how the FEEDBACK pin passes little current.

To generate the required reverse current, typically a resistor is connected from a supply voltage higher than the reference voltage. Varying that voltage, and so varying I_r, has small effect with the equivalent series resistance of less than an ohm at the higher currents. Alternatively, an active current source, such as the LM134 series, may generate I_r.



TL/H/9226–30

FIGURE 2. Reference Equivalent Circuit



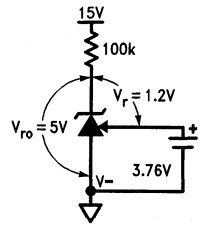
TL/H/9226–31

FIGURE 3. 1.2V Reference

Capacitors in parallel with the reference are allowed. See the Reference AC Stability Range typical curve for capacitance values—from 20 μA to 3 mA any capacitor value is stable. With the reference's wide stability range with resistive and capacitive loads, a wide range of RC filter values will perform noise filtering.

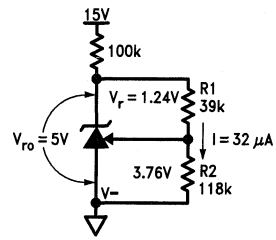
Adjustable Reference

The FEEDBACK pin allows the reference output voltage, V_{ro}, to vary from 1.24V to 6.3V. The reference attempts to hold V_r at 1.24V. If V_r is above 1.24V, the reference will conduct current from Cathode to Anode; FEEDBACK current always remains low. If FEEDBACK is connected to Anode, then $V_{ro} = V_r = 1.24V$. For higher voltages FEEDBACK is held at a constant voltage above Anode—say 3.76V for $V_{ro} = 5V$. Connecting a resistor across the constaint V_r generates a current $I = R1/V_r$ flowing from Cathode into FEEDBACK node. A Thevenin equivalent 3.76V is generated from FEEDBACK to Anode with $R2 = 3.76/I$. Keep I greater than one thousand times larger than FEEDBACK bias current for <0.1% error—$I \geq 32$ μA for the military grade over the military temperature range ($I \geq 5.5$ μA for a 1% untrimmed error for a commercial part).



TL/H/9226–32

FIGURE 4. Thevenin Equivalent of Reference with 5V Output



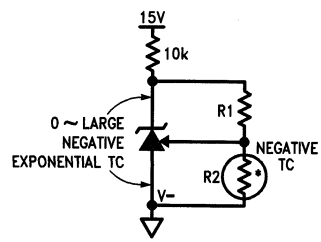
TL/H/9226–33

$R1 = Vr/I = 1.24/32\mu = 39k$

$R2 = R1\ \{(Vro/Vr) - 1\} = 39k\ \{(5/1.24) - 1)\} = 118k$

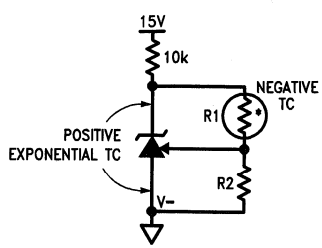
FIGURE 5. Resistors R1 and R2 Program Reference Output Voltage to be 5V

Understanding that V_r is fixed and that voltage sources, resistors, and capacitors may be tied to the FEEDBACK pin, a range of V_r temperature coefficients may be synthesized.



TL/H/9226–34

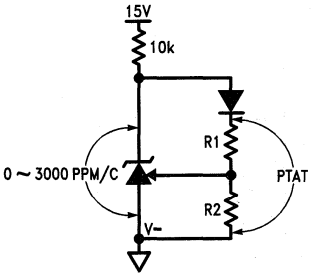
FIGURE 6. Output Voltage has Negative Temperature Coefficient (TC) if R2 has Negative TC



TL/H/9226–35

FIGURE 7. Output Voltage has Positive TC if R1 has Negative TC

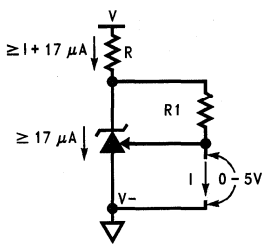
Application Information (Continued)



TL/H/9226-36

FIGURE 8. Diode in Series with R1 Causes Voltage Across R1 and R2 to be Proportional to Absolute Temperature (PTAT)

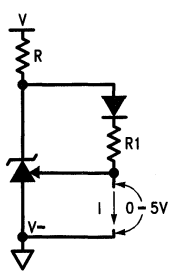
Connecting a resistor across Cathode-to-FEEDBACK creates a 0 TC current source, but a range of TCs may be synthesized.



TL/H/9226-37

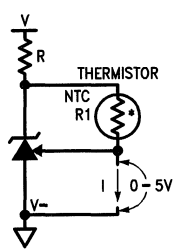
$I = Vr/R1 = 1.24/R1$

FIGURE 9. Current Source is Programmed by R1



TL/H/9226-38

FIGURE 10. Proportional-to-Absolute-Temperature Current Source



TL/H/9226-39

FIGURE 11. Negative-TC Current Source

Reference Hysteresis

The reference voltage depends, slightly, on the thermal history of the die. Competitive micro-power products vary—always check the data sheet for any given device. Do not assume that no specification means no hysteresis.

OPERATIONAL AMPLIFIERS AND COMPARATORS

Any amp, comparator, or the reference may be biased in any way with no effect on the other sections of the LM613, except when a substrate diode conducts (see Electrical Characteristics Note 1). For example, one amp input may be outside the common-mode range, another amp may be operating as a comparator, and all other sections may have all terminals floating with no effect on the others. Tying inverting input to output and non-inverting input to V^- on unused amps is preferred. Unused comparators should have non-inverting input and output tied to V^+, and inverting input tied to V^-. Choosing operating points that cause oscillation, such as driving too large a capacitive load, is best avoided.

Op Amp Output Stage

These op amps, like the LM124 series, have flexible and relatively wide-swing output stages. There are simple rules to optimize output swing, reduce cross-over distortion, and optimize capacitive drive capability:

1) Output Swing: Unloaded, the 42 μA pull-down will bring the output within 300 mV of V^- over the military temperature range. If more than 42 μA is required, a resistor from output to V^- will help. Swing across any load may be improved slightly if the load can be tied to V^+, at the cost of poorer sinking open-loop voltage gain.
2) Cross-Over Distortion: The LM613 has lower cross-over distortion (a 1 V_{BE} deadband versus 3 V_{BE} for the LM124), and increased slew rate as shown in the characteristic curves. A resistor pull-up or pull-down will force class-A operation with only the PNP or NPN output transistor conducting, eliminating cross-over distortion.
3) Capacitive Drive: Limited by the output pole caused by the output resistance driving capacitive loads, a pull-down resistor conducting 1 mA or more reduces the output stage NPN r_e until the output resistance is that of the current limit 25Ω. 200 pF may then be driven without oscillation.

Comparator Output Stage

The comparators, like the LM139 series, have open-collector output stages. A pull-up resistor must be added from each output pin to a positive voltage for the output transistor to switch properly. When the output transistor is OFF, the output voltage will be this external positive voltage.

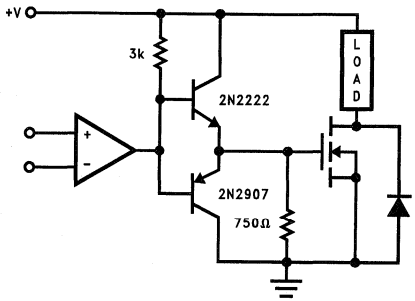
For the output voltage to be under the TTL-low voltage threshold when the output transistor is ON, the output current must be less than 8 mA (over temperature). This impacts the minimum value of pull-up resistor.

The offset voltage may increase when the output voltage is low and the output current is less than 30 μA. Thus, for best accuracy, the pull-up resistor value should be low enough to allow the output transistor to sink more than 30 μA.

Op Amp and Comparator Input Stage

The lateral PNP input transistors, unlike those of most op amps, have BV_{EBO} equal to the absolute maximum supply voltage. Also, they have no diode clamps to the positive supply nor across the inputs. These features make the inputs look like high impedances to input sources producing large differential and common-mode voltages.

Typical Applications



TL/H/9226–40

FIGURE 12. High Current, High Voltage Switch

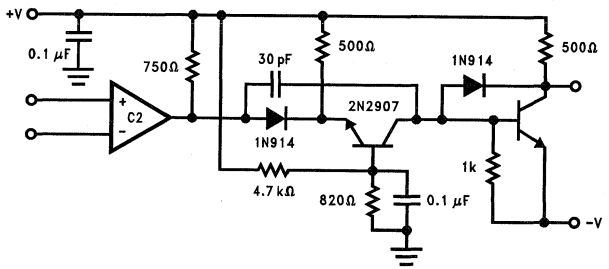


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FIGURE 13. High Speed Level Shifter. Response time is approximately 1.5 μs, where output is either approximately +V or −V.

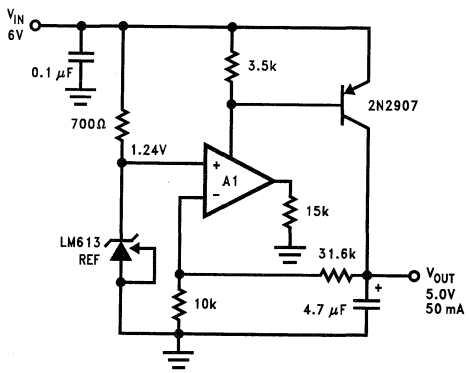

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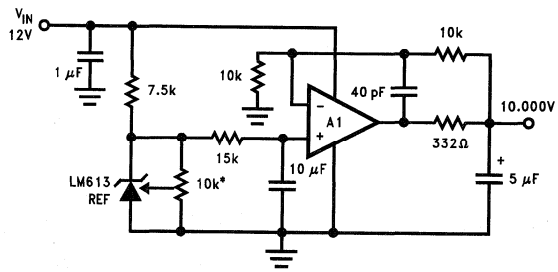
FIGURE 14. Low Voltage Regulator. Dropout voltage is approximately 0.2V.



*10k must be low t.c. trimpot

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FIGURE 15. Ultra Low Noise, 10.00V Reference. Total output noise is typically 14 μV_{RMS}.

Typical Applications (Continued)

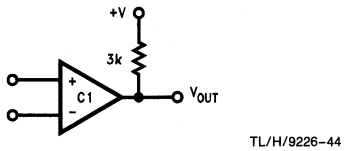

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FIGURE 16. Basic Comparator

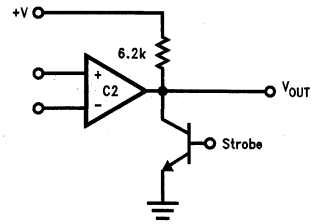

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FIGURE 17. Basic Comparator with External Strobe

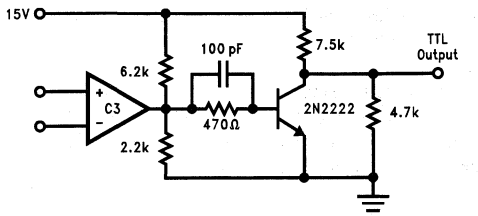

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FIGURE 18. Wide-Input Range Comparator with TTL Output

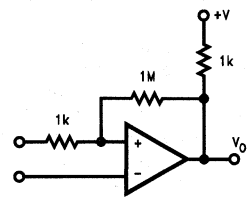

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FIGURE 19. Comparator with Hysteresis ($\Delta V_H = {}^{+}V(1k/1M)$)

National Semiconductor

LM614 Quad Operational Amplifier and Adjustable Reference

General Description

The LM614 consists of four op-amps and a programmable voltage reference in a 16-pin package. The op-amp out-performs most single-supply op-amps by providing higher speed and bandwidth along with low supply current. This device was specifically designed to lower cost and board space requirements in transducer, test, measurement and data acquisition systems.

Combining a stable voltage reference with four wide output swing op-amps makes the LM614 ideal for single supply transducers, signal conditioning and bridge driving where large common-mode-signals are common. The voltage reference consists of a reliable band-gap design that maintains low dynamic output impedance (1Ω typical), excellent initial tolerance (0.6%), and the ability to be programmed from 1.2V to 6.3V via two external resistors. The voltage reference is very stable even when driving large capacitive loads, as are commonly encountered in CMOS data acquisition systems.

As a member of National's new Super-Block™ family, the LM614 is a space-saving monolithic alternative to a multi-chip solution, offering a high level of integration without sacrificing performance.

Features

Op Amp

- Low operating current 300 μA
- Wide supply voltage range 4V to 36V
- Wide common-mode range V^- to ($V^+ - 1.8V$)
- Wide differential input voltage ±36V
- Available in plastic package rated for Military Temperature Range Operation

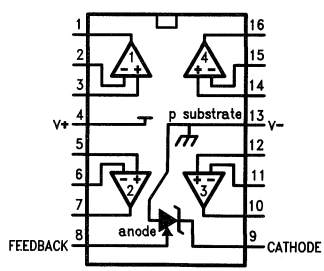
Reference

- Adjustable output voltage 1.2V to 6.3V
- Tight initial tolerance available ±0.6%
- Wide operating current range 17 μA to 20 mA
- Tolerant of load capacitance

Applications

- Transducer bridge driver and signal processing
- Process and mass flow control systems
- Power supply voltage monitor
- Buffered voltage references for A/D's

Connection Diagram



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Ordering Information

Reference Tolerance & V_{OS}	Temperature Range			Package	NSC Drawing
	Military $-55°C \le T_A \le +125°C$	Industrial $-40°C \le T_A \le +85°C$	Commercial $0°C \le T_A \le +70°C$		
±0.6%@ 80 ppm/°C max $V_{OS} \le 3.5$ mV max	LM614AMN	LM614AIN	—	16-pin Molded DIP	N16E
	LM614AMJ/883 (Note 13)	—	—	16-pin Ceramic DIP	J16A
±2.0%@ 150 ppm/°C max $V_{OS} \le 5.0$ mV	LM614MN	LM614BIN	LM614CN	16-pin Molded DIP	N16E
	—	LM614WM	LM614CWM	16-pin Wide Surface Mount	M16B

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Voltage on Any Pins except V_R (referred to V^- pin)
- (Note 2) 36V (Max)
- (Note 3) −0.3V (Min)

Current through Any Input Pin & V_R Pin ±20 mA

Differential Input Voltage
- Military and Industrial ±36V
- Commercial ±32V

Storage Temperature Range $-65°C \le T_J \le +150°C$

Maximum Junction Temperature 150°C

Thermal Resistance, Junction-to-Ambient (Note 4)
- N Package 100°C
- WM Package 150°C

Soldering Information (Soldering, 10 seconds)
- N Package 260°C
- WM Package 220°C

ESD Tolerance (Note 5) ±1kV

Operating Temperature Range

LM614AI, LM614I, LM614BI $-40°C \le T_J \le +85°C$
LM614AM, LM614M $-55°C \le T_J \le +125°C$
LM614C $0°C \le T_J \le +70°C$

Electrical Characteristics

These specifications apply for V^- = GND = 0V, V^+ = 5V, $V_{CM} = V_{OUT}$ = 2.5V, I_R = 100 μA, FEEDBACK pin shorted to GND, unless otherwise specified. Limits in standard typeface are for T_J = 25°C; limits in **boldface type** apply over the **Operating Temperature Range.**

Symbol	Parameter	Conditions	Typical (Note 6)	LM614AM LM614AI Limits (Note 7)	LM614M LM614BI LM614I LM614C Limits (Note 7)	Units
I_S	Total Supply Current	$R_{LOAD} = \infty$, $4V \le V^+ \le 36V$ (32V for LM614C)	450 **550**	940 **1000**	1000 **1070**	μA max μA max
V_S	Supply Voltage Range		2.2 **2.9**	2.8 **3**	2.8 **3**	V min V min
			46 **43**	36 **36**	32 **32**	V max V max
OPERATIONAL AMPLIFIER						
V_{OS1}	V_{OS} Over Supply	$4V \le V^+ \le 36V$ ($4V \le V^+ \le 32V$ for LM614C)	1.5 **2.0**	3.5 **6.0**	5.0 **7.0**	mV max mV max
V_{OS2}	V_{OS} Over V_{CM}	V_{CM} = 0V through V_{CM} = ($V^+ - 1.8V$), V^+ = 30V	1.0 **1.5**	3.5 **6.0**	5.0 **7.0**	mV max mV max
$\frac{V_{OS3}}{\Delta T}$	Average V_{OS} Drift	(Note 7)	**15**			μV/°C max
I_B	Input Bias Current		10 **11**	25 **30**	35 **40**	nA max nA max
I_{OS}	Input Offset Current		0.2 **0.3**	4 **5**	4 **5**	nA max nA max
$\frac{I_{OS1}}{\Delta T}$	Average Offset Drift Current		**4**			pA/°C
R_{IN}	Input Resistance	Differential	1800			MΩ
		Common-Mode	3800			MΩ
C_{IN}	Input Capacitance	Common-Mode Input	5.7			pF
e_n	Voltage Noise	f = 100 Hz, Input Referred	74			$nV/\sqrt{Hz}$
I_n	Current Noise	f = 100 Hz, Input Referred	58			$fA/\sqrt{Hz}$
CMRR	Common-Mode Rejection Ratio	V^+ = 30V, $0V \le V_{CM} \le (V^+ - 1.8V)$, CMRR = 20 log ($\Delta V_{CM}/\Delta V_{OS}$)	95 **90**	80 **75**	75 **70**	dB min dB min
PSRR	Power Supply Rejection Ratio	$4V \le V^+ \le 30V$, $V_{CM} = V^+/2$, PSRR = 20 log ($\Delta V^+/\Delta V_{OS}$)	110 **100**	80 **75**	75 **70**	dB min dB min
A_V	Open Loop Voltage Gain	R_L = 10 kΩ to GND, V^+ = 30V, $5V \le V_{OUT} \le 25V$	500 **50**	100 **40**	94 **40**	V/mV min

Electrical Characteristics (Continued)

These specifications apply for V^- = GND = 0V, V^+ = 5V, V_{CM} = V_{OUT} = 2.5V, I_R = 100 μA, FEEDBACK pin shorted to GND, unless otherwise specified. Limits in standard typeface are for T_J = 25°C; limits in **boldface type** apply over the **Operating Temperature Range.**

Symbol	Parameter	Conditions	Typical (Note 6)	LM614AM LM614AI Limits (Note 8)	LM614M LM614BI LM614I LM614C Limits (Note 8)	Units
SR	Slew Rate	V^+ = 30V (Note 8)	±0.70 **±0.65**	±0.55 **±0.45**	±0.50 **±0.45**	V/μs
GBW	Gain Bandwidth	C_L = 50 pF	0.8 **0.52**			MHz MHz
V_{O1}	Output Voltage Swing High	R_L = 10 kΩ to GND V^+ = 36V (32V for LM614C)	$V^+ - 1.4$ **$V^+ - 1.6$**	$V^+ - 1.7$ **$V^+ - 1.9$**	$V^+ - 1.8$ **$V^+ - 1.9$**	V min V min
V_{O2}	Output Voltage Swing Low	R_L = 10 kΩ to V^+ V^+ = 36V (32V for LM614C)	$V^- + 0.8$ **$V^- + 0.9$**	$V^- + 0.9$ **$V^- + 1.0$**	$V^- + 0.95$ **$V^- + 1.0$**	V max V max
I_{OUT}	Output Source	V_{OUT} = 2.5V, V_{+IN} = 0V, V_{-IN} = −0.3V	25 **15**	20 **13**	16 **13**	mA min mA min
I_{SINK}	Output Sink Current	V_{OUT} = 1.6V, V_{+IN} = 0V, V_{-IN} = 0.3V	17 **9**	14 **8**	13 **8**	mA min mA min
I_{SHORT}	Short Circuit Current	V_{OUT} = 0V, V_{+IN} = 3V, V_{-IN} = 2V, Source	30 **40**	50 **60**	50 **60**	mA max mA max
		V_{OUT} = 5V, V_{+IN} = 2V, V_{-IN} = 3V, Sink	30 **32**	60 **80**	70 **90**	mA max mA max
VOLTAGE REFERENCE						
V_R	Voltage Reference	(Note 9)	1.244	1.2365 1.2515 (±0.6%)	1.2191 1.2689 (±2.0%)	V min V max
$\frac{\Delta V_R}{\Delta T}$	Average Temperature Drift	(Note 10)	**10**	**80**	**150**	PPM/°C max
$\frac{\Delta V_R}{\Delta T_J}$	Hysteresis	(Note 11)	**3.2**			μV/°C
$\frac{\Delta V_R}{\Delta I_R}$	V_R Change with Current	$V_{R(100\ \mu A)} - V_{R(17\ \mu A)}$	0.05 **0.1**	1 **1.1**	1 **1.1**	mV max mV max
		$V_{R(10\ mA)} - V_{R(100\ \mu A)}$ (Note 12)	1.5 **2.0**	5 **5.5**	5 **5.5**	mV max mV max
R	Resistance	$\Delta V_{R(10 \rightarrow 0.1\ mA)}$/9.9 mA $\Delta V_{R(100 \rightarrow 17\ \mu A)}$/83 μA	**0.2** **0.6**	**0.56** **13**	**0.56** **13**	Ω max Ω max
$\frac{\Delta V_R}{\Delta V_{RO}}$	V_R Change with High V_{RO}	$V_{R(Vro\ =\ Vr)} - V_{R(Vro\ =\ 6.3V)}$ (5.06V between Anode and FEEDBACK)	2.5 **2.8**	7 **10**	7 **10**	mV max mV max
$\frac{\Delta V_R}{\Delta V^+}$	V_R Change with V^+ Change	$V_{R(V+\ =\ 5V)} - V_{R(V+\ =\ 36V)}$ (V^+ = 32V for LM614C)	0.1 **0.1**	1.2 **1.3**	1.2 **1.3**	mV max mV max
		$V_{R(V+\ =\ 5V)} - V_{R(V+\ =\ 3V)}$	0.01 **0.01**	1 **1.5**	1 **1.5**	mV max mV max
I_{FB}	FEEDBACK Bias Current	$V_{ANODE} \leq V_{FB} \leq$ 5.06V	22 **29**	35 **40**	50 **55**	nA max nA max
e_n	Voltage Noise	BW = 10 Hz to 10 kHz, $V_{RO} = V_R$	30			μV_{RMS}

Electrical Characteristics (Continued)

Note 1: Absolute maximum ratings indicate limits beyond which damage to the component may occur. Electrical specifications do not apply when operating the device beyond its rated operating conditions.

Note 2: Input voltage above V^+ is allowed.

Note 3: More accurately, it is excessive current flow, with resulting excess heating, that limits the voltages on all pins. When any pin is pulled a diode drop below V^-, a parasitic NPN transistor turns ON. No latch-up will occur as long as the current through that pin remains below the Maximum Rating. Operation is undefined and unpredictable when any parasitic diode or transistor is conducting.

Note 4: Junction temperature may be calculated using $T_J = T_A + P_D\theta_{jA}$. The given thermal resistance is worst-case for packages in sockets in still air. For packages soldered to copper-clad board with dissipation from one comparator or reference output transistor, nominal θ_{jA} are 90°C/W for the N package, WM package.

Note 5: Human body model, 100 pF discharged through a 1.5 kΩ resistor.

Note 6: Typical values in standard typeface are for $T_J = 25°C$; values in **boldface type** apply for the full operating temperature range. These values represent the most likely parametric norm.

Note 7: All limits are guaranteed at room temperature (standard type face) or at operating temperature extremes **(bold type face)**.

Note 8: Slew rate is measured with op amp in a voltage follower configuration. For rising slew rate, the input voltage is driven from 5V to 25V, and the output voltage transition is sampled at 10V and @20V. For falling slew rate, the input voltage is driven from 25V to 5V, and the output voltage transition is sampled at 20V and 10V.

Note 9: V_R is the Cathode-feedback voltage, nominally 1.244V.

Note 10: Average reference drift is calculated from the measurement of the reference voltage at 25°C and at the temperature extremes. The drift, in ppm/°C, is $10^6 \bullet \Delta V_R / (V_{R[25°C]} \bullet \Delta T_J)$, where ΔV_R is the lowest value subtracted from the highest, $V_{R[25°C]}$ is the value at 25°C, and ΔT_J is the temperature range. This parameter is guaranteed by design and sample testing.

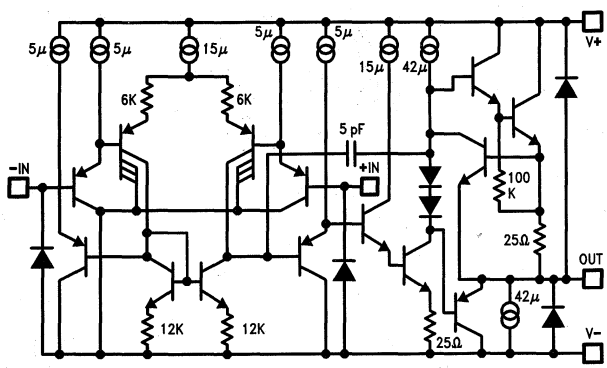
Note 11: Hysteresis is the change in V_R caused by a change in T_J, after the reference has been "dehysterized". To dehysterize the reference; that is minimize the hysteresis to the typical value, cycle its junction temperature in the following pattern, spiraling in toward 25°C: 25°C, 85°C, −40°C, 70°C, 0°C, 25°C.

Note 12: Low contact resistance is required for accurate measurement.

Note 13: A military RETSLM614AMX electrical test specification is available on request. The LM614AMJ/883 can also be procured as a Standard Military Drawing.

Simplified Schematic Diagrams

Op Amp



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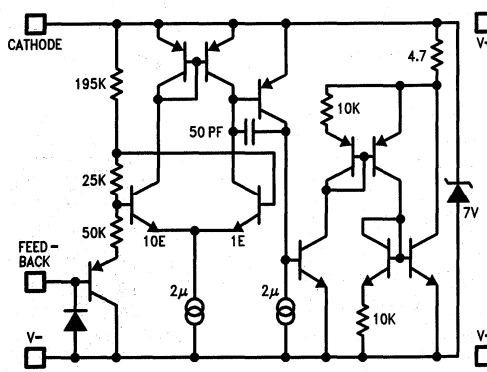
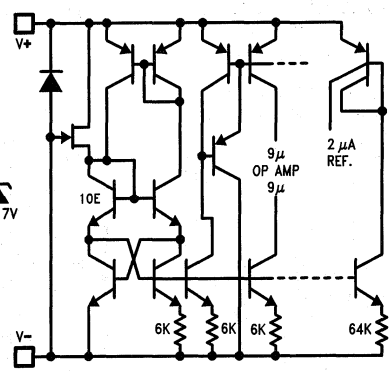
Reference



Bias

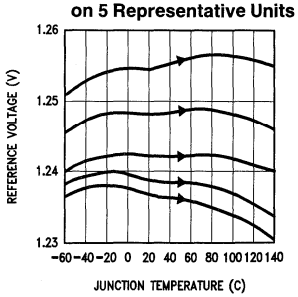


TL/H/9326–3

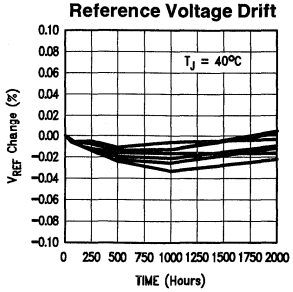
Typical Performance Characteristics (Reference)

T_J = 25°C, FEEDBACK pin shorted to V^- = 0V, unless otherwise noted

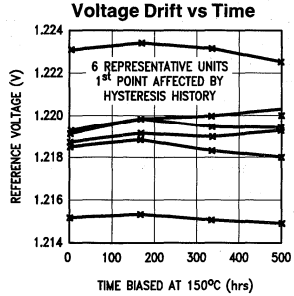
Reference Voltage vs Temperature on 5 Representative Units



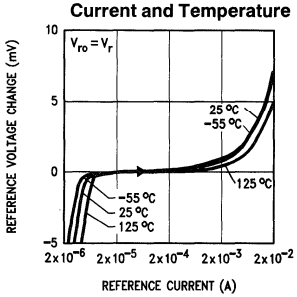
Reference Voltage Drift



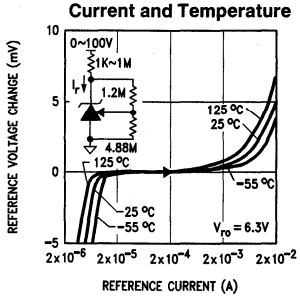
Accelerated Reference Voltage Drift vs Time



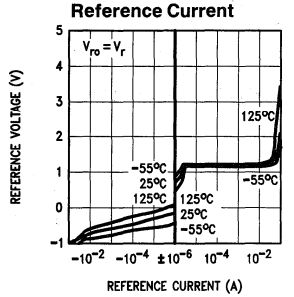
Reference Voltage vs Current and Temperature



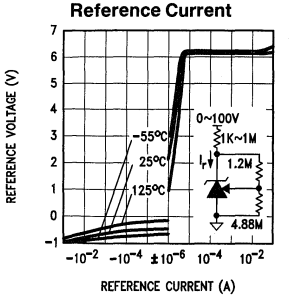
Reference Voltage vs Current and Temperature



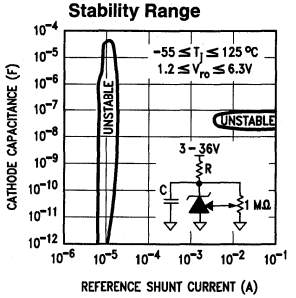
Reference Voltage vs Reference Current



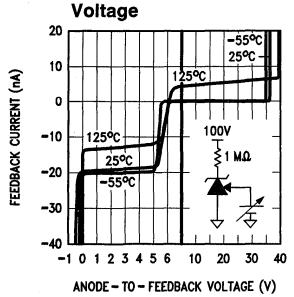
Reference Voltage vs Reference Current



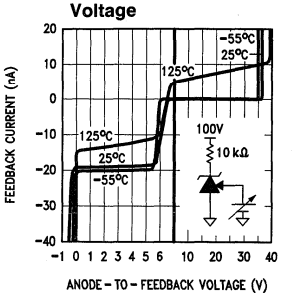
Reference AC Stability Range



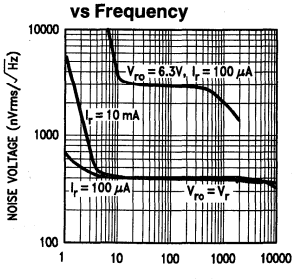
FEEDBACK Current vs FEEDBACK-to-Anode Voltage



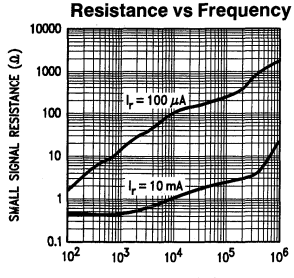
FEEDBACK Current vs FEEDBACK-to-Anode Voltage



Reference Noise Voltage vs Frequency



Reference Small-Signal Resistance vs Frequency

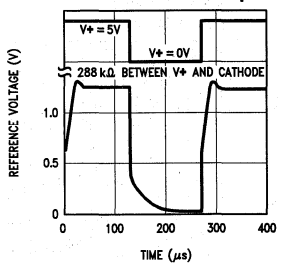


TL/H/9326–4

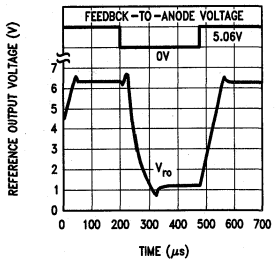
Typical Performance Characteristics (Reference) (Continued)

T_J = 25°C, FEEDBACK pin shorted to V^- = 0V, unless otherwise noted

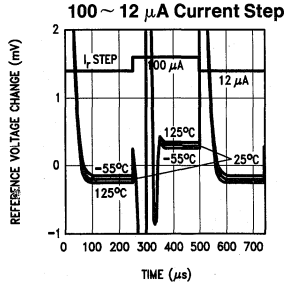
Reference Power-Up Time



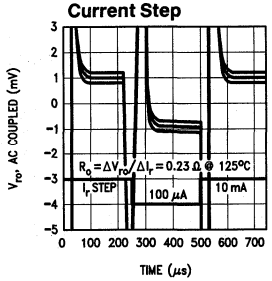
Reference Voltage with FEEDBACK Voltage Step



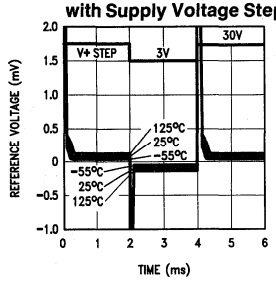
Reference Voltage with 100 ~ 12 μA Current Step



Reference Step Response for 100 μA ~ 10 mA Current Step



Reference Voltage Change with Supply Voltage Step

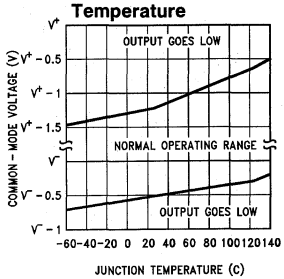


TL/H/9326–8

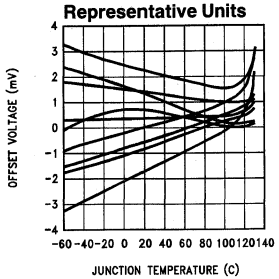
Typical Performance Characteristics (Op Amps)

V^+ = 5V, V^- = GND = OV, $V_{CM} = V^+/2$, $V_{OUT} = V^+/2$, T_J = 25°C, unless otherwise noted

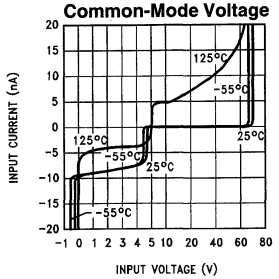
Input Common-Mode Voltage Range vs Temperature



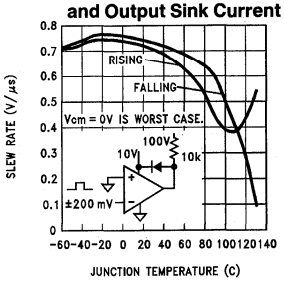
V_{OS} vs Junction Temperature on 9 Representative Units



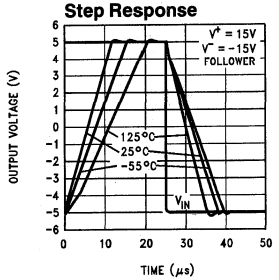
Input Bias Current vs Common-Mode Voltage



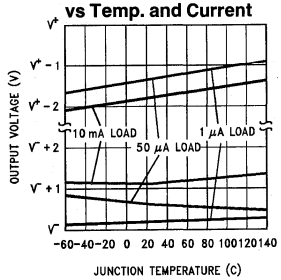
Slew Rate vs Temperature and Output Sink Current



Large-Signal Step Response



Output Voltage Swing vs Temp. and Current

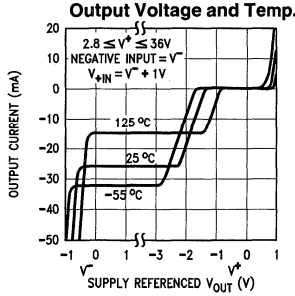


TL/H/9326–5

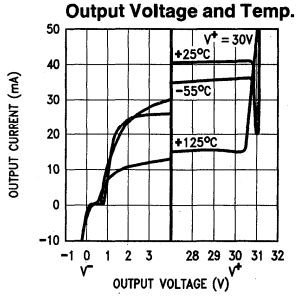
Typical Performance Characteristics (Op Amps) (Continued)

$V^+ = 5V$, $V^- = GND = 0V$, $V_{CM} = V^+/2$, $V_{OUT} = V^+/2$, $T_J = 25°C$, unless otherwise noted

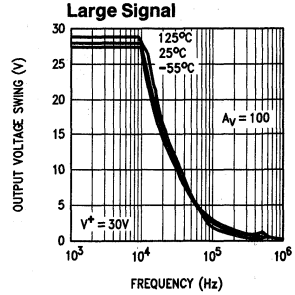
Output Source Current vs Output Voltage and Temp.



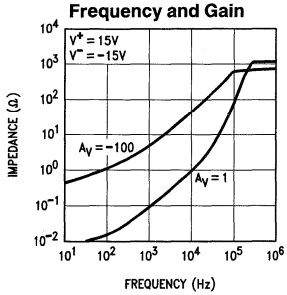
Output Sink Current vs Output Voltage and Temp.



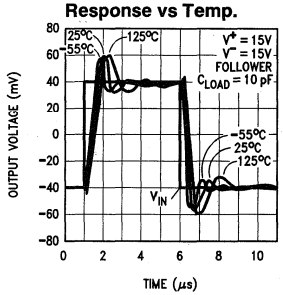
Output Swing, Large Signal



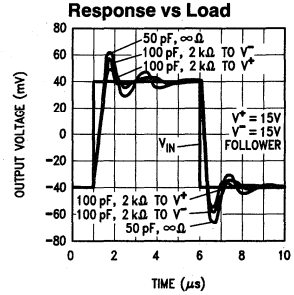
Output Impedance vs Frequency and Gain



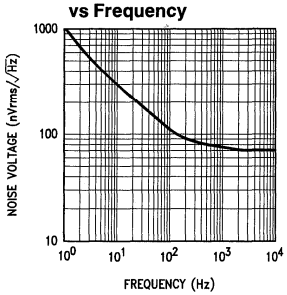
Small-Signal Pulse Response vs Temp.



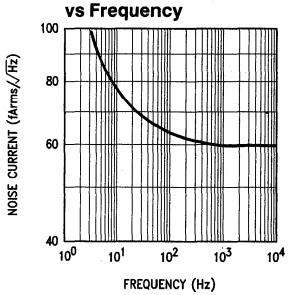
Small-Signal Pulse Response vs Load



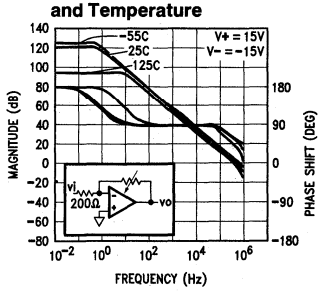
Op Amp Voltage Noise vs Frequency



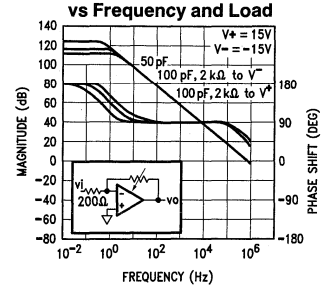
Op Amp Current Noise vs Frequency



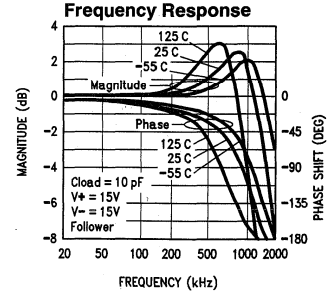
Small-Signal Voltage Gain vs Frequency and Temperature



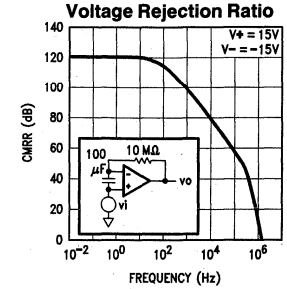
Small-Signal Voltage Gain vs Frequency and Load



Follower Small-Signal Frequency Response



Common-Mode Input Voltage Rejection Ratio

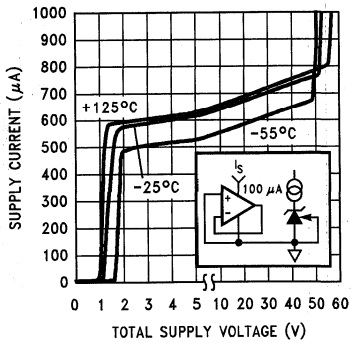


TL/H/9326–6

Typical Performance Characteristics (Op Amps) (Continued)

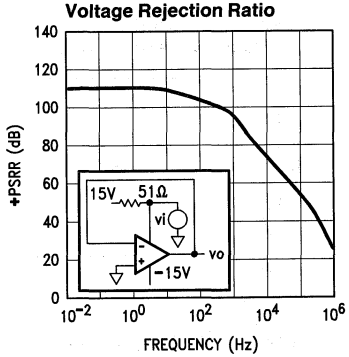
$V^+ = 5V$, $V^- = GND = 0V$, $V_{CM} = V^+/2$, $V_{OUT} = V^+/2$, $T_J = 25°C$, unless otherwise noted

Power Supply Current vs Power Supply Voltage



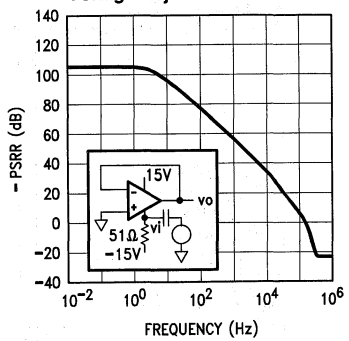
TL/H/9326–7

Positive Power Supply Voltage Rejection Ratio



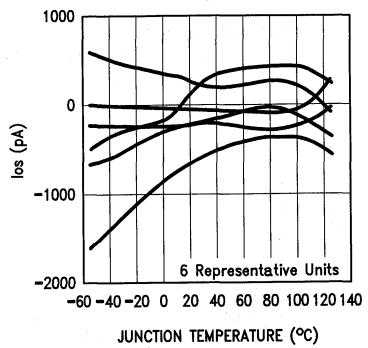
TL/H/9326–21

Negative Power Supply Voltage Rejection Ratio



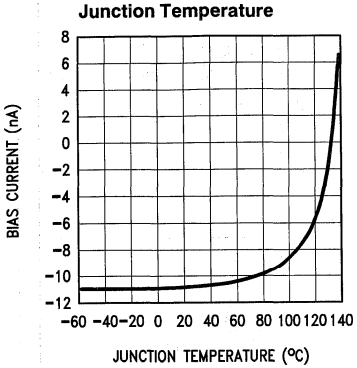
TL/H/9326–22

Input Offset Current vs Junction Temperature



TL/H/9326–24

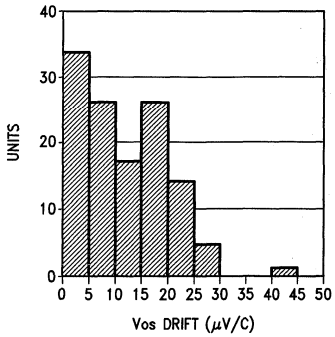
Input Bias Current vs Junction Temperature



TL/H/9326–38

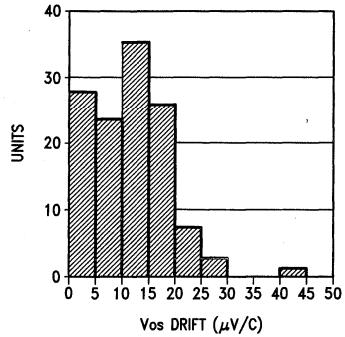
Typical Performance Distributions

Average V_{OS} Drift Military Temperature Range



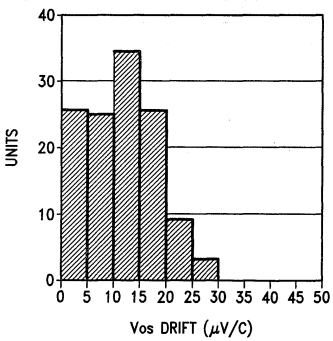
TL/H/9326–29

Average V_{OS} Drift Industrial Temperature Range



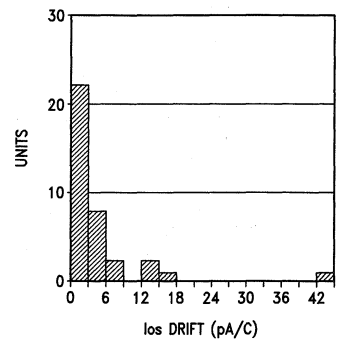
TL/H/9326–30

Average V_{OS} Drift Commercial Temperature Range



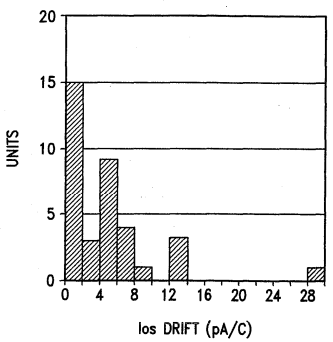
TL/H/9326–31

Average I_{OS} Drift Military Temperature Range



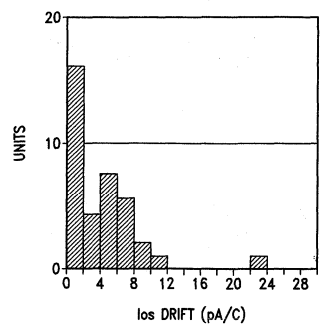
TL/H/9326–32

Average I_{OS} Drift Industrial Temperature Range



TL/H/9326–33

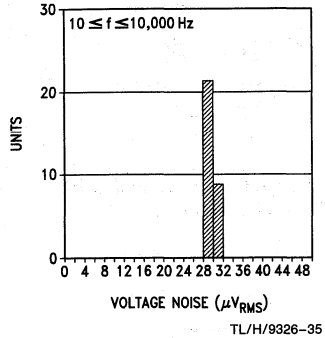
Average I_{OS} Drift Commercial Temperature Range



TL/H/9326–34

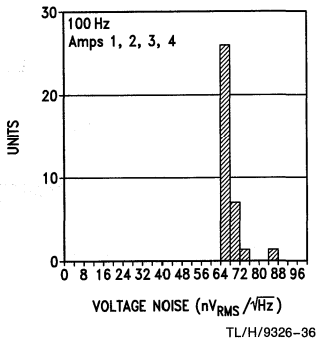
Typical Performance Distributions (Continued)

Voltage Reference Broad-Band Noise Distribution



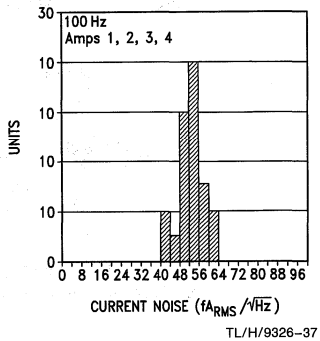
TL/H/9326-35

Op Amp Voltage Noise Distribution



TL/H/9326-36

Op Amp Current Noise Distribution



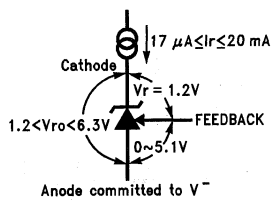
TL/H/9326-37

Application Information

VOLTAGE REFERENCE

Reference Biasing

The voltage reference is of a shunt regulator topology that models as a simple zener diode. With current I_r flowing in the 'forward' direction there is the familiar diode transfer function. I_r flowing in the reverse direction forces the reference voltage to be developed from cathode to anode. The cathode may swing from a diode drop below V^- to the reference voltage or to the avalanche voltage of the parallel protection diode, nominally 7V. A 6.3V reference with V^+ = 3V is allowed.



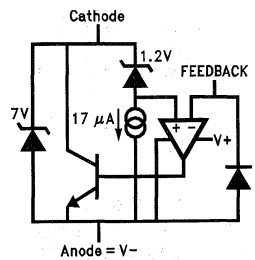
TL/H/9326-9

FIGURE 1. Voltages Associated with Reference (Current Source I_r is External)

The reference equivalent circuit reveals how V_r is held at the constant 1.2V by feedback, and how the FEEDBACK pin passes little current.

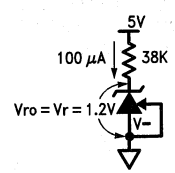
To generate the required reverse current, typically a resistor is connected from a supply voltage higher than the reference voltage. Varying that voltage, and so varying I_r, has small effect with the equivalent series resistance of less than an ohm at the higher currents. Alternatively, an active current source, such as the LM134 series, may generate I_r.

Capacitors in parallel with the reference are allowed. See the Reference AC Stability Range typical curve for capacitance values—from 20 μA to 3 mA any capacitor value is stable. With the reference's wide stability range with resistive and capacitive loads, a wide range of RC filter values will perform noise filtering.



TL/H/9326-10

FIGURE 2. Reference Equivalent Circuit



TL/H/9326-11

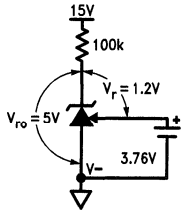
FIGURE 3. 1.2V Reference

Adjustable Reference

The FEEDBACK pin allows the reference output voltage, V_{ro}, to vary from 1.24V to 6.3V. The reference attempts to hold V_r at 1.24V. If V_r is above 1.24V, the reference will conduct current from Cathode to Anode; FEEDBACK current always remains low. If FEEDBACK is connected to Anode, then V_{ro} = V_r = 1.24V. For higher voltages FEEDBACK is held at a constant voltage above Anode—say 3.76V for V_{ro} = 5V. Connecting a resistor across the constaint V_r generates a current $I = R1/V_r$ flowing from Cathode into FEEDBACK node. A Thevenin equivalent 3.76V is generated from FEEDBACK to Anode with $R2 = 3.76/I$. Keep I

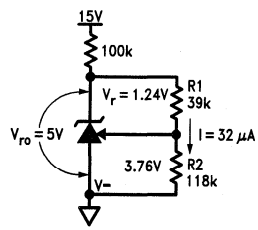
Application Information (Continued)

greater than one thousand times larger than FEEDBACK bias current for <0.1% error—I≥32 μA for the military grade over the military temperature range (I≥5.5 μA for a 1% untrimmed error for a commercial part.)



TL/H/9326–12

FIGURE 4. Thevenin Equivalent of Reference with 5V Output



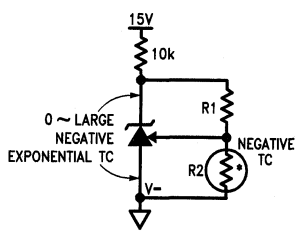
TL/H/9326–13

$$R1 = Vr/I = 1.24/32\mu = 39k$$

$$R2 = R1\{(Vro/Vr) - 1\} = 39k\{(5/1.24) - 1)\} = 118k$$

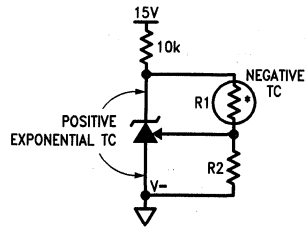
FIGURE 5. Resistors R1 and R2 Program Reference Output Voltage to be 5V

Understanding that V_r is fixed and that voltage sources, resistors, and capacitors may be tied to the FEEDBACK pin, a range of V_r temperature coefficients may be synthesized.



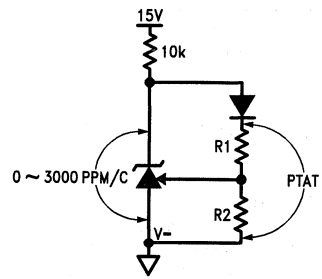
TL/H/9326–14

FIGURE 6. Output Voltage has Negative Temperature Coefficient (TC) if R2 has Negative TC



TL/H/9326–15

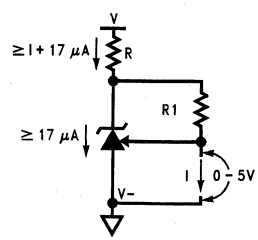
FIGURE 7. Output Voltage has Positive TC if R1 has Negative TC



TL/H/9326–16

FIGURE 8. Diode in Series with R1 Causes Voltage across R1 and R2 to be Proportional to Absolute Temperature (PTAT)

Connecting a resistor across Cathode-to-FEEDBACK creates a 0 TC current source, but a range of TCs may be synthesized.

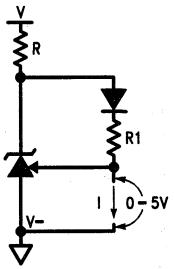


TL/H/9326–17

$$I = Vr/R1 = 1.24/R1$$

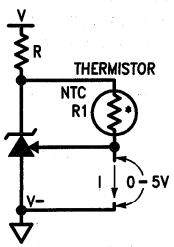
FIGURE 9. Current Source is Programmed by R1

Application Information (Continued)



TL/H/9326–18

FIGURE 10. Proportional-to-Absolute-Temperature Current Source



TL/H/9326–19

FIGURE 11. Negative-TC Current Source

Hysteresis

The reference voltage depends, slightly, on the thermal history of the die. Competitive micro-power products vary—always check the data sheet for any given device. Do not assume that no specification means no hysteresis.

OPERATIONAL AMPLIFIERS

Any amp or the reference may be biased in any way with no effect on the other amps or reference, except when a substrate diode conducts (see Guaranteed Electrical Characteristics Note 1). One amp input may be outside the common-mode range, another amp may be operated as a comparator, another with all terminals floating with no effect on the others (tying inverting input to output and non-inverting input to V^- on unused amps is preferred). Choosing operating points that cause oscillation, such as driving too large a capacitive load, is best avoided.

Op Amp Output Stage

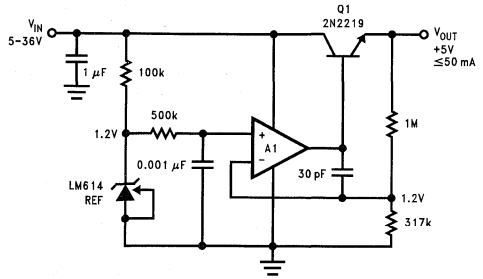
These op amps, like their LM124 series, have flexible and relatively wide-swing output stages. There are simple rules to optimize output swing, reduce cross-over distortion, and optimize capacitive drive capability:

1) Output Swing: Unloaded, the 42 μA pull-down will bring the output within 300 mV of V^- over the military temperature range. If more than 42 μA is required, a resistor from output to V^- will help. Swing across any load may be improved slightly if the load can be tied to V^+, at the cost of poorer sinking open-loop voltage gain
2) Cross-over Distortion: The LM614 has lower cross-over distortion (a 1 V_{BE} deadband versus 3 V_{BE} for the LM124), and increased slew rate as shown in the characteristic curves. A resistor pull-up or pull-down will force class-A operation with only the PNP or NPN output transistor conducting, eliminating cross-over distortion
3) Capacitive Drive: Limited by the output pole caused by the output resistance driving capacitive loads, a pull-down resistor conducting 1 mA or more reduces the output stage NPN r_e until the output resistance is that of the current limit 25Ω. 200 pF may then be driven without oscillation.

Op Amp Input Stage

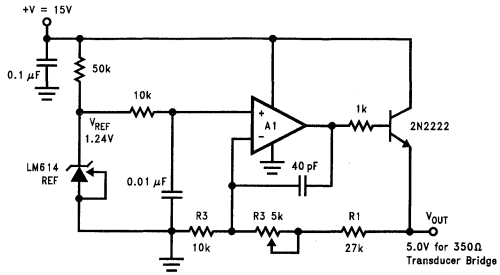
The lateral PNP input transistors, unlike most op amps, have BV_{EBO} equal to the absolute maximum supply voltage. Also, they have no diode clamps to the positive supply nor across the inputs. These features make the inputs look like high impedances to input sources producing large differential and common-mode voltages.

Typical Applications



TL/H/9326-42

FIGURE 12. Simple Low Quiescent Drain Voltage Regulator. Total supply current approximately 320 μA, when $V_{IN} = +5V$.



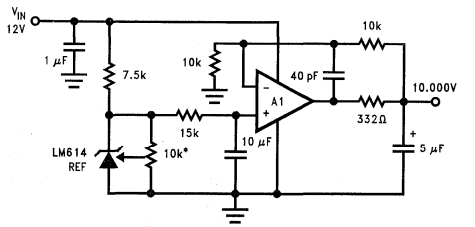
$V_{OUT} = (R_1 / Pe + 1) V_{REF}$

TL/H/9326-44

R_1, R_2 should be 1% metal film

P_β should be low T.C. trim pot

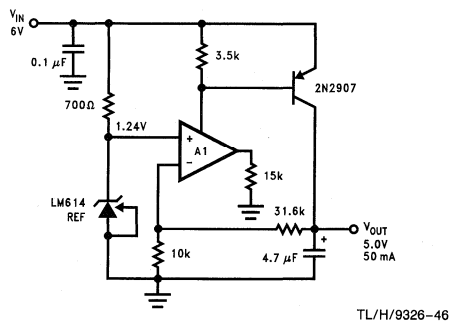
FIGURE 14. Slow Rise Time Upon Power-Up, Adjustable Transducer Bridge Driver. Rise time is approximately 1 ms.



TL/H/9326-43

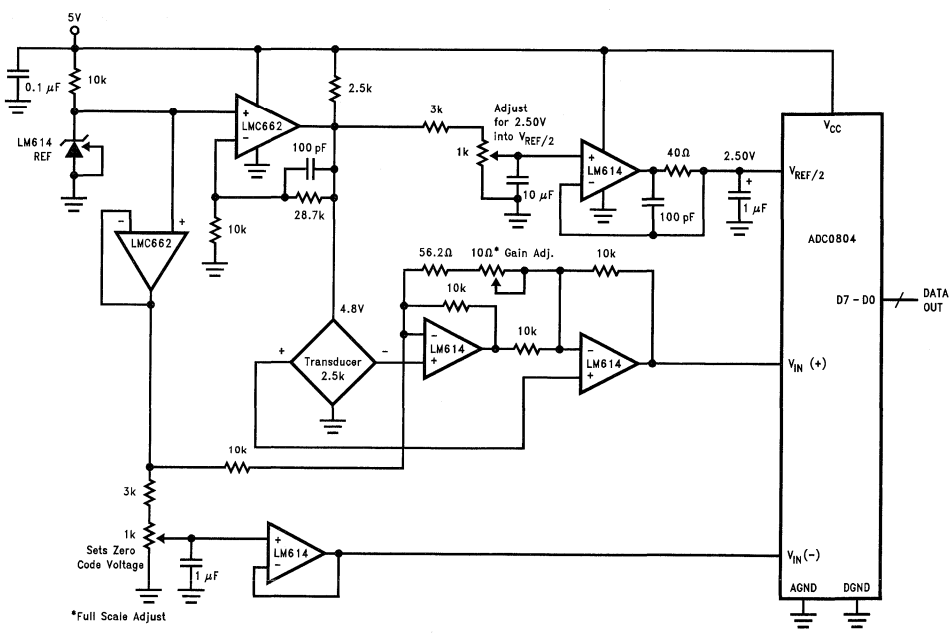
*10k must be low t.c. trimpot.

FIGURE 13. Ultra Low Noise 10.00V Reference. Total output noise is typically 14 μV_{RMS}.



TL/H/9326-46

FIGURE 16. Low Drop-Out Voltage Regulator Circuit, drop-out voltage is typically 0.2V.



TL/H/9326-45

FIGURE 15. Transducer Data Acquisition System. Set zero code voltage, then adjust 10Ω gain adjust pot for full scale.

National Semiconductor

LM627/LM637
Precision Operational Amplifiers

General Description

The LM627/LM637 series feature extremely low noise and excellent precision along with high speed. Voltage noise is a low 3 nV/$\sqrt{Hz}$ in the flat band and rises to only 3.5 nV/$\sqrt{Hz}$ at 10 Hz. The A grades offer guaranteed specifications of 25 μV offset voltage and 0.3 μV/°C drift, and their *guaranteed* 126 dB CMRR, 120 dB PSRR and voltage gain of 5 Million ensure an ultra-low V_{OS} under all conditions.

The unity-gain stable LM627 is nearly twice as fast as the OP-27 with a slew rate of 4.5 V/μs and a 14 MHz gain-bandwidth product. Stable at gains of 5 or more, the decompensated LM637 is considerably faster.

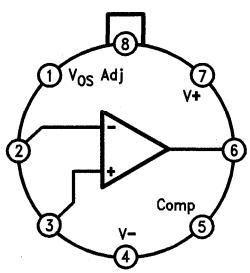
Other enhancements of the LM627/LM637 include a guaranteed 600Ω load drive capability over temperature: ±10V output swing at voltage gains over one million. Bias current has been reduced to 10 nA for the A and B grades and 25 nA for the C grade. Furthermore the LM627 may be overcompensated to allow it to drive capacitive loads up to 2000 pF while maintaining its superb dc specs.

Features

- Low Noise — 3 nV/$\sqrt{Hz}$@1 kHz; 3.5 nV/$\sqrt{Hz}$@ 10 Hz
- Low V_{OS} — 25 μV Max
- Low Drift — 0.3 μV/°C Max
- Offset Drift 100% Tested (A and B grades)
- Noise Voltage 100% Tested (A and B grades)
- High Gain — 5 Million Min
- High CMRR — 126 dB Min
- High PSRR — 120 dB Min
- High Speed
  - LM627: 14 MHz Gain-Bandwidth; 4.5 V/μs Slew Rate
  - LM637: 65 MHz Gain-Bandwidth; 14 V/μs Slew Rate
- *Guaranteed* 600Ω drive over temperature
- Wide Power Supply Range — ±4V to ±18V
- Overcompensation Pin — Allows driving high C_L

Connection Diagrams

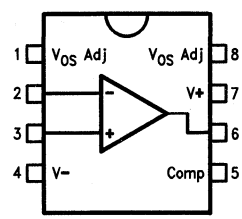
Metal Can Package



TL/H/9212–1

Top View

DIP Packages



TL/H/9212–2

Ordering Information

LM627

Package	Temperature Range		NSC Drawing
	Military	Commercial	
TO-99	LM627AMH LM627BMH	LM627ACH LM627BCH LM627CH	H08C
8-Pin Molded DIP		LM627CN	N08E

LM637

Package	Temperature Range		NSC Drawing
	Military	Commercial	
TO-99	LM637AMH LM637BMH	LM637ACH LM637BCH LM637CH	H08C
8-Pin Molded DIP		LM637CN	N08E

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Differential Input Overdrive Current (Note 7)	±25 mA
Supply Voltage	44V
Input Voltage	Supply Voltage
Output Short Circuit to Gnd	Continuous
Power Dissipation (Note 8)	
Molded DIP	1300 mW
Metal Can	830 mW
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 5 sec.)	260°C
Maximum Junction Temperature	150°C
ESD Rating	3 kV
C_{ZAP} = 100 pF, R_{ZAP} = 1.5 kΩ	

Operating Ratings

Temperature Range (Note 8)	
AM and BM grades	$-55°C \le T_J \le +125°C$
AC, BC, and C grades	$-25°C \le T_J \le +85°C$

Electrical Characteristics

All limits guaranteed for T_J = 25°C, V_{CM} = 0, V_O = 0 and ±15V supplies unless otherwise specified. **Boldface limits apply at operating temperature extremes.**

Parameter	Conditions	Typ	LM627AM LM637AM		LM627BM LM637BM		Units
			Tested Limit (Note 5)	Design Limit (Note 6)	Tested Limit (Note 5)	Design Limit (Note 6)	
Input Offset Voltage	(Note 2)	15	25 **55**		50 **110**		μV Max
Input Offset Voltage Drift	(Note 3)	0.2	**0.3**		**0.6**		μV/°C Max
Input Offset Voltage Long Term Stability	(Note 4)	0.2					μV/mo Max
Input Bias Current		3	10 **20**		10 **20**		nA Max
Input Offset Current		2	10 **20**		10 **20**		nA Max
Input Noise Voltage	0.1 to 10Hz	0.08		0.18		0.18	μV p-p Max
Input Noise Voltage Density	f = 10Hz f = 30Hz f = 1kHz	3.5 3.1 3.0	5.5 4.5 3.8		5.5 4.5 3.8		$nV/\sqrt{Hz}$ Max
Input Noise Current Density	f = 10Hz f = 30Hz f = 1kHz	1.7 1.0 0.4					$pA/\sqrt{Hz}$ Max
Input Resistance	Common-Mode	20					GΩ
Input Voltage Range		±12	±11 **±10.3**		±11 **10.3**		V Min
Common-Mode Rejection Ratio	V_{CM} = ±11V **V_{CM} = ±10V**	140	126 **120**		126 **120**		dB Min
Power Supply Rejection Ratio	V_S = ±4V to ±18V **V_S = ±4.5V to ±18V**	140	120 **117**		120 **117**		dB Min
Large-Signal Voltage Gain	V_O = ±12V $R_L \ge 2$ kΩ	10000	5000 **3000**		5000 **2000**		V/mV Min
	V_O = ±10V $R_L \ge 1$ kΩ	7000	4000 **2000**		3500 **1500**		
	$R_L \ge 600Ω$ V_O = ±10V	6000	3000 **1500**		2000 **1000**		

Electrical Characteristics (Continued)

Parameter	Conditions	Typ	LM627AM LM637AM		LM627BM LM637BM		Units
			Tested Limit (Note 5)	Design Limit (Note 6)	Tested Limit (Note 5)	Design Limit (Note 6)	
Output Voltage Swing	$R_L \geq 2\,k\Omega$	±13.8	±13 **±12.5**		±13 **±12.5**		V
	$R_L \geq 600\Omega$	±12.5	±11 **±10.5**		±11 **±10.5**		Min
Slew Rate	LM627 R_L = 2k	4.5		3		3	V/μs
	LM637	14		10		10	Min
Gain-Bandwidth Product	LM627 f = 10 kHz	14		10		10	MHz
	LM637	65		45		45	Min
Output Resistance	Open Loop	50					Ω
Supply Current		3	4.5 **5.5**		4.5 **5.5**		mA Max
Offset Adjust Range	$R_P \geq 10\,k\Omega$	±2					mV

Electrical Characteristics All limits guaranteed for T_J = 25°C, V_{CM} = 0, V_O = 0 and ±15V supplies unless otherwise specified. **Boldface limits apply at operating temperature extremes.**

Parameter	Conditions	Typ	LM627AC LM637AC		LM627BC LM637BC		LM627C LM637C		Units
			Tested Limit (Note 5)	Design Limit (Note 6)	Tested Limit (Note 5)	Design Limit (Note 6)	Tested Limit (Note 5)	Design Limit (Note 6)	
Input Offset Voltage	(Note 2)	15	25 **50**		50 **110**		100	**210**	μV Max
Input Offset Voltage Drift	(Note 3)	0.2	**0.6**		**1.0**			**1.8**	μV/°C Max
Input Offset Voltage Long Term Stability	(Note 4)	0.2							μV/mo Max
Input Bias Current		3	10	**20**	10	**20**	25	**50**	nA Max
Input Offset Current		2	10	**20**	10	**20**	25	**50**	nA Max
Input Noise Voltage	0.1 to 10 Hz	0.08		0.18		0.18		0.25	μV p-p Max
Input Voltage Noise Density	f = 10 Hz	3.5	5.5		5.5			8.0	nV/√Hz
	f = 30 Hz	3.1	4.5		4.5			5.6	Max
	f = 1 kHz	3.0	3.8		3.8			4.5	
Input Noise Current Density	f = 10 Hz	1.7							pA/√Hz
	f = 30 Hz	1.0							Max
	f = 1 kHz	0.4							
Input Resistance	Common Mode	20							GΩ
Input Voltage Range		±12	±11	**±10.3**	±11	**±10.3**	±11	**±10.3**	V Min
Common-Mode Rejection Ratio	V_{CM} = ±11V	140	126	**120**	126	**120**	120	**116**	dB
	V_{CM} = ±10V								Min
Power Supply Rejection Ratio	V_S = ±4V to ±18V	140	120	**117**	120	**117**	110	**108**	dB
	V_S = ±4.5V to ±18V								Min

Electrical Characteristics (Continued)

Parameter	Conditions	Typ	LM627AC LM637AC		LM627BC LM637BC		LM627C LM637C		Units
			Tested Limit (Note 5)	Design Limit (Note 6)	Tested Limit (Note 5)	Design Limit (Note 6)	Tested Limit (Note 5)	Design Limit (Note 6)	
Large-Signal Voltage Gain	$V_O = \pm 12V$ $R_L \geq 2 k\Omega$ $V_O = \pm 10V$	10000	5000	**3000**	5000	**3000**	4000	**2500**	V/mV Min
	$R_L \geq 1 k\Omega$	7000	4000	**2500**	3500	**2000**	2500	**1500**	
	$R_L \geq 600\Omega$	6000	3000	**2000**	2000	**1500**	1500	**1000**	
Output Voltage Swing	$R_L \geq 2 k\Omega$	±13.8	±13	±**12.5**	±13	±**12.5**	±13	±**12.5**	V Min
	$R_L \geq 600\Omega$	±12.5	±11	±**10.5**	±11	±**10.5**	±10.5	±**10**	
Slew Rate	LM627 $R_L = 2k$	4.5		3		3		3	V/μs Min
	LM637	14		10		10		10	
Gain-Bandwidth Product	LM627 $f = 10$ kHz	14		10		10		10	MHz Min
	LM637	65		45		45		45	
Output Resistance	Open Loop	50							Ω
Supply Current		3	4.5	**5**	4.5	**5**	4.8	**5.2**	mA Max
Offset Adjust Range	$R_P \geq 10 k\Omega$	±2							mV

Note 1: Absolute maximum ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed.

Note 2: Input offset voltage for A and B grades is tested and guaranteed with the device fully warmed up. See *Figure 1* in the Application Hints for test circuit. Warmup drift is typically 5 μV settling out in 5 minutes. The LM627C/LM637C offset voltage is measured by automated test equipment within 200 ms of applying power.

Note 3: Input offset voltage drift is defined as $(V_{OS}(85°C) - V_{OS}(-25°C))/110°C$ for the industrial temperature range. For the military temperature range, the input offset voltage drift is measured from room temperature to both extremes: both $(V_{OS}(25°C) - V_{OS}(-55°C))/80°C$ and $(V_{OS}(125°C) - V_{OS}(25°C))/100°C$.

Note 4: Input offset voltage long term stability refers to the average trend line of V_{OS} vs. time over extended periods of time after the first 30 days of operation. Excluding the initial hour of operation, changes in V_{OS} during the first 30 days are typically 2 μV.

Note 5: Guaranteed and 100% production tested. These limits are used to calculate outgoing quality levels.

Note 6: Guaranteed but not 100% production tested. These limits are not used to calculate outgoing quality levels.

Note 7: Inputs are protected by back-to-back diodes to prevent zener breakdown of the input transistors. Series limiting resistors have not been included since they degrade noise performance. Excessive current may flow if a differential voltage in excess of 0.7V is applied.

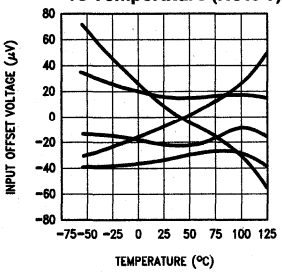
Note 8: For operation above 25°C, the maximum power dissipation specification must be derated. Typical junction-to-ambient thermal resistance of the molded DIP is 105°C/W. The metal can package has a typical junction-to-ambient thermal resistance of 150°C/W and a typical junction-to-case thermal resistance of 17°C/W.

Note 9: These units selected to illustrate the types of variations that may be encountered. (This note refers to particular curves within the Typical Performance Characteristics.)

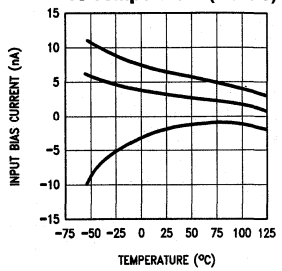
Typical DC Performance Characteristics (LM627, LM637)

$V_S = \pm 15V$, $T_A = 25°C$, $R_L = 2k$ unless othewise indicated.

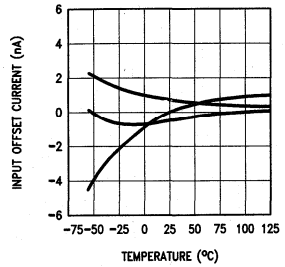
Input Offset Voltage of 5 Representative Units vs Temperature (Note 9)



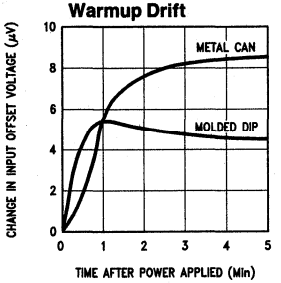
Input Bias Current of 3 Representative Units vs Temperature (Note 9)



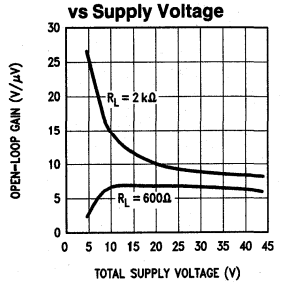
Input Offset Current of 3 Representative Units vs Temperature (Note 9)



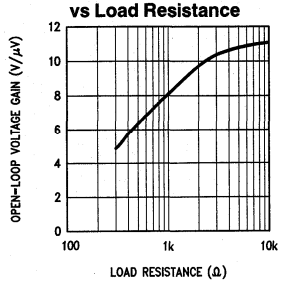
Warmup Drift



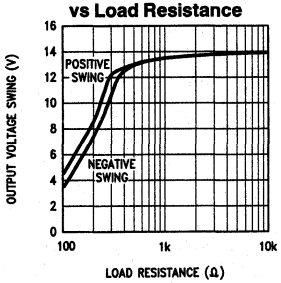
Open Loop Gain vs Supply Voltage



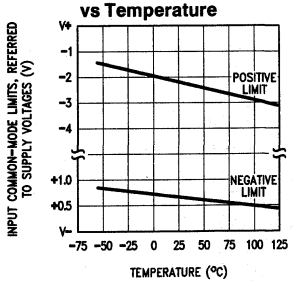
Open Loop Gain vs Load Resistance



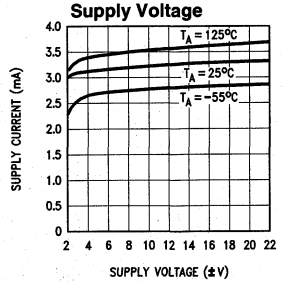
Output Voltage Swing vs Load Resistance



Input Common-Mode Limits vs Temperature



Supply Current vs Supply Voltage

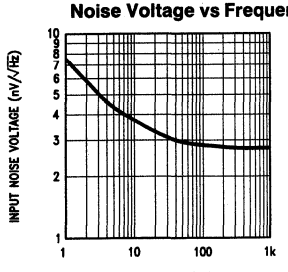


TL/H/9212-9

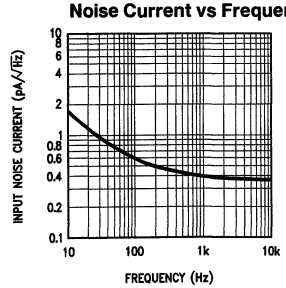
Typical Noise Characteristics (LM627, LM637)

$V_S = \pm 15V$, $T_A = 25°C$

Noise Voltage vs Frequency



Noise Current vs Frequency

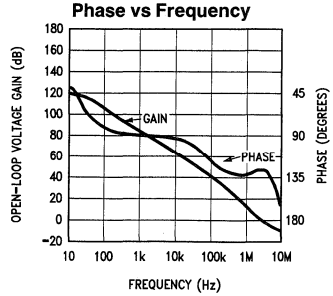


TL/H/9212-10

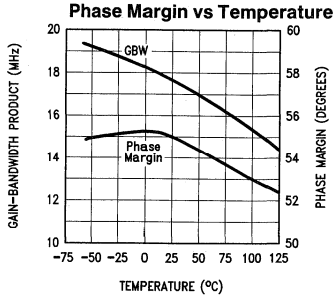
Typical AC Performance Characteristics (LM627)

$V_S = \pm 15V$, $T_A = 25°C$, $R_L = 2k$

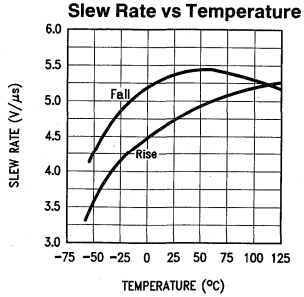
Open-Loop Gain and Phase vs Frequency



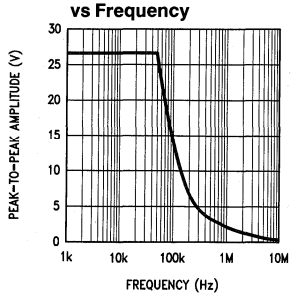
Gain-Bandwidth Product, Phase Margin vs Temperature



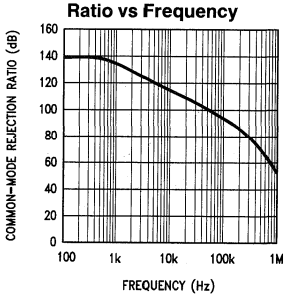
Slew Rate vs Temperature



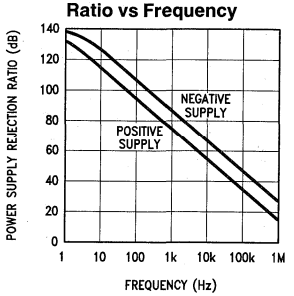
Maximum Output Swing vs Frequency



Common-Mode Rejection Ratio vs Frequency

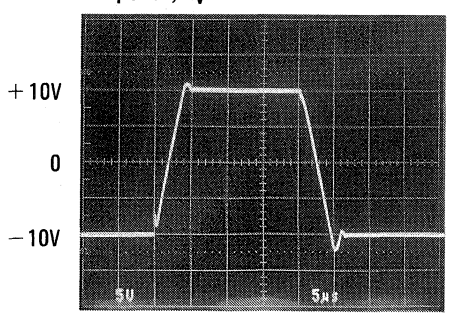


Power Supply Rejection Ratio vs Frequency



TL/H/9212–11

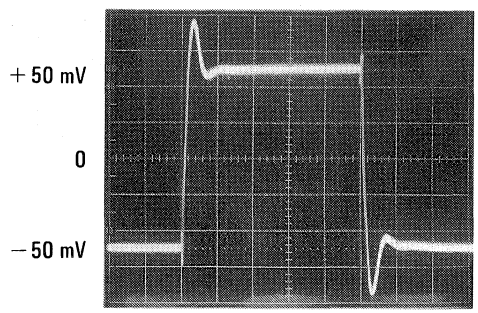
Large-Signal Pulse Response, $A_V = +1$



TIME (5 μs/DIV)

TL/H/9212–12

Small-Signal Pulse Response, $A_V = +1$



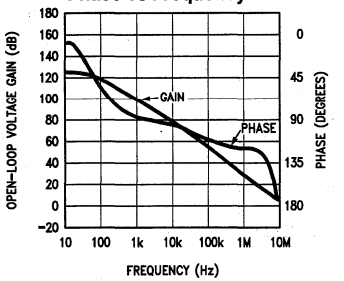
TIME (500 ns/DIV)

TL/H/9212–13

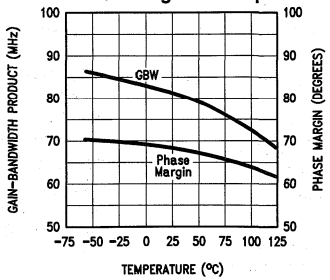
Typical AC Performance Characteristics (LM637)

$V_S = \pm 15V$, $T_A = 25°C$, $R_L = 2k$

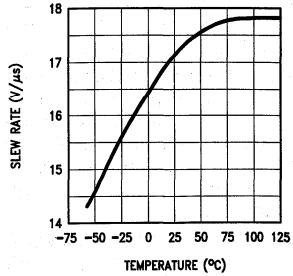
Open-Loop Gain and Phase vs Frequency



Gain-Bandwidth Product, Phase Margin vs Temperature

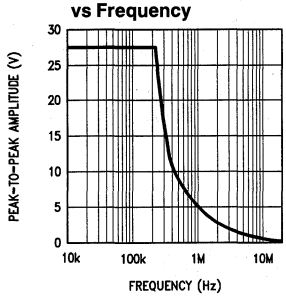


Slew Rate vs Temperature

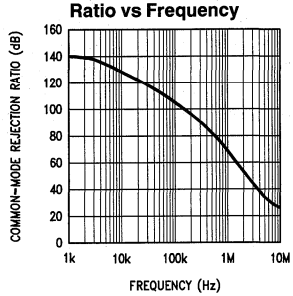


TL/H/9212–14

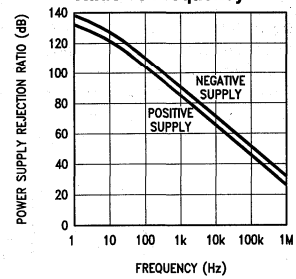
Maximum Output Swing vs Frequency



Common-Mode Rejection Ratio vs Frequency

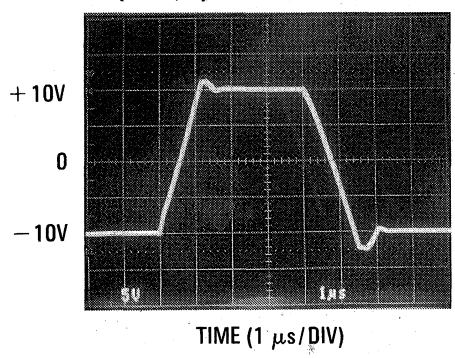


Power Supply Rejection Ratio vs Frequency



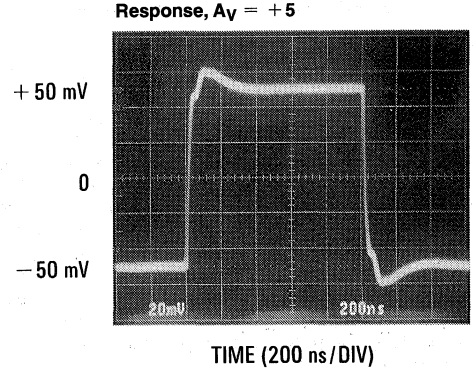
TL/H/9212–15

Large-Signal Pulse Response, $A_V = +5$



TL/H/9212–16

Small-Signal Pulse Response, $A_V = +5$



TL/H/9212–17

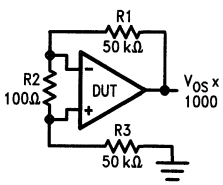
Application Hints

OFFSET VOLTAGE

Offset voltage of the LM627/637 is internally trimmed to a very low value. The data sheet V_{OS} specification applies at $T_J = 25°C$, $V_{CM} = 0$ and $\pm 15V$ supplies. For other temperatures, common-mode voltages, and supply voltages, temperature drift, common-mode rejection and power-supply rejection errors must be taken into account.

Since the LM627/LM637C offset voltage is measured within 200 ms of applying power, the 5 μV typical warmup drift is not accounted for in the measurement. Fortunately, the warmup drift is a small fraction of its 100 μV max offset. For the 25 μV A and 50μV B grades, the offset voltage is measured with the circuit of *Figure 1* approximately 5 minutes after applying power.

To measure V_{OS} with high accuracy, V_{OS} must be amplified right at the device as shown; otherwise the offset voltage can be obscured by noise and thermoelectric voltages. Thermocouples occur in the devices, the IC socket and the resistor across the device inputs (R2), all of which must be held isothermal. Usually best results are obtained by placing the circuit in a box or chamber to minimize airflow and employing a long thermal soak time. R2 should be mounted symmetrically with respect to potential thermal gradients: e.g. *not* perpendicular to the board but instead parallel to the board and the device socket. In addition, R2 should have low thermal EMF. Cermet or nichrome metal film types are acceptable; avoid tin-oxide resistors.

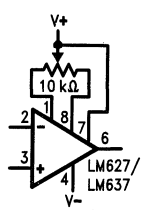


TL/H/9212–3

FIGURE 1. Offset Voltage Test Circuit

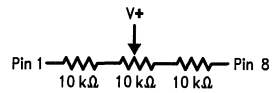
OFFSET NULLING

This is usually not required on the LM627/637 family since its offset voltage is internally trimmed. An offset adjust range of approximately ± 2 mV is available using a single 10 or 20 kΩ potentiometer as shown in *Figure 2.* With these values, the adjustment is relatively linear over the entire range. If a 100 kΩ potentiomer is used, the adjustment becomes very coarse at the extremes (above 700 μV) but fine in the center, which makes it easier to precisely null the offset. For even more sensitivity, employ a pot in conjunction with two fixed resistors. The circuit of *Figure 3,* which uses this technique, has an adjustment range of ± 200 μV. Because adjusting the offset voltage of an LM627/637 will alter its offset voltage temperature drift, caution is advised.



TL/H/9212–4

FIGURE 2. Offset Adjust Circuit



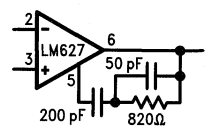
TL/H/9212–5

FIGURE 3. Improved Sensitivity Offset Adjust

Every 100μV of offset will produce a 0.33 μV/°C drift component. For this reason the offset adjust potentiometer should not be used to null out a sensor offset if system temperature drift is important; rather a stable voltage reference must be added to the sensor voltage. Offset voltage drift is guaranteed by design for the LM627C either with or without external nulling. The higher precision A and B grades are 100% drift tested and guaranteed without nulling only.

OVERCOMPENSATION

Without any external compensation, the LM627 is stable at unity gain and up to 500 pF load capacitance. It has a slew rate of 4.5 V/μs and a gain-bandwidth product of 14 MHz. If desired, the amplifier may be overcompensated by adding external components as shown in *Figure 4.* This increases maximum capacitive loading to 2000 pF while decreasing slew rate to 1.5 V/μs and bandwidth to 1.5 MHz. If overcompensation of the LM627 (or the LM637) is not desired, pin 5 should be left open.

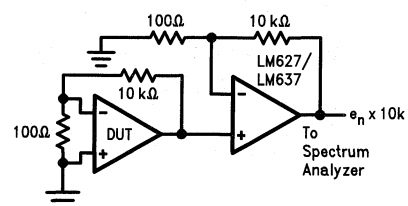


TL/H/9212–6

FIGURE 4. Overcompensation

NOISE

When measuring spot noise voltage, a circuit as shown in *Figure 5* is recommended. The DUT running at a gain of 100 will not roll off until approximately 140 kHz. Adding the second gain of 100 amplifier brings total DUT-input-referred gain up to 10,000, which minimizes to minimize sensitivity to EMI in the environment. When measuring spot noise at 30 Hz, it is recommended that the spectrum analyzer bandwidth be 20 Hz or less to minimize pickup at line frequency.

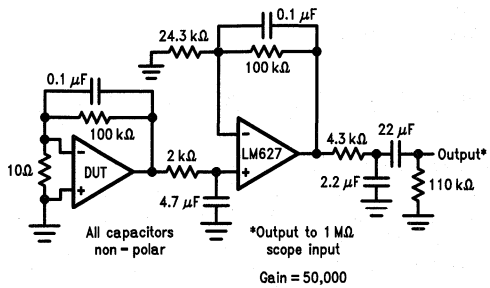


TL/H/9212–7

FIGURE 5. Spot Noise Test Circuit

Application Hints (Continued)

The circuit used to measure peak-to-peak noise voltage in the 0.1 to 10 Hz range is shown in *Figure 6.* The device should be warmed up for about 2 minutes and shielded from air currents to minimize warmup drift and thermoelectric voltages. The test time should be limited to only 10 seconds, as this limits noise contributions below 0.1 Hz, as does the single zero rolloff. The measuring equipment must be flat down to 0.1 Hz. DC coupling must be employed to ensure this. Certain types of X-Y plotters may not be usable because of severe rolloff above a few Hz.



TL/H/9212–8

FIGURE 6. 0.1 Hz to 10 Hz Noise Test Circuit

National Semiconductor

LM675 Power Operational Amplifier

General Description

The LM675 is a monolithic power operational amplifier featuring wide bandwidth and low input offset voltage, making it equally suitable for AC and DC applications.

The LM675 is capable of delivering output currents in excess of 3 amps, operating at supply voltages of up to 60V. The device overload protection consists of both internal current limiting and thermal shutdown. The amplifier is also internally compensated for gains of 10 or greater.

Features

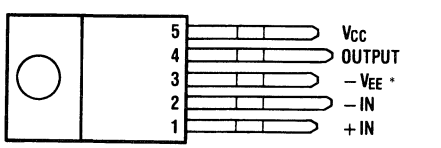
- 3A current capability
- A_{VO} typicaly 90 dB
- 5.5 MHz gain bandwidth product
- 8 V/μs slew rate
- Wide power bandwidth 70 kHz
- 1 mV typical offset voltage
- Short circuit protection
- Thermal protection with parole circuit (100% tested)
- 16V–60V supply range
- Wide common mode range
- Internal output protection diodes
- 90 dB ripple rejection
- Plastic power package TO-220

Applications

- High performance power op amp
- Bridge amplifiers
- Motor speed controls
- Servo amplifiers
- Instrument systems

Connection Diagram

TO-220 Power Package (T)



TL/H/6739–1

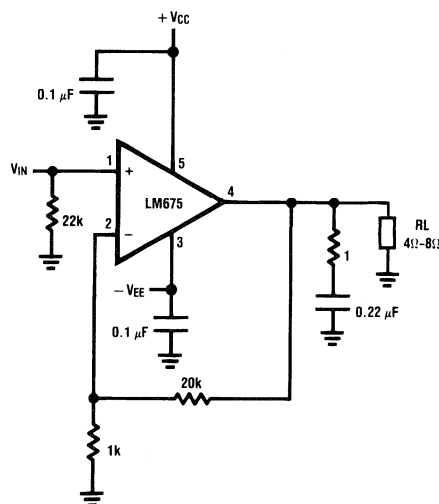
Front View

Order Number LM675T
See NS Package T05B

*The tab is internally connected to pin 3 ($-V_{EE}$)

Typical Applications

Non-Inverting Amplifier



TL/H/6739–2

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	±30V
Input Voltage	$-V_{EE}$ to V_{CC}
Operating Temperature	0°C to +70°C
Storage Temperature	−65°C to +150°C
Junction Temperature	150°C
Power Dissipation (Note 1)	30W
Lead Temperature (Soldering, 10 seconds)	260°C

ESD rating to be determined.

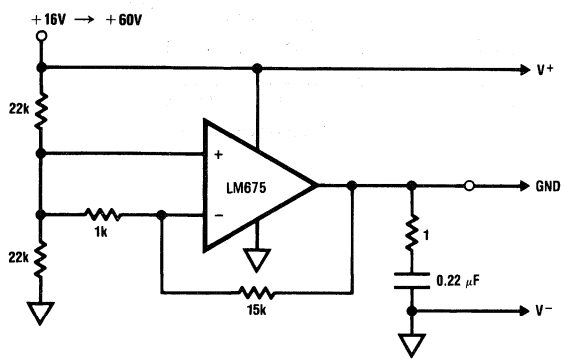
Electrical Characteristics $V_S = \pm 25V$, $T_A = 25°C$ unless otherwise specified.

Parameter	Conditions	Typical	Tested Limit	Units
Supply Current	$P_{OUT} = 0W$	18	50 (max)	mA
Input Offset Voltage	$V_{CM} = 0V$	1	10 (max)	mV
Input Bias Current	$V_{CM} = 0V$	0.2	2 (max)	μA
Input Offset Current	$V_{CM} = 0V$	50	500 (max)	nA
Open Loop Gain	$R_L = \infty\Omega$	90	70 (min)	dB
PSRR	$\Delta V_S = \pm 5V$	90	70 (min)	dB
CMRR	$V_{IN} = \pm 20V$	90	70 (min)	dB
Output Voltage Swing	$R_L = 8\Omega$	±21	±18 (min)	V
Offset Voltage Drift Versus Temperature	$R_S < 100\ k\Omega$	25		μV/°C
Offset Voltage Drift Versus Output Power		25		μV/W
Output Power	THD = 1%, f_O = 1 kHz, $R_L = 8\Omega$	25	20	W
Gain Bandwidth Product	f_O = 20 kHz, A_{VCL} = 1000	5.5		MHz
Max Slew Rate		8		V/μs
Input Common Mode Range		±22	±20 (min)	V

Note 1: Assumes T_A equal to 70°C. For operation at higher tab temperatures, the LM675 must be derated based on a maximum junction temperature of 150°C.

Typical Applications (Continued)

Generating a Split Supply From a Single Supply

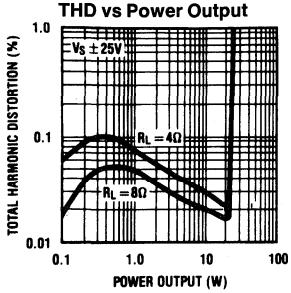


$V_S = \pm 8V \rightarrow \pm 30V$

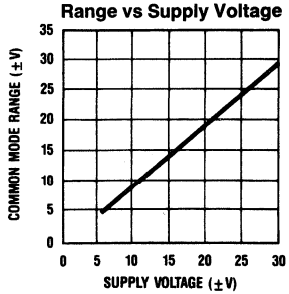
TL/H/6739–3

Typical Performance Characteristics

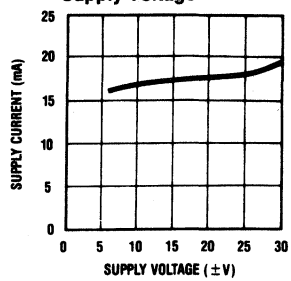
THD vs Power Output



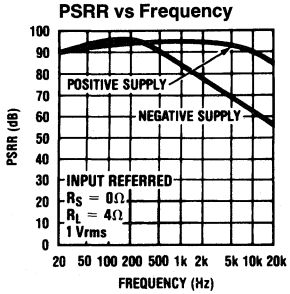
Input Common Mode Range vs Supply Voltage



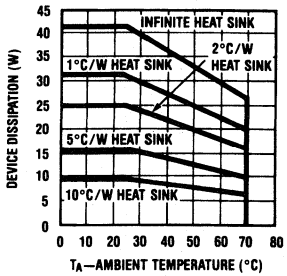
Supply Current vs Supply Voltage



PSRR vs Frequency

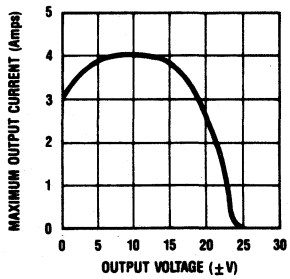


Device Dissipation vs Ambient Temperature†



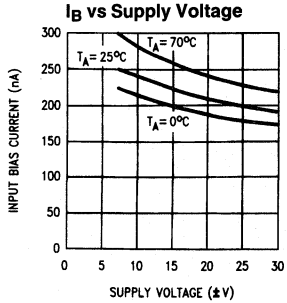
†θ INTERFACE = 1° C/W.
See Application Hints.

Current Limit vs Output Voltage*

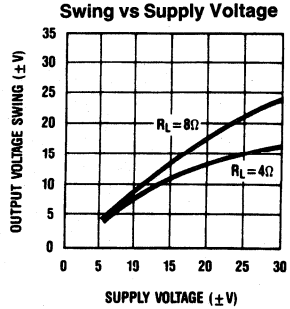


*VS = ±25V

IB vs Supply Voltage

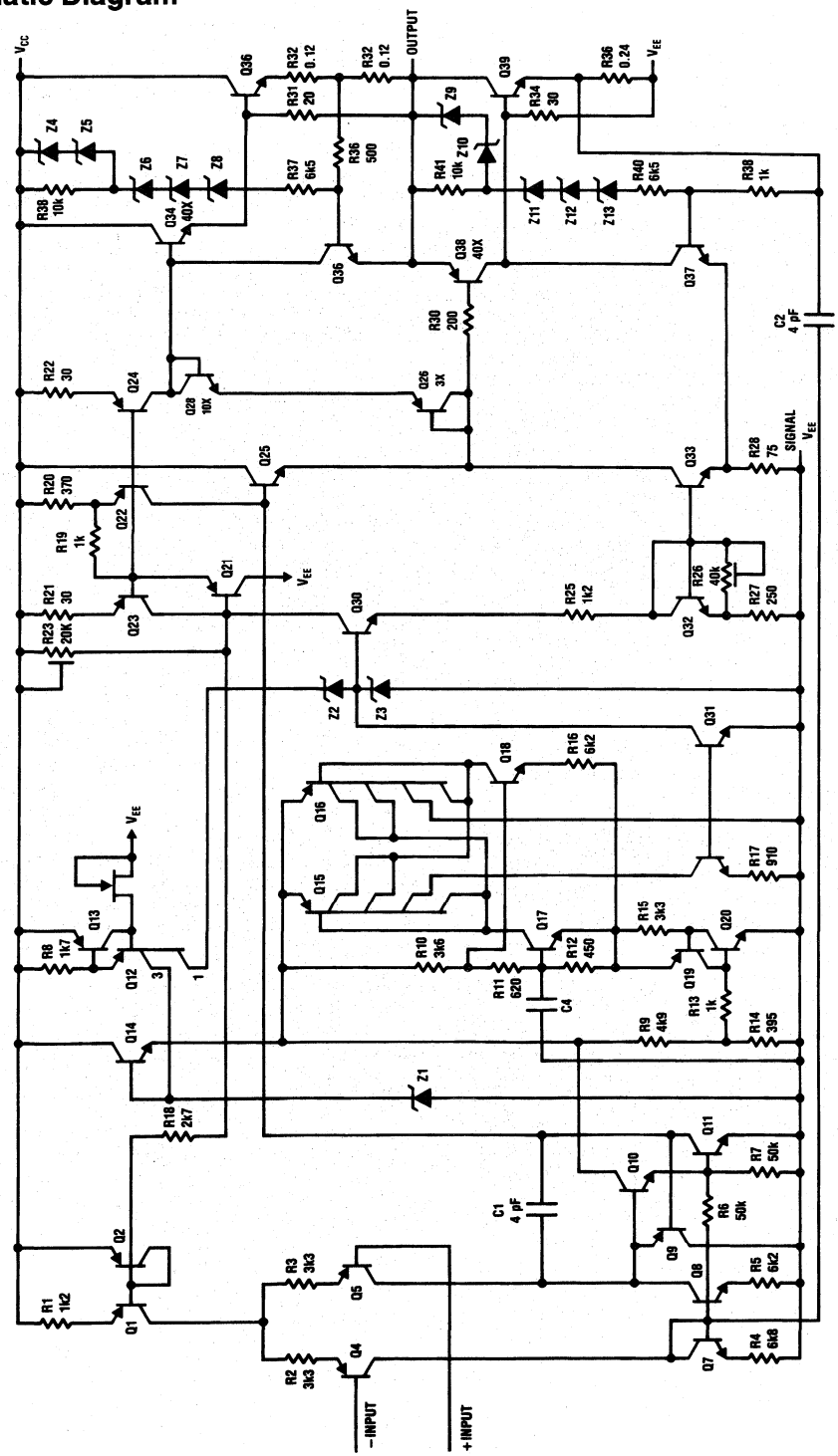


Output Voltage Swing vs Supply Voltage



TL/H/6739–4

Schematic Diagram



Application Hints

STABILITY

The LM675 is designed to be stable when operated at a closed-loop gain of 10 or greater, but, as with any other high-current amplifier, the LM675 can be made to oscillate under certain conditions. These usually involve printed circuit board layout or output/input coupling.

When designing a printed circuit board layout, it is important to return the load ground, the output compensation ground, and the low level (feedback and input) grounds to the circuit board ground point through separate paths. Otherwise, large currents flowing along a ground conductor will generate voltages on the conductor which can effectively act as signals at the input, resulting in high frequency oscillation or excessive distortion. It is advisable to keep the output compensation components and the 0.1 μF supply decoupling capacitors as close as possible to the LM675 to reduce the effects of PCB trace resistance and inductance. For the same reason, the ground return paths for these components should be as short as possible.

Occasionally, current in the output leads (which function as antennas) can be coupled through the air to the amplifier input, resulting in high-frequency oscillation. This normally happens when the source impedance is high or the input leads are long. The problem can be eliminated by placing a small capacitor (on the order of 50 pF to 500 pF) across the circuit input.

Most power amplifiers do not drive highly capacitive loads well, and the LM675 is no exception. If the output of the LM675 is connected directly to a capacitor with no series resistance, the square wave response will exhibit ringing if the capacitance is greater than about 0.1 μF. The amplifier can typically drive load capacitances up to 2 μF or so without oscillating, but this is not recommended. If highly capacitive loads are expected, a resistor (at least 1Ω) should be placed in series with the output of the LM675. A method commonly employed to protect amplifiers from low impedances at high frequencies is to couple to the load through a 10Ω resistor in parallel with a 5 μH inductor.

CURRENT LIMIT AND SAFE OPERATING AREA (SOA) PROTECTION

A power amplifier's output transistors can be damaged by excessive applied voltage, current flow, or power dissipation. The voltage applied to the amplifier is limited by the design of the external power supply, while the maximum current passed by the output devices is usually limited by internal circuitry to some fixed value. Short-term power dissipation is usually not limited in monolithic operational power amplifiers, and this can be a problem when driving reactive loads, which may draw large currents while high voltages appear on the output transistors. The LM675 not only limits current to around 4A, but also reduces the value of the limit current when an output transistor has a high voltage across it.

When driving nonlinear reactive loads such as motors or loudspeakers with built-in protection relays, there is a possibility that an amplifier output will be connected to a load whose terminal voltage may attempt to swing beyond the power supply voltages applied to the amplifier. This can cause degradation of the output transistors or catastrophic failure of the whole circuit. The standard protection for this type of failure mechanism is a pair of diodes connected between the output of the amplifier and the supply rails. These are part of the internal circuitry of the LM675, and needn't be added externally when standard reactive loads are driven.

THERMAL PROTECTION

The LM675 has a sophisticated thermal protection scheme to prevent long-term thermal stress to the device. When the temperature on the die reaches 170°C, the LM675 shuts down. It starts operating again when the die temperature drops to about 145°C, but if the temperature again begins to rise, shutdown will occur at only 150°C. Therefore, the device is allowed to heat up to a relatively high temperature if the fault condition is temporary, but a sustained fault will limit the maximum die temperature to a lower value. This greatly reduces the stresses imposed on the IC by thermal cycling, which in turn improves its reliability under sustained fault conditions. This circuitry is 100% tested without a heat sink.

Since the die temperature is directly dependent upon the heat sink, the heat sink should be chosen for thermal resistance low enough that thermal shutdown will not be reached during normal operaton. Using the best heat sink possible within the cost and space constraints of the system will improve the long-term reliability of any power semiconductor.

POWER DISSIPATION AND HEAT SINKING

The LM675 should always be operated with a heat sink, even though at idle worst case power dissipation will be only 1.8W (30 mA $\times$ 60V) which corresponds to a rise in die temperature of 97°C above ambient assuming θ_{jA} = 54°C/W for a TO-220 package. This in itself will not cause the thermal protection circuitry to shut down the amplifier when operating at room temperature, but a mere 0.9W of additional power dissipation will shut the amplifier down since T_J will then increase from 122°C (97°C + 25°C) to 170°C.

In order to determine the appropriate heat sink for a given application, the power dissipation of the LM675 in that application must be known. When the load is resistive, the maximum average power that the IC will be required to dissipate is approximately:

$$P_{D\,(MAX)} \approx \frac{V_S^2}{2\pi^2 R_L} + P_Q$$

where V_S is the total power supply voltage across the LM675, R_L is the load resistance and P_Q is the quiescent power dissipation of the amplifier. The above equation is only an approximation which assumes an "ideal" class B output stage and constant power dissipation in all other parts of the circuit. As an example, if the LM675 is operated on a 50V power supply with a resistive load of 8Ω, it can develop up to 19W of internal power dissipation. If the die temperature is to remain below 150°C for ambient temperatures up to 70°C, the total junction-to-ambient thermal resistance must be less than

$$\frac{150°C - 70°C}{19W} = 4.2°C/W.$$

Using θ_{JC} = 2°C/W, the sum of the case-to-heat sink interface thermal resistance and the heat-sink-to-ambient

Application Hints (Continued)

thermal resistance must be less than 2.2°C/W. The case-to-heat-sink thermal resistance of the TO-220 package varies with the mounting method used. A metal-to-metal interface will be about 1°C/W if lubricated, and about 1.2°C/W if dry. If a mica insulator is used, the thermal resistance will be about 1.6°C/W lubricated and 3.4°C/W dry. For this example, we assume a lubricated mica insulator between the LM675 and the heat sink. The heat sink thermal resistance must then be less than

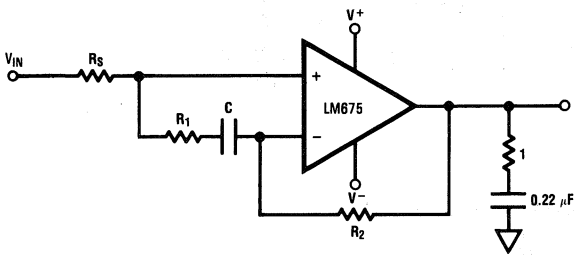
$$4.2°C/W - 2°C/W - 1.6°C/W = 0.6°C/W.$$

This is a rather large heat sink and may not be practical in some applications. If a smaller heat sink is required for reasons of size or cost, there are two alternatives. The maximum ambient operating temperature can be restricted to 50°C (122°F), resulting in a 1.6°C/W heat sink, or the heat sink can be isolated from the chassis so the mica washer is not needed. This will change the required heat sink to a 1.2°C/W unit if the case-to-heat-sink interface is lubricated.

The thermal requirements can become more difficult when an amplifier is driving a reactive load. For a given magnitude of load impedance, a higher degree of reactance will cause a higher level of power dissipation within the amplifier. As a general rule, the power dissipation of an amplifier driving a 60° reactive load will be roughly that of the same amplifier driving the resistive part of that load. For example, some reactive loads may at some frequency have an impedance with a magnitude of 8Ω and a phase angle of 60°. The real part of this load will then be 8Ω × cos 60° or 4Ω, and the amplifier power dissipation will roughly follow the curve of power dissipation with a 4Ω load.

Typical Applications (Continued)

Non-Inverting Unity Gain Operation



TL/H/6739–6

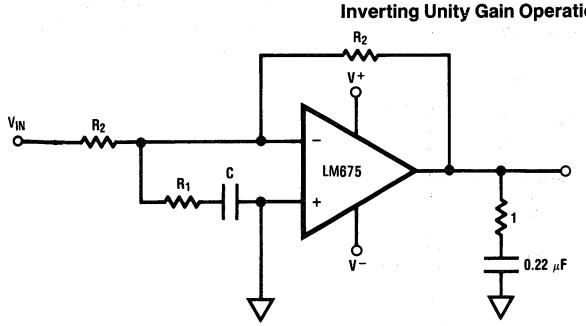
$$R_1C \geq \frac{1}{2\pi 500\ kHz}$$

$$R_1 \leq \frac{R_S + R_2}{10}$$

$$A_{V(DC)} = 1$$

UNITY GAIN BANDWIDTH ≅ 50 kHz

Inverting Unity Gain Operation



TL/H/6739–7

$$R_1C \geq \frac{1}{2\pi 500\ kHz}$$

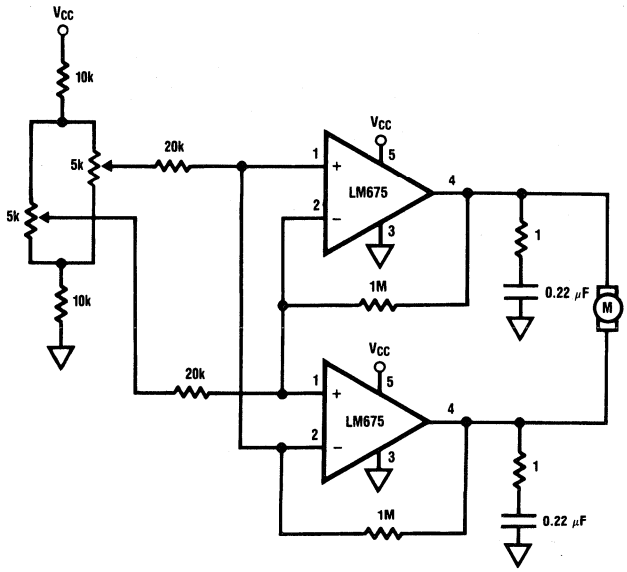
$$R_1 \leq \frac{R_2}{10}$$

$$A_{V(DC)} = -1$$

UNITY GAIN BANDWIDTH ≅ 50 kHz

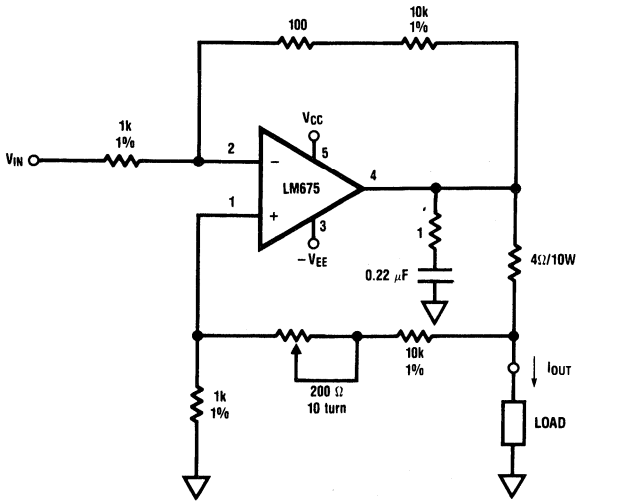
Typical Applications (Continued)

Servo Motor Control



TL/H/6739–8

High Current Source/Sink



TL/H/6739–9

$I_{OUT} = V_{IN} \times 2.5$ amps/volt
i.e. $I_{OUT} = 1A$ when $V_{IN} = 400$ mV
Trim pot for max R_{OUT}

National Semiconductor

LM709
Operational Amplifier

General Description

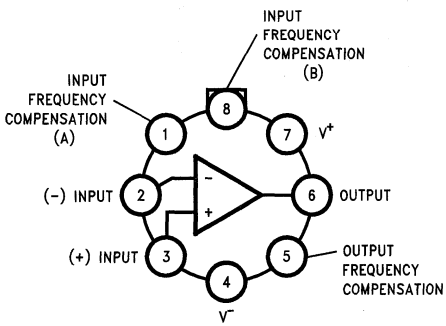
The LM709 series is a monolithic operational amplifier intended for general-purpose applications. Operation is completely specified over the range of voltages commonly used for these devices. The design, in addition to providing high gain, minimizes both offset voltage and bias currents. Further, the class-B output stage gives a large output capability with minimum power drain.

External components are used to frequency compensate the amplifier. Although the unity-gain compensation network specified will make the amplifier unconditionally stable in all feedback configurations, compensation can be tailored to optimize high-frequency performance for any gain setting.

The LM709C is the commercial-industrial version of the LM709. It is identical to the LM709 except that it is specified for operation from 0°C to +70°C.

Connection Diagrams

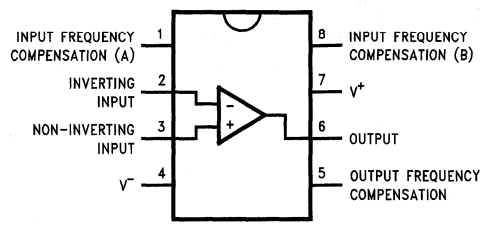
Metal Can Package



TL/H/11477–4

Order Number LM709AH, LM709H or LM709CH
See NS Package Number H08C

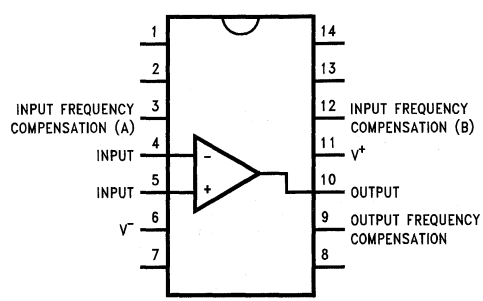
Dual-In-Line Package



TL/H/11477–6

Order Number LM709CN-8
See NS Package Number N08E

Dual-In-Line Package



TL/H/11477–5

Order Number LM709CN
See NS Package Number N14A

Absolute Maximum Ratings (Note 3)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage
LM709/LM709A/LM709C ±18V

Power Dissipation (Note 1)
LM709/LM709A 300 mW
LM709C 250 mW

Differential Input Voltage
LM709/LM709A/LM709C ±5V

Input Voltage
LM709/LM709A/LM709C ±10V

Output Short-Circuit Duration (T_A = +25°C)
LM709/LM709A/LM709C 5 seconds

Storage Temperature Range
LM709/LM709A/LM709C −65°C to +150°C

Lead Temperature (Soldering, 10 sec.)
LM709/LM709A/LM709C 300°C

Operating Ratings (Note 3)

Junction Temperature Range (Note 1)
LM709/LM709A −55°C to +150°C
LM709C 0°C to +100°C

Thermal Resistance (θ_{JA})
H Package 150°C/W, (θ_{JC}) 45°C/W
8-Pin N Package 134°C/W
14-Pin N Package 109°C/W

Electrical Characteristics (Note 2)

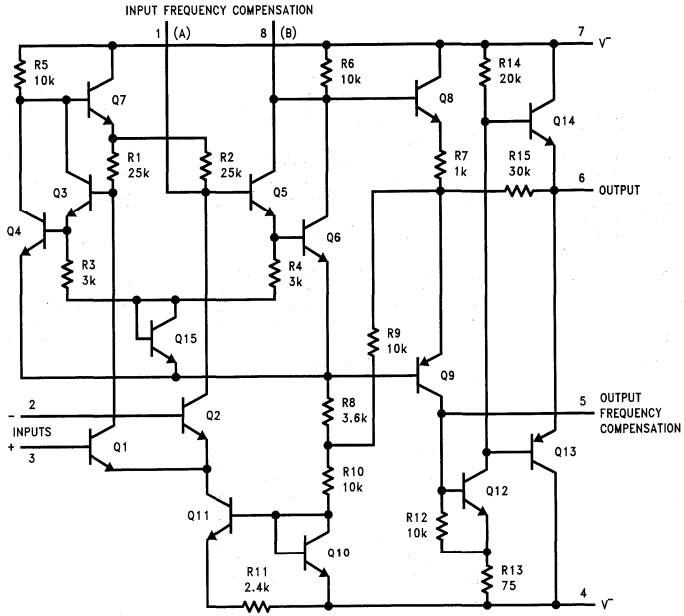
Parameter	Conditions	LM709A			LM709			LM709C			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	T_A = 25°C, $R_S \le 10\ k\Omega$		0.6	2.0		1.0	5.0		2.0	7.5	mV
Input Bias Current	T_A = 25°C		100	200		200	500		300	1500	nA
Input Offset Current	T_A = 25°C		10	50		50	200		100	500	nA
Input Resistance	T_A = 25°C	350	700		150	400		50	250		kΩ
Output Resistance	T_A = 25°C		150			150			150		Ω
Supply Current	T_A = 25°C, V_S = ±15V		2.5	3.6		2.6	5.5		2.6	6.6	mA
Transient Response Risetime Overshoot	V_{IN} = 20 mV, $C_L \le 100$ pF T_A = 25°C			1.5 30		0.3 10	1.0 30		0.3 10	1.0 30	 µs %
Slew Rate	T_A = 25°C		0.25			0.25			0.25		V/µs
Input Offset Voltage	$R_S \le 10\ k\Omega$			3.0			6.0			10	mV
Average Temperature Coefficient of Input Offset Voltage	R_S = 50Ω, T_A = 25°C to T_{MAX} T_A = 25°C to T_{MIN} R_S = 10 kΩ, T_A = 25°C to T_{MAX} T_A = 25°C to T_{MIN}		1.8 1.8 2.0 4.8	10 10 15 25		3.0 6.0			6.0 12		µV/°C
Large Signal Voltage Gain	V_S = ±15V, $R_L \ge 2\ k\Omega$ V_{OUT} = ±10V	25		70	25	45	70	15	45		V/mV
Output Voltage Swing	V_S = ±15V, R_L = 10 kΩ V_S = ±15V, R_L = 2 kΩ	±12 ±10	±14 ±13		±12 ±10	±14 ±13		±12 ±10	±14 ±13		V
Input Voltage Range	V_S = ±15V	±8			±8	±10		±8	±10		V
Common-Mode Rejection Ratio	$R_S \le 10\ k\Omega$	80	110		70	90		65	90		dB
Supply Voltage Rejection Ratio	$R_S \le 10\ k\Omega$		40	100		25	150		25	200	µV/V
Input Offset Current	$T_A = T_{MAX}$ $T_A = T_{MIN}$		3.5 40	50 250		20 100	200 500		75 125	400 750	nA
Input Bias Current	$T_A = T_{MIN}$		0.3	0.6		0.5	1.5		0.36	2.0	µA
Input Resistance	$T_A = T_{MIN}$	85	170		40	100		50	250		kΩ

Note 1: For operating at elevated temperatures, the device must be derated based on a 150°C maximum junction temperature for LM709/LM709A and 100°C maximum for L709C. For operating at elevated temperatures, the device must be derated based on thermal resistance θ_{JA}, $T_{J(MAX)}$ and T_A.

Note 2: These specifications apply for $-55°C \le T_A \le +125°C$ for the LM709/LM709A and $0°C \le T_A \le +70°C$ for the LM709C with the following conditions: $\pm 9V \le V_S \le \pm 15V$, C1 = 5000 pF, R1 = 1.5 kΩ, C2 = 200 pF and R2 = 51Ω.

Note 3: Absolute Maximum Ratings indicate limits which if exceeded may result in damage. Operating Ratings are conditions where the device is expected to be functional but not necessarily within the guaranteed performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics.

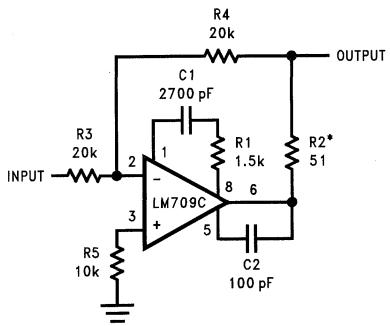
Schematic Diagram**



TL/H/11477–1

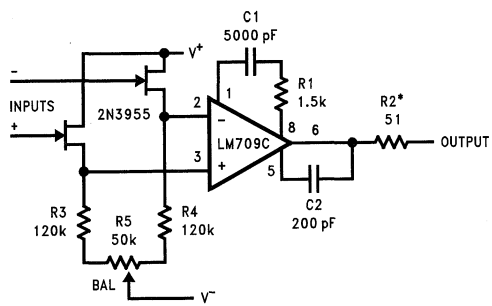
Typical Applications**

Unity Gain Inverting Amplifier



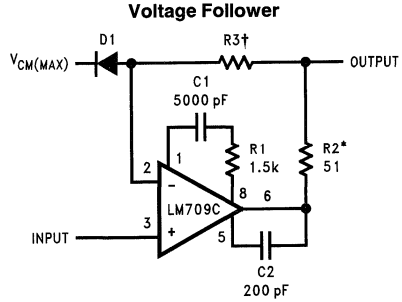
TL/H/11477–2

FET Operational Amplifier



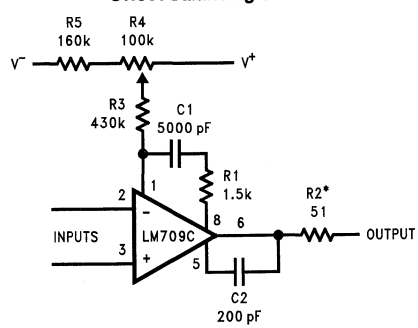
TL/H/11477–3

Voltage Follower



TL/H/11477–7

Offset Balancing Circuit



TL/H/11477–8

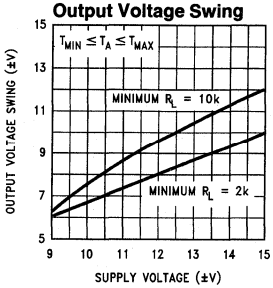
*To be used with any capacitive loading on output.

**Pin connections shown are for metal can package.

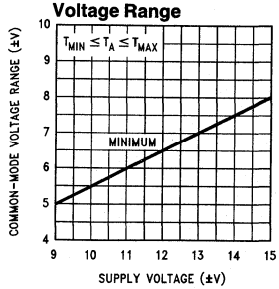
†Should be equal to DC source resistance on input.

Guaranteed Performance Characteristics

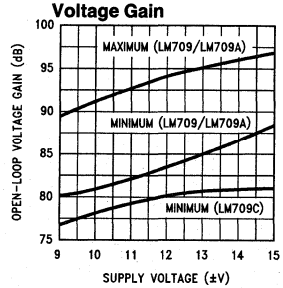
Output Voltage Swing



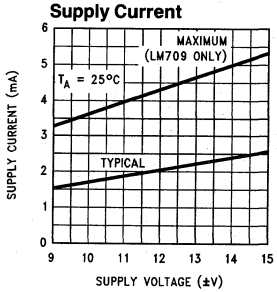
Input Common-Mode Voltage Range



Voltage Gain



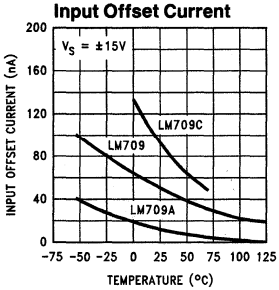
Supply Current



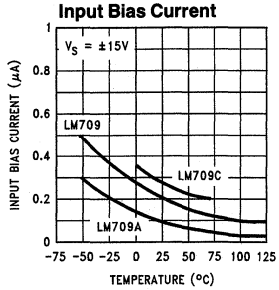
TL/H/11477–9

Typical Performance Characteristics

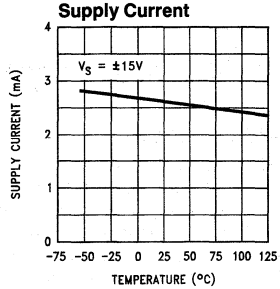
Input Offset Current



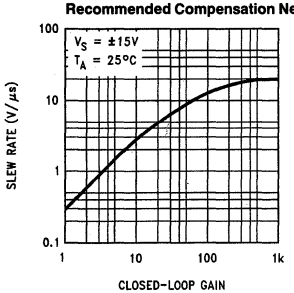
Input Bias Current



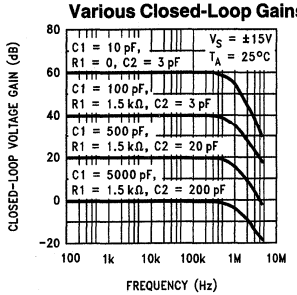
Supply Current



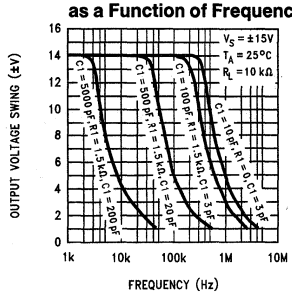
Slew Rate as a Function of Closed-Loop Gain Using Recommended Compensation Networks



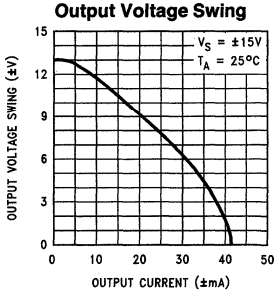
Frequency Response for Various Closed-Loop Gains



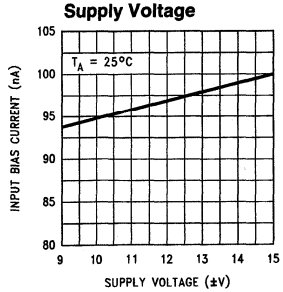
Output Voltage Swing as a Function of Frequency



Output Voltage Swing



Input Bias Current as a Function of Supply Voltage



TL/H/11477–10

National Semiconductor

LM715
High Speed Operational Amplifier

General Description

The LM715 is a high speed, high gain, monolithic operational amplifier intended for use in a wide range of applications where fast signal acquisition or wide bandwidth is required. The LM715 features fast settling time, high slew rate, low offsets, and high output swing for large signal applications. In addition, the device displays excellent temperature stability and will operate over a wide range of supply voltages.

Features

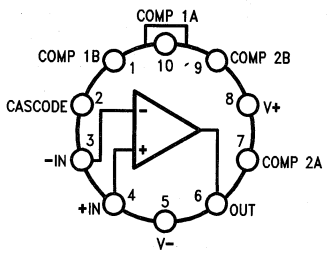
- High slew rate— 100 V/μs (Inverting, A_V = 1) typically
- Fast settling time— 800 ns typically
- Wide bandwidth— 65 MHz typically
- Wide operating supply range
- Wide input voltage ranges

Applications

- Video amplifiers
- Active filters
- High speed data conversion

Connection Diagrams

10-Lead Metal Package



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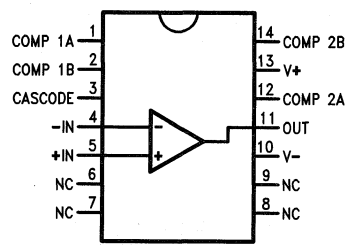
Top View

Lead 5 connected to case.

14-Lead DIP



TL/H/10059-2

Top View

Ordering Information

Device Code	Package Code	Package Description
LM715MH	H10C	Metal
LM715CH	H10C	Metal
LM715MJ	J14A	Ceramic DIP
LM715CJ	J14A	Ceramic DIP

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature Range	−65°C to +175°C
Operating Temperature Range	
Extended (LM715M)	−55°C to +125°C
Commercial (LM715C)	0°C to +70°C
Lead Temperature	
Metal Can and Ceramic DIP (Soldering, 60 sec.)	300°C
Internal Power Dissipation (Notes 1, 2)	
10L-Metal Can	1.07W
14L-Ceramic DIP	1.36W
Supply Voltage	±18V
Differential Input Voltage	±5V
Input Voltage (Note 3)	±15V

LM715M and LM715C Electrical Characteristics

$T_A = 25°C$, $V_{CC} = \pm 15V$, unless otherwise specified

Symbol	Parameter		Conditions	LM715M			LM715C			Units
				Min	Typ	Max	Min	Typ	Max	
V_{IO}	Input Offset Voltage		$R_S \le 10\ k\Omega$		2.0	5.0		2.0	7.5	mV
I_{IO}	Input Offset Current				70	250		70	250	nA
I_{IB}	Input Bias Current				400	750		400	1500	nA
Z_I	Input Impedance				1.0			1.0		MΩ
R_O	Output Resistance				75			75		Ω
I_{CC}	Supply Current				5.5	7.0		5.5	10	mA
P_c	Power Consumption				165	210		165	300	mW
V_{IR}	Input Voltage Range			±10	±12		±10	±12		V
A_{VS}	Large Signal Voltage Gain		$R_L \ge 2.0\ k\Omega$, $V_O = \pm 10V$	15	30		10	30		V/mV
V	Settling Time		$V_O = \pm 5.0V$, $A_V = 1.0$		800			800		ns
TR	Transient Response	Rise Time	$V_I = 400\ mV$, $A_V = 1.0$		30	60		30	75	ns
		Overshoot			25	40		25	50	%
SR	Slew Rate		$A_V = 100$		70			70		V/μs
			$A_V = 10$		38			38		
			$A_V = 1.0$ (Non-Inverting)	15	18		10	18		
			$A_V = 1.0$ (Inverting)		100			100		

The following specifications apply over the range of $-55°C \le T_A \le +125°C$ for the LM715M, and $0°C \le T_A \le +70°C$ for the LM715C

Symbol	Parameter	Conditions	LM715M			LM715C			Units
			Min	Typ	Max	Min	Typ	Max	
V_{IO}	Input Offset Voltage	$R_S \le 10\ k\Omega$			7.5			10	mV
I_{IO}	Input Offset Current	$T_A = T_{A\ Max}$			250			250	nA
		$T_A = T_{A\ Min}$			800			750	
I_{IB}	Input Bias Current	$T_A = T_{A\ Max}$			0.75			1.5	μA
		$T_A = T_{A\ Min}$			4.0			7.5	
CMR	Common Mode Rejection	$R_S \le 10\ k\Omega$	74	92		74 (Note 4)	92 (Note 4)		dB
PSRR	Power Supply Rejection Ratio	$R_S \le 10\ k\Omega$		45	300		45 (Note 4)	400 (Note 4)	μV/V
A_{VS}	Large Signal Voltage Gain	$R_L \ge 2.0\ k\Omega$, $V_O = \pm 10V$	10			8			V/mV
V_{OP}	Output Voltage Swing	$R_L = 2.0\ k\Omega$	±10	±13		±10	±13		V

Note 1: $T_{J\ Max} = 175°C$.

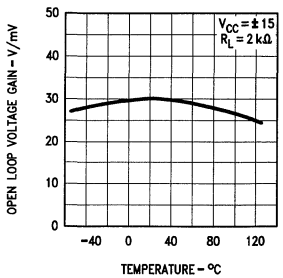
Note 2: Ratings apply to ambient temperature at 25°C. Above this temperature, derate the 10L-Metal Can at 7.1 mW/°C, and the 14L-Ceramic DIP at 9.1 mW/°C.

Note 3: For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

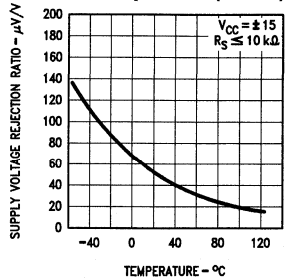
Note 4: $T_A = 25°C$ only.

Typical Performance Characteristics for LM715M and LM715C

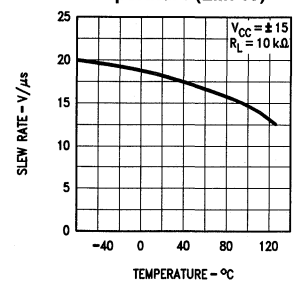
Voltage Gain vs Temperature (LM715)



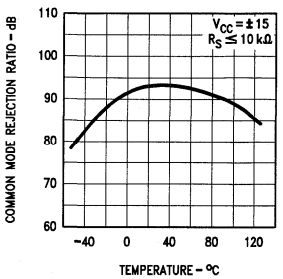
Supply Voltage Rejection Ratio vs Temperature (LM715)



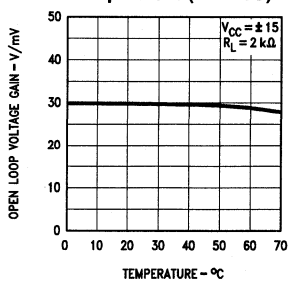
Slew Rate vs Temperature (LM715)



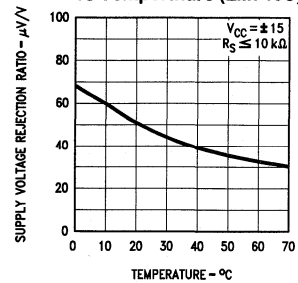
Common Mode Rejection Ratio vs Temperature (LM715)



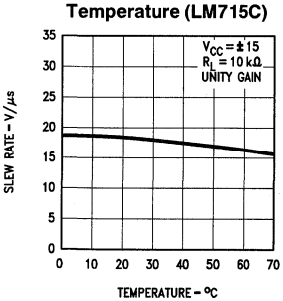
Voltage Gain vs Temperature (LM715C)



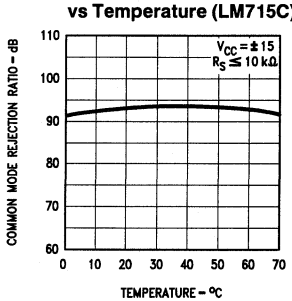
Supply Voltage Rejection Ratio vs Temperature (LM715C)



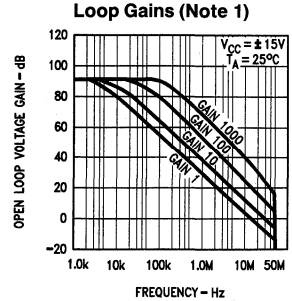
Slew Rate vs Temperature (LM715C)



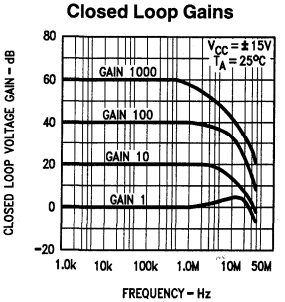
Common Mode Rejection Ratio vs Temperature (LM715C)



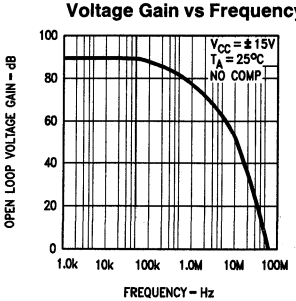
Frequency Response for Open Loop Gains (Note 1)



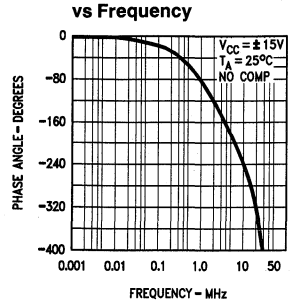
Frequency Response for Closed Loop Gains



Voltage Gain vs Frequency



Open Loop Phase vs Frequency



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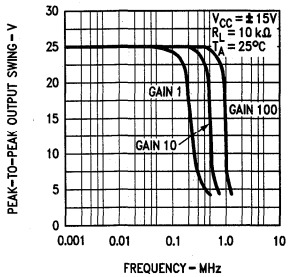
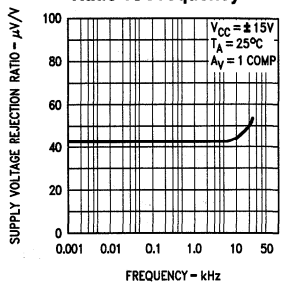
Note 1: See "Non-Inverting Compensation Components Value Table" for Closed Loop Gain values.

Typical Performance Characteristics for LM715M and LM715C (Continued)

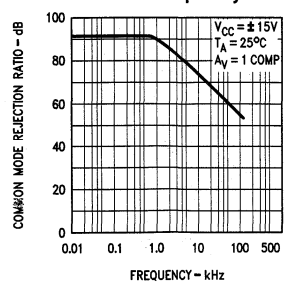
Output Swing vs Frequency for Closed Loop Gains



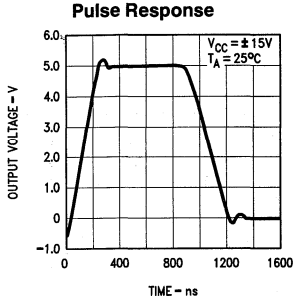
Supply Voltage Rejection Ratio vs Frequency



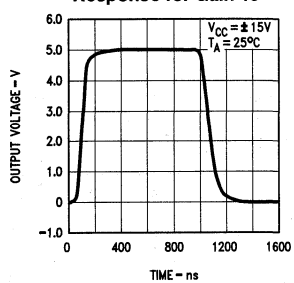
Common Mode Rejection Ratio vs Frequency



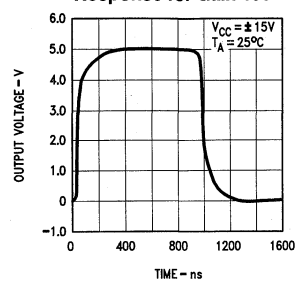
Unity Gain Large Signal Pulse Response



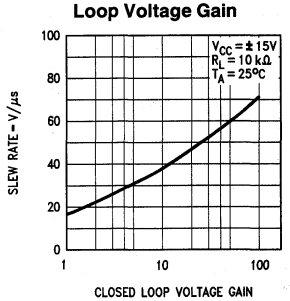
Large Signal Pulse Response for Gain 10



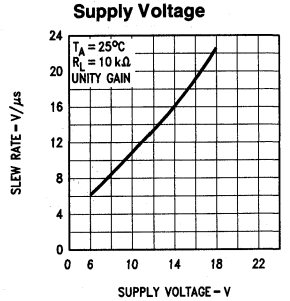
Large Signal Pulse Response for Gain 100



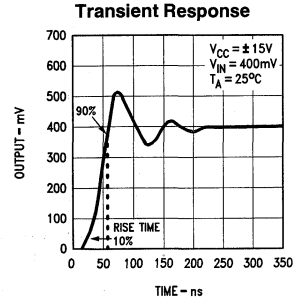
Slew Rate vs Closed Loop Voltage Gain



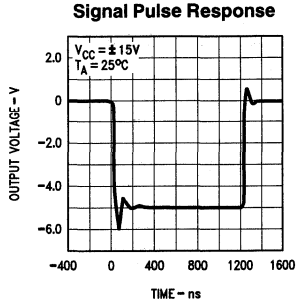
Slew Rate vs Supply Voltage



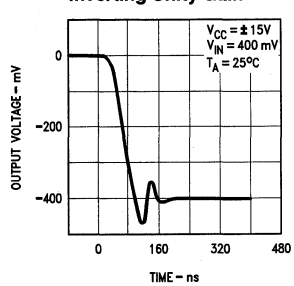
Voltage Follower Transient Response



Inverting Unity Gain Large Signal Pulse Response



Small Signal Pulse Response Inverting Unity Gain



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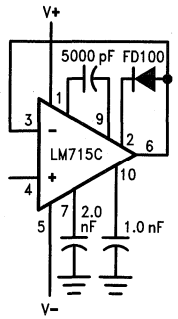
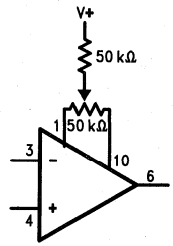
Typical Performance Characteristics for LM715M and LM715C (Continued)

Voltage Follower (Note 2)



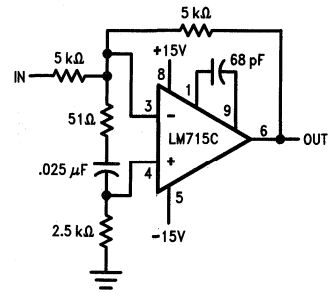
TL/H/10059–6

Voltage Offset Null Circuit (Note 2)



TL/H/10059–7

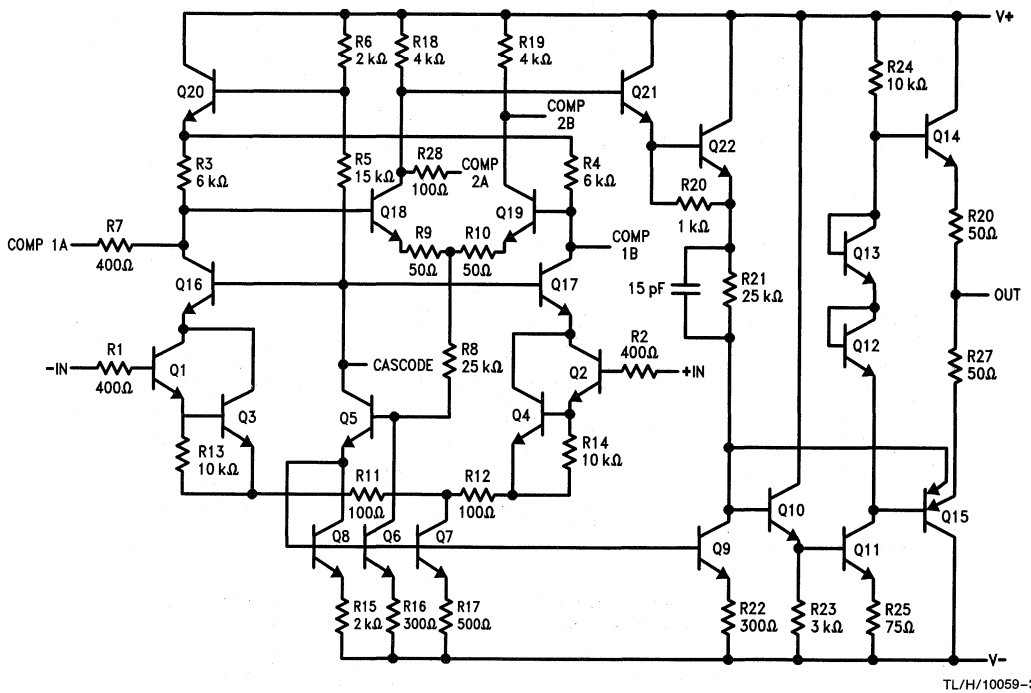
High Slew Rate Circuit (Note 2)



TL/H/10059–8

Note 2: Lead numbers apply to metal package.

Equivalent Circuit



TL/H/10059–3

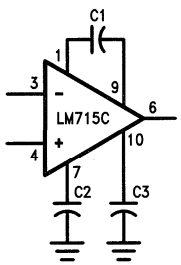
Applications Information

Non-Inverting Compensation Components Values

Closed Loop Gain	C1	C2	C3
1000	10 pF		
100	50 pF		250 pF
10 (Note)	100 pF	500 pF	1000 pF
1	500 pF	2000 pF	1000 pF

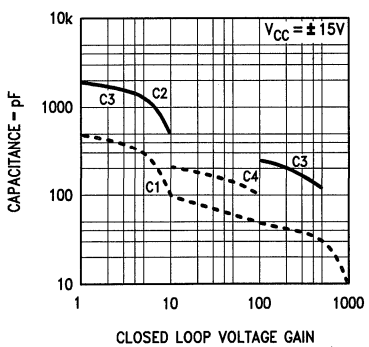
Note: For gain 10, compensation may be simplified by removing C2, C3 and adding a 200 pF capacitor (C4) between Lead 7 and 10.

Frequency Compensation Circuit



TL/H/10059–9

Suggested Values of Compensation Capacitors vs Closed Loop Voltage Gain



TL/H/10059–10

Layout Instructions

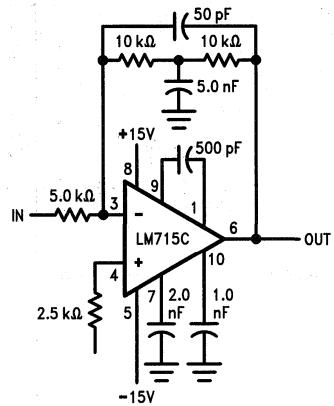
Layout—The layout should be such that stray capacitance is minimal.

Supplies—The supplies should be adequately bypassed. Used of 0.1 μF high quality ceramic capacitors is recommended.

Ringing—Excessive ringing (long acquisition time) may occur with large capacitive loads. This may be reduced by isolating the capacitive load with a resistance of 100Ω. Large source resistances may also give rise to the same problem and this may be decreased by the addition of a capacitance across the feedback resistance. A value of around 50 pF for unity gain configuration and around 3.0 pF for gain 10 should be adequate.

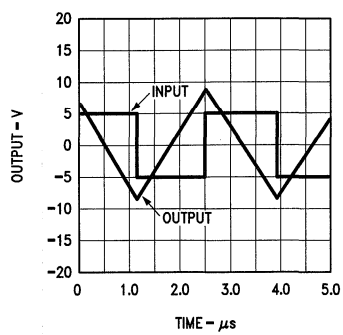
Latch Up—This may occur when the amplifier is used as a voltage follower. The inclusion of a diode between leads 6 and 2 with the cathode toward lead 2 is the recommended preventive measure.

Typical Applications



TL/H/10059–14

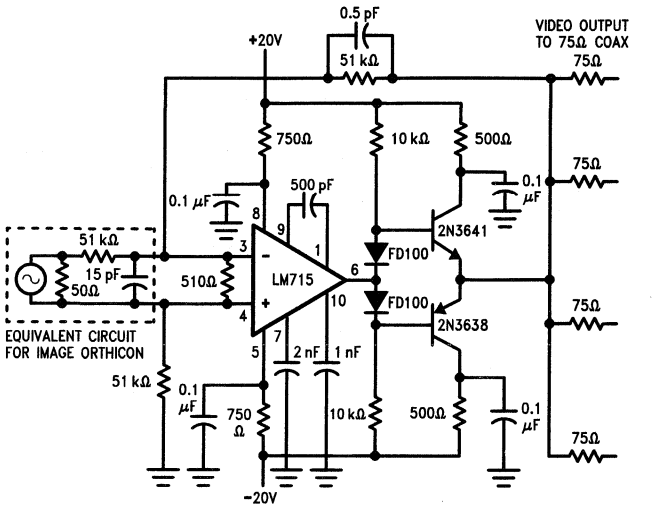
High Speed Integrator



TL/H/10059–13

Note: All lead numbers on this page apply to metal package.

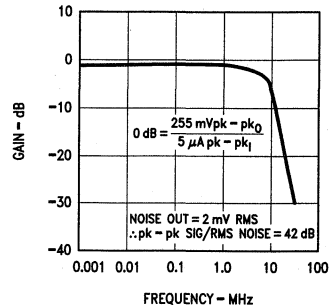
Typical Applications (Continued)



TL/H/10059–12

Note: All lead numbers shown refer to metal package.

Wide Band Video Amplifier Drive Capability with 75Ω Coax Cable



TL/H/10059–11

National Semiconductor

LM725 Operational Amplifier

General Description

The LM725/LM725A/LM725C are operational amplifiers featuring superior performance in applications where low noise, low drift, and accurate closed-loop gain are required. With high common mode rejection and offset null capability, it is especially suited for low level instrumentation applications over a wide supply voltage range.

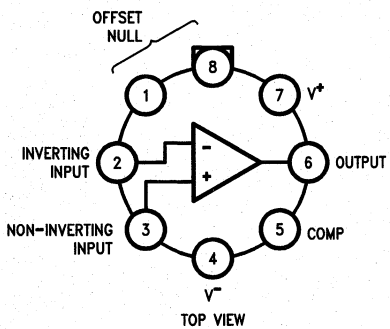
The LM725A has tightened electrical performance with higher input accuracy and like the LM725, is guaranteed over a −55°C to +125°C temperature range. The LM725C has slightly relaxed specifications and has its performance guaranteed over a 0°C to 70°C temperature range.

Features

■ High open loop gain	3,000,000
■ Low input voltage drift	0.6 μV/°C
■ High common mode rejection	120 dB
■ Low input noise current	0.15 pA/$\sqrt{Hz}$
■ Low input offset current	2 nA
■ High input voltage range	±14V
■ Wide power supply range	±3V to ±22V
■ Offset null capability	
■ Output short circuit protection	

Connection Diagrams and Ordering Information

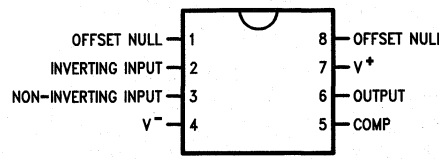
Metal Can Package



TL/H/10474–1

Order Number LM725H, LM725H/883, LM725AH, LM725CH or LM725AH/883
See NS Package Number H08C

Dual-In-Line Package



TL/H/10474–2

Order Number LM725CN
See NS Package Number N08E

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	±22V
Internal Power Dissipation (Note 1)	500 mW
Differential Input Voltage	±5V
Input Voltage (Note 2)	±22V

Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 Sec.)	260°C
Maximum Junction Temperature	150°C

Operating Temperature Range	$T_{A(MIN)}$		$T_{A(MAX)}$
LM725	−55°C	to	+125°C
LM725A	−55°C	to	+125°C
LM725C	0°C	to	+70°C

Electrical Characteristics (Note 3)

Parameter	Conditions	LM725A			LM725			LM725C			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage (Without External Trim)	T_A = 25°C, $R_S \leq 10\ k\Omega$			0.5		0.5	1.0		0.5	2.5	mV
Input Offset Current	T_A = 25°C		2.0	5.0		2.0	20		2.0	35	nA
Input Bias Current	T_A = 25°C		42	80		42	100		42	125	nA
Input Noise Voltage	T_A = 25°C f_o = 10 Hz f_o = 100 Hz f_o = 1 kHz		 15 9.0 8.0			 15 9.0 8.0			 15 9.0 8.0		 nV/√Hz nV/√Hz nV/√Hz
Input Noise Current	T_A = 25°C f_o = 10 Hz f_o = 100 Hz f_o = 1 kHz		 1.0 0.3 0.15			 1.0 0.3 0.15			 1.0 0.3 0.15		 pA/√Hz pA/√Hz pA/√Hz
Input Resistance	T_A = 25°C		1.5			1.5			1.5		MΩ
Input Voltage Range	T_A = 25°C	±13.5	±14		±13.5	±14		±13.5	±14		V
Large Signal Voltage Gain	T_A = 25°C, $R_L \geq 2\ k\Omega$, V_{OUT} = ±10V	1000	3000		1000	3000		250	3000		V/mV
Common-Mode Rejection Ratio	T_A = 25°C, $R_S \leq 10\ k\Omega$	120			110	120		94	120		dB
Power Supply Rejection Ratio	T_A = 25°C, $R_S \leq 10\ k\Omega$		2.0	5.0		2.0	10		2.0	35	μV/V
Output Voltage Swing	T_A = 25°C, $R_L \geq 10\ k\Omega$ $R_L \geq 2\ k\Omega$	 ±12.5 ±12.0	 ±13.5 ±13.5		 ±12 ±10	 ±13.5 ±13.5		 ±12 ±10	 ±13.5 ±13.5		 V V
Power Consumption	T_A = 25°C		80	105		80	105		80	150	mW
Input Offset Voltage (Without External Trim)	$R_S \leq 10\ k\Omega$			0.7			1.5			3.5	mV
Average Input Offset Voltage Drift (Without External Trim)	R_S = 50Ω			2.0		2.0	5.0		2.0		μV/°C
Average Input Offset Voltage Drift (With External Trim)	R_S = 50Ω		0.6	1.0		0.6			0.6		μV/°C
Input Offset Current	$T_A = T_{MAX}$ $T_A = T_{MIN}$		1.2 7.5	4.0 18.0		1.2 7.5	20 40		1.2 4.0	35 50	nA nA
Average Input Offset Current Drift			35	90		35	150		10		pA/°C
Input Bias Current	$T_A = T_{MAX}$ $T_A = T_{MIN}$		20 80	70 180		20 80	100 200			125 250	nA nA

Electrical Characteristics (Note 3) (Continued)

Parameter	Conditions	LM725A			LM725			LM725C			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Large Signal Voltage Gain	$R_L \geq 2\ k\Omega$ $T_A = T_{MAX}$	1,000,000			1,000,000			125,000			V/V
	$R_L \geq 2\ k\Omega$ $T_A = T_{MIN}$	500,000			250,000			125,000			V/V
Common-Mode Rejection Ratio	$R_S \leq 10\ k\Omega$	110			100				115		dB
Power Supply Rejection Ratio	$R_S \leq 10\ k\Omega$			8.0			20		20		μV/V
Output Voltage Swing	$R_L \geq 2\ k\Omega$	±12			±10			±10			V

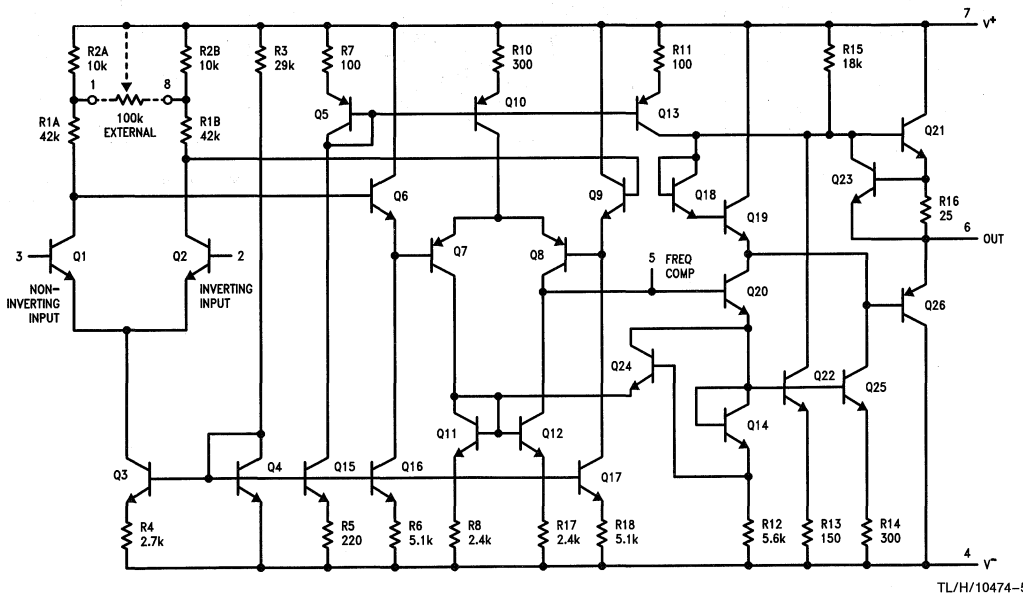
Note 1: Derate at 150°C/W for operation at ambient temperatures above 75°C.

Note 2: For supply voltages less than ±22V, the absolute maximum input voltage is equal to the supply voltage.

Note 3: These specifications apply for V_S = ±15V unless otherwise specified.

Note 4: For Military electrical specifications RETS725AX are available for LM725AH and RETS725X are available for LM725H.

Schematic Diagram



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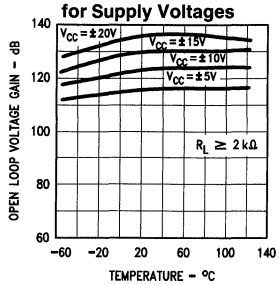
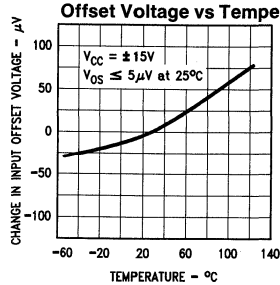
Typical Performance Characteristics

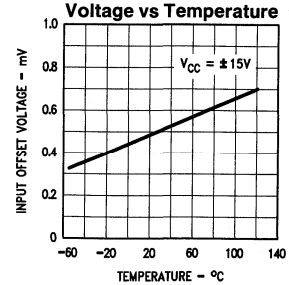
Voltage Gain vs Temperature for Supply Voltages



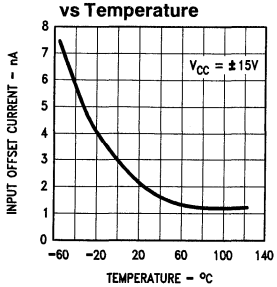
Change in Trimmed Input Offset Voltage vs Temperature



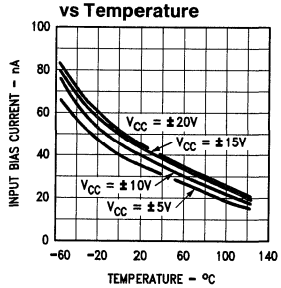
Untrimmed Input Offset Voltage vs Temperature



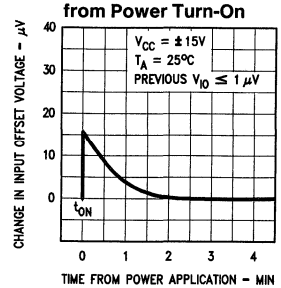
Input Offset Current vs Temperature



Input Bias Current vs Temperature



Stabilization Time of Input Offset Voltage from Power Turn-On



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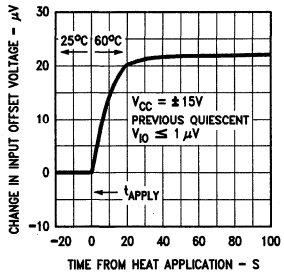
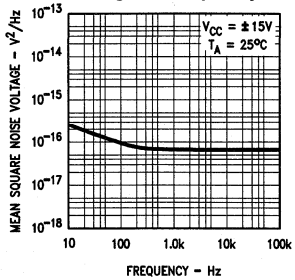
Typical Performance Characteristics (Continued)

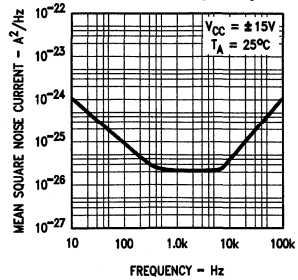
Change in Input Offset Voltage Due to Thermal Shock vs Time



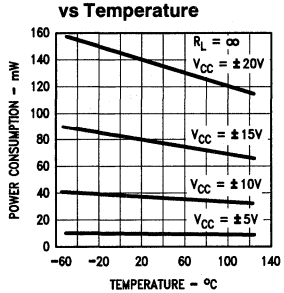
Input Noise Voltage vs Frequency



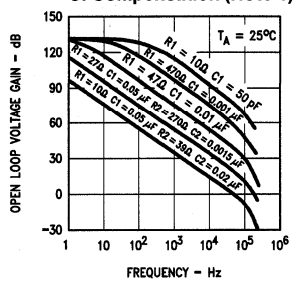
Input Noise Current vs Frequency



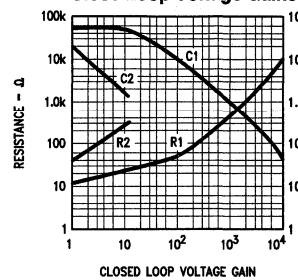
Power Consumption vs Temperature



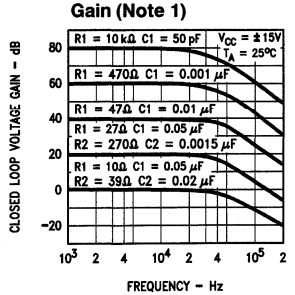
Open Loop Frequency Response for Values of Compensation (Note 1)



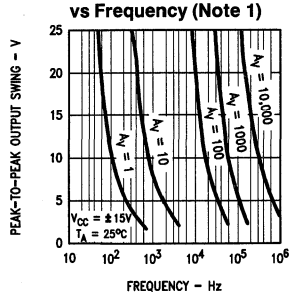
Values for Suggested Compensation Networks vs Various Close Loop Voltage Gains



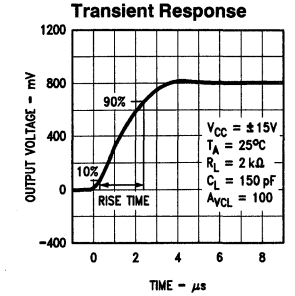
Frequency Response for Various Close Loop Gain (Note 1)



Output Voltage Swing vs Frequency (Note 1)



Transient Response



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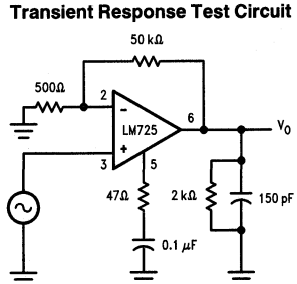
Note 1: Performance is shown using recommended compensation networks.

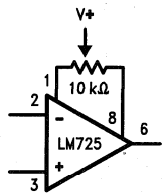
Transient Response Test Circuit



TL/H/10474–8

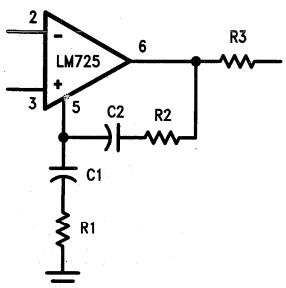
Auxiliary Circuits

Voltage Offset Null Circuit



TL/H/10474–3

Frequency Compensation Circuit



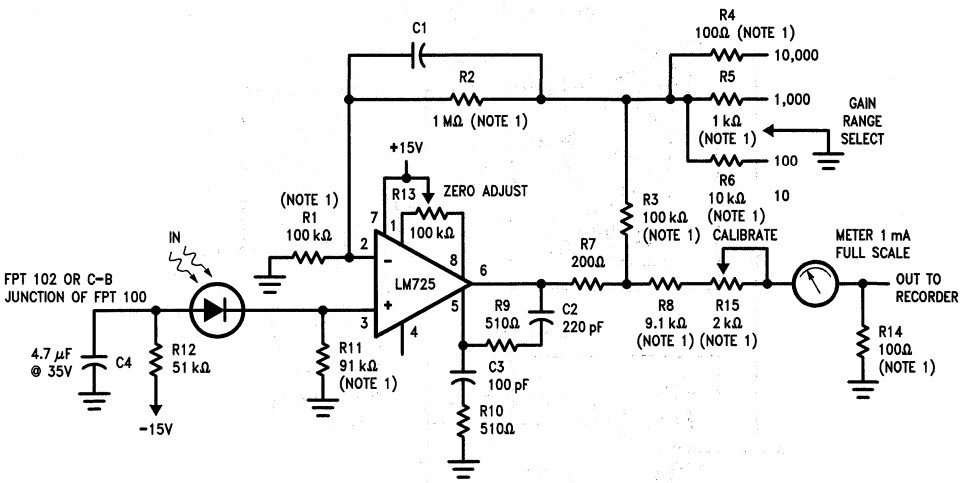
TL/H/10474–4

Compensation Component Values

A_V	R_1 (Ω)	C_1 (μF)	R_2 (Ω)	C_2 (μF)
10,000	10k	50 pF		
1,000	470	0.001		
100	47	0.01		
10	27	0.05	270	0.0015
1	10	0.05	39	0.02

Typical Applications

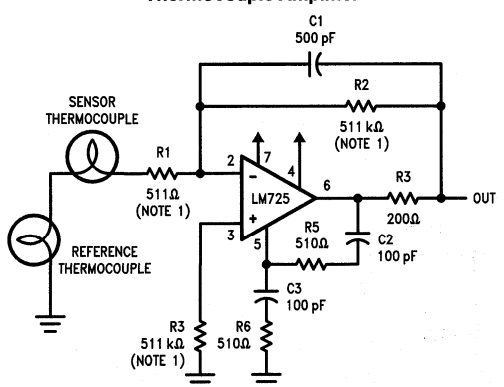
Photodiode Amplifier



TL/H/10474–9

DC Gains = 10,000; 1,000; 100; and 10
Bandwidth = Determined by value of C1

Thermocouple Amplifier



TL/H/10474–10

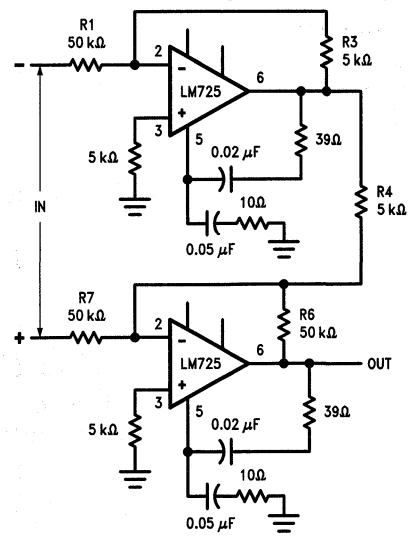
$\frac{R2}{R5} = \frac{R6}{R7}$ for best CMR

R1 = R4
R2 = R5

$\text{Gain} = \frac{R6}{R2} + \left(\frac{2R1}{R3}\right)$

DC Gain = 1000
Bandwidth = DC to 540 Hz
Equivalent Input Noise = 0.24 μV_{rms}

± 100V Common Mode Range Differential Amplifier

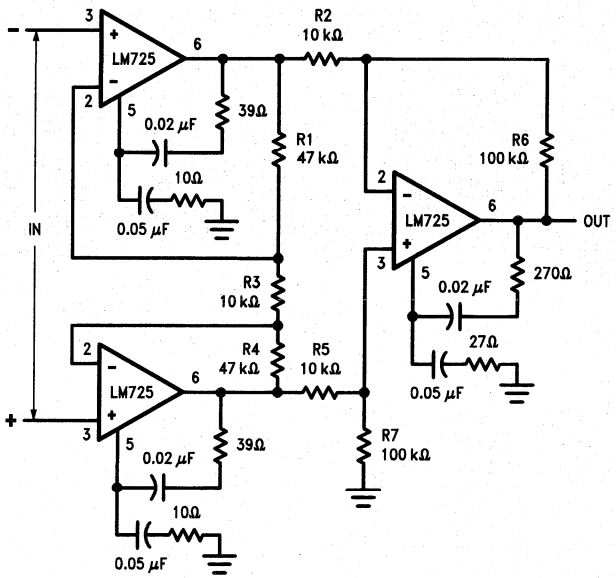


TL/H/10474–11

Note 1: Indicates ±1% metal film resistors recommended for temperature stability.

Typical Applications (Continued)

Instrumentation Amplifier with High Common Mode Rejection



TL/H/10474–12

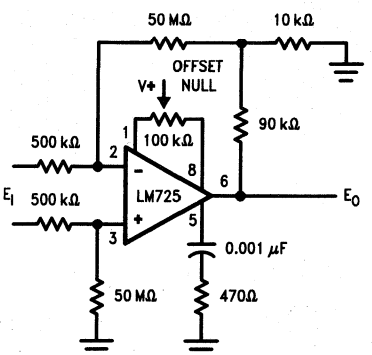
$\frac{R1}{R6} = \frac{R3}{R4}$ for best CMRR

R3 = R4

R1 = R6 = 10 R3

Gain = $\frac{R6}{R7}$

Precision Amplifier A_{VCL} = 1000



TL/H/10474–13

National Semiconductor

LM741 Operational Amplifier

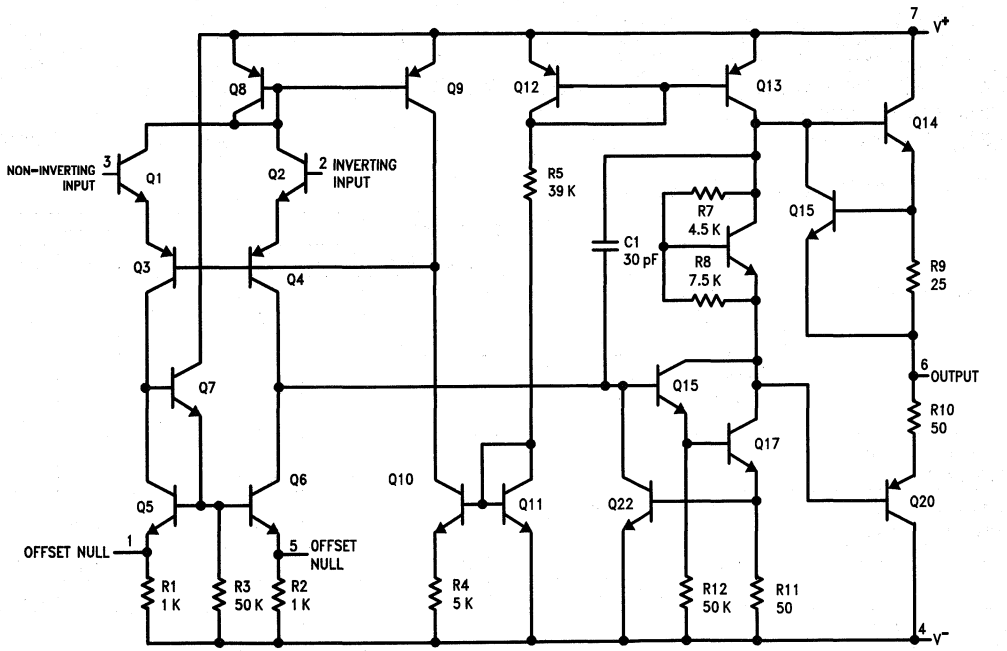
General Description

The LM741 series are general purpose operational amplifiers which feature improved performance over industry standards like the LM709. They are direct, plug-in replacements for the 709C, LM201, MC1439 and 748 in most applications.

The amplifiers offer many features which make their application nearly foolproof: overload protection on the input and output, no latch-up when the common mode range is exceeded, as well as freedom from oscillations.

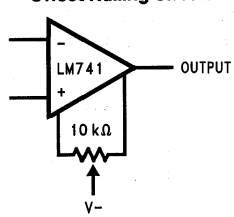
The LM741C/LM741E are identical to the LM741/LM741A except that the LM741C/LM741E have their performance guaranteed over a 0°C to +70°C temperature range, instead of −55°C to +125°C.

Schematic Diagram



TL/H/9341–1

Offset Nulling Circuit



TL/H/9341–7

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.
(Note 5)

	LM741A	LM741E	LM741	LM741C
Supply Voltage	±22V	±22V	±22V	±18V
Power Dissipation (Note 1)	500 mW	500 mW	500 mW	500 mW
Differential Input Voltage	±30V	±30V	±30V	±30V
Input Voltage (Note 2)	±15V	±15V	±15V	±15V
Output Short Circuit Duration	Continuous	Continuous	Continuous	Continuous
Operating Temperature Range	−55°C to +125°C	0°C to +70°C	−55°C to +125°C	0°C to +70°C
Storage Temperature Range	−65°C to +150°C	−65°C to +150°C	−65°C to +150°C	−65°C to +150°C
Junction Temperature	150°C	100°C	150°C	100°C
Soldering Information				
N-Package (10 seconds)	260°C	260°C	260°C	260°C
J- or H-Package (10 seconds)	300°C	300°C	300°C	300°C
M-Package				
Vapor Phase (60 seconds)	215°C	215°C	215°C	215°C
Infrared (15 seconds)	215°C	215°C	215°C	215°C
See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.				
ESD Tolerance (Note 6)	400V	400V	400V	400V

Electrical Characteristics (Note 3)

Parameter	Conditions	LM741A/LM741E			LM741			LM741C			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	$T_A = 25°C$ $R_S \leq 10\,k\Omega$ $R_S \leq 50\Omega$		 0.8	 3.0		1.0	5.0		2.0	6.0	mV mV
	$T_{AMIN} \leq T_A \leq T_{AMAX}$ $R_S \leq 50\Omega$ $R_S \leq 10\,k\Omega$			4.0			 6.0			 7.5	 mV mV
Average Input Offset Voltage Drift				15							μV/°C
Input Offset Voltage Adjustment Range	$T_A = 25°C, V_S = \pm 20V$	±10				±15			±15		mV
Input Offset Current	$T_A = 25°C$		3.0	30		20	200		20	200	nA
	$T_{AMIN} \leq T_A \leq T_{AMAX}$			70		85	500			300	nA
Average Input Offset Current Drift				0.5							nA/°C
Input Bias Current	$T_A = 25°C$		30	80		80	500		80	500	nA
	$T_{AMIN} \leq T_A \leq T_{AMAX}$			0.210			1.5			0.8	μA
Input Resistance	$T_A = 25°C, V_S = \pm 20V$	1.0	6.0		0.3	2.0		0.3	2.0		MΩ
	$T_{AMIN} \leq T_A \leq T_{AMAX}$, $V_S = \pm 20V$	0.5									MΩ
Input Voltage Range	$T_A = 25°C$							±12	±13		V
	$T_{AMIN} \leq T_A \leq T_{AMAX}$				±12	±13					V
Large Signal Voltage Gain	$T_A = 25°C, R_L \geq 2\,k\Omega$ $V_S = \pm 20V, V_O = \pm 15V$ $V_S = \pm 15V, V_O = \pm 10V$	50			 50	 200		 20	 200		 V/mV V/mV
	$T_{AMIN} \leq T_A \leq T_{AMAX}$, $R_L \geq 2\,k\Omega$, $V_S = \pm 20V, V_O = \pm 15V$ $V_S = \pm 15V, V_O = \pm 10V$ $V_S = \pm 5V, V_O = \pm 2V$	 32 10			 25			 15			 V/mV V/mV V/mV

Electrical Characteristics (Note 3) (Continued)

Parameter	Conditions	LM741A/LM741E			LM741			LM741C			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Output Voltage Swing	$V_S = \pm 20V$										
	$R_L \geq 10\ k\Omega$	± 16									V
	$R_L \geq 2\ k\Omega$	± 15									V
	$V_S = \pm 15V$										
	$R_L \geq 10\ k\Omega$				± 12	± 14		± 12	± 14		V
	$R_L \geq 2\ k\Omega$				± 10	± 13		± 10	± 13		V
Output Short Circuit Current	$T_A = 25°C$	10	25	35		25			25		mA
	$T_{AMIN} \leq T_A \leq T_{AMAX}$	10		40							mA
Common-Mode Rejection Ratio	$T_{AMIN} \leq T_A \leq T_{AMAX}$										
	$R_S \leq 10\ k\Omega$, $V_{CM} = \pm 12V$				70	90		70	90		dB
	$R_S \leq 50\Omega$, $V_{CM} = \pm 12V$	80	95								dB
Supply Voltage Rejection Ratio	$T_{AMIN} \leq T_A \leq T_{AMAX}$, $V_S = \pm 20V$ to $V_S = \pm 5V$										
	$R_S \leq 50\Omega$	86	96								dB
	$R_S \leq 10\ k\Omega$				77	96		77	96		dB
Transient Response	$T_A = 25°C$, Unity Gain										
Rise Time			0.25	0.8		0.3			0.3		μs
Overshoot			6.0	20		5			5		%
Bandwidth (Note 4)	$T_A = 25°C$	0.437	1.5								MHz
Slew Rate	$T_A = 25°C$, Unity Gain	0.3	0.7			0.5			0.5		V/μs
Supply Current	$T_A = 25°C$					1.7	2.8		1.7	2.8	mA
Power Consumption	$T_A = 25°C$										
	$V_S = \pm 20V$		80	150							mW
	$V_S = \pm 15V$					50	85		50	85	mW
LM741A	$V_S = \pm 20V$										
	$T_A = T_{AMIN}$			165							mW
	$T_A = T_{AMAX}$			135							mW
LM741E	$V_S = \pm 20V$										
	$T_A = T_{AMIN}$			150							mW
	$T_A = T_{AMAX}$			150							mW
LM741	$V_S = \pm 15V$										
	$T_A = T_{AMIN}$					60	100				mW
	$T_A = T_{AMAX}$					45	75				mW

Note 1: For operation at elevated temperatures, these devices must be derated based on thermal resistance, and T_j max. (listed under "Absolute Maximum Ratings"). $T_j = T_A + (\theta_{jA} P_D)$.

Thermal Resistance	Cerdip (J)	DIP (N)	HO8 (H)	SO-8 (M)
θ_{jA} (Junction to Ambient)	100°C/W	100°C/W	170°C/W	195°C/W
θ_{jC} (Junction to Case)	N/A	N/A	25°C/W	N/A

Note 2: For supply voltages less than $\pm 15V$, the absolute maximum input voltage is equal to the supply voltage.

Note 3: Unless otherwise specified, these specifications apply for $V_S = \pm 15V$, $-55°C \leq T_A \leq +125°C$ (LM741/LM741A). For the LM741C/LM741E, these specifications are limited to $0°C \leq T_A \leq +70°C$.

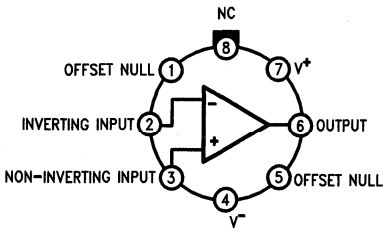
Note 4: Calculated value from: BW (MHz) = 0.35/Rise Time(μs).

Note 5: For military specifications see RETS741X for LM741 and RETS741AX for LM741A.

Note 6: Human body model, 1.5 kΩ in series with 100 pF.

Connection Diagrams

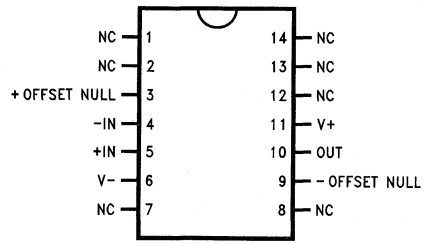
Metal Can Package



TL/H/9341-2

Order Number LM741H, LM741H/883*, LM741AH/883
LM741CH or LM741EH
See NS Package Number H08C

Ceramic Dual-In-Line Package



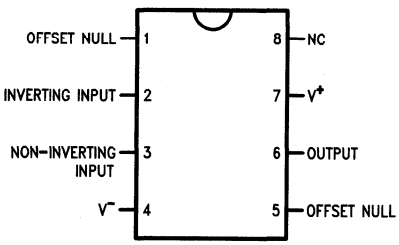
TL/H/9341-5

Order Number LM741J-14/883*, LM741AJ-14/883**
See NS Package Number J14A

*also available per JM38510/10101

**also available per JM38510/10102

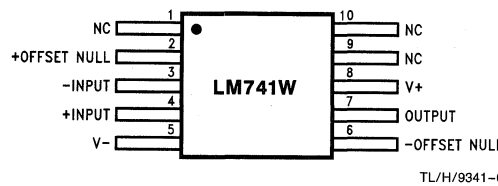
Dual-In-Line or S.O. Package



TL/H/9341-3

Order Number LM741J, LM741J/883, LM741CJ,
LM741CM, LM741CN or LM741EN
See NS Package Number J08A, M08A or N08E

Ceramic Flatpak



TL/H/9341-6

Order Number LM741W/883
See NS Package Number W10A

*LM741H is available per JM38510/10101

National Semiconductor

LM747
Dual Operational Amplifier

General Description

The LM747 is a general purpose dual operational amplifier. The two amplifiers share a common bias network and power supply leads. Otherwise, their operation is completely independent.

Additional features of the LM747 are: no latch-up when input common mode range is exceeded, freedom from oscillations, and package flexibility.

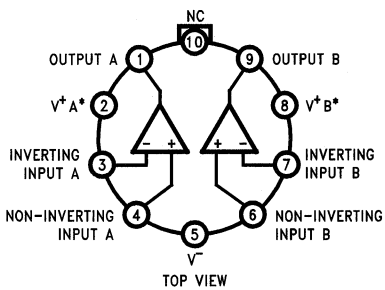
The LM747C/LM747E is identical to the LM747/LM747A except that the LM747C/LM747E has its specifications guaranteed over the temperature range from 0°C to +70°C instead of −55°C to +125°C.

Features

- No frequency compensation required
- Short-circuit protection
- Wide common-mode and differential voltage ranges
- Low power consumption
- No latch-up
- Balanced offset null

Connection Diagrams

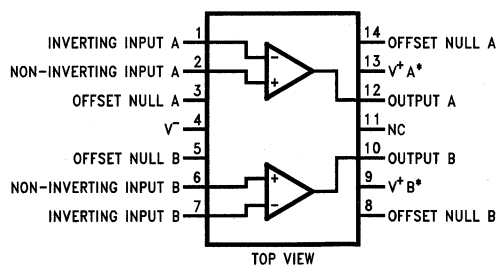
Metal Can Package



TL/H/11479–4

Order Number LM747H, LM747AH or LM747CH
See NS Package Number H10C

Dual-In-Line Package



TL/H/11479–5

Order Number LM747J, LM747AJ, LM747CJ or LM747EJ
See NS Package Number J14A

Order Number LM747CN or LM747EN
See NS Package Number N14A

*V+A and V+B are internally connected.

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	
LM747/LM747A	±22V
LM747C/LM747E	±18V
Power Dissipation (Note 1)	800 mW
Differential Input Voltage	±30V
Input Voltage (Note 2)	±15V
Output Short-Circuit Duration	Indefinite
Operating Temperature Range	
LM747/LM747A	−55°C to +125°C
LM747C/LM747E	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec.)	300°C

Electrical Characteristics (Note 3)

Parameter	Conditions	LM747A/LM747E			LM747			LM747C			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	$T_A = 25°C$ $R_S \le 10\ k\Omega$ $R_S \le 50\Omega$		0.8	3.0		1.0	5.0		2.0	6.0	mV
	$R_S \le 50\Omega$ $R_S \le 10\ k\Omega$			4.0			6.0			7.5	mV
Average Input Offset Voltage Drift				15							μV/°C
Input Offset Voltage Adjustment Range	$T_A = 25°C, V_S = \pm 20V$	±10				±15			±15		mV
Input Offset Current	$T_A = 25°C$		3.0	30		20	200		20	200	nA
				70		85	500			300	
Average Input Offset Current Drift				0.5							nA/°C
Input Bias Current	$T_A = 25°C$		30	80		80	500		80	500	nA
	$T_{AMIN} \le T_A \le T_{AMAX}$			0.210			1.5			0.8	μA
Input Resistance	$T_A = 25°C, V_S = \pm 20V$	1.0	6.0		0.3	2.0		0.3	2.0		MΩ
	$V_S = \pm 20V$	0.5									
Input Voltage Range	$T_A = 25°C$							±12	±13		V
		±12	±13		±12	±13					
Large Signal Voltage Gain	$T_A = 25°C, R_L \ge 2\ k\Omega$ $V_S = \pm 20V, V_O = \pm 15V$	50									V/mV
	$V_S = \pm 15V, V_O = \pm 10V$ $R_L \ge 2\ k\Omega$				50	200		20	200		V/mV
	$V_S = \pm 20V, V_O = \pm 15V$	32									V/mV
	$V_S = \pm 15V, V_O = \pm 10V$				25			15			V/mV
	$V_S = \pm 5V, V_O = \pm 2V$	10									V/mV
Output Voltage Swing	$V_S = \pm 20V$ $R_L \ge 10\ k\Omega$ $R_L \ge 2\ k\Omega$	±16 ±15									V
	$V_S = \pm 15V$ $R_L \ge 10\ k\Omega$ $R_L \ge 2\ k\Omega$				±12 ±10	±14 ±13		±12 ±10	±14 ±13		V
Output Short Circuit Current	$T_A = 25°C$	10 10	25	35 40		25			25		mA
Common-Mode Rejection Ratio	$R_S \le 10\ k\Omega, V_{CM} = \pm 12V$				70	90		70	90		dB
	$R_S \le 50\ k\Omega, V_{CM} = \pm 12V$	80	95								

Electrical Characteristics (Note 3) (Continued)

Parameter	Conditions	LM747A/LM747E			LM747			LM747C			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Supply Voltage Rejection Ratio	$V_S = \pm 20V$ to $V_S = \pm 5V$ $R_S \leq 50\Omega$ $R_S \leq 10\ k\Omega$	86	96		77	96		77	96		dB
Transient Response Rise Time Overshoot	$T_A = 25°C$, Unity Gain		0.25 6.0	0.8 20		0.3 5			0.3 5		μs %
Bandwidth (Note 4)	$T_A = 25°C$	0.437	1.5								MHz
Slew Rate	$T_A = 25°C$, Unity Gain	0.3	0.7			0.5			0.5		V/μs
Supply Current/Amp	$T_A = 25°C$			2.5		1.7	2.8		1.7	2.8	mA
Power Consumption/Amp	$T_A = 25°C$ $V_S = \pm 20V$ $V_S = \pm 15V$		80	150		50	85		50	85	mW
LM747A	$V_S = \pm 20V$ $T_A = T_{AMIN}$ $T_A = T_{AMAX}$			165 135							mW
LM747E	$V_S = \pm 20V$ $T_A = T_{AMIN}$ $T_A = T_{AMAX}$			150 150 150							mW
LM747	$V_S = \pm 15V$ $T_A = T_{AMIN}$ $T_A = T_{AMAX}$					60 45	100 75				mW

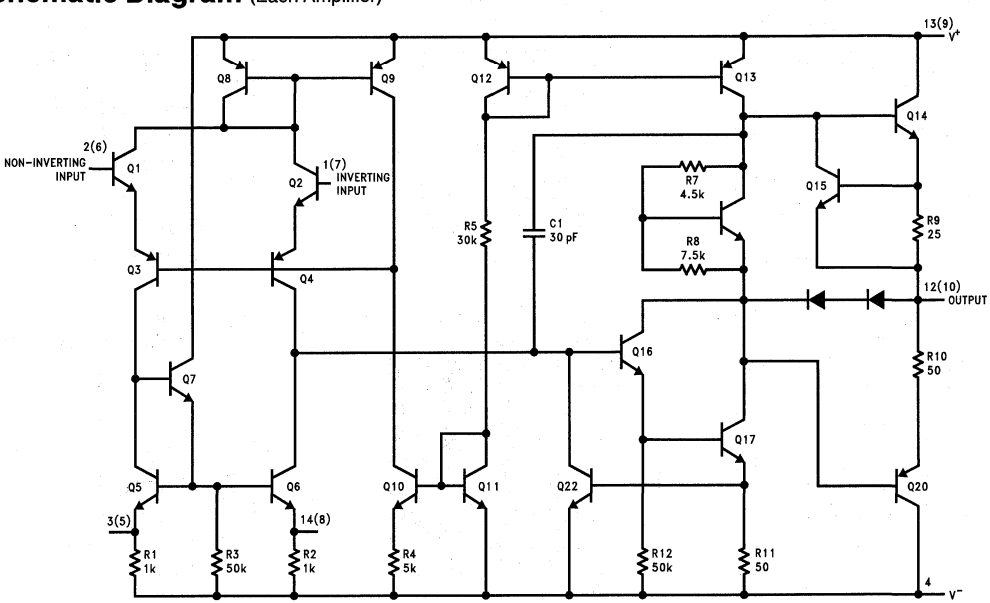
Note 1: The maximum junction temperature of the LM747/LM747A is 150°C. while that of the LM747C/LM747E is 100°C. For operating at elevated temperatures, devies in the TO-5 package must be derated based on a thermal resistance of 150°C/W, junction to ambient, or 45°C/W, junction to case. The thermal resistance of the dual-in-line package is 100°C/W, junction to ambient.

Note 2: For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

Note 3: These specifications apply for $\pm 5V \leq V_S \leq \pm 20V$ and $-55°C \leq T_A \leq 125°C$ for the LM747A and $0°C \leq T_A \leq 70°C$ for the LM747E unless otherwise specified. The LM747 and LM747C are specified for $V_S = \pm 15V$ and $-55°C \leq T_A \leq 125°C$ and $0°C \leq T_A \leq 70°C$, respectively, unless otherwise specified.

Note 4: Calculated value from: 0.35/Rise Time (μs).

Schematic Diagram (Each Amplifier)



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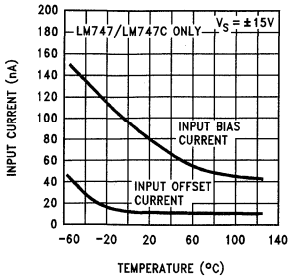
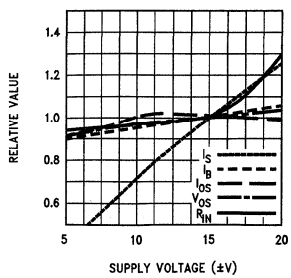
Note: Numbers in parentheses are pin numbers for amplifier B. DIP only.

Typical Performance Characteristics

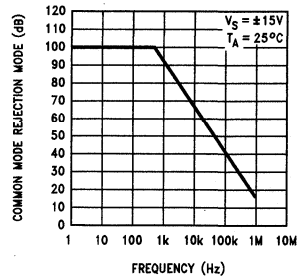
Input Bias and Offset Currents vs Ambient Temperature



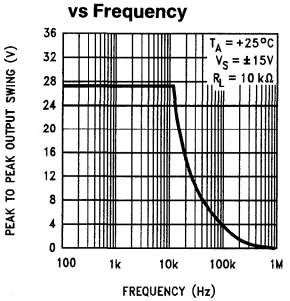
DC Parameters vs Supply Voltage



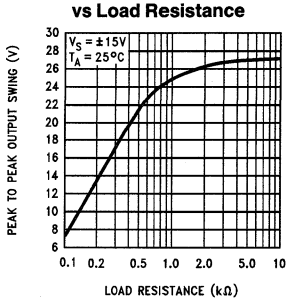
Common Mode Rejection Ratio vs Frequency



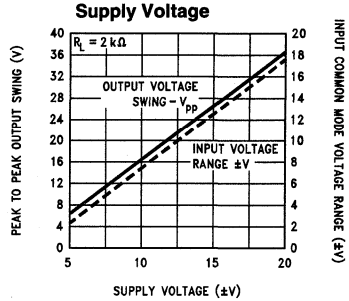
Output Voltage Swing vs Frequency



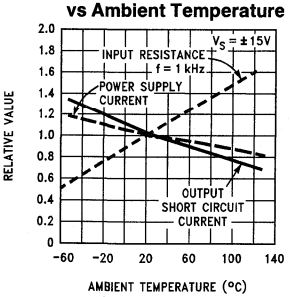
Output Voltage Swing vs Load Resistance



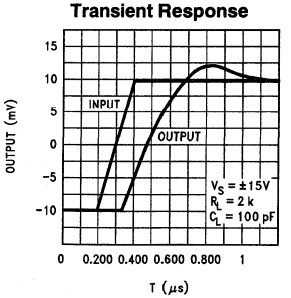
Output Swing and Input Range vs Supply Voltage



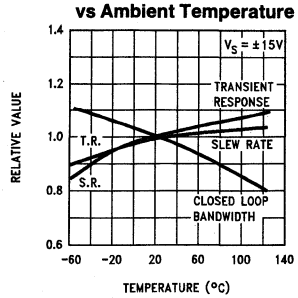
Normalized DC Parameters vs Ambient Temperature



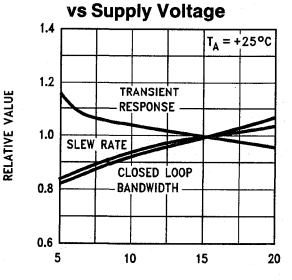
Transient Response



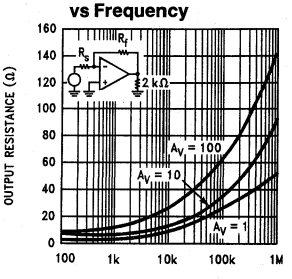
Frequency Characteristics vs Ambient Temperature



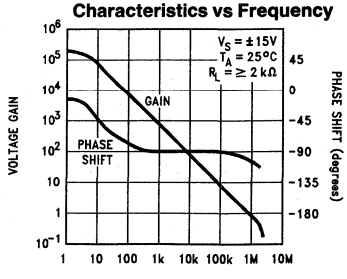
Frequency Characteristics vs Supply Voltage



Output Resistance vs Frequency



Open Loop Transfer Characteristics vs Frequency



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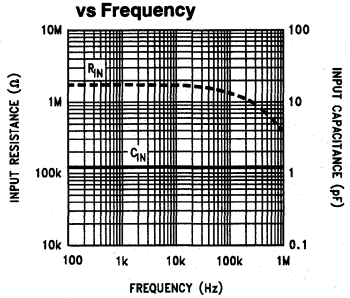
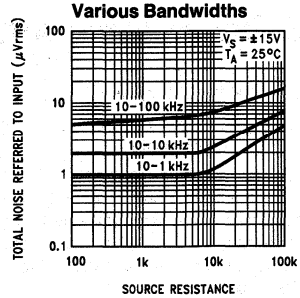
Typical Performance Characteristics (Continued)

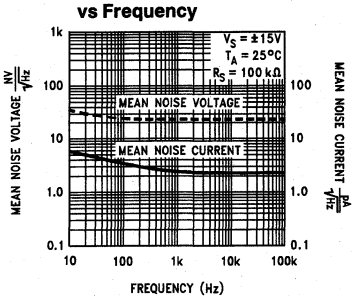
Input Resistance and Input Capacitance vs Frequency



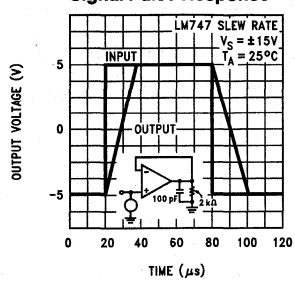
Broadband Noise for Various Bandwidths



Input Noise Voltage and Current vs Frequency



Voltage Follower Large Signal Pulse Response



TL/H/11479–3

National Semiconductor

LM748 Operational Amplifier

General Description

The LM748 is a general purpose operational amplifier with external frequency compensation.

The unity-gain compensation specified makes the circuit stable for all feedback configurations, even with capacitive loads. It is possible to optimize compensation for best high frequency performance at any gain. As a comparator, the output can be clamped at any desired level to make it compatible with logic circuits.

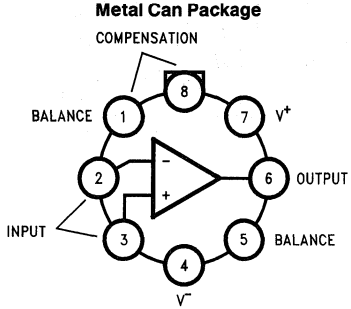
The LM748 is specified for operation over the −55°C to +125°C military temperature range. The LM748C is specified for operation over the 0°C to +70°C temperature range.

Features

- Frequency compensation with a single 30 pF capacitor
- Operation from ±5V to ±20V
- Continuous short-circuit protection
- Operation as a comparator with differential inputs as high as ±30V
- No latch-up when common mode range is exceeded
- Same pin configuration as the LM101

Connection Diagrams

Metal Can Package

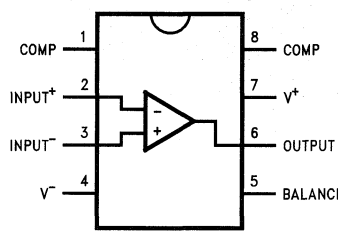


Note: Pin 4 connected to case. TL/H/11478–1

Top View

Order Number LM748H or LM748CH
See NS Package Number H08C

Dual-In-Line Package



TL/H/11478–2

Top View

Order Number LM748CJ
See NS Package Number J08A

Order Number LM748CN
See NS Package Number N08B

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	±22V
Power Dissipation (Note 1)	500 mW
Differential Input Voltage	±30V
Input Voltage (Note 2)	±15V
Output Short-Circuit Duration (Note 3)	Indefinite
Operating Temperature Range:	
LM748	−55°C to +125°C
LM748C	0°C to +70C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec.)	+300°C

Electrical Characteristics (Note 4)

Parameter	Conditions	Min	Typ	Max	Units
Input Offset Voltage	$T_A = 25°C$, $R_S \leq 10\ k\Omega$		1.0	5.0	mV
Input Offset Current	$T_A = 25°C$		40	200	nA
Input Bias Current	$T_A = 25°C$		120	500	nA
Input Resistance	$T_A = 25°C$	300	800		kΩ
Supply Current	$T_A = 25°C$, $V_S = \pm 15V$		1.8	2.8	mA
Large Signal Voltage Gain	$T_A = 25°C$, $V_S = \pm 15V$ $V_{OUT} = \pm 10V$, $R_L \geq 2\ k\Omega$	50	160		V/mV
Input Offset Voltage	$R_S \leq 10\ k\Omega$			6.0	mV
Average Temperature Coefficient of Input Offset Voltage	$R_S \leq 50\Omega$		3.0		μV/°C
	$R_S \leq 10\ k\Omega$		6.0		μV/°C
Input Offset Current	$T_A = 0°C$ to $+70°C$			300	nA
	$T_A = -55°C$ to $+125°C$			500	nA
Input Bias Current	$T_A = 0°C$ to $+70°C$			0.8	μA
	$T_A = -55°C$ to $+125°C$			1.5	μA
Supply Current	$T_A = +125°C$, $V_S = \pm 15V$		1.2	2.25	mA
	$T_A = -55°C$ to $+125°C$		1.9	3.3	mA
Large Signal Voltage Gain	$V_S = \pm 15V$, $V_{OUT} = \pm 10V$ $R_L \geq 2\ k\Omega$	25			V/mV
Output Voltage Swing	$V_S = \pm 15V$, $R_L = 10\ k\Omega$	±12	±14		V
	$V_S = \pm 15V$, $R_L = 2\ k\Omega$	±10	±13		V
Input Voltage Range	$V_S = \pm 15V$	±12			V
Common-Mode Rejection Ratio	$R_S \leq 10\ k\Omega$	70	90		dB
Supply Voltage Rejection Ratio	$R_S \leq 10\ k\Omega$	77	90		dB

Note 1: For operating at elevated temperatures, the device must be derated based on a maximum junction to case thermal resistance of 45°C per watt, or 150°C per watt junction to ambient. (See Curves).

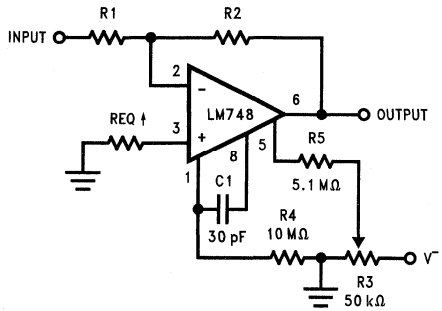
Note 2: For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

Note 3: Continuous short circuit is allowed for case temperatures to +125°C and ambient temperatures to +70°C.

Note 4: These specifications apply for $\pm 5V \leq V_S \leq +15V$ and $-55°C \leq T_A \leq 125°C$, unless otherwise specified. With the LM748C, however, all temperature specifications are limited to $0°C \leq T_A \leq +70°C$.

Typical Applications

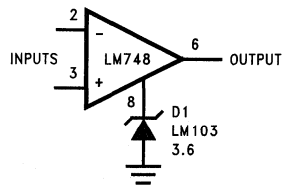
Inverting Amplifier with Balancing Circuit



†May be zero or equal to parallel combination of R1 and R2 for minimum offset.

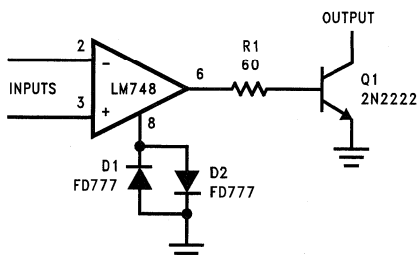
TL/H/11478–3

Voltage Comparator for Driving DTL or TTL Integrated Circuits



TL/H/11478–4

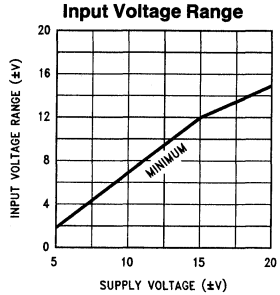
Voltage Comparator for Driving RTL Logic or High Current Driver



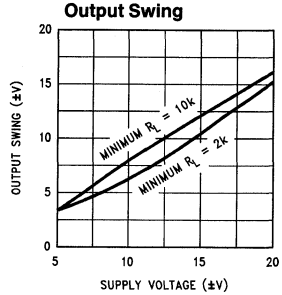
TL/H/11478–5

Guaranteed Performance Characteristics (Note 4)

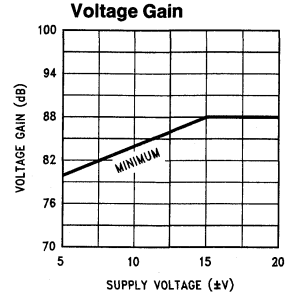
Input Voltage Range



Output Swing



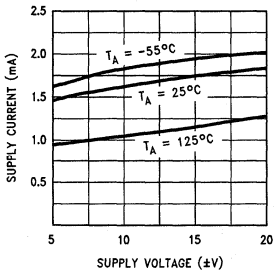
Voltage Gain



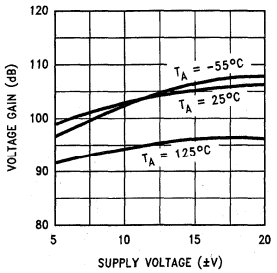
TL/H/11478–6

Typical Performance Characteristics

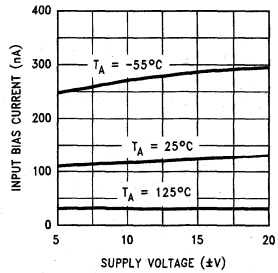
Supply Current



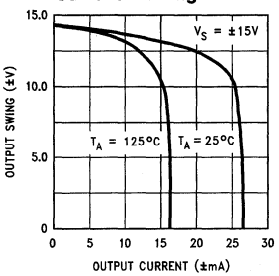
Voltage Gain



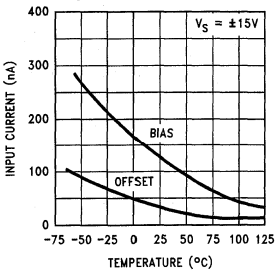
Input Bias Current



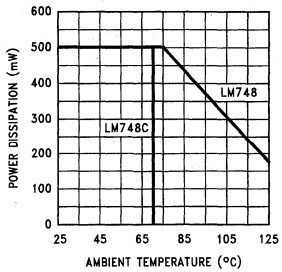
Current Limiting



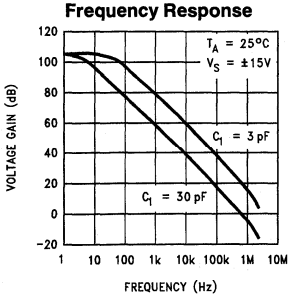
Input Current



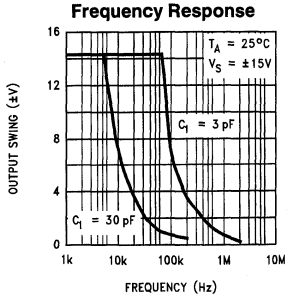
Maximum Power Dissipation



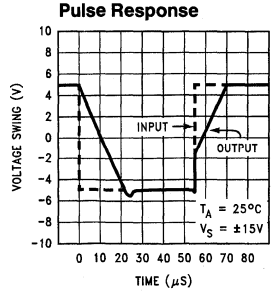
Open Loop Frequency Response



Large Signal Frequency Response



Voltage Follower Pulse Response



TL/H/11478–7

National Semiconductor

LM759/LM77000
Power Operational Amplifiers

General Description

The LM759 and LM77000 are high performance operational amplifiers that feature high output current capability. The LM759 is capable of providing 325 mA and the LM77000 providing 250 mA. Both amplifiers feature small signal characteristics that are better than the LM741. The amplifiers are designed to operate from a single or dual power supply with an input common mode range that includes the negative supply. The high gain and high output power provide superior performance. Internal current limiting, thermal shutdown, and safe area compensation are employed making the LM759 and LM77000 essentially indestructible.

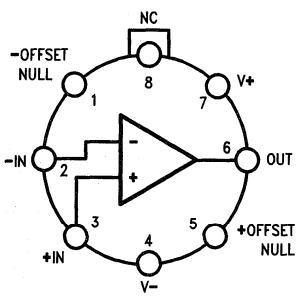
Features

- Output current
  - LM759—325 mA minimum
  - LM77000—250 mA minimum
- Internal short circuit current limiting
- Internal thermal overload protection
- Internal output transistors safe-area protection
- Input common mode voltage range includes ground or negative supply

Applications

- Voltage regulators
- Audio amplifiers
- Servo amplifiers
- Power drivers

Connection Diagrams and Ordering Information

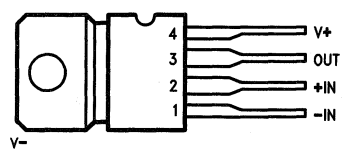


TL/H/10075–1

Lead 4 connected to case.

Top View

Order Number LM759MH, LM759CH or LM759H/883
See NS Package Number H08C



TL/H/10075–2

Top View

Order Number LM759CP or LM77000CP
See NS Package Number P04A

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature Range
- Metal Can: −65°C to +175°C
- Plastic Package: −65°C to +150°C

Operating Junction Temperature Range
- Military (LM759M): −55°C to +150°C
- Commercial (LM759C, LM77000C): 0°C to +125°C

Lead Temperature
- Metal Can (soldering, 60 sec): 300°C
- Plastic Package (soldering, 10 sec): 265°C

Internal Power Dissipation (Note 1)	Internally Limited
Supply Voltage	±18V
Differential Input Voltage	30V
Input Voltage (note 2)	±15V

LM759
Electrical Characteristics $T_J = 25°C$, $V_{CC} = \pm 15V$, unless otherwise specified

Symbol	Parameter		Conditions	Min	Typ	Max	Units
V_{IO}	Input Offset Voltage		$R_S \leq 10\ k\Omega$		1.0	3.0	mV
I_{IO}	Input Offset Current				5.0	30	nA
I_{IB}	Input Bias Current				50	150	nA
Z_I	Input Impedance			0.25	1.5		MΩ
I_{CC}	Supply Current				12	18	mA
V_{IR}	Input Voltage Range			$V^+ - 2V$ to V^-	$V^+ - 2V$ to V^-		V
I_{OS}	Output Short Circuit Current		$\lvert V_{CC}-V_O \rvert = 30V$		±200		mA
$I_{O\ PEAK}$	Peak Output Current		$3.0V \leq \lvert V_{CC}-V_O \rvert \leq 10V$	±325	±500		mA
A_{VS}	Large Signal Voltage Gain		$R_L \geq 50\Omega$, $V_O = \pm 10V$	50	200		V/mV
TR	Transient Response	Rise Time	$R_L = 50\Omega$, $A_V = 1.0$		300		ns
		Overshoot			5.0		%
SR	Slew Rate		$R_L = 50\Omega$, $A_V = 1.0$		0.6		V/μs
BW	Bandwidth		$A_V = 1.0$		1.0		MHz
The following specifications apply for $-55°C \leq T_J \leq +150°C$							
V_{IO}	Input Offset Voltage		$R_S \leq 10\ k\Omega$			4.5	mV
I_{IO}	Input Offset Current					60	nA
I_{IB}	Input Bias Current					300	nA
CMRR	Common Mode Rejection Ratio		$R_S \leq 10\ k\Omega$	80	100		dB
PSRR	Power Supply Rejection Ratio		$R_S \leq 10\ k\Omega$	80	100		dB
A_{VS}	Large Signal Voltage Gain		$R_L \geq 50\Omega$, $V_O = \pm 10V$	25	200		V/mV
V_{OP}	Output Voltage Swing		$R_L = 50\Omega$	±10	±12.5		V

LM759C

Electrical Characteristics $T_J = 25°C$, $V_{CC} = \pm 15V$, unless otherwise specified

Symbol	Parameter		Conditions	Min	Typ	Max	Units
V_{IO}	Input Offset Voltage		$R_S \leq 10\ k\Omega$		1.0	6.0	mV
I_{IO}	Input Offset Current				5.0	50	nA
I_{IB}	Input Bias Current				50	250	nA
Z_I	Input Impedance			0.25	1.5		MΩ
I_{CC}	Supply Current				12	18	mA
V_{IR}	Input Voltage Range			$V^+ - 2V$ to V^-	$V^+ - 2V$ to V^-		V
I_{OS}	Output Short Circuit Current		$\lvert V_{CC}-V_O \rvert = 30V$		±200		mA
$I_{O\ PEAK}$	Peak Output Current		$3.0V \leq \lvert V_{CC}-V_O \rvert \leq 10V$	±325	±500		mA
A_{VS}	Large Signal Voltage Gain		$R_L \geq 50\Omega$, $V_O = \pm 10V$	25	200		V/mV
TR	Transient Response	Rise Time	$R_L = 50\Omega$, $A_V = 1.0$		300		ns
		Overshoot			10		%
SR	Slew Rate		$R_L = 50\Omega$, $A_V = 1.0$		0.5		V/μs
BW	Bandwidth		$A_V = 1.0$		1.0		MHz
The following specifications apply for $0° \leq T_J \leq +125°C$							
V_{IO}	Input Offset Voltage		$R_S \leq 10\ k\Omega$			7.5	mV
I_{IO}	Input Offset Current					100	nA
I_{IB}	Input Bias Current					400	nA
CMRR	Common Mode Rejection Ratio		$R_S \leq 10\ k\Omega$	70	100		dB
PSRR	Power Supply Rejection Ratio		$R_S \leq 10\ k\Omega$	80	100		dB
A_{VS}	Large Signal Voltage Gain		$R_L \geq 50\Omega$, $V_O = \pm 10V$	25	200		V/mV
V_{OP}	Output Voltage Swing		$R_L = 50\Omega$	±10	±12.5		V

LM77000
Electrical Characteristics $T_J = 25°C$, $V_{CC} = \pm 15V$, unless otherwise specified

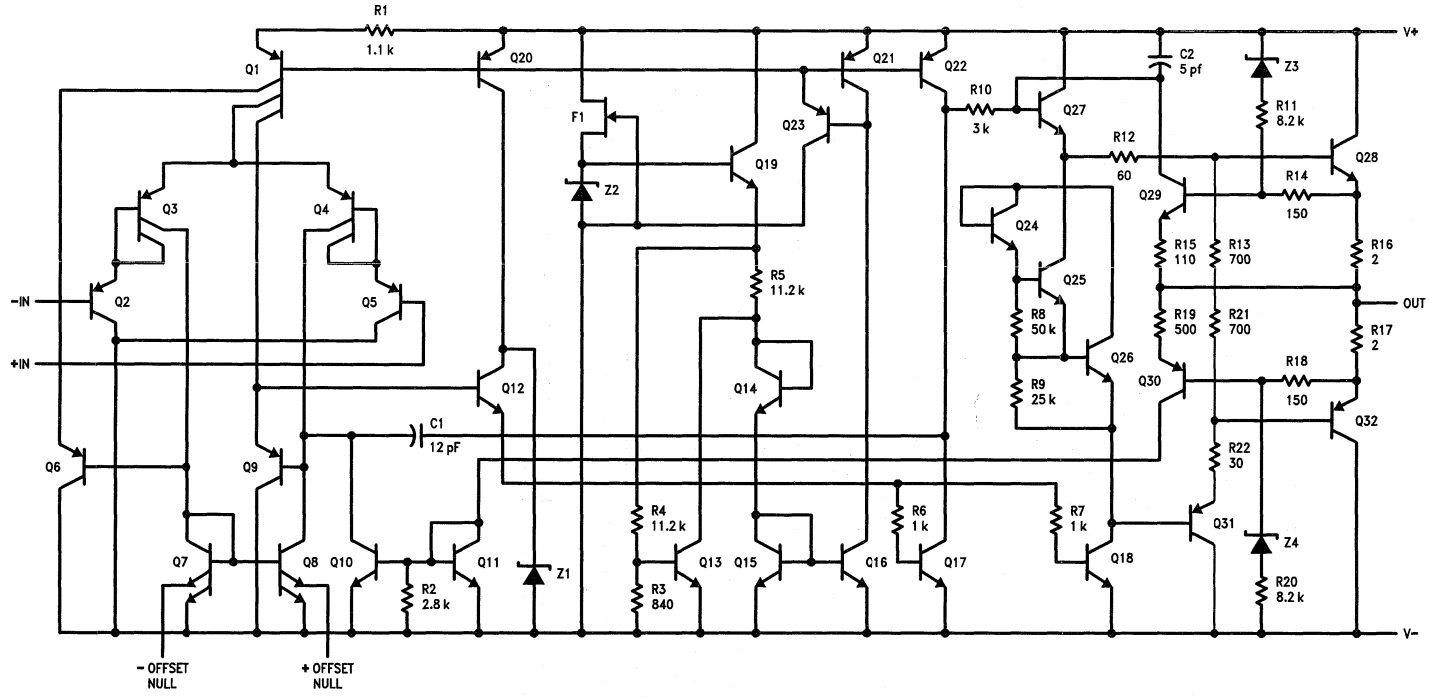
Symbol	Parameter		Conditions	Min	Typ	Max	Units
V_{IO}	Input Offset Voltage		$R_S \leq 10\ k\Omega$		1.0	8.0	mV
I_{IO}	Input Offset Current				5.0	50	nA
I_{IB}	Input Bias Current				50	250	nA
Z_I	Input Impedance			0.25	1.5		MΩ
I_{CC}	Supply Current				12	18	mA
V_{IR}	Input Voltage Range			+13 to V^-	+13 to V^-		V
I_{OS}	Output Short Circuit Current		$\lvert V_{CC}-V_O \rvert = 30V$		±200		mA
$I_{O\ PEAK}$	Peak Output Current		$3.0V \leq \lvert V_{CC}-V_O \rvert \leq 10V$	±250	±400		mA
A_{VS}	Large Signal Voltage Gain		$R_L \geq 50\Omega$, $V_O = \pm 10V$	25	200		V/mV
TR	Transient Response	Rise Time	$R_L = 50\Omega$, $A_V = 1.0$		300		ns
		Overshoot			10		%
SR	Slew Rate		$R_L = 50\Omega$, $A_V = 1.0$		0.5		V/μs
BW	Bandwidth		$A_V = 1.0$		1.0		MHz
The following specifications apply for $0° \leq T_J \leq +125°C$							
V_{IO}	Input Offset Voltage		$R_S \leq 10\ k\Omega$			10	mV
I_{IO}	Input Offset Current					100	nA
I_{IB}	Input Bias Current					400	nA
CMR	Common Mode Rejection		$R_S \leq 10\ k\Omega$	70	100		dB
PSRR	Power Supply Rejection Ratio		$R_S \leq 10\ k\Omega$	80	100		dB
A_{VS}	Large Signal Voltage Gain		$R_L \geq 50\Omega$, $V_O = \pm 10V$	25	200		V/mV
V_{OP}	Output Voltage Swing		$R_L = 50\Omega$	±10	±12.5		V

Note 1: Although the internal power dissipation is limited, the junction temperature must be kept below the maximum specified temperature in order to meet data sheet specifications. To calculate the maximum junction temperature or heat sink required, use the thermal resistance values which follow the Equivalent Circuit Schematic.

Note 2: For a supply voltage less than 30V between V^+ and V^-, the absolute maximum input voltage is equal to the supply voltage.

Note 3: For military electrical specifications RETS759X are available for LM759H.

Equivalent Circuit



TL/H/10075–3

Note: All resistor values in ohms.

Package	Typ θ_{JC} °C/W	Max θ_{JC} °C/W	Typ θ_{JA} °C/W	Max θ_{JA} °C/W
Plastic Package (P)	8.0	12	75	80
Metal Can (H)	30	40	120	150

$$P_{D\,Max} = \frac{T_{J\,Max} - T_A}{\theta_{JC} + \theta_{CA}} \text{ or}$$

$$= \frac{T_{J\,Max} - T_A}{\theta_{JA}} \text{ (without a heat sink)}$$

$$\theta_{CA} = \theta_{CS} + \theta_{SA}$$

Solving T_J:

$$T_J = T_A + P_D(\theta_{JC} + \theta_{CA}) \text{ or}$$

$$= T_A + P_D\theta_{JA} \text{ (without a heat sink)}$$

Where:

T_J = Junction Temperature
T_A = Ambient Temperature
P_D = Power Dissipation
θ_{JA} = Junction to ambient thermal resistance
θ_{JC} = Junction to case thermal resistance
θ_{CA} = Case to ambient thermal resistance
θ_{CS} = Case to heat sink thermal resistance
θ_{SA} = Heat sink to ambient thermal resistance

Mounting Hints

Metal Can Package (LM759CH/LM759MH)

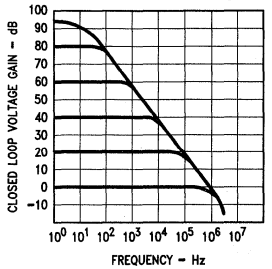
The LM759 in the 8-Lead TO-99 metal can package must be used with a heat sink. With ±15V power supplies, the LM759 can dissipate up to 540 mW in its quiescent (no load) state. This would result in a 100°C rise in chip temperature to 125°C (assuming a 25°C ambient temperature). In order to avoid this problem, it is advisable to use either a slip on or stud mount heat sink with this package. If a stud mount heat sink is used, it may be necessary to use insulating washers between the stud and the chassis because the case of the LM759 is internally connected to the negative power supply terminal.

Plastic Package (LM759CP/LM77000CP)

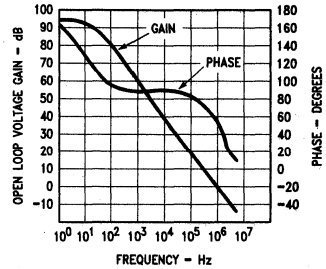
The LM759CP and LM77000CP are designed to be attached by the tab to a heat sink. This heat sink can be either one of the many heat sinks which are commercially available, a piece of metal such as the equipment chassis, or a suitable amount of copper foil as on a double sided PC board. The important thing to remember is that the negative power supply connection to the op amp must be made through the tab. Furthermore, adequate heat sinking must be provided to keep the chip temperature below 125°C under worst case load and ambient temperature conditions.

Typical Performance Characteristics

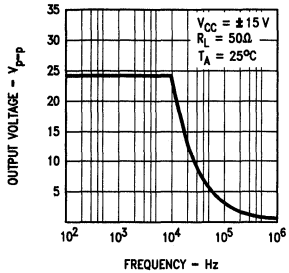
Frequency Response for Various Closed Loop Gains



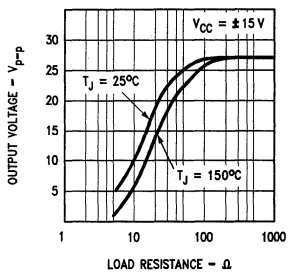
Open Loop vs Frequency Response



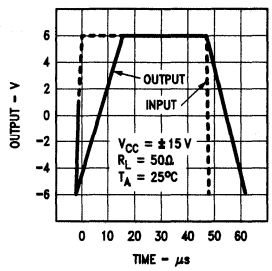
Output Voltage vs Frequency



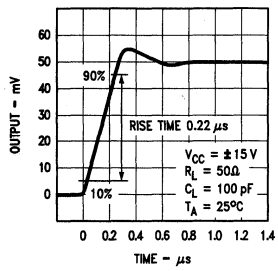
Output Voltage vs Load Resistance



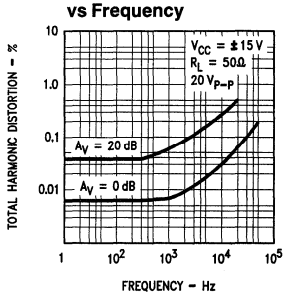
Voltage Follower Large Signal Pulse Response



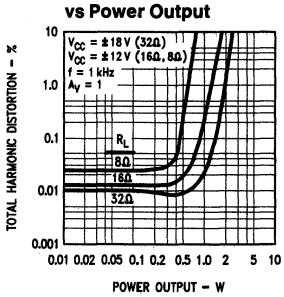
Voltage Follower Transient Response



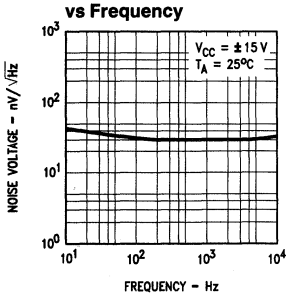
Total Harmonic Distortion vs Frequency



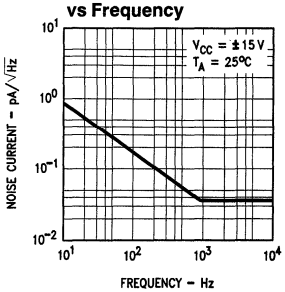
Total Harmonic Distortion vs Power Output



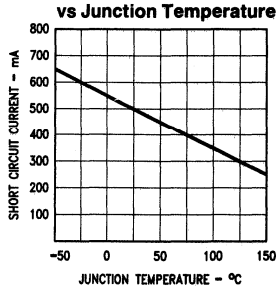
Input Noise Voltage vs Frequency



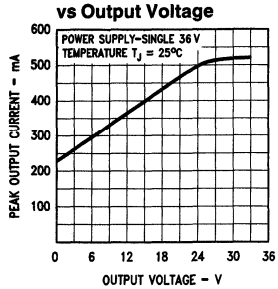
Noise Current vs Frequency



Short Circuit Current vs Junction Temperature



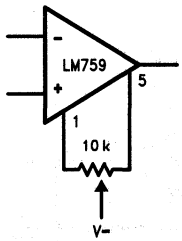
Peak Output Current vs Output Voltage



TL/H/10075–4

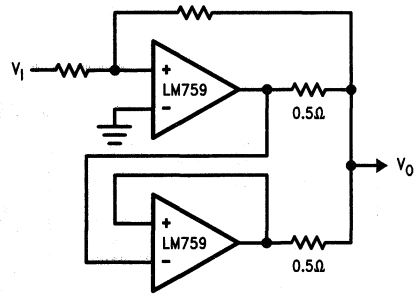
Applications

Offset Null Circuit



TL/H/10075–5

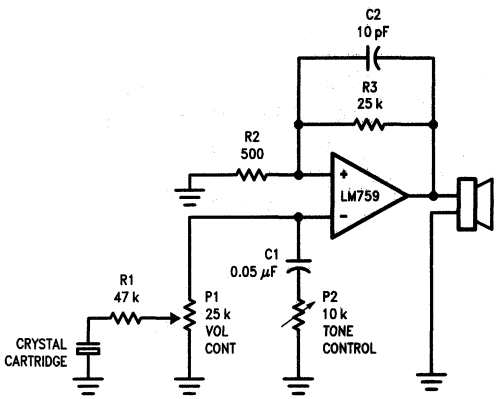
Paralleling LM759 Power Op Amps



TL/H/10075–6

Audio Applications

Low Cost Phono Amplifier

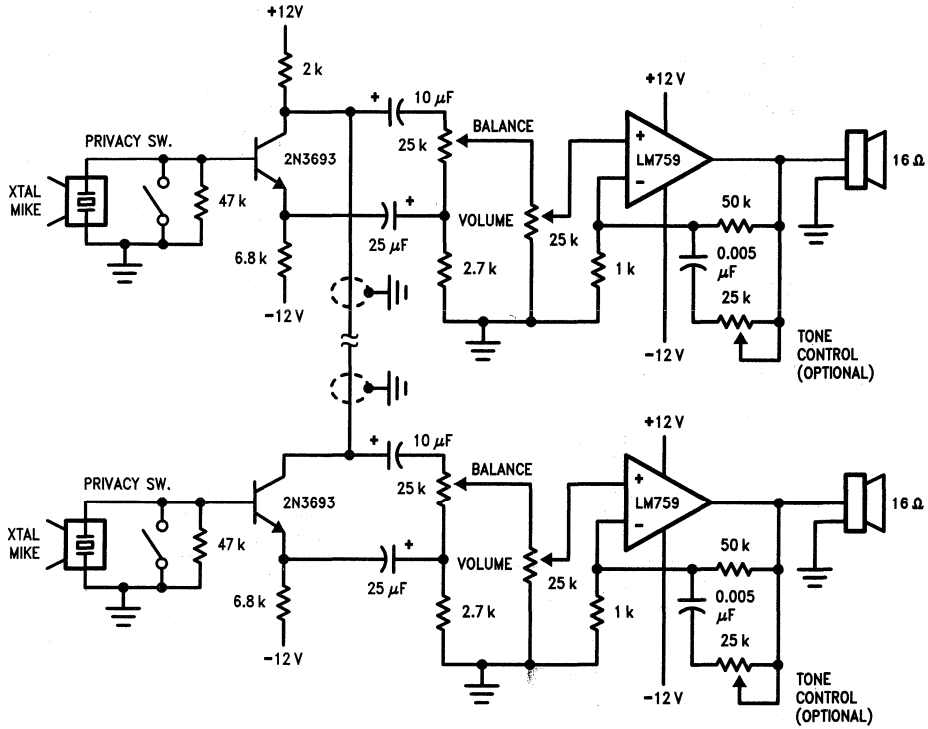


TL/H/10075–7

Speaker Impedance (Ohms)	Output Power (Watts)	Min Supply (Volts)	V_{OP-P} (Volts)
4	0.18	9	2.4
8	0.36	12	4.8
16	0.72	15	9.6
32	1.44	25	19.2

Applications (Continued)

Bi-Directional Intercom System Using the LM759 Power Op Amp



TL/H/10075–9

Features:

Circuit Simplicity

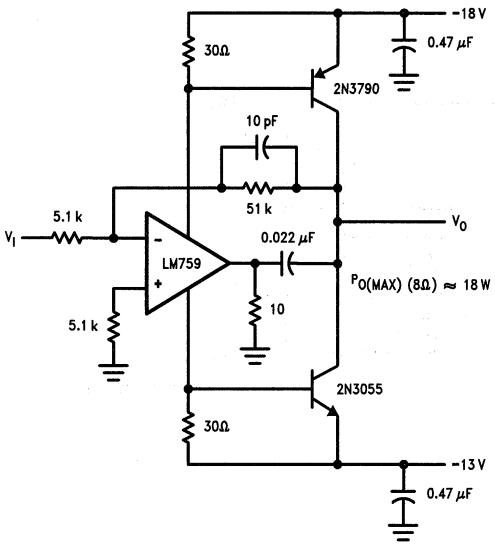
1 Watt of Audio Output

Duplex operation with only one two-wire cable as interconnect.

Note 1: All resistor values in ohms.

Applications (Continued)

High Slew Rate Power Op Amp/Audio Amp



TL/H/10075–10

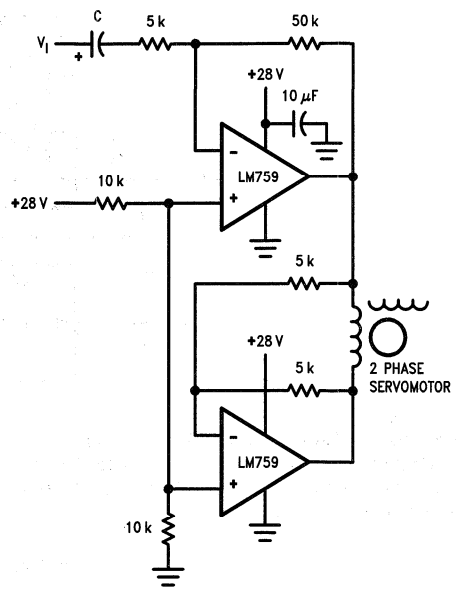
Features:

High Slew Rate 9 V/μs
High 3 dB Power Bandwidth 85 kHz
18 Watts Output Power into an 8Ω load.
Low Distortion—0.2%, 10 Vrms, 1 kHz into 8Ω

Design Consideration
$A_V \geq 10$

Servo Applications

AG Servo Amplifier—Bridge Type



TL/H/10075–11

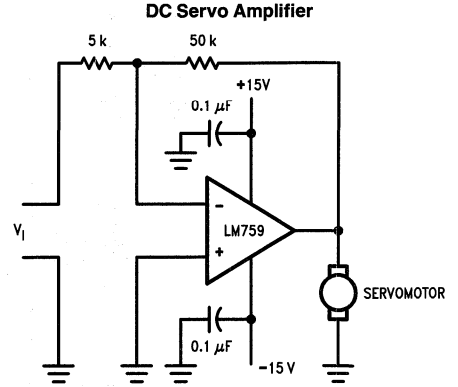
Features:

Gain of 10
Use of LM759 Means Simple Inexpensive Circuit

Design Considerations:

325 mA Max Output Current

DC Servo Amplifier



TL/H/10075–12

Features:

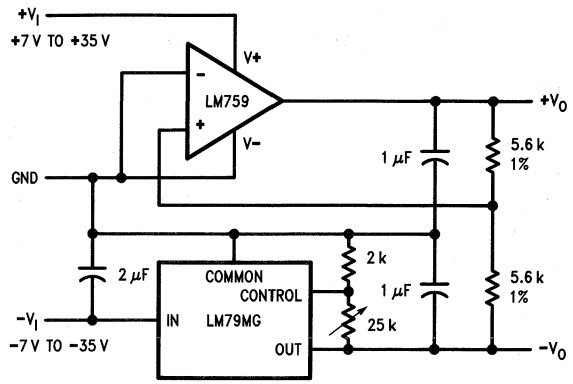
Circuit Simplicity
One Chip Means Excellent Reliability

Design Considerations
$I_O \leq 325$ mA

Note 1: All resistor values in ohms.

Regulator Applications

Adjustable Dual Tracking Regulator



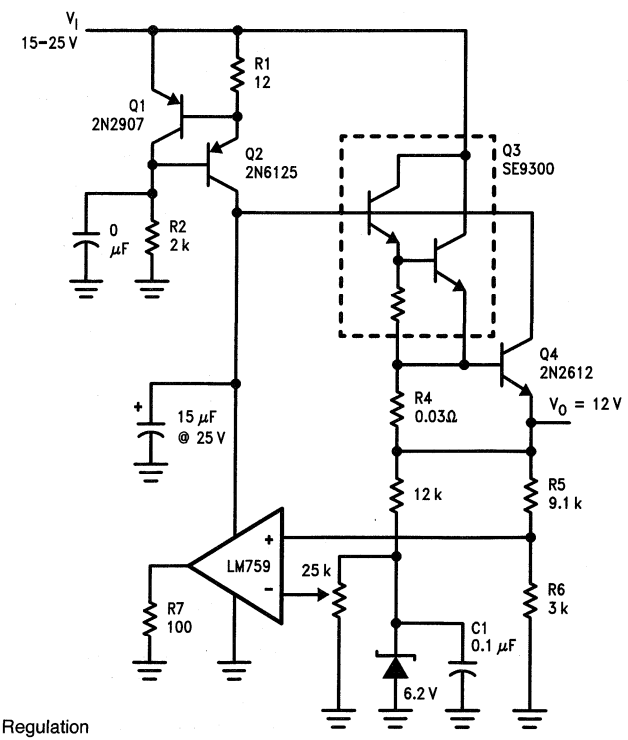
TL/H/10075–13

Features:

Wide Output Voltage Range (±2.2V to ±30V)
Excellent Load Regulation $\Delta V_O < \pm 5$ mV for $\Delta I_O = \pm 0.2$ A
Excellent Line Regulation $\Delta V_O < \pm 2$ mV for $\Delta V_I = 10$V

Note 1: All resistor values in ohms.

10 Amp — 12 Volt Regulator



TL/H/10075–14

Features:

Excellent Load and Line Regulation
Excellent Temperature Coefficient-Depends
Largely on Tempco of the Reference Zener

Note 1: All resistor values in ohms.

National Semiconductor

LM1201 Video Amplifier System

General Description

The LM1201 is a wideband video amplifier system intended for high resolution monochrome or RGB monitor applications. In addition to the wideband video amplifier the LM1201 contains a gated differential input black level clamp comparator for brightness control and an attenuator circuit for contrast control. The LM1201 also contains a voltage reference for the video input. For medium resolution RGB color monitor applications also see the LM1203 Video Amplifier System data sheet.

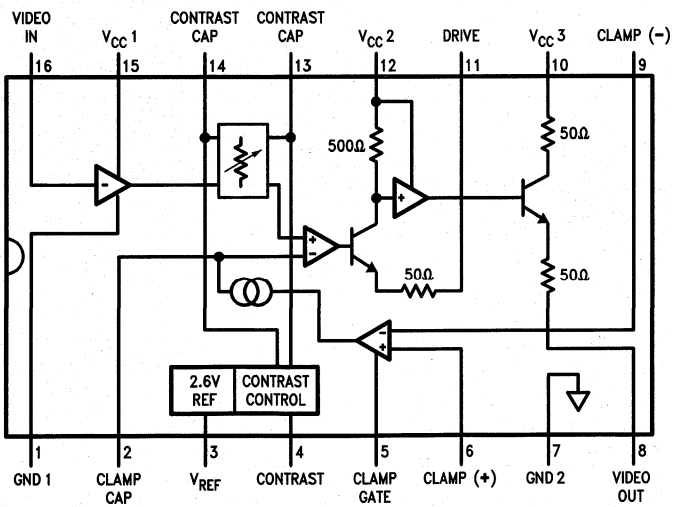
Features

- Wideband video amplifier (200 MHz @ −3 dB)
- Attenuator circuit for contrast control (>40 dB range)
- Externally gated comparator for brightness control
- Provisions for external gain set and peaking of video amplifier
- Video input voltage reference
- Low impedance output driver

Typical Applications

- CRT video amplifiers
- Video switches
- High frequency video preamplifiers
- Wideband gain controls
- PC monitors
- Workstations
- Facsimile machines
- Printers

Block and Connection Diagram



TL/H/10006–1

FIGURE 1

Order Number LM1201M or LM1201N
See NS Package Number M16A or N16E

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage V_{CC} Pins 10, 12, 15 to Ground Pins, 1, 7	13.5V
Voltage at Any Input Pin (V_{IN})	$V_{CC} \geq V_{IN} \geq$ GND
Video Output Current (I_8)	28 mA
Package Power Dissipation at $T_A = 25°C$ (Above 25°C derate based on θ_{JA} and T_J)	1.56W
Package Thermal Resistance (θ_{JA}) N16E	80°C/W
Package Thermal Resistance (θ_{JA}) M16A	100°C/W
Junction Temperature (T_J)	150°C
Operating Temperature Range (T_A)	0°C to +70°C
Storage Temperature Range (T_{STG})	−65°C to +150°C
Lead Temperature (Soldering, 10 sec.)	265°C
ESD Susceptibility	2 kV

Human body model: 100 pF discharged through a 1.5 kΩ resistor

Electrical Characteristics

See Test Circuit (Figure 2), $T_A = 25°C$; $V_{CC1} = V_{CC2} = V_{CC3} = 12V$

DC Static Tests

S9 Open; V4 = 6V; V5 = 0V; V6 = 2.0V unless otherwise stated

Symbol	Parameter	Conditions	Typical	Tested Limit (Note 1)	Design Limit (Note 2)	Units (Limits)
I_S	Supply Current	V_{CC} Pins 12, 15 Only	45	57		mA(max)
V_3	Video Input Reference Voltage		2.65	2.4		V(min)
				2.95		V(max)
I_{16}	Video Input Bias Current	$(V_3-V_{16})/10\ k\Omega$	5.0	20		μA(max)
V_{5L}	Clamp Gate Low Input Voltage	Clamp Comparator On	1.2	0.8		V(min)
V_{5H}	Clamp Gate High Input Voltage	Clamp Comparator Off	1.6	2.0		V(max)
I_{5L}	Clamp Gate Low Input Current	$V_5 = 0V$	−0.5	−5.0		μA(max)
I_{5H}	Clamp Gate High Input Current	$V_5 = 12V$	0.005	1		μA(max)
I_{2+}	Clamp Cap Charge Current	$V_2 = 0V$	1	0.55		mA(min)
I_{2-}	Clamp Cap Discharge Current	$V_2 = 5V$	−1	−0.55		mA(min)
V_{8L}	Video Output Low Voltage	$V_2 = 0V$	0.5	0.9		V(max)
V_{8H}	Video Output High Voltage	$V_2 = 5V$	8.5	8.0		V(min)
V_{OS}	Comparator Input Offset Voltage	V_6-V_9	±0.5	±25		mV(max)

AC Dynamic Tests

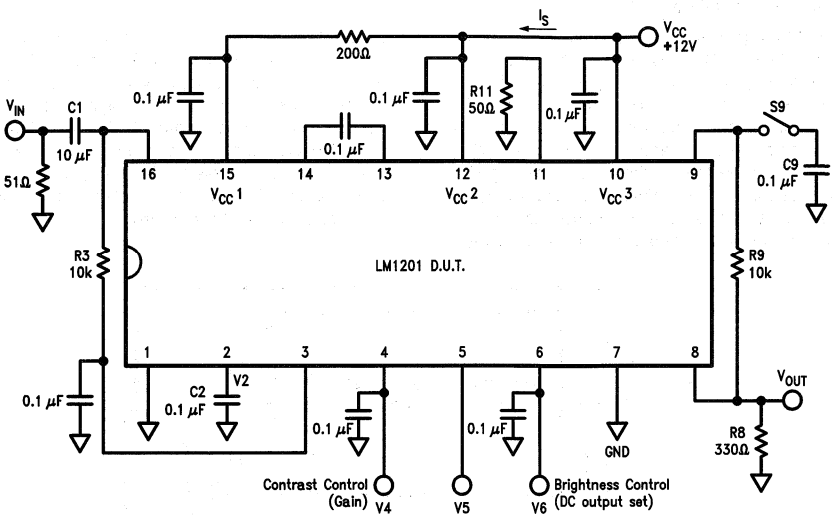
S9 Closed, $V_5 = 0V$, $V_6 = 4V$

Symbol	Parameter	Conditions	Typ	Tested Limit (Note 1)	Design Limit (Note 2)	Units (Limits)
Av max	Video Amplifier Gain	$V_4 = 12V$	8	5.5		V/V(min)
ΔAv 5V	Attenuation @ 5V	Ref: Av max, $V_4 = 5V$	−10			dB
ΔAv 2V	Attenuation @ 2V	Ref: Av max, $V_4 = 2V$	−45			dB
THD	Video Amplifier Distortion	$V_4 = 5V$, $V_O = 1\ V_{p-p}$	0.3			%
f (−3dB)	Video Amplifier Bandwidth (Note 3)	$V_4 = 12V$, $V_O = 100\ mV_{rms}$	200		170	MHz(min)
t_r	Output Rise Time (Note 3)	$V_O = 4\ V_{p-p}$	2.5			ns
t_f	Output Fall Time (Note 3)	$V_O = 4\ V_{p-p}$	3			ns

Note 1: These parameters are guaranteed and 100% production tested.

Note 2: Design limits are guaranteed (but not 100% production tested). These limits are not used to calculate outgoing quality levels.

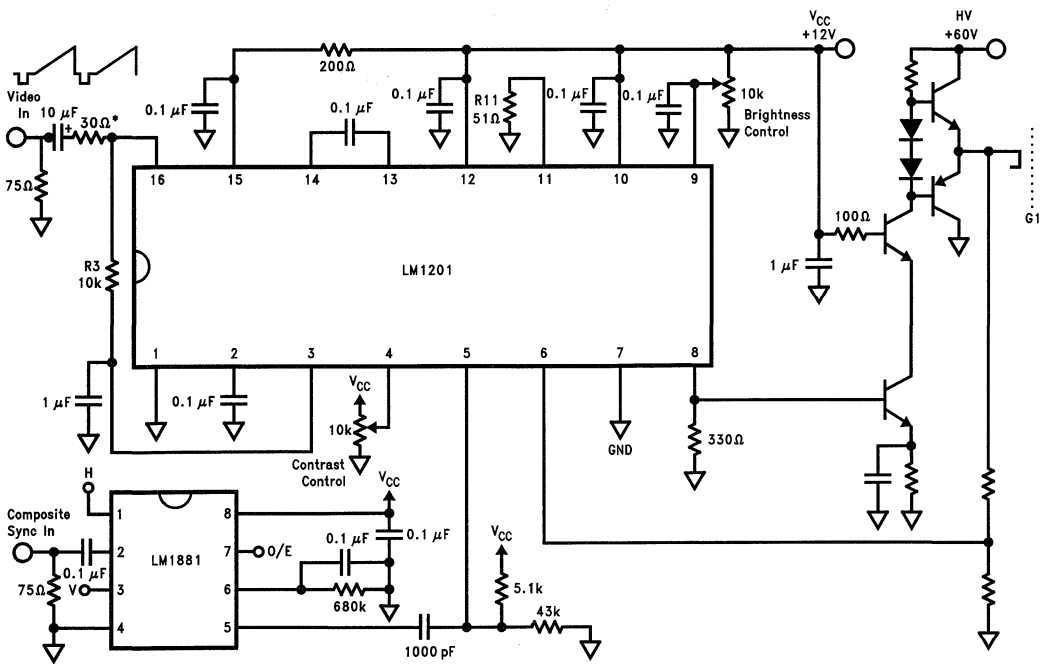
Note 3: When measuring video amplifier bandwidth or pulse rise and fall times, a double sided full ground plane printed circuit board without socket is recommended.



TL/H/10006–2

FIGURE 2. LM1201 AC/DC Test Circuit

Note: When $V_5 \leq 0.8V$ and S9 is closed, DC feedback around the Video Amplifier is provided by the clamp comparator. Under these conditions sine wave or 50% duty cycle square waves can be used for test purposes. The low frequency dominant pole is determined by C2 at Pin 2. Capacitor C9 at pin 9 prevents overloading the clamp comparator inverting input. See applications section for additional information.



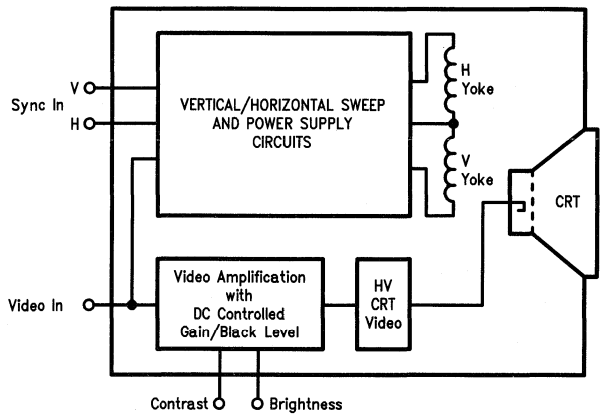
TL/H/10006–3

FIGURE 3. Typical Application of the LM1201

* 30Ω resistor is added to the input pin for protection against current surges coming from the 10 μF input capacitor. By increasing this resistor to well over 100Ω the rise and fall times of the LM1201 can be increased for EMI considerations.

APPLICATIONS INFORMATION

Figure 4 shows the block diagram of a typical analog monochrome monitor. The monitor is used with CAD/CAM work stations, PCs, arcade games and in a wide range of other applications that benefit from the use of high resolution display terminals. Monitor characteristics may differ in such ways as sweep rates, screen size, or in video amplifier speed but will still be generally configured as shown in *Figure 4*. Separate horizontal and vertical sync signals may be required or they may be contained as a composite signal in the video input signal. The video input signal is usually supplied by coaxial cable which is terminated in 75Ω at the monitor input and internally AC coupled to the video amplifier. The input signal is approximately 1V peak-to-peak in amplitude and at the input of the high voltage video section, approximately 6V peak-to-peak. At the cathode of the CRT the video signals can be as high as 60V peak to peak. The block in *Figure 4* labeled "Video Amplification with DC Controlled Gain/Black Level" contains the function of the LM1201 video amplifier system.



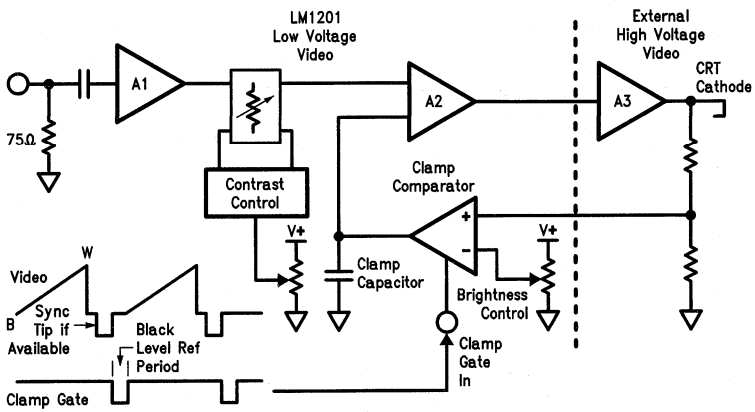
TL/H/10006–4

FIGURE 4. Typical Monochrome Monitor Block Diagram

Circuit Description

Figure 5 is a block diagram of the LM1201 along with the contrast and brightness controls. The contrast control is a DC operated attenuator which varies the AC gain of the amplifier without introducing any signal distortions or DC output shift. The brightness control function requires a "sample and hold" circuit (black level clamp) which holds the DC bias of the video amplifier and CRT cathodes constant during the black level reference portion of the video waveform. The clamp comparator, when gated on during this reference period, will charge or discharge the clamp capacitor until the non-inverting input of the clamp comparator matches that of the inverting input voltage which was set by the brightness control.

Figure 6 is a simplified schematic of the LM1201 video amplifier along with the recommended external components. The IC pin numbers are circled with all external components shown outside of the dashed line. The video input is applied to pin 16 via the 10 μF coupling capacitor. DC bias to the video input is through the 10 kΩ resistor which is connected to the 2.6V reference at pin 3. The low frequency roll-off of the amplifier is set by these two components. Transistor Q1 buffers the video signal to the base of Q2. The Q2 collector current is then directed to the V_{CC1} supply through Q3 or to V_{CC2} through Q4 and the 500Ω load resistor depending upon the differential DC voltage at the bases of Q3 and Q4. The Q3 and Q4 differential base voltage is determined by the contrast control circuit which is described below. The black level DC voltage at the collector of Q4 is maintained by Q5 and Q6 which are part of the black level clamp circuit also described below. The video signal appearing at the collector of Q4 is then buffered by Q7 and level shifted down by Z1 and Q8 to the base of Q9 which will then provide additional system gain.



TL/H/10006–5

FIGURE 5. Block Diagram of LM201 Video Amplifier with Contrast and Black Level Control

Circuit Description (Continued)

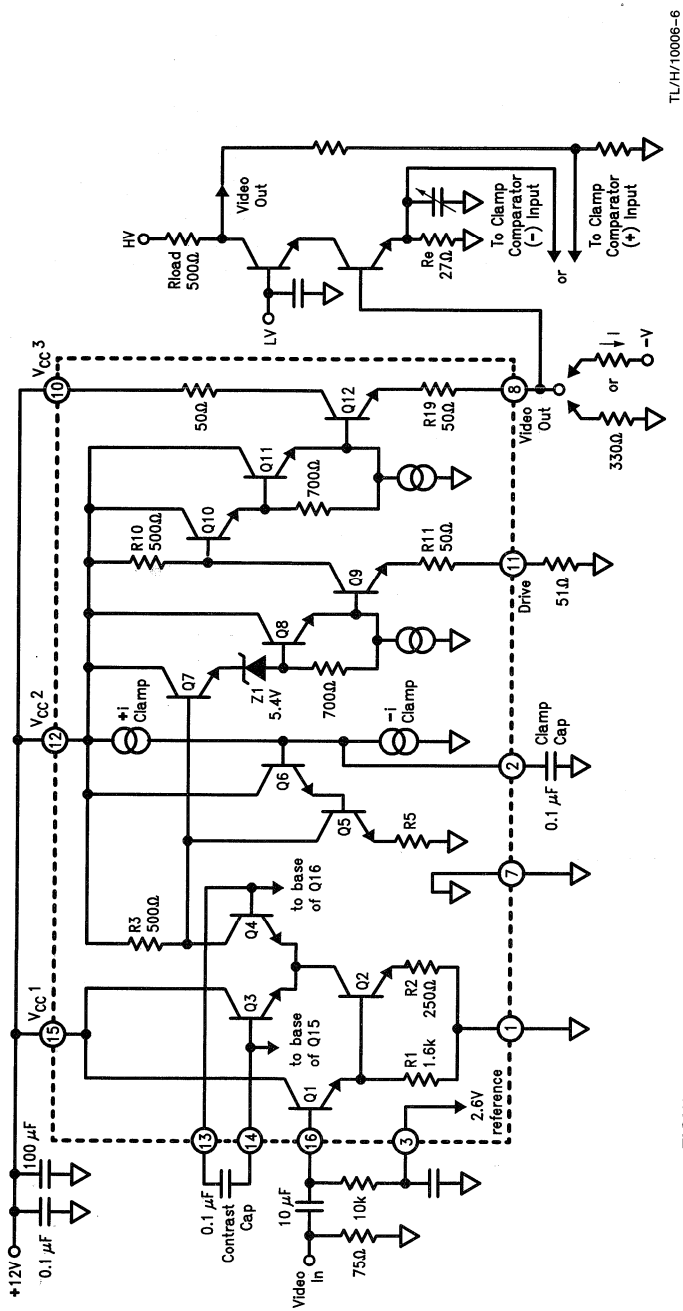


FIGURE 6. Simplified LM1201 Video Amplifier Section with Recommended External Components

Circuit Description (Continued)

The "Drive" pin will allow the user to set the maximum gain of the amplifier based on the range of input video signal levels and the CRT stage gain if it is fixed or limited. When using three LM1201 devices for high resolution RGB applications, the "Drive" pin allows the user to trim the gain of each channel to correct for differences in the three CRT cathodes. A small capacitor (12 pF) in shunt with a 51Ω drive resistor at this pin will extend the high frequency gain of the video amplifier by compensating for some of the internal high frequency roll off. The 51Ω resistor will set the system gain to approximately 8 or 18 dB. The video signal at the collector of Q9 is buffered and level shifted down by Q10 and Q11 to the base of the output emitter follower Q12. Between the emitter of Q12 and the video output pin is a 50Ω resistor which is included to prevent spurious oscillations when driving capacitive loads. An external emitter resistor must be added between the video output pin and ground. The value of this resistor should not be less than 330Ω, otherwise package power limitations may be exceeded when worst case (high supply, max supply current, max temp) calculations are made. If negative going pulse slewing is a problem because of high capacitive loads (>10 pF), a more efficient method of emitter pull down would be to connect a suitable resistor to a negative supply voltage. This has the effect of a current source pull down when the minus supply voltage is −12V, and the emitter current is approximately 10 mA. The system gain will also increase slightly because less signal will be lost across the internal 50Ω resistor. Precautions must be taken to prevent the video output pin from going below ground since IC substrate currents may cause erratic operation. The collector current from the video output transistor is returned to the power supply at V_{CC3}, pin 10. When making power dissipation calculations note that the datasheet specifies only the V_{CC1} and V_{CC2} supply currents at 12V. The IC power dissipation contribution of V_{CC3} is dependent upon the video output emitter pull down load.

In normal operation the minimum black level voltage that can be set at the video output pin is approximately 2V at maximum contrast setting. In applications that require a lower black level voltage, a resistor (approximately 16 kΩ) can be added from pin 3 to ground. This has the effect of raising the DC voltage at the collector of Q4 which will extend the range of the black level clamp by allowing Q5 to remain active. In applications that require video amplifier shutdown due to fault conditions detected by monitor protection circuits, pin 3 and the wiper arms of the contrast and brightness controls can be grounded without harming the IC. This assumes some series resistance between the top of the control potentiometers and V_{CC}.

Figure 7 shows the internal construction of the pin 3 2.6V reference circuit which is used to provide temperature and supply voltage tracking compensation for the video amplifier input. The value of the external DC biasing resistors should not be larger than 10 kΩ when using more than one LM1201 (e.g. in RGB systems) because minor differences in input bias currents on the individual video amplifiers may cause offsets in gain.

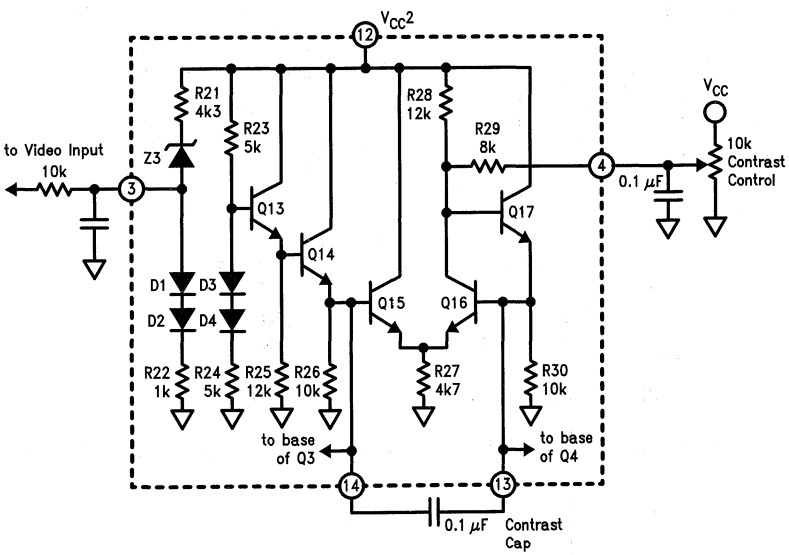


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FIGURE 7. LM1201 Video Input Voltage Reference and Contrast Control Circuits

Circuit Description (Continued)

Figure 7 also shows how the contrast control circuit is configured. Resistors R23, R24, diodes D3, D4, and transistor Q13 are used to establish a low impedance zero TC half supply voltage reference at the base of Q14. The differential amplifier formed by Q15, Q16 and feedback transistor Q17 along with resistors R27, R28 establish a differential base voltage for Q3 and Q4 in *Figure 6*. When externally adding or subtracting current from the collector of Q16, a new differential voltage is generated that reflects the change in the ratio of currents in Q15 and Q16. To provide voltage control of the Q16 current, resistor R29 is added between the Q16 collector and pin 4. A capacitor should be added from pin 4 to ground to prevent noise from the contrast control pot from entering the IC.

Figure 8 is a simplified schematic of the clamp gate and clamp comparator section of the LM1201. The clamp gate circuit consists of a PNP input buffer transistor (Q18), a PNP emitter coupled pair referenced on one side to 2.1V (Q19, Q20) and an output switch (Q21). When the clamp gate input at pin 5 is high (>1.5V), the Q21 switch is on and shunts the I1 1mA current to ground. When pin 5 is low (<1.3V), the Q21 switch is off and the I1 1mA current source is mirrored or "turned around" by reference diode D5 and Q26 to provide a 1mA current source for the clamp comparator. The inputs to the comparator are similar to the clamp gate input except that an NPN emitter coupled pair is used to control the current which will charge or discharge the clamp capacitor at pin 2. PNP transistors are used at the inputs because they offer a number of advantages over NPNs. PNPs will operate with base voltages at or near ground and will usually have a greater reverse emitter-base breakdown voltage (BVebo). Because the differential input voltage to the clamp comparator during the video scan period could be greater than the BVebo of NPN transistors, resistor R34 with a value one half that of R33 or R35 is connected between the bases of Q23 and Q27. This resistor will limit the maximum differential input to Q24, Q25 to approximately 350 mV. The clamp comparator common mode range extends from ground to approximately 9V and the maximum differential input voltage is V_{CC} and ground.

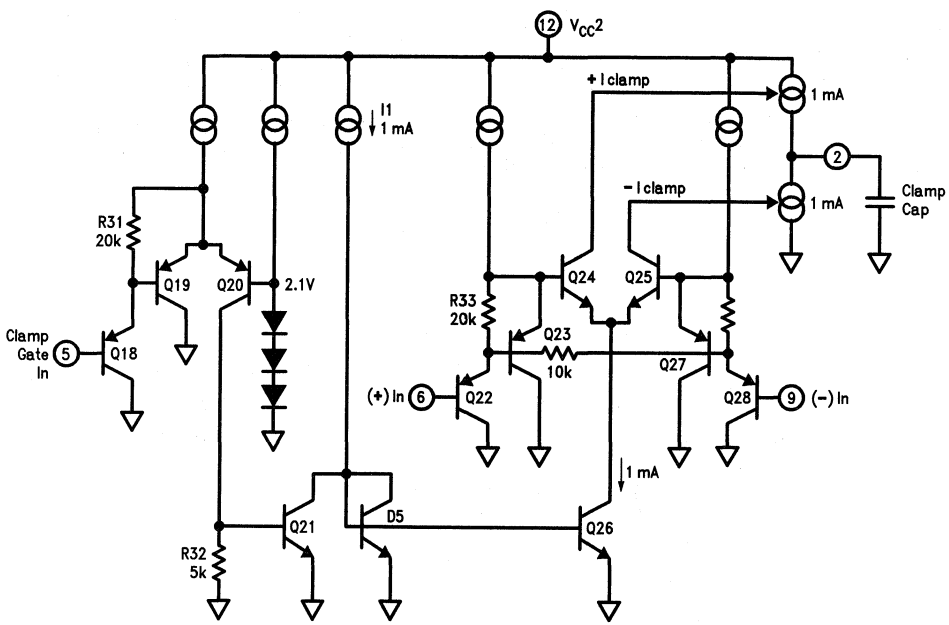

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FIGURE 8. Simplified Schematic of LM1201 Clamp Gate and Clamp Comparator Circuits

Applications Information

Figure 9 shows the configuration of a high frequency amplifier with non-gated DC feedback. Pin 5 is tied low to turn on the clamp comparator (feedback amplifier). The inverting input (pin 9) is connected to the amplifier output from a low pass filter. Additional low frequency filtering is provided by the clamp capacitor. The Drive pin is grounded to allow for the widest range of output signals. Maximum output swing is achieved when the DC output is set to approximately 4.5V.

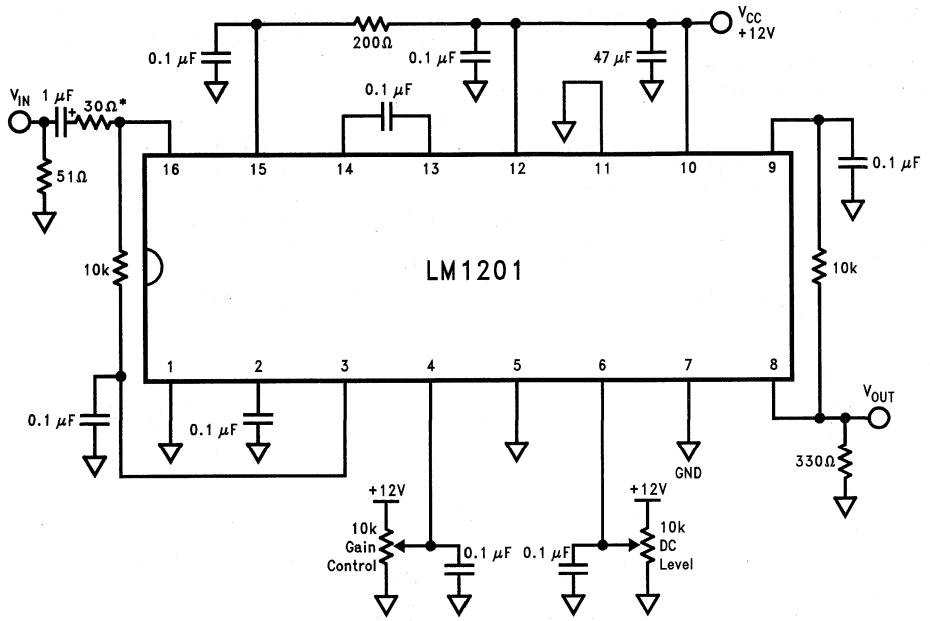

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FIGURE 9. High Frequency Amplifier/Attenuator Circuit with Non-Gated DC Feedback (Non-Video Applications)

Applications Information (Continued)

Figure 10 shows the LM1201 set up as a video amplifier with biphase outputs. Because the collector of output transistor Q12 is the only internal connection to V_{CC3}, a 75Ω termination to the power supply voltage allows one to obtain inverted video at pin 10. Black level on the non-inverted video output (pin 8) is set to 1.5V by the voltage divider on pin 6.

Figure 11 shows how a high frequency video switch may be designed using multiple LM1201 devices. All outputs can be OR'ed together assuming no more than one channel is selected at any given time. Channel selection is accomplished by keeping the appropriate SELECT SWITCH open. Closing the SELECT SWITCH on a given channel disables that channel's output (pin 8) leaving it in a high impedance state. A single pair of contrast and brightness potentiometers control the selected channel's gain and output DC level.

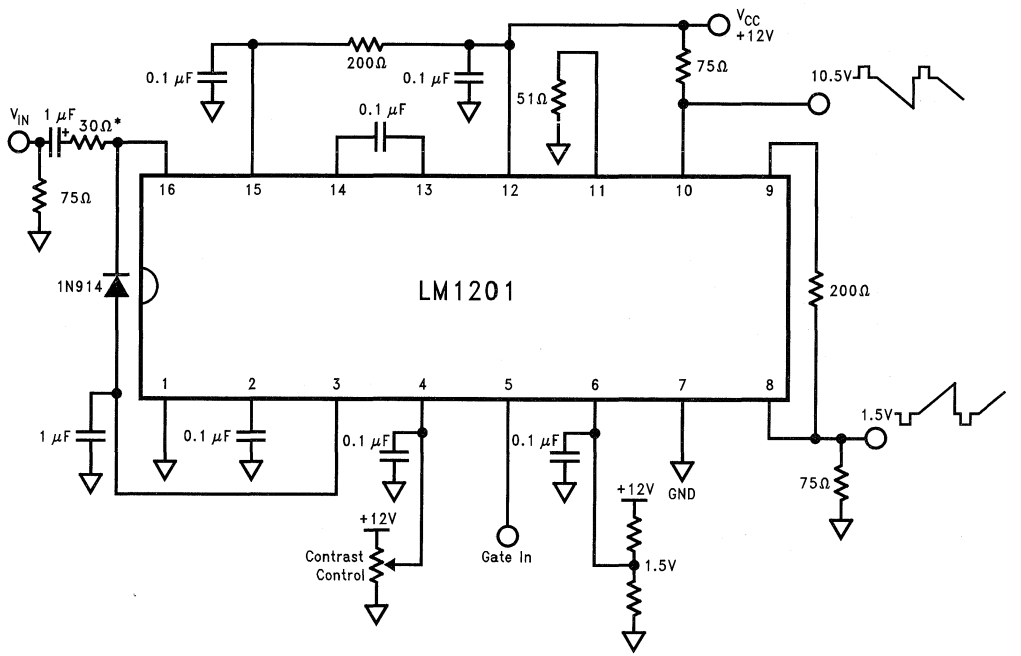

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FIGURE 10. Preclamped Video Amplifier with Biphase Outputs

Applications Information (Continued)

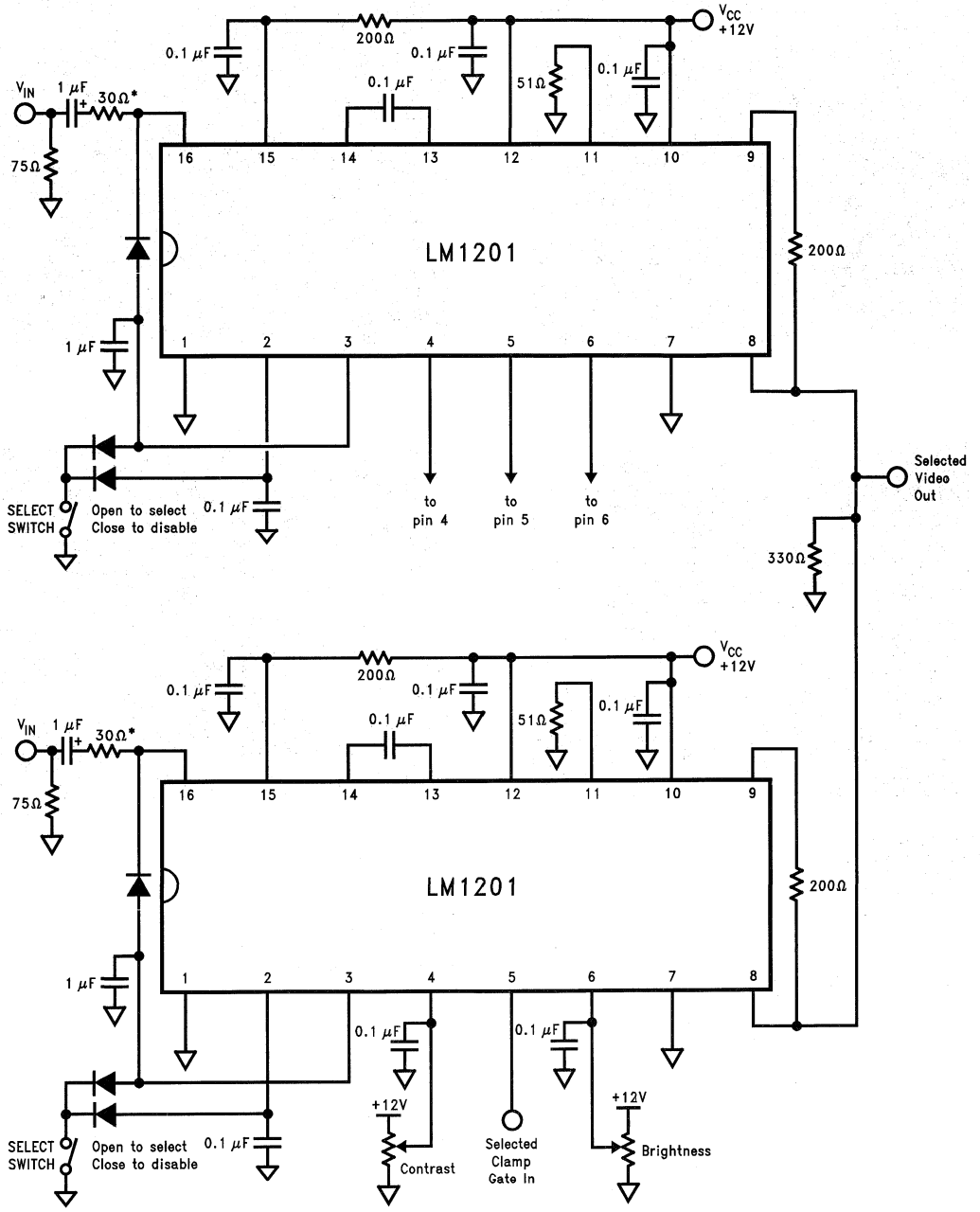

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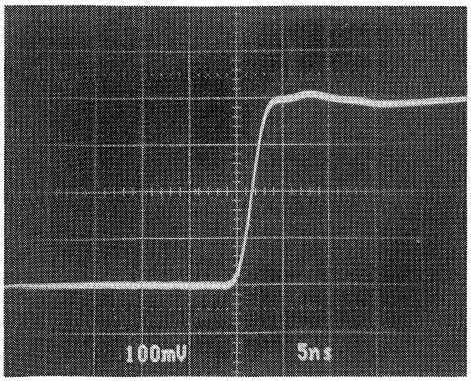
FIGURE 11. High Frequency Video Switch with Common Contrast and Brightness Controls

Rise Time No Socket



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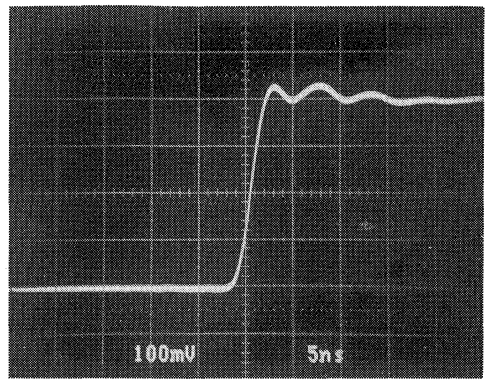
Rise Time In Socket



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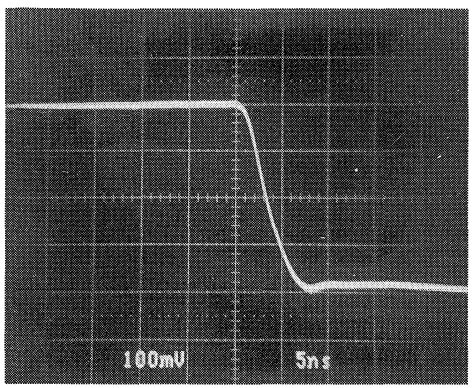
Fall Time No Socket



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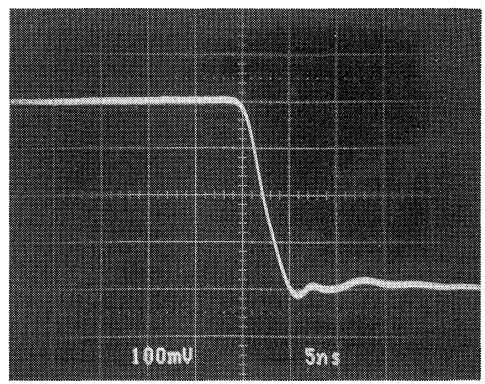
Fall Time In Socket

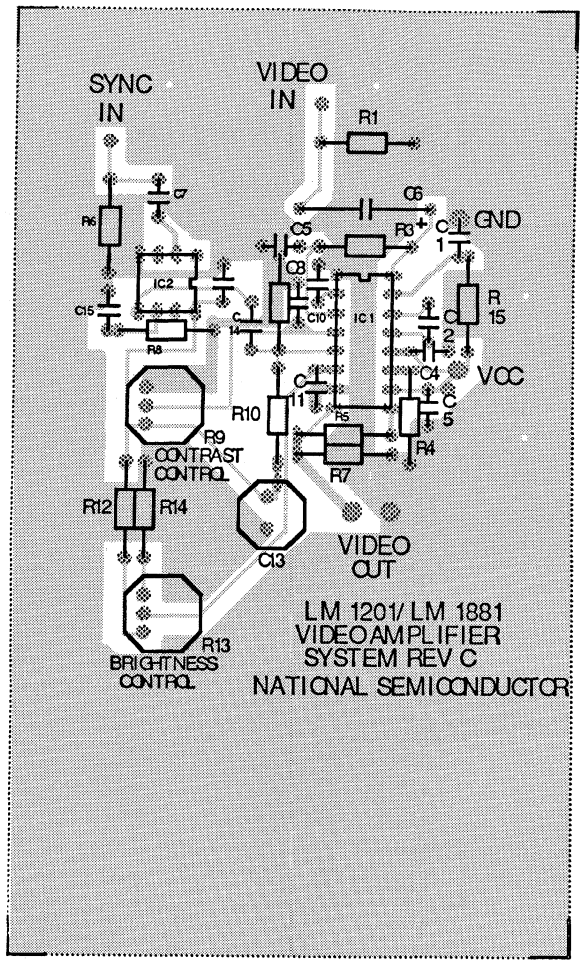


TL/H/10006–15

HP8082 pulse generator
HP10241A 10:1 voltage divider
HP1120A 500 MHz FET probe
Tektronix 2465A 350 MHz scope

Scale for All Photos—Vert: 1V/Div
Horiz: 5 ns/Div

- Actual output signal swings 4 V_{p-p} (10:1 divider is used)
- Contrast is set to maximum
- V_{IN} = 500 mV_{p-p}
- R_{DRIVE} = 50Ω
- Vertical scale is actually 1V/div and not 100 mV/div due to 10:1 attenuator used.
- Outputs are centered at 4V DC.



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Note: The p.c.b. layout shown above is suitable for evaluating the performance of the LM1201. Although it is similar to the typical application circuit of Figure 3, there is no c.r.t. driver stage. Instead, a feedback resistor is connected between Pins 8 and 9 and the brightness control is connected to Pin 6. Again, for best results, a socket should not be used for the LM1201.

COMPONENT VALUES:

R1	75Ω, 5%, 1/4 watt, carbon composition	C1	0.1 μF, ceramic
R3	10 kΩ, 5%, 1/4 watt, carbon composition	C2	0.1 μF, ceramic
R4	50Ω, 5%, 1/4 watt, carbon composition	C4	0.1 μF, ceramic
R5	200Ω, 5%, 1/4 watt, carbon composition	C5	0.1 μF, ceramic
R6	75Ω, 5%, 1/4 watt, carbon composition	C6	10 μF/6V, electrolytic
R7	330Ω, 5%, 1/4 watt, carbon composition	C7	0.1 μF, ceramic
R8	680 kΩ, 5%, 1/4 watt, carbon composition	C8	0.1 μF, ceramic
R9	10 kΩ, trim pot, helitrim model 91	C9	0.1 μF, ceramic
R10	5.1 kΩ, 5%, 1/4 watt, carbon composition	C10	0.1 μF, ceramic
R11	43 kΩ, 5%, 1/4 watt, carbon composition	C11	0.1 μF, ceramic
R12	12 kΩ, 5%, 1/4 watt, carbon composition	C12	0.1 μF, ceramic
R13	10 kΩ, trim pot, helitrim model 91	C13	100 μF/15V, electrolytic
R14	2 kΩ, 5%, 1/4 watt, carbon composition	C14	0.001 μF, mica
R15	200Ω, 5%, 1/4 watt, carbon composition	C15	0.1 μF, ceramic
IC1	LM1201		
IC2	LM1881		

National Semiconductor

LM1202 230 MHz Video Amplifier System

General Description

The LM1202 is a very high frequency video amplifier system intended for use in high resolution monochrome or RGB color monitor applications. In addition to the wideband video amplifier the LM1202 contains a gated differential input black level clamp comparator for brightness control, a DC controlled attenuator for contrast control and a DC controlled sub contrast attenuator for drive control. The DC control for the contrast attenuator is pinned out separately to provide a more accurate control system for RGB color monitor applications. All DC controls offer a high input impedance and operate over a 0V to 4V range for easy interface to bus controlled alignment systems. The LM1202 operates from a nominal 12V supply but can be operated with supply voltages down to 8V for applications that require reduced IC package power dissipation characteristics.

Features

- Wideband video amplifier (f_{-3dB} = 230 MHz at V_O = 4 V_{PP})
- t_r, t_f = 1.5 ns at V_O = 4 V_{PP}
- Externally gated comparator for brightness control
- 0V to 4V high input impedance DC contrast control (>40 dB range)
- 0V to 4V high input impedance DC drive control (±3 dB range)
- Easy to parallel three LM1202s for optimum color tracking in RGB systems
- Output stage clamps to 0.65V and provides up to 9V output voltage swing
- Output stage directly drives most hybrid or discrete CRT amplifier stages

Applications

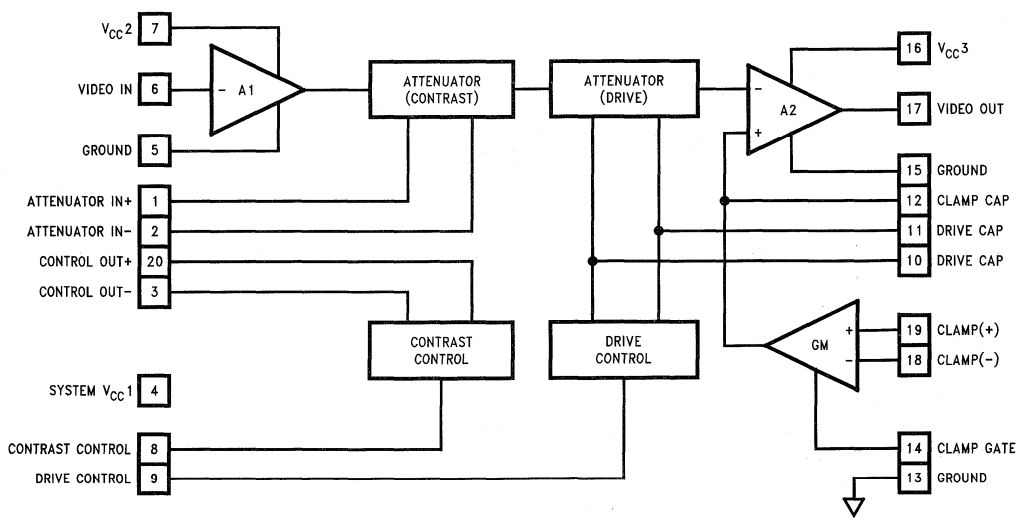
High resolution CRT monitors

Video switches

Video AGC amplifier

Wideband amplifier with gain and DC offset control

Block and Connection Diagram



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Order Number LM1202N or LM1202M
See NS Package Number N20A or M20B

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage V_{CC} Pins 4, 7, 16 to Ground Pins 5, 13, 15 — 13.5V

Voltage at Any Input Pin (V_{IN}) — $V_{CC} \geq V_{IN} \geq GND$

Video Output Current (I_{17}) — 28 mA

Package Power Dissipation at $T_A = 25°C$ (Above 25°C Derate Based θ_{JA} and T_J) — 1.56W

Package Thermal Resistance (θ_{JA})
- N20A — 68°C/W
- M20B — 90°C/W

Junction Temperature (T_J) — 150°C

Storage Temperature Range (T_{stg}) — −65°C to +150°C

Lead Temperature
- N Package (Soldering, 10 sec.) — 265°C

ESD Susceptibility
- Human Body Model: 100 pF Discharged through a 1.5k Resistor — 1.5 kV

Operating Ratings (Note 2)

Temperature Range — −20°C to +80°C

Supply Voltage (V_{CC}) — $8V \leq V_{CC} \leq 13.2V$

DC Electrical Characteristics

See Test Circuit *(Figure 1)*, $T_A = 25°C$, V4 = V7 = V16 = 12V, S1 Open, V19 = 4V, V8 = 4V, V9 = 4V, V14 = 0V unless otherwise noted.

Symbol	Parameter	Conditions	Typical (Note 3)	Limit (Note 4)	Units
I_S 4, 7, 16	Total Supply Current	$R_{Load} = \infty$ (Note 5)	48	60	mA (max)
V_6	Video Input Bias Voltage		2.4	2	V (min)
V_{14L}	Clamp Gate Low Input Voltage	Clamp Comparator On		0.8	V (max)
V_{14H}	Clamp Gate High Input Voltage	Clamp Comparator Off		2	V (min)
I_{14L}	Clamp Gate Low Input Current	$V_{14} = 0V$	−0.5		μA
I_{14H}	Clamp Gate High Input Current	$V_{14} = 12V$	0.005		μA
I_{12+}	Clamp Cap Charge Current	$V_{12} = 0V$	800	500	μA (min)
I_{12-}	Clamp Cap Discharge Current	$V_{12} = 5V$	−800	−500	μA (min)
V_{17L}	Video Output Low Voltage	$V_{12} = 0V$	0.2	0.65	V (max)
V_{17H}	Video Output High Voltage	$V_{12} = 6V$	10	9	V (min)
V_{OS}	Comparator Input Offset Voltage	$V_{18} - V_{19}$	15	±50	mV (max)

AC Electrical Characteristics

See Test Circuit *(Figure 1)*, $T_A = 25°C$, V4 = V7 = V16 = 12V, S1 Closed, V19 = 4V, V8 = 4V, V9 = 4V, V14 = 0V unless otherwise noted.

Symbol	Parameter	Conditions	Typical (Note 3)	Limit (Note 4)	Units
R_{IN}	Video Amplifier Input Resistance	$f_{IN} = 12$ kHz	20		kΩ
A_V max	Video Amplifier Gain	$V_8 = 4V$, $V_9 = 4V$	20	16	V/V (min)
ΔA_V 2V	Attenuation at 2V	Ref: A_V max, $V_8 = 2V$	−6		dB
ΔA_V 0.5V	Attenuation at 0.5V	Ref: A_V max, $V_8 = 0.5V$	−38	−23	dB (min)
Δ Drive	Δ Gain Range	$V_9 = 0V$ to 4V	6	5	dB (min)
THD	Video Amplifier Distortion	$V_O = 4\ V_{PP}$, $f_{IN} = 12$ kHz	0.5	1	% (max)
$f_{-3\ dB}$	Video Amplifier Bandwidth (Note 6)	$V_O = 4\ V_{PP}$	230		MHz
t_r	Output Rise Time (Note 6)	$V_O = 4\ V_{PP}$	1.5	2	ns (max)
t_f	Output Fall Time (Note 6)	$V_O = 4\ V_{PP}$	1.5	2	ns (max)

Electrical Characteristics (Continued)

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur.

Note 2: Operating Ratings indicate conditions for which the device is functional but do not guarantee specific performance limits. For guaranteed specifications and test conditions see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

Note 3: Typical specifications are specified at +25°C and represent the most likely parametric norm.

Note 4: Tested limits are guaranteed to National's AOQL (Average Outgoing Quality Level).

Note 5: The supply current specified is the quiescent current for V_{CC1}, V_{CC2} and V_{CC3} with $R_{Load} = \infty$, see *Figure 1's* test circuit. The total supply current also depends on the output load, R_{Load}. The increase in device power dissipation due to R_{Load} must be taken into account when operating the device at the maximum ambient temperature.

Note 6: When measuring video amplifier bandwidth or pulse rise and fall times, a double sided full ground plane printed circuit board is recommended. The measured rise and fall times are effective rise and fall times, taking into account the rise and fall times of the generator and the oscilloscope.

Test Circuit

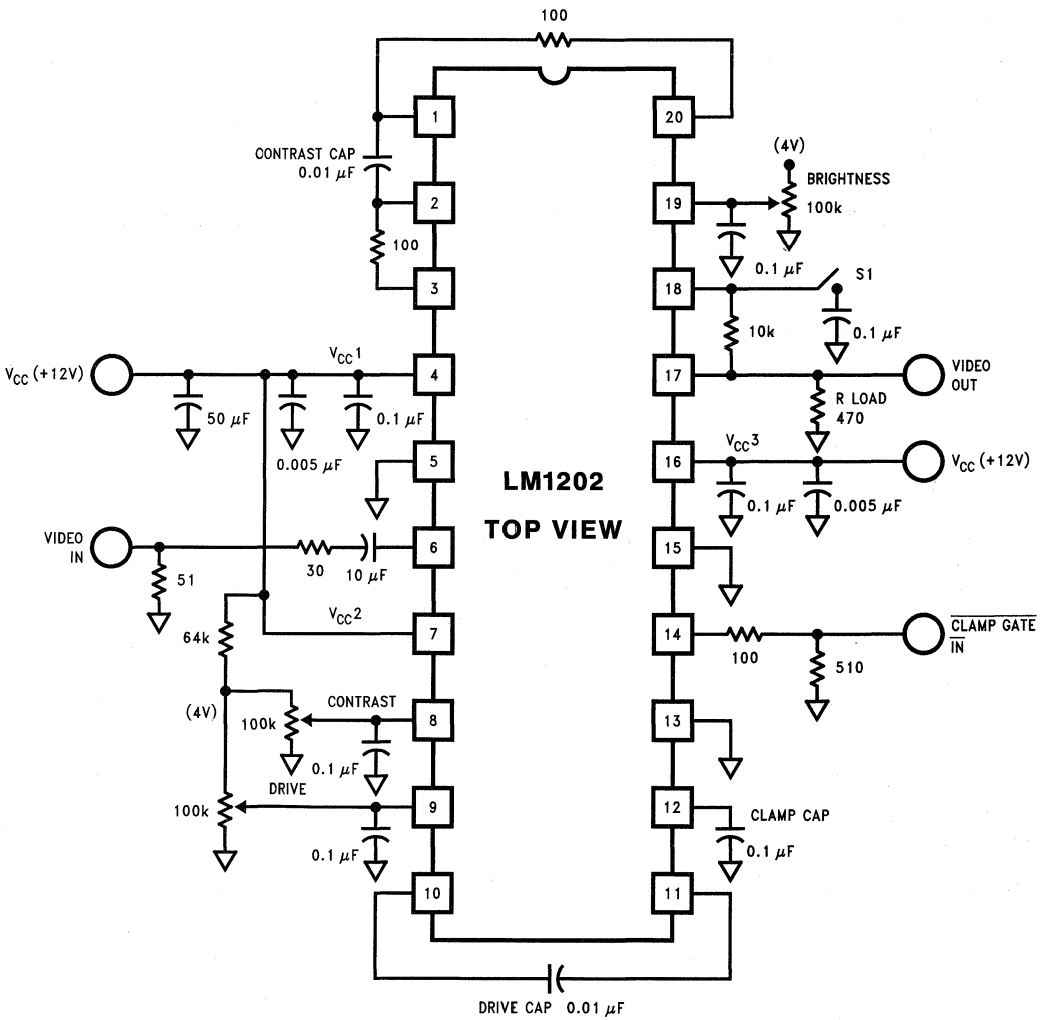

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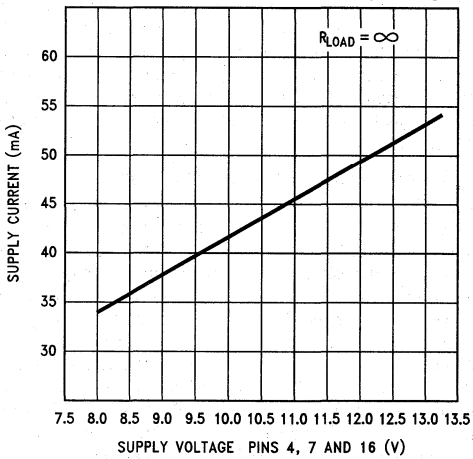
FIGURE 1. LM1202 Test Circuit

Typical Performance Characteristics (V_{CC} = 12V, T_A = 25°C unless otherwise specified)

Quiescent Supply Current vs Supply Voltage



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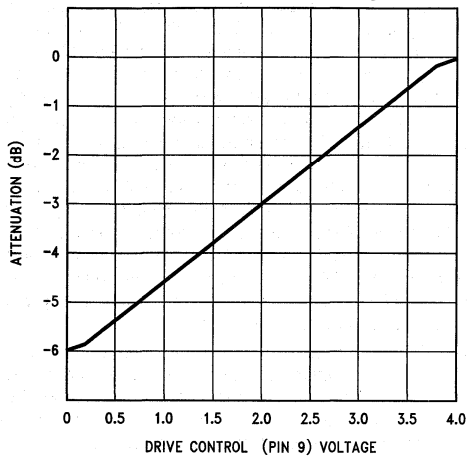
Attenuation vs Drive Control Voltage



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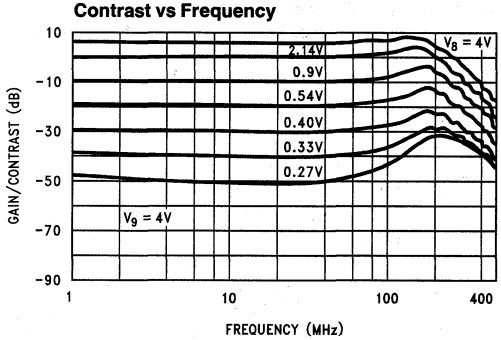
Contrast vs Frequency



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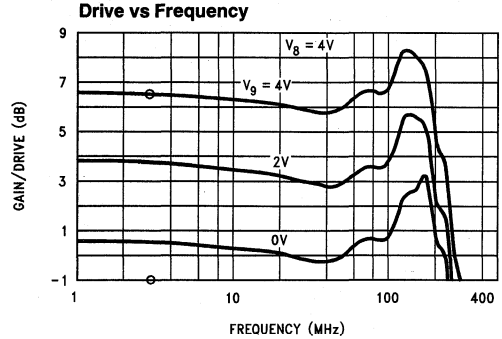
Drive vs Frequency



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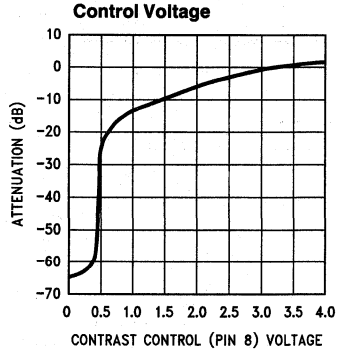
Attenuation vs Contrast Control Voltage



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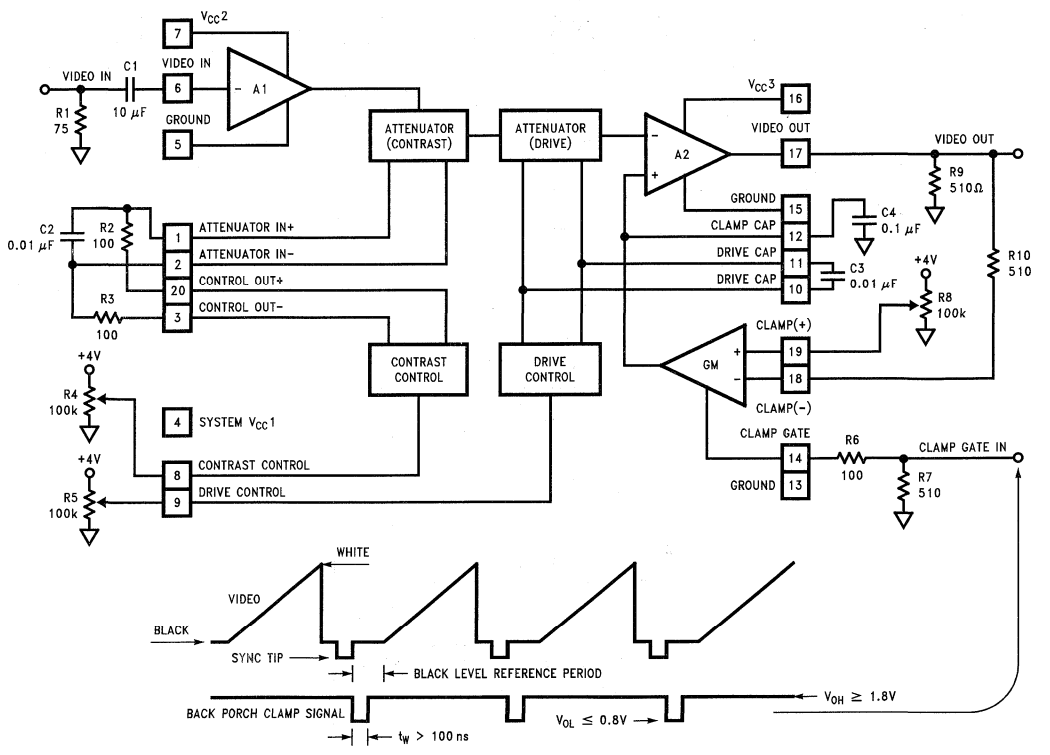
Circuit Description

Figure 2 shows a block diagram of the LM1202 video amplifier along with contrast and brightness (black level) control. Contrast control is a DC-operated attenuator which varies the AC gain of the amplifier. Signal attenuation (contrast) is achieved by varying the base drive to a differential pair and thereby unbalancing the current through the differential pair. As shown in *Figure 2*, pin 20 provides a 5.3V bias voltage for the positive input of the attenuator (pin 1). Pin 3 provides a control voltage for the negative input (pin 2) of the attenuator. The voltage at pin 3 varies as the voltage at the contrast control input (pin 8) varies thus providing signal attenuation. The gain is maximum (0 dB attenuation) if the voltage at pin 8 is 4V and is minimum (maximum attenuation) if the voltage at pin 8 is 0V. The 0V to 4V DC-operated drive control at pin 9 provides a 6 dB gain adjustment range. This feature is necessary for RGB applications where independent gain adjustment of each channel is required.

The brightness or black level clamping requires a "sample and hold" circuit which holds the DC bias of the video amplifier constant during the black level reference portion of the video waveform. Black level clamping, often referred to as DC restoration, is accomplished by applying a back porch clamp signal to the clamp gate input pin (pin 14). The clamp comparator is enabled when the clamp signal goes low during the black level reference period (see *Figure 2*). When the clamp comparator is enabled, the clamp capacitor connected to pin 12 is either charged or discharged until the voltage at the minus input of the comparator matches the voltage set at the plus input of the comparator. During the video portion of the signal, the clamp comparator is disabled and the clamp capacitor holds the proper DC bias. In a DC coupled cathode drive application, picture brightness function can be achieved by varying the voltage at the comparator's plus input. Note that the back porch clamp pulse width (t_W in *Figure 2*) must be greater than 100 ns for proper operation.

VIDEO AMPLIFIER SECTION (Input Stage)

A simplified schematic of LM1202's video amplifier input stage is shown in *Figure 3*. The 5.4V zener diode, Q1, Q6 and R2 bias the base of Q7 at 2.6V. The AC coupled video signal applied to pin 6 is referenced to the 2.6V bias voltage. Transistor Q7 buffers the video signal, V_{IN}, and Q8 converts the voltage to current. The AC collector current through Q8 is $I_{C8} = V_{IN}/R9$. Under maximum gain condition, transistors Q9 and Q11 are off and all of I_{C8} flows through the load resistors R10 and R11. The maximum signal gain at the base of Q13 is, $A_{V1} = -(R10 + R11)/R9 = -2$. Signal attenuation is achieved by varying the base drive to the differential pairs Q9, Q10 and Q11, Q12 thereby unbalancing the collector currents through the transistor pairs. Base of Q10 is biased at 5.3V by externally connecting pin 1 to pin 20 through a 100Ω resistor. Pin 2 is connected to pin 3 through a 100Ω resistor. Adjusting the contrast voltage at



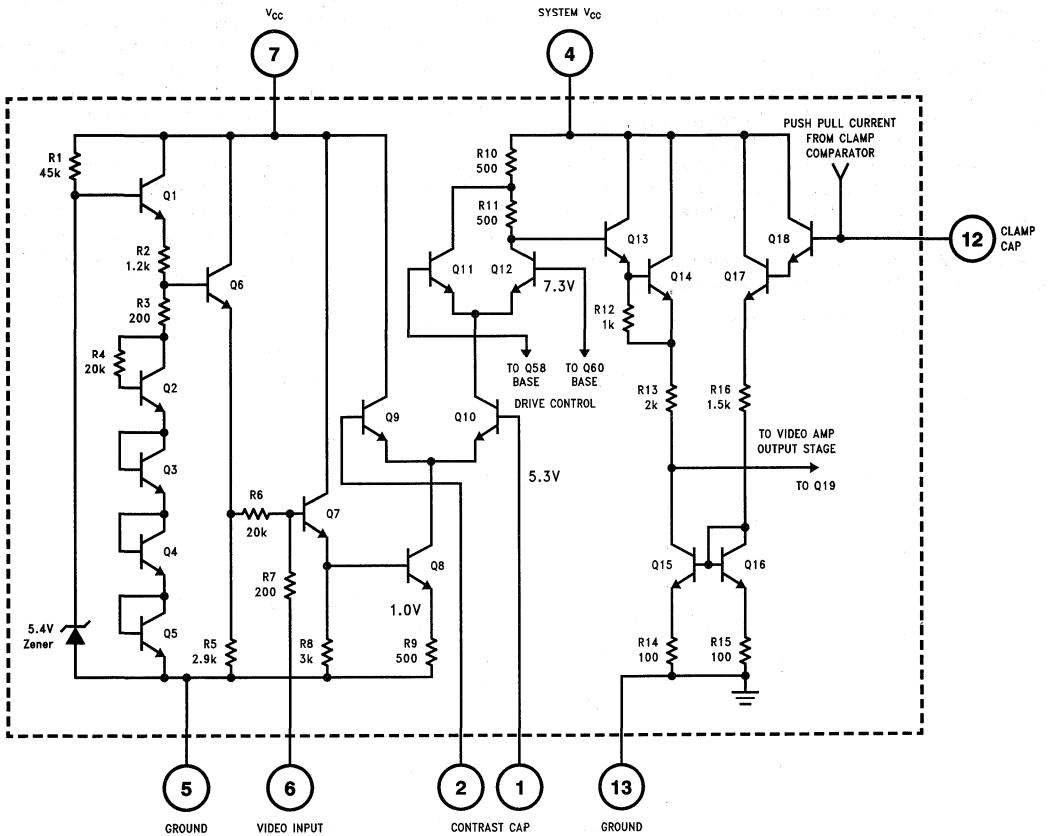
TL/H/11440–3

FIGURE 2. Block Diagram of the LM1202 Video Amplifier with Contrast and Brightness (Black Level) Control

Circuit Description (Continued)

pin 8 produces a control voltage at pin 3 which drives the base of Q9. By varying the voltage at the base of Q9, Q8's collector current (I_{C8}) is diverted away from the load resistors R10 and R11, thereby providing signal attenuation. Maximum attenuation is achieved when all of I_{C8} flows through Q9 and no current flows through the load resistors.

The differential pair Q11 and Q12 provide drive control. Q12's base is internally biased at 7.3V. Adjusting the voltage at the drive control input (pin 9) produces a control voltage at the base of Q11. With Q9 off and Q12 off, all of I_{C8} flows through R10, thus providing a gain of $A_{V1} = -(R10/R9) \times V_{IN} = -1$. Drive control thus provides a 6 dB attenuation range.



TL/H/11440–4

FIGURE 3. Simplified Schematic of the LM1202 Video Amplifier Input Stage

Circuit Description (Continued)

VIDEO AMPLIFIER SECTION (Output Stage)

A simplified schematic of LM1202's video amplifier output stage is shown in *Figure 4*. The output stage is the second gain stage. Ideally the gain of the second gain stage would be $A_{V2} = -R21/R18 = -16$. Because of the output stage's low open loop gain, the gain is approximately $A_{V2} = -10$. Thus the maximum gain of the video amplifier is $A_V = A_{V1} \times A_{V2} = 20$. Transistors Q23 and Q24 provide a push-pull drive to the load. The output voltage can swing from 0.2V to 10V.

CONTRAST CONTROL SECTION

A simplified schematic of LM1202's contrast control section is shown in *Figure 5*. A 0V to 4V DC voltage is applied at the contrast input (pin 8). Transistors Q29, Q30 and Q34 buffer and level shift the contrast voltage to the base of Q36. The voltage at the emitter of Q36 equals the contrast voltage (V_{cont}) and the current through Q36's collector is given by $I_{C36} = V_{cont}/R28$.

Transistor Q36's collector current is used to unbalance the current through the differential pair comprised of Q38 and Q40. Q40's base is internally biased at 5.3V and made available at pin 20. Pin 20 is externally connected to pin 1 through a 100Ω resistor (see *Figures 2* and *3*). The base of Q38 (pin 3) is externally connected to pin 2 through a 100Ω resistor (see *Figures 2* and *3*). With $V_{cont} = 2V$, the differential pair (Q38, Q40) is balanced and the voltage at pins 1 and 2 is 5.3V. Under this condition, Q8's collector current is equally split between Q9 and Q10 (see *Figure 3*) and the amplifier's gain is half the maximum gain. If contrast voltage at pin 8 is greater than 2V then Q36's collector current increases, thus pulling Q38's collector node lower and consequently moving Q38's base below 5.3V. With pin 2 at a lower voltage than pin 1, current through Q10 (see *Figure 3*) increases and the amplifier's gain increases. With $V_{cont} = 4V$, the amplifier's gain is maximum.

If the contrast voltage at pin 8 is less than 2V then Q36's collector current decreases and Q38's base is pulled above 5.3V. With pin 2 voltage greater than pin 1 voltage, less current flows through Q10 (see *Figure 3*), consequently the amplifier's gain decreases. With $V_{cont} = 0V$, the amplifier's gain is minimum (i.e., maximum attenuation).

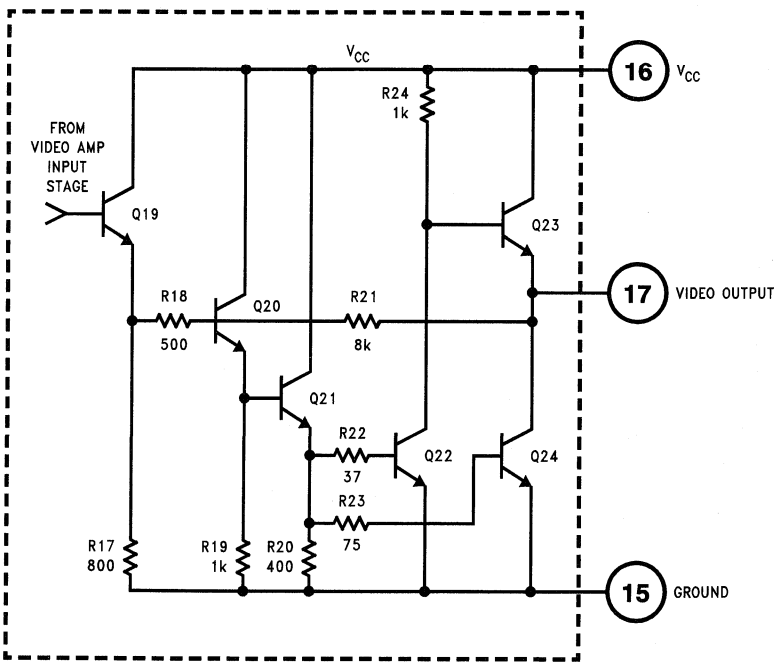


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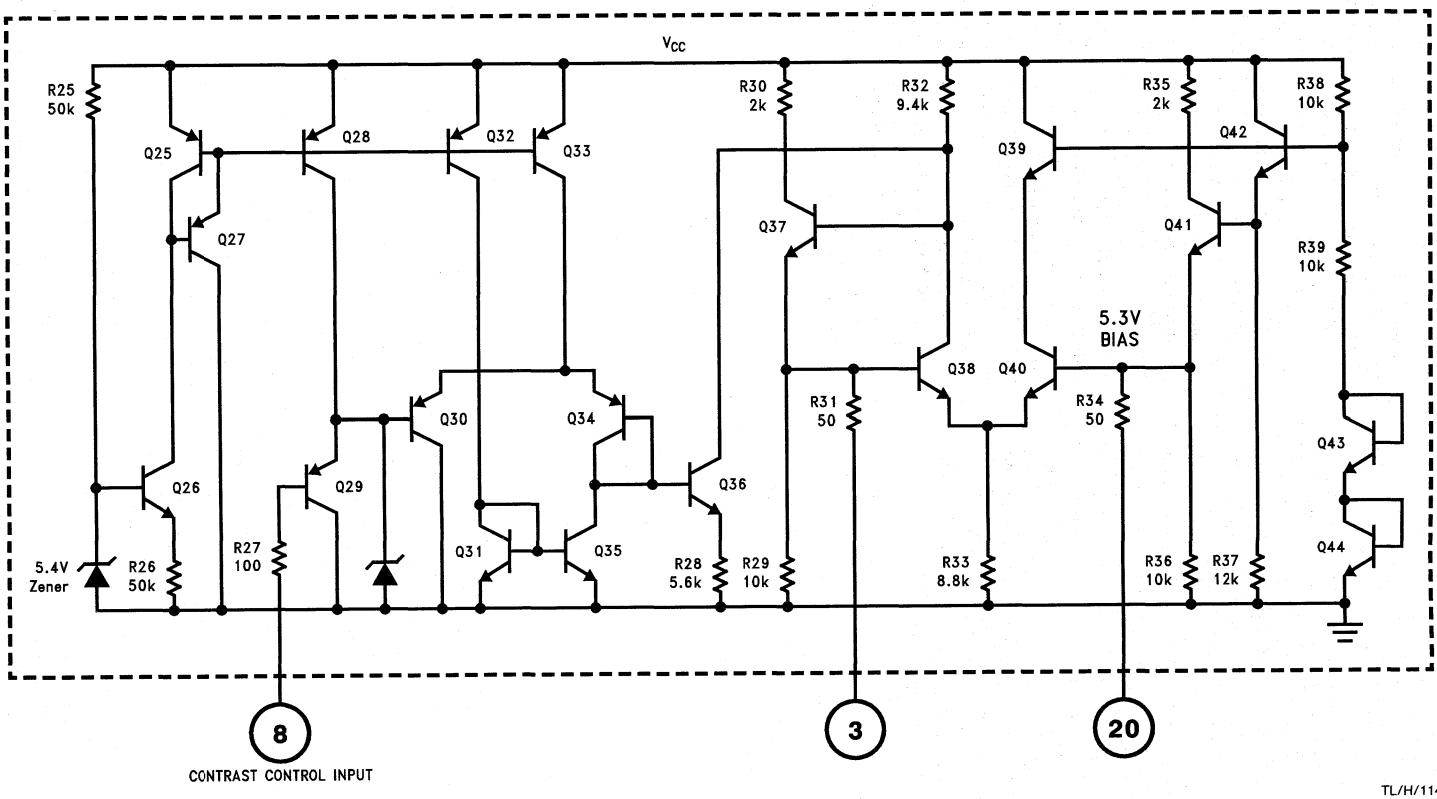
FIGURE 4. Simplified Schematic of LM1202 Video Amplifier Output Stage



TL/H/11440–6

FIGURE 5. Simplified Schematic of LM1202 Contrast Control

Circuit Description (Continued)

DRIVE CONTROL SECTION

A simplified schematic of the LM1202's drive control section is shown in *Figure 6*. A 0V to 4V DC voltage is applied at the drive control input (pin 9). Transistors Q49, Q50 and Q54 buffer and level shift the contrast voltage to the base of Q56. The voltage at the emitter of Q56 equals the drive voltage, V_{drive} and the current through Q56's collector is given by $I_{C56} = V_{drive}/R43$.

Transistor Q56's collector current is used to unbalance the current through the differential pair comprised of Q58 and Q60. Q60's base is internally biased at 7.3V and connected to the base of Q12 (see *Figure 3*). Q58's base is internally connected to the base of Q11 (see *Figure 3*). With V_{cont} = 2V, the differential pair (Q58, Q60) is balanced and the voltage at the bases of Q11 and Q12 is 7.3V. Under this condition, Q10's collector current is equally split between Q11 and Q12 (see *Figure 3*). If the drive voltage at pin 9 is greater than 2V then Q56's collector current increases, thus pulling Q58's collector node lower and consequently moving Q58's base below 7.3V. With base of Q11 below 7.3V, current through Q12 (see *Figure 3*) increases and the amplifier's gain increases. With V_{drive} = 4V, the amplifier's gain is maximum under maximum contrast condition (i.e., V_{cont} = 4V).

If the drive voltage at pin 8 is less than 2V then Q56's collector current decreases and Q58's base is pulled above 7.3V. With base of Q11 greater than 7.3V, less current flows through Q12 (see *Figure 3*), consequently the amplifier's gain decreases. With V_{drive} = 0V, the amplifier's gain is 6 dB less than the maximum gain.

CLAMP GATE AND CLAMP COMPARATOR SECTION

Figures 7 and *8* show simplified schematics of the clamp gate and clamp comparator circuits. The clamp gate circuit *(Figure 7)* consists of a PNP input buffer transistor (Q82), a PNP emitter coupled pair (Q85 and Q86) referenced on one side to 2.1V and an output switch transistor Q89. When the clamp gate input at pin 14 is high (> 1.5V) the Q89 switch is on and shunts the 200 μA current from current source Q90 to ground. When pin 14 is low (< 1.3V) the Q89 switch is off and the 200 μA current is mirrored by the current mirror comprised of Q91 and Q75 (see *Figure 8*). Consequently the clamp comparator comprised of the differential pair Q74 and Q77 is enabled. The input of the clamp comparator is similar to the clamp gate except that an NPN emitter coupled pair is used to control the current that will charge or discharge the clamp capacitor externally connected from pin 12 to ground. PNP transistors are used at the inputs because they offer a number of advantages over NPNs. PNPs will operate with base voltages at or near ground and will usually have a greater emitter base breakdown voltage (BVebo). Because the differential input voltage to the clamp comparator during the video scan period could be greater than the BVebo of NPN transistors, a resistor (R63) with a value one half that of R60 or R68 is connected between the bases of Q71 and Q79. The clamp comparator's common mode range is from ground to approximately 9V and the maximum differential input voltage is V_{CC}.

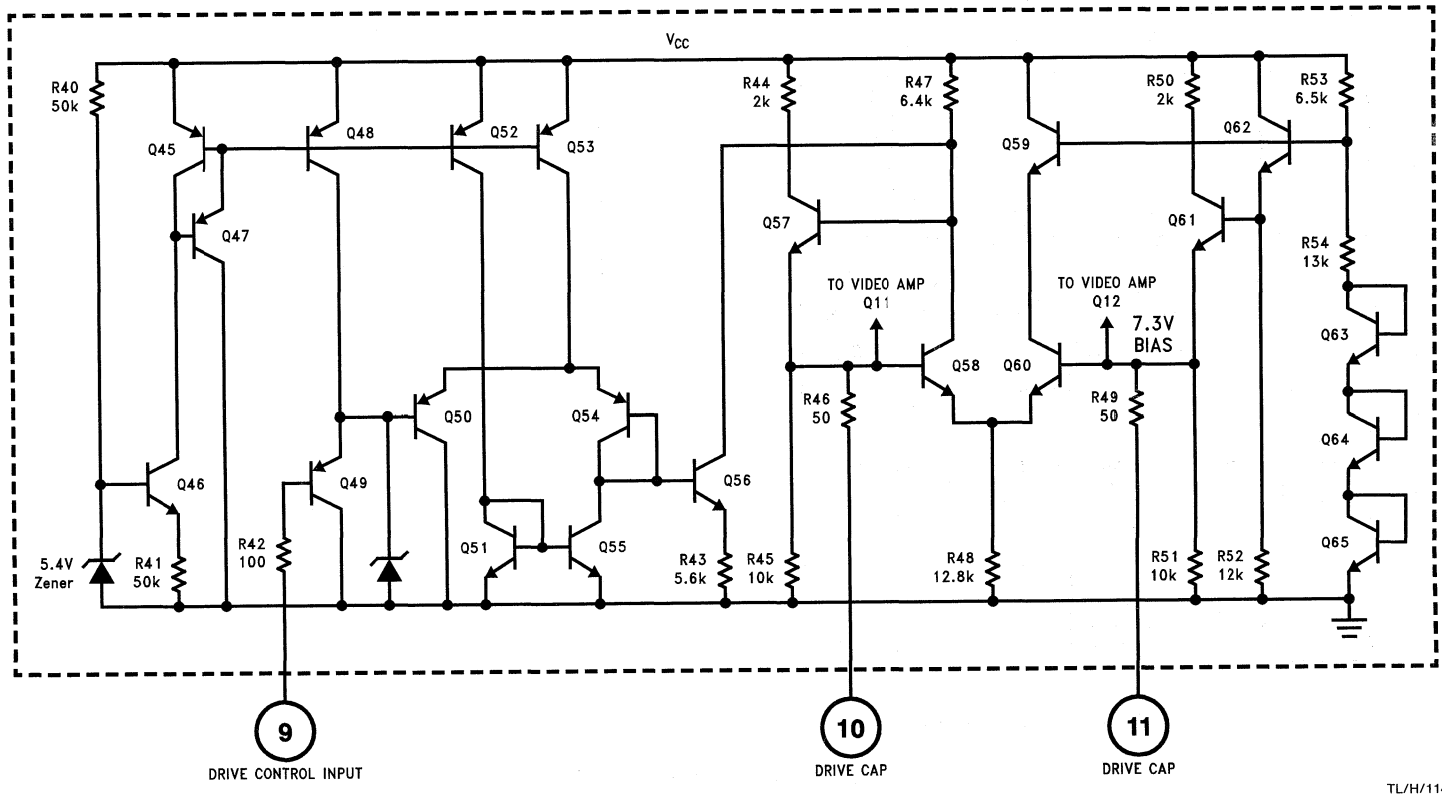


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FIGURE 6. Simplified Schematic of the LM1202 Drive Control

Circuit Description (Continued)

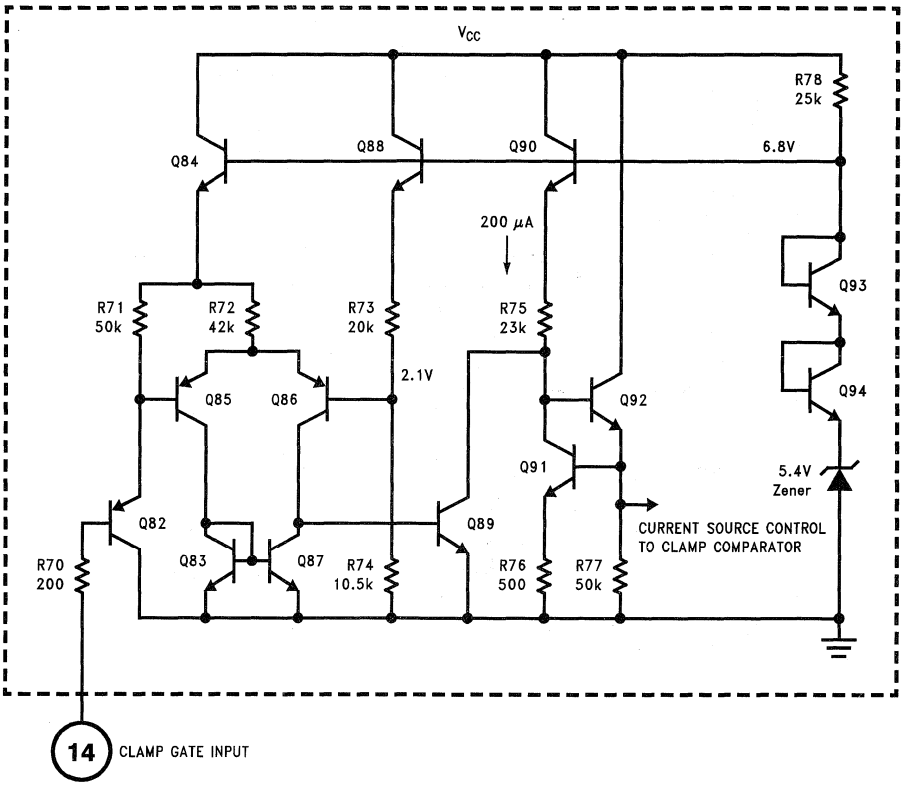

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FIGURE 7. Simplified Schematic of the LM1202 Clamp Gate Circuit

Circuit Description (Continued)

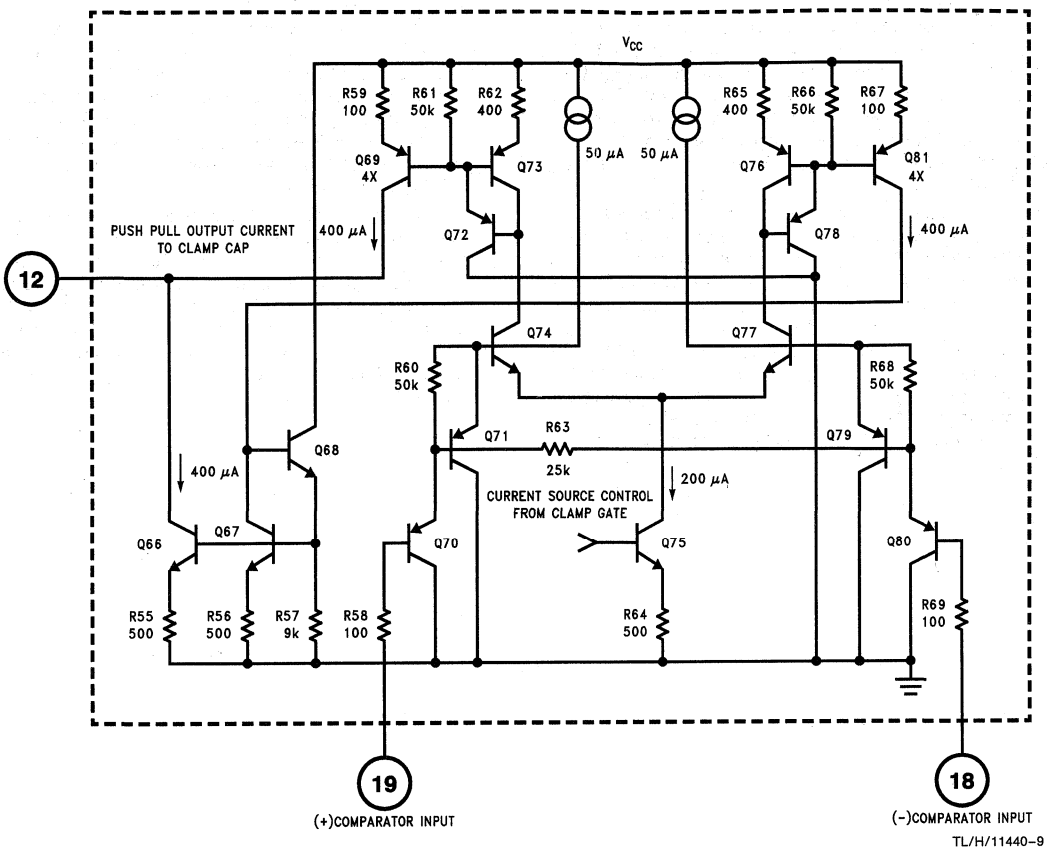

FIGURE 8. Simplified Schematic of the LM1202 Clamp Comparator Circuit

Applications of the LM1202

SINGLE VIDEO CHANNEL

A typical application for a single video channel is shown in *Figure 9*. The video signal is AC coupled to pin 6. The LM1202 internally biases the video signal to 2.6 V_{DC}. Contrast control is achieved by applying a 0V to 4V DC voltage at pin 8. The amplifier's gain is minimum (i.e., maximum signal attenuation) if pin 8 is at 0V and is maximum if pin 8 is at 4V. With pin 9 (drive control) at 0V, the amplifier has a maximum gain of 10.

For DC restoration, a clamp signal must be applied to the clamp gate input (pin 14). The clamp signal should be logic low (less than 0.8V) only during the back porch (black level reference period) interval (see *Figure 2*). The clamp gate input is TTL compatible. Brightness control is provided by applying a 0V to 4V DC voltage at pin 19. For example, if pin 19 is biased at 1V then the video signal's black level will be clamped at 1V. A 510Ω load resistor is connected from the video output pin (pin 17) to ground. This resistor biases the output stage of the amplifier. For power dissipation considerations, the load resistor should not be much less than 510Ω.

RGB VIDEO PREAMPLIFIER

Figure 10 shows an RGB video preamplifier circuit using three LM1202s. Note that pins 1 and 2 of IC1 are connected to pins 1 and 2 of IC2 and IC3 respectively. This allows IC1 to provide a master contrast control and optimum contrast tracking. Adjusting the contrast voltage at pin 8 of IC1 will vary the gain of all three video channels. Drive control input (pin 9) of each LM1202 allows individual gain adjustment for achieving white balance.

The black level of each video channel can be individually adjusted to the desired voltage by adjusting the voltage at pin 19. In a DC-coupled cathode drive application, adjusting the voltage at pin 19 of each IC will provide cutoff adjustment. In an AC-coupled cathode drive application, the video signal is AC coupled and DC restored at the cathode. In such an application, the video signal's black level may be clamped to the desired level by simply biasing pin 19 to the black level voltage by using a voltage divider at pin 19.

Applications of the LM1202 (Continued)

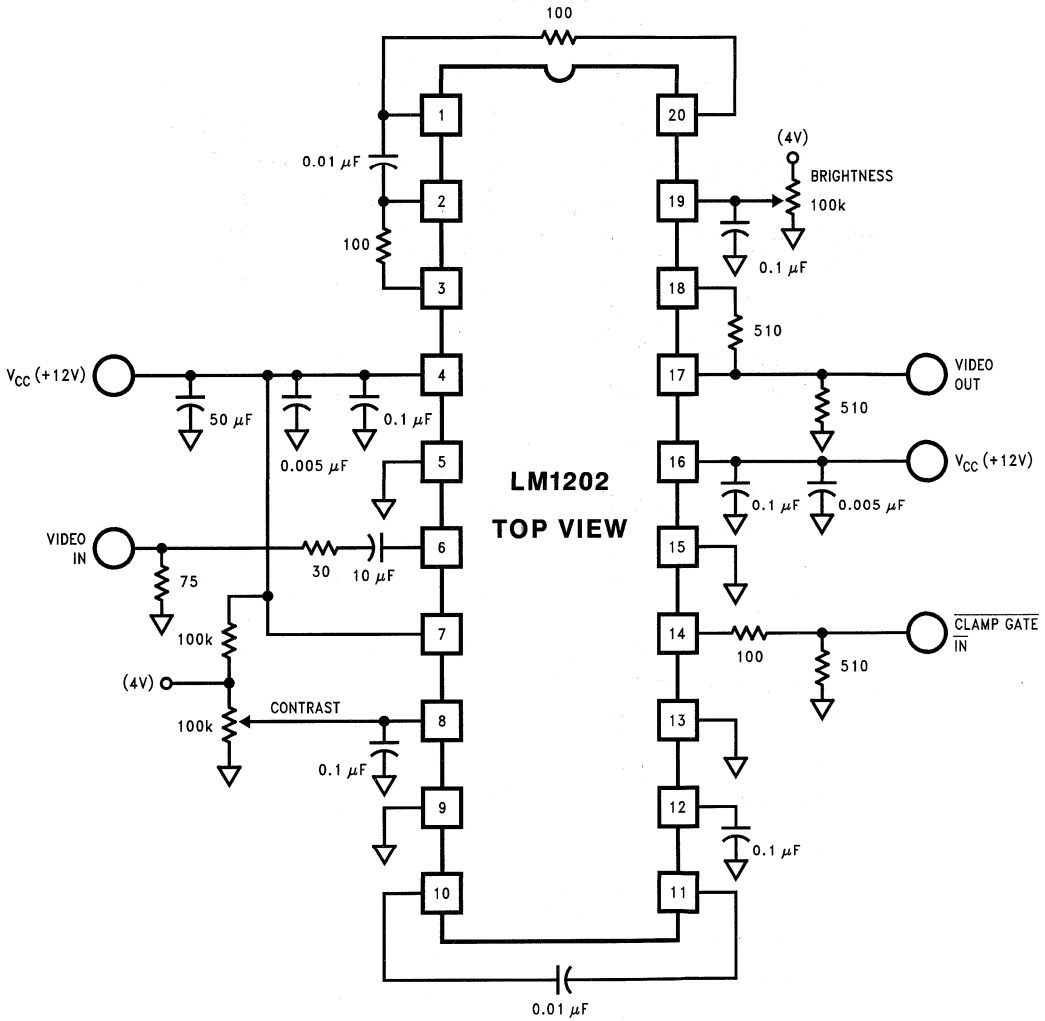

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FIGURE 9. Typical LM1202 Application (Single Video Channel)

Applications of the LM1202 (Continued)

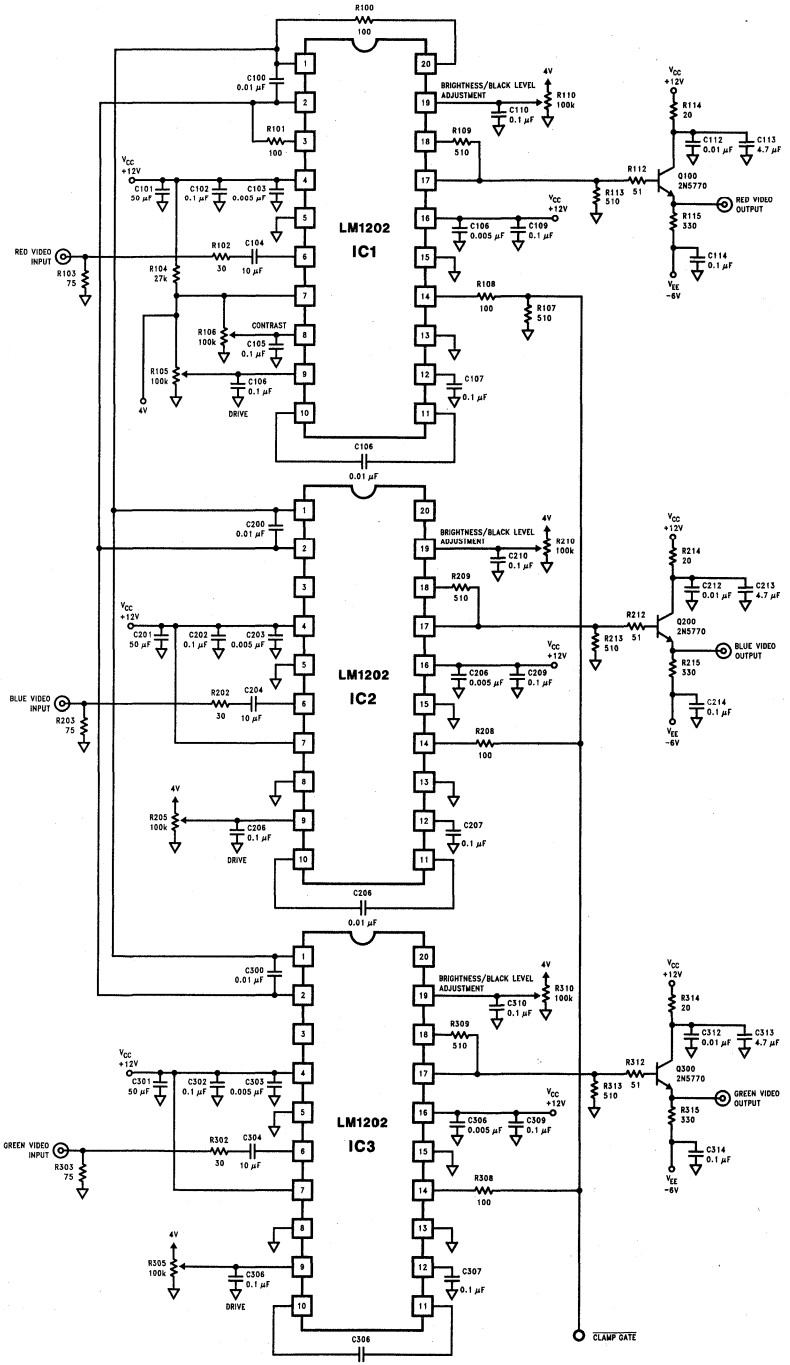

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FIGURE 10. Typical RGB Application with Contrast, Drive and Black Level (Cutoff) Control

Power Down Characteristics

The LM1202 includes a built-in power down spot killer to prevent a flash on the screen upon power down. The LM1202's output voltage decreases as the device is being powered down, thus preventing a flash on the screen. In some preamplifiers, the video output signal may go high as the device is being powered down. This may cause a whiter-than-white level at the output of the CRT driver, thus causing a flash on the screen.

PC Board Layout Considerations

For optimum performance and stable operation, a double-sided printed circuit board with adequate ground plane and power supply decoupling as close to the V_{CC} pins as possible is recommended. For suggestions on optimum PC board layout, please see the reference section below.

Reference

Ott, Henry W, *Noise Reduction Techniques in Electronic Systems*, John Wiley & Sons, New York, 1976.

National Semiconductor

LM1203 RGB Video Amplifier System

General Description

The LM1203 is a wideband video amplifier system intended for high resolution RGB color monitor applications. In addition to three matched video amplifiers, the LM1203 contains three gated differential input black level clamp comparators for brightness control and three matched attenuator circuits for contrast control. Each video amplifier contains a gain set or "Drive" node for setting maximum system gain (Av = 4 to 10) as well as providing trim capability. The LM1203 also contains a voltage reference for the video inputs. For high resolution monochrome monitor applications see the LM1201 Video Amplifier System datasheet.

Features

- Three wideband video amplifiers (70 MHz @ −3dB)
- Inherently matched (±0.1 dB or 1.2%) attenuators for contrast control
- Three externally gated comparators for brightness control
- Provisions for independent gain control (Drive) of each video amplifier
- Video input voltage reference
- Low impedance output driver

Block and Connection Diagram

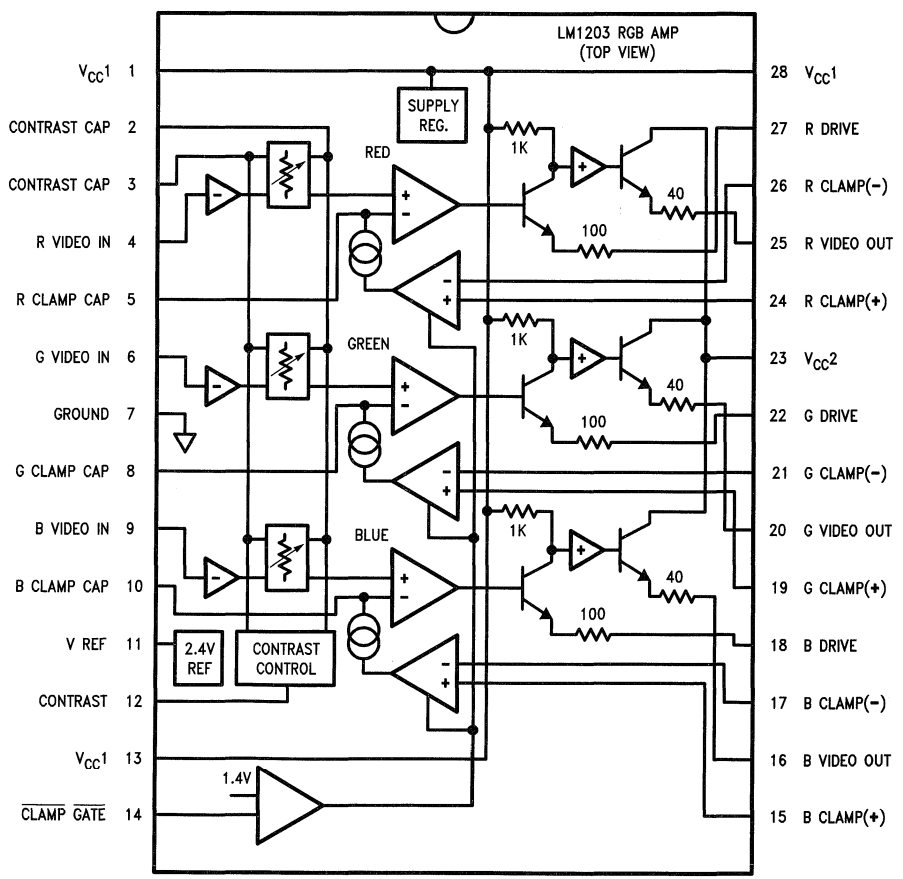

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FIGURE 1
Order Number LM1203N
See NS Package Number N28B

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage, V_{CC} Pins 1, 13, 23, 28 (Note 1) 13.5V

Voltage at Any Input Pin, V_{IN} $V_{CC} \geq V_{IN} \geq$ GND

Video Output Current, I16, 20 or 25 28 mA

Power Dissipation, P_D 2.5W

(Above 25°C) Derate Based on θ_{JA} and T_J

Thermal Resistance, θ_{JA} 50°C/W

Junction Temperature, T_J 150°C

Operating Temperature Range, T_A 0°C to +70°C

Storage Temperature Range, T_{STG} −65°C to +150°C

Lead Temperature, (Soldering, 10 sec.) 265°C

ESD susceptibility 1 kV

Human body model: 100 pF discharged through a 1.5 kΩ resistor

Electrical Characteristics

See Test Circuit *(Figure 2)*, T_A = 25°C; $V_{CC1} = V_{CC2}$ = 12V

DC Static Tests

S17, 21, 26 Open; V12 = 6V; V14 = 0V; V15 = 2.0V unless otherwise stated

Label	Parameter	Conditions	Typ	Tested Limit (Note 2)	Design Limit (Note 3)	Units (Limits)
Is	Supply Current	V_{CC} 1 only	73	90.0		mA(max)
V11	Video Input Reference Voltage		2.4	2.2		V(min)
				2.6		V(max)
Ib	Video Input Bias Current	Any One Amplifier	5.0	20		μA(max)
V14 l	Clamp Gate Low Input Voltage	Clamp Comparators On	1.2	0.8		V(max)
V14 h	Clamp Gate High Input Voltage	Clamp Comparators Off	1.6	2.0		V(min)
I14 l	Clamp Gate Low Input Current	V14 = 0V	−0.5	−5.0		μA(max)
I14 h	Clamp Gate High Input Current	V14 = 12V	0.005	1		μA(max)
Iclamp+	Clamp Cap Charge Current	V5, 8 or 10 = 0V	850	500		μA(min)
Iclamp−	Clamp Cap Discharge Current	V5, 8 or 10 = 5V	−850	−500		μA(min)
Vol	Video Output Low Voltage	V5, 8 or 10 = 0V	0.9	1.25		V(max)
Voh	Video Output High Voltage	V5, 8 or 10 = 5V	8.9	8.2		V(min)
ΔVo(2V)	Video Output Offset Voltage	Between Any Two Amplifiers V15 = 2V	±0.5	±50		mV(max)
ΔVo(4V)	Video Output Offset Voltage	Between Any Two Amplifiers V15 = 4V	±0.5	±50		mV(max)

AC Dynamic Tests

S17, 21, 26 Closed; V14 = 0V; V15 = 4V; unless otherwise stated

Symbol	Parameter	Conditions	Typ	Tested Limit (Note 2)	Design Limit (Note 3)	Units (Limits)
Av max	Video Amplifier Gain	V12 = 12V, V_{IN} = 560 mVp-p	6.0	4.5		V/V(min)
ΔAv 5V	Attenuation @ 5V	Ref: Av max, V12 = 5V	−10			dB
ΔAv 2V	Attenuation @ 2V	Ref: Av max, V12 = 2V	−40			dB
Av match	Absolute gain match @ Av max	V12 = 12V (Note 5)	±0.5			dB
ΔAv track1	Gain change between amplifiers	V12 = 5V (Notes 5, 8)	±0.1		±0.5	dB(max)
ΔAv track2	Gain change between amplifiers	V12 = 2V (Notes 5, 8)	±0.3		±0.7	dB(max)
THD	Video Amplifier Distortion	V12 = 3V, V_O = 1 Vp-p	0.5			%
f (−3 dB)	Video Amplifier Bandwidth (Notes 4, 6)	V12 = 12V, V_O = 100 mV_{rms}	70			MHz
t_r	Output Rise Time (Note 4)	V_O = 4 Vp-p	5			ns
t_f	Output Fall Time (Note 4)	V_O = 4 Vp-p	7			ns

AC Dynamic Tests S17, 21, 26 Closed; V14 = 0V; V15 = 4V; unless otherwise stated (Continued)

Symbol	Parameter	Conditions	Typ	Tested Limit (Note 2)	Design Limit (Note 3)	Units
Vsep 10 kHz	Video Amplifier 10 kHz Isolation	V12 = 12V (Note 7)	−65			dB
Vsep 10 MHz	Video Amplifier 10 MHz Isolation	V12 = 12V (Notes 4, 7)	−46			dB

Note 1: V_{CC} supply pins 1, 13, 23, 28 must be externally wired together to prevent internal damage during V_{CC} power on/off cycles.

Note 2: These parameters are guaranteed and 100% production tested.

Note 3: Design limits are guaranteed (but not 100% production tested). These limits are not used to calculate outgoing quality levels.

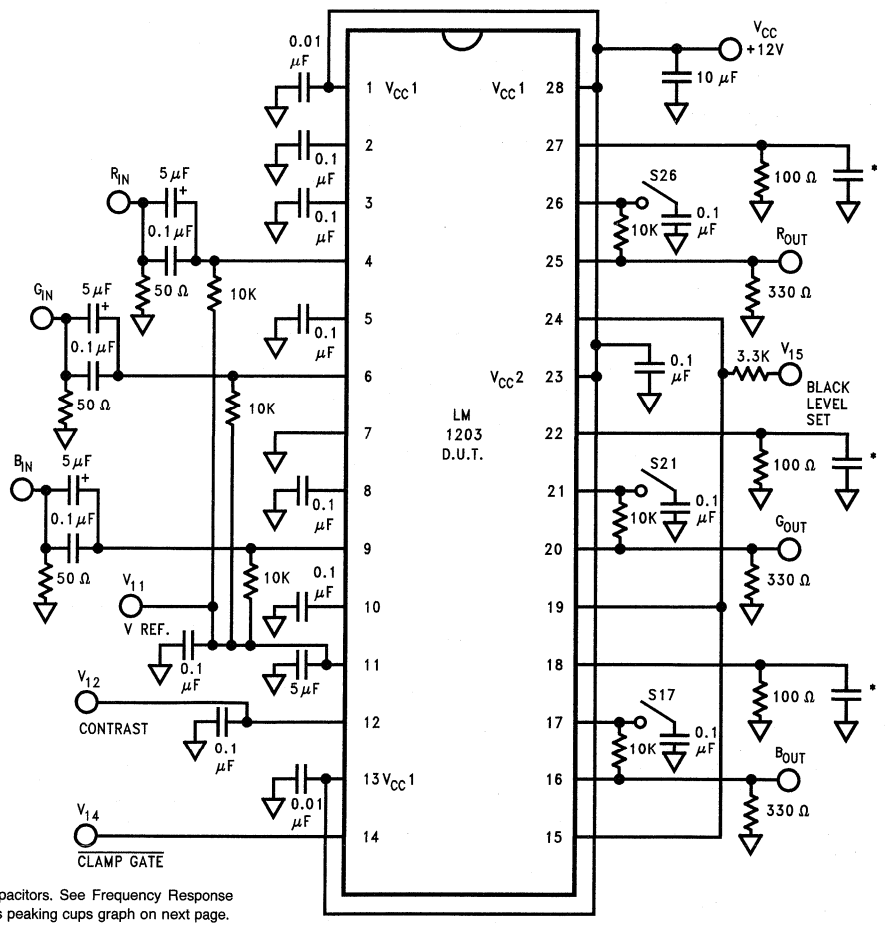
Note 4: When measuring video amplifier bandwidth or pulse rise and fall times, a double sided full ground plane printed circuit board without socket is recommended. Video Amplifier 10 MHz isolation test also requires this printed circuit board.

Note 5: Measure gain difference between any two amplifiers. V_{IN} = 1 Vp-p.

Note 6: Adjust input frequency from 10 kHz (Av_{max} ref level) to the −3 dB corner frequency (f −3 dB).

Note 7: Measure output levels of the other two undriven amplifiers relative to driven amplifier to determine channel separation. Terminate the undriven amplifier inputs to simulate generator loading. Repeat test at f_{IN} = 10 MHz for Vsep = 10 MHz.

Note 8: ΔAv track is a measure of the ability of any two amplifiers to track each other and quantifies the matching of the three attenuators. It is the difference in gain change between any two amplifiers with the Contrast Voltage V12 at either 5V or 2V measured relative to an Av max condition V12 = 12V. For example, at Av max the three amplifiers gains might be 17.4 dB, 16.9 dB, and 16.4 dB and change to 7.3 dB, 6.9 dB, and 6.5 dB respectively for V12 = 5V. This yields the measured typical ±0.1 dB channel tracking.



*Peaking capacitors. See Frequency Response using various peaking cups graph on next page.

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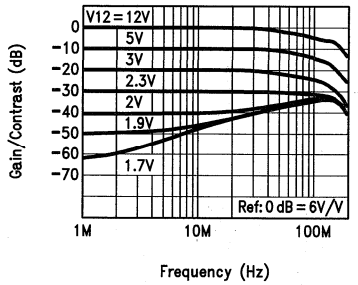
FIGURE 2. LM1203 Test Circuit

Typical Performance Characteristics

Contrast vs Frequency



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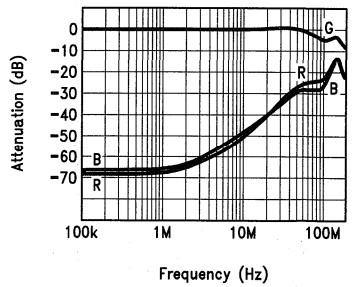
Crosstalk vs Frequency



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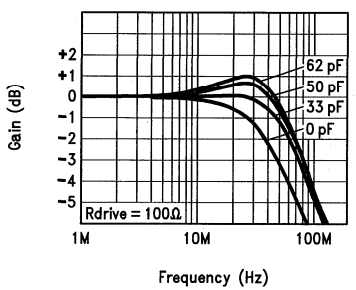
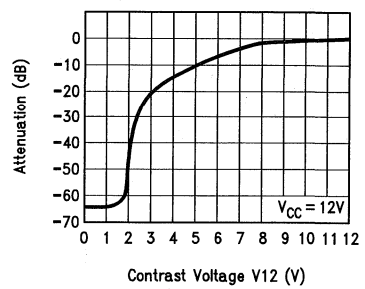
Frequency Response Using Various Peaking Caps



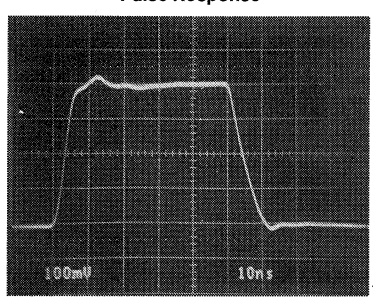
TL/H/9178–13

Attenuation vs Contrast Voltage



TL/H/9178–14

Pulse Response



Rise & Fall Times
Vert. = 1V/Div.
Horiz. = 10 ns/Div.

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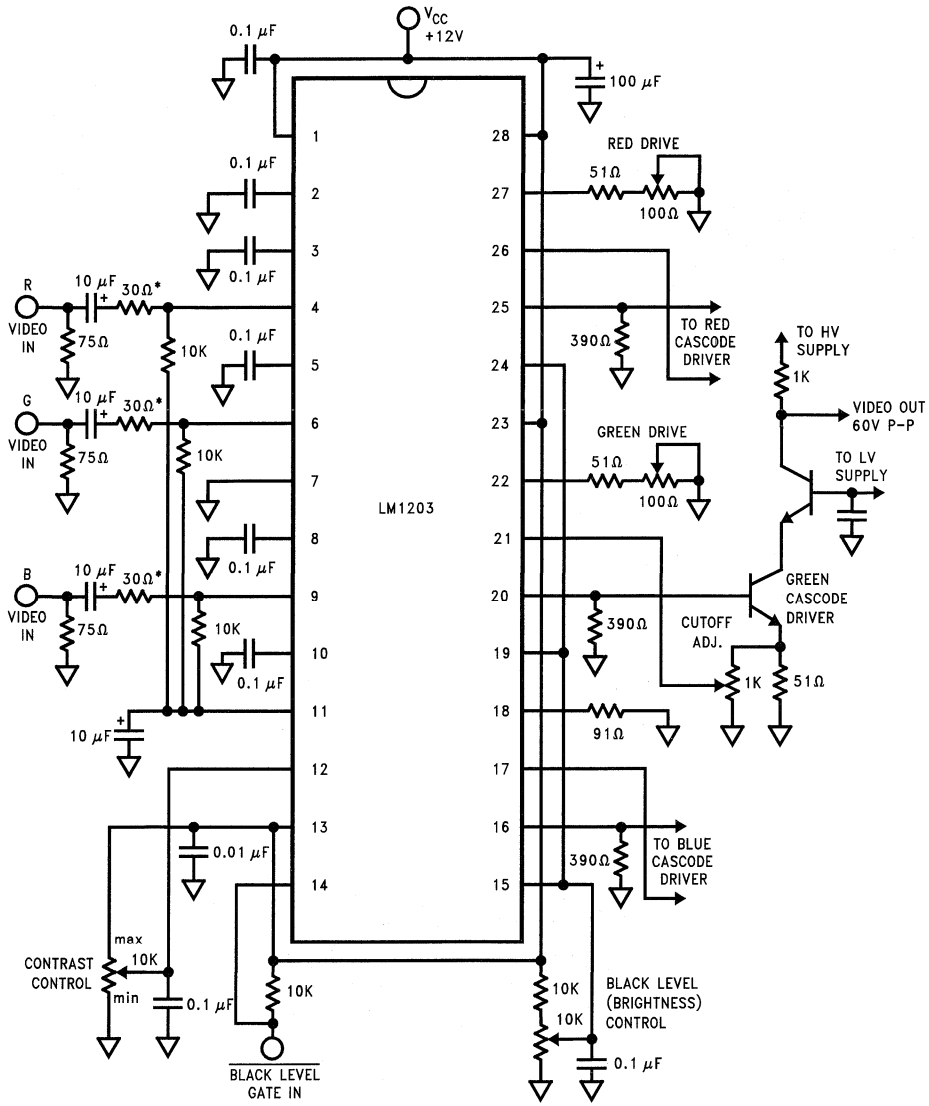

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FIGURE 3. LM1203 Typical Application

* 30Ω resistors are added to the input pins for protection against current surges coming through the 10 μF input capacitors. By increasing these resistors to well over 100Ω the rise and fall times of the LM1203 can be increased for EMI considerations.

Applications Information

Figure 4 shows the block diagram of a typical analog RGB color monitor. The RGB monitor is used with CAD/CAM work stations, PC's, arcade games and in a wide range of other applications that benefit from the use of color display terminals. The RGB color monitor characteristics may differ in such ways as sweep rates, screen size, CRT color trio spacing (dot pitch), or in video amplifier bandwidths but will still be generally configured as shown in *Figure 4*. Separate horizontal and vertical sync signals may be required or they may be contained in the green video input signal. The video input signals are usually supplied by coax cable which is terminated in 75Ω at the monitor input and internally ac coupled to the video amplifiers. These input signals are approximately 1 volt peak to peak in amplitude and at the input of the high voltage video section, approximately 6V peak to peak. At the cathode of the CRT the video signals can be as high as 60V peak to peak. One important requirement of the three video amplifiers is that they match and track each other over the contrast and brightness control range. The *Figure 4* block labeled "VIDEO AMPLIFICATION WITH GAIN AND DC CONTROL" describes the function of the LM1203 which contains the three matched video amplifiers, contrast control and brightness control.

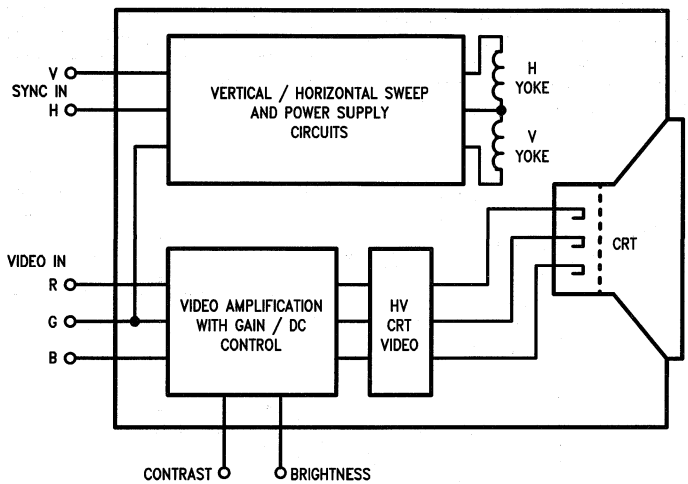

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FIGURE 4. Typical RGB Color Monitor Block Diagram

Circuit Description

Figure 5 is a block diagram of one of the video amplifiers along with the contrast and brightness controls. The contrast control is a dc-operated attenuator which varies the ac gain of all three amplifiers simultaneously while not introducing any signal distortions or tracking errors. The brightness control function requires a "sample and hold" circuit (black level clamp) which holds the dc bias of the video amplifiers and CRT cathodes constant during the black level reference portion of the video waveform. The clamp comparator, when gated on during this reference period, will charge or discharge the clamp capacitor until the plus input of the clamp comparator matches that of the minus input voltage which was set by the brightness control.

Figure 6 is a simplified schematic of one of the three video amplifiers along with the recommended external components. The IC pin numbers are circled with all external components shown outside of the dashed line. The video input is applied to pin 6 via the 10 μF coupling capacitor. DC bias to the video input is through the 10 kΩ resistor which is connected to the 2.4V reference at pin 11. The low frequency roll-off of the amplifier is set by these two components. Transistor Q1 buffers the video signal to the base of Q2. The Q2 collector current is then directed to the V_{CC} 1 supply directly or through the 1k load resistor depending upon the differential DC voltage at the bases of Q3 and Q4. The Q3 and Q4 differential base voltage is determined by the contrast control circuit which is described below. RF decoupling capacitors are required at pins 2 and 3 to insure high frequency isolation between the three video amplifiers which share these common connections. The black level dc voltage at the collector of Q4 is maintained by Q5 and Q6 which are part of the black level clamp circuit also described below. The video signal appearing at the collector of Q4 is then buffered by Q7 and level shifted down by Z1 and Q8 to the base of Q9 which will then provide additional system gain.

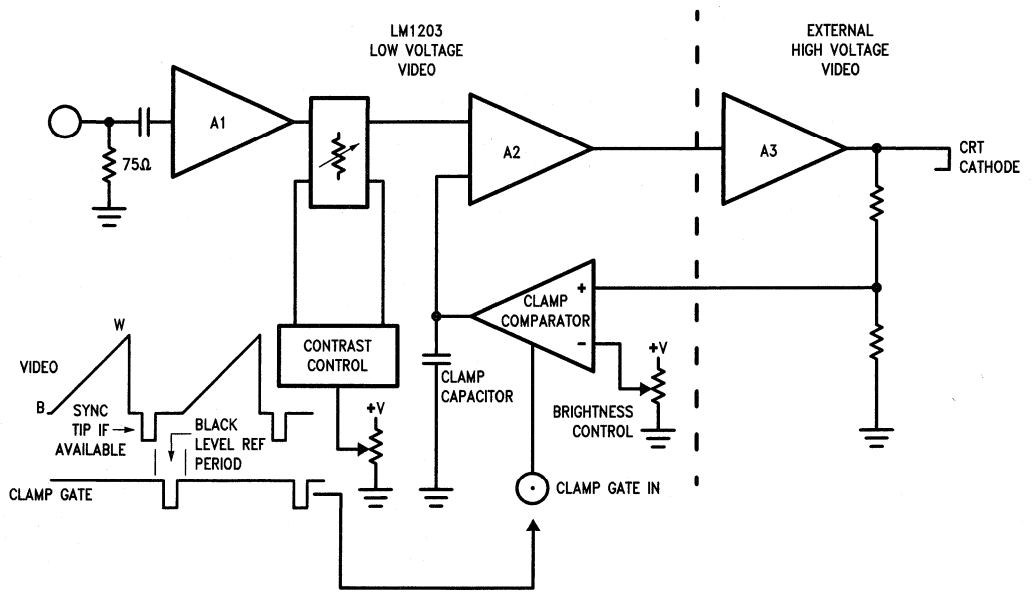

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FIGURE 5. Block Diagram of LM1203 Video Amplifier with Contrast and Black Level Control

Circuit Description (Continued)

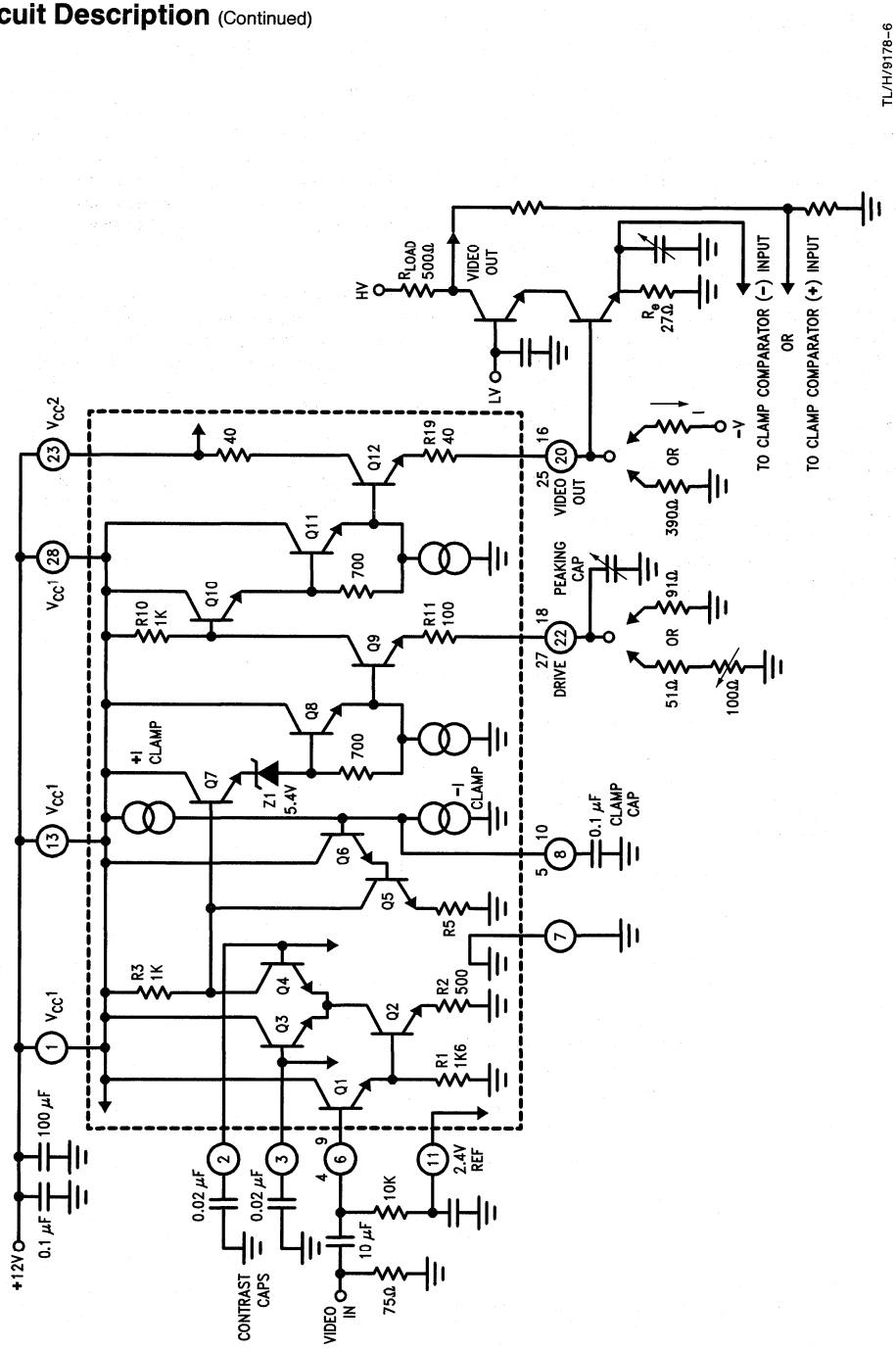

FIGURE 6. Simplified LM1203 Video Amplifier Section with Recommended External Components

Circuit Description (Continued)

The "Drive" pin will allow the user to trim the Q9 gain of each amplifier to correct for differences in the CRT and high voltage cathode driver gain stages. A small capacitor (33 pF) at this pin will extend the high frequency gain of the video amplifier by compensating for some of the internal high frequency roll off. To use this capacitor and still provide variable gain adjustment, the 51Ω and series 100Ω pot should be used with the red and green drive pins. The 91Ω resistor used with the blue drive pin will set the system gain to approximately 6.2 and allow adjustment of the red and green gains to 6.2 plus or minus 25%. The video signal at the collector of Q9 is buffered and level shifted down by Q10 and Q11 to the base of the output emitter follower Q12. Between the emitter of Q12 and the video output pin is a 40Ω resistor which was included to prevent spurious oscillations when driving capacitive loads. An external emitter resistor must be added between the video output pin and ground. The value of this resistor should not be less than 390Ω or package power limitations may be exceeded when worst case (high supply, max supply current, max temp) calculations are made. If negative going pulse slewing is a problem because of high capacitive loads (>10 pF), a more efficient method of emitter pull down would be to connect a suitable resistor to a negative supply voltage. This has the effect of a current source pull down when the minus supply voltage is −12V and the emitter current is approximately 10 mA. The system gain will also increase slightly because less signal will be lost across the internal 40Ω resistor. Precautions must be taken to prevent the video output pin from going below ground because IC substrate currents may cause erratic operation. The collector currents from the video output transistors are returned to the power supply at V_{CC} 2 pin 23. When making power dissipation calculations note that the data sheet specifies only the V_{CC} 1 supply current at 12V. The IC power dissipation contribution of V_{CC} 2 is dependent upon the video output emitter pull down load.

In applications that require video amplifier shut down because of fault conditions detected by monitor protection circuits, pin 11 and the wiper arms of the contrast and brightness controls can be grounded without harming the IC. This assumes some series resistance between the top of the control pots and V_{CC}.

Figure 7 shows the internal construction of the pin 11 2.4V reference circuit which is used to provide temperature and supply voltage tracking compensation for the video amplifier inputs. The value of the external DC biasing resistors should not be larger than 10 kΩ because minor differences in input bias currents to the individual video amplifiers may cause offsets in gain.

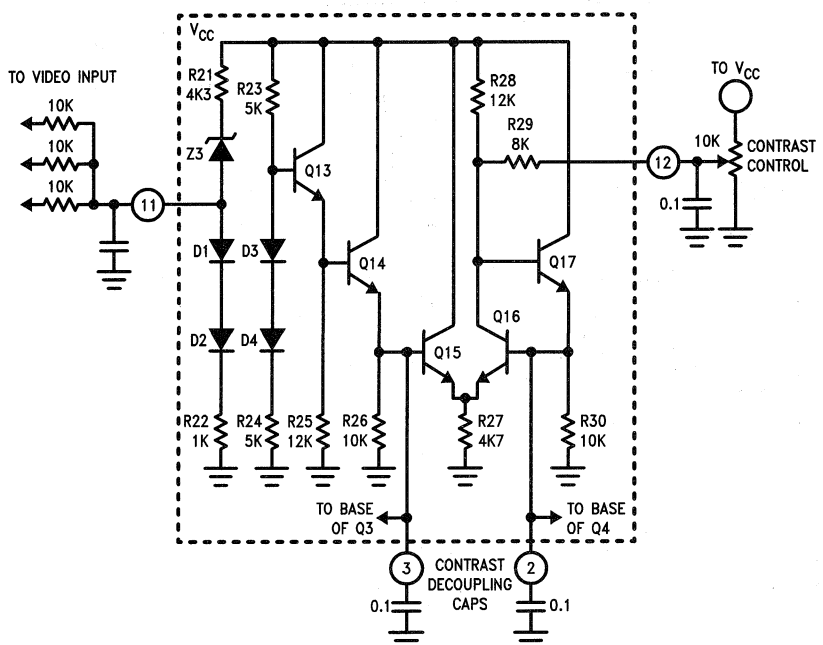

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FIGURE 7. LM1203 Video Input Voltage Reference and Contrast Control Circuits

Circuit Description (Continued)

Figure 7 also shows how the contrast control circuit is configured. Resistors R23, 24, diodes D3, 4 and transistor Q13 are used to establish a low impedance zero TC half supply voltage reference at the base of Q14. The differential amplifier formed by Q15, 16 and feedback transistor Q17 along with resistors R27, 28 establish a diferential base voltage for Q3 and Q4 in *Figure 6*. When externally adding or subtracting current from the collector of Q16, a new differential voltage is generated that reflects the change in the ratio of currents in Q15 and Q16. To provide voltage control of the Q16 current, resistor R29 is added between the Q16 collector and pin 12. A capacitor should be added from pin 12 to ground to prevent noise from the contrast control pot from entering the IC.

Figure 8 is a simplified schematic of the clamp gate and clamp comparator sections of the LM1203. The clamp gate circuit consists of a PNP input buffer transistor (Q18), a PNP emitter coupled pair referenced on one side to 2.1V (Q19, 20) and an output switch (Q21). When the clamp gate input at pin 14 is high (>1.5V) the Q21 switch is on and shunts the I1 850 μA current to ground. When pin 14 is low (<1.3V) the Q21 switch is off and the I1 850 μA current source is mirrored or "turned around" by reference diode D5 and Q26 to provide a 850 μA current source for the clamp comparator(s). The inputs to the comparator are similar to the clamp gate input except that an NPN emitter coupled pair is used to control the current which will charge or discharge the clamp capacitors at pins 5, 8, or 10. PNP transistors are used at the inputs because they offer a number of advantages over NPNs. PNPs will operate with base voltages at or near ground and will usually have a greater reverse emitter base breakdown voltage (BVebo). Because the differential input voltage to the clamp comparator during the video scan period could be greater than the BVebo of NPN transistors a resistor (R34) with a value one half that of R33 or R35 is connected between the bases of Q23 and Q27. This resistor will limit the maximum differential input to Q24, 25 to approximately 350 mV. The clamp comparator common mode range is from ground to approximately 9V and the maximum differential input voltage is V_{CC} and ground.

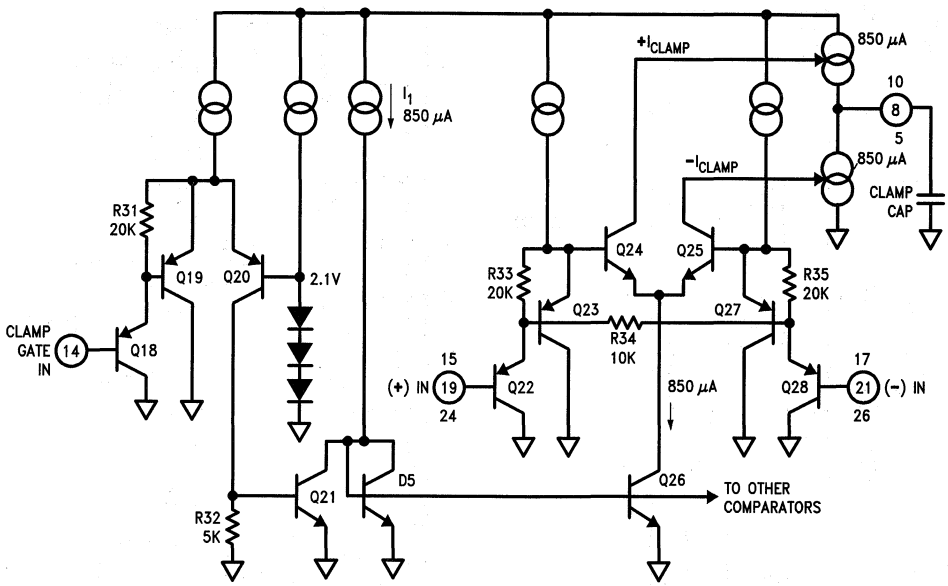

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FIGURE 8. Simplified Schematic of LM1203 Clamp Gate and Clamp Comparator Circuits

Additional Applications of the LM1203

Figure 9 shows how the LM1203 can be set up as a video buffer which could be used in low cost video switcher applications. Pin 14 is tied high to turn off the clamp comparators. The comparator input pins should be grounded as shown. Sync tip (black level if sync is not included) clamping is provided by diodes at the amplifier inputs. Note that the clamp cap pins are tied to the Pin 11 2.4V reference. This was done, along with the choice of 200Ω for the drive pin resistor, to establish an optimum DC output voltage. The contrast control (Pin 12) will provide the necessary gain or attenuation required for channel balancing. Changing the contrast control setting will cause minor DC shifts at the amplifier output which will not be objectionable as the output is AC coupled to the load. The dual NPN/PNP emitter follower will provide a low impedance output drive to the AC coupled 75Ω output impedance setting resistor. The dual 500 μF capacitors will set the low frequency response to approximately 4 Hz.

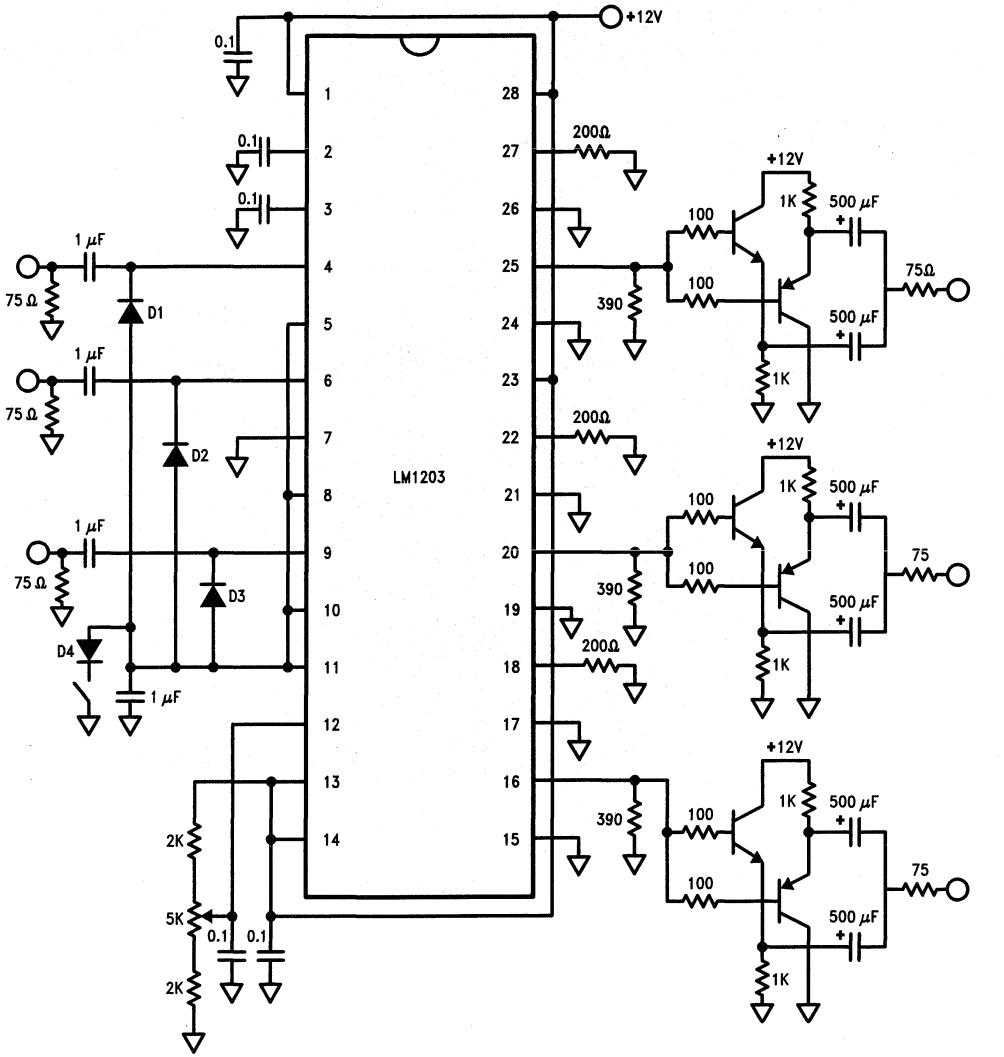

FIGURE 9. RGB Video Buffer with Diode Sync Tip Clamps and 75Ω Cable Driver

Additional Applications of the LM1203 (Continued)

When diode D4 at Pin 11 is switched to ground the input video signals will be DC shifted down and clamped at a voltage near ground (approximately 250 mV). This will disable the video amplifiers and force the output DC level low. The DC outputs from other similarly configured LM1203s could overide this lower DC level and provide the output signals to the 75Ω cable drivers. In this case any additional LM1203s would share the same 390Ω output resistor. The maximum DC plus peak white output voltage should not be allowed to exceed 7V because the "off" amplifier output stage could suffer internal zener damage. See *Figure 3* and text for a description of the internal configuration of the video amplifier.

Figure 10 shows the configuration for a three channel high frequency amplifier with non gated DC feedback. Pin 14 is tied low to turn on the clamp comparators (feedback amplifiers). The inverting inputs (Pins 17, 21, 26) are connected to the amplifier outputs from a low pass filter. Additional low frequency filtering is provided by the clamp caps. The drive resistors can be made variable or fixed at values between 0 and 300Ω. Maximum output swings are achieved when the DC output is set to approximately 4V. The high frequency response will be dependent upon external peaking at the drive pins.

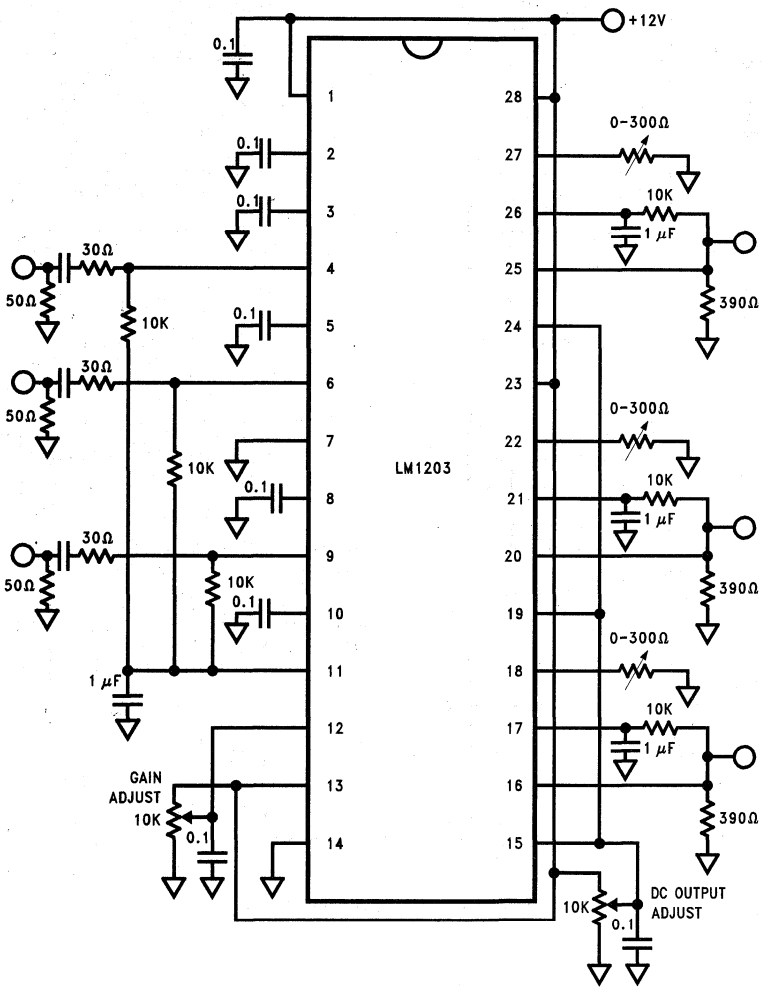

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FIGURE 10. Three Channel High Frequency Amplifier with Non-gated DC Feedback (Non-video Applications)

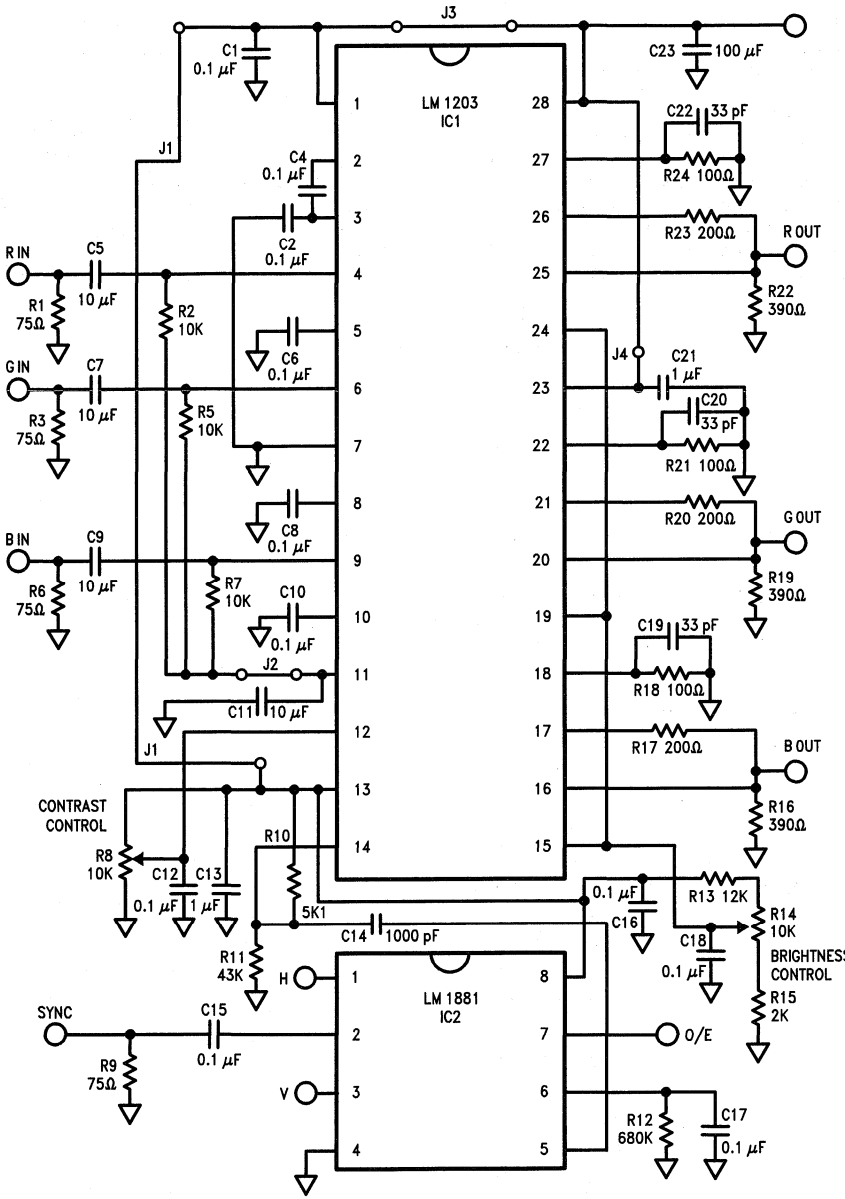

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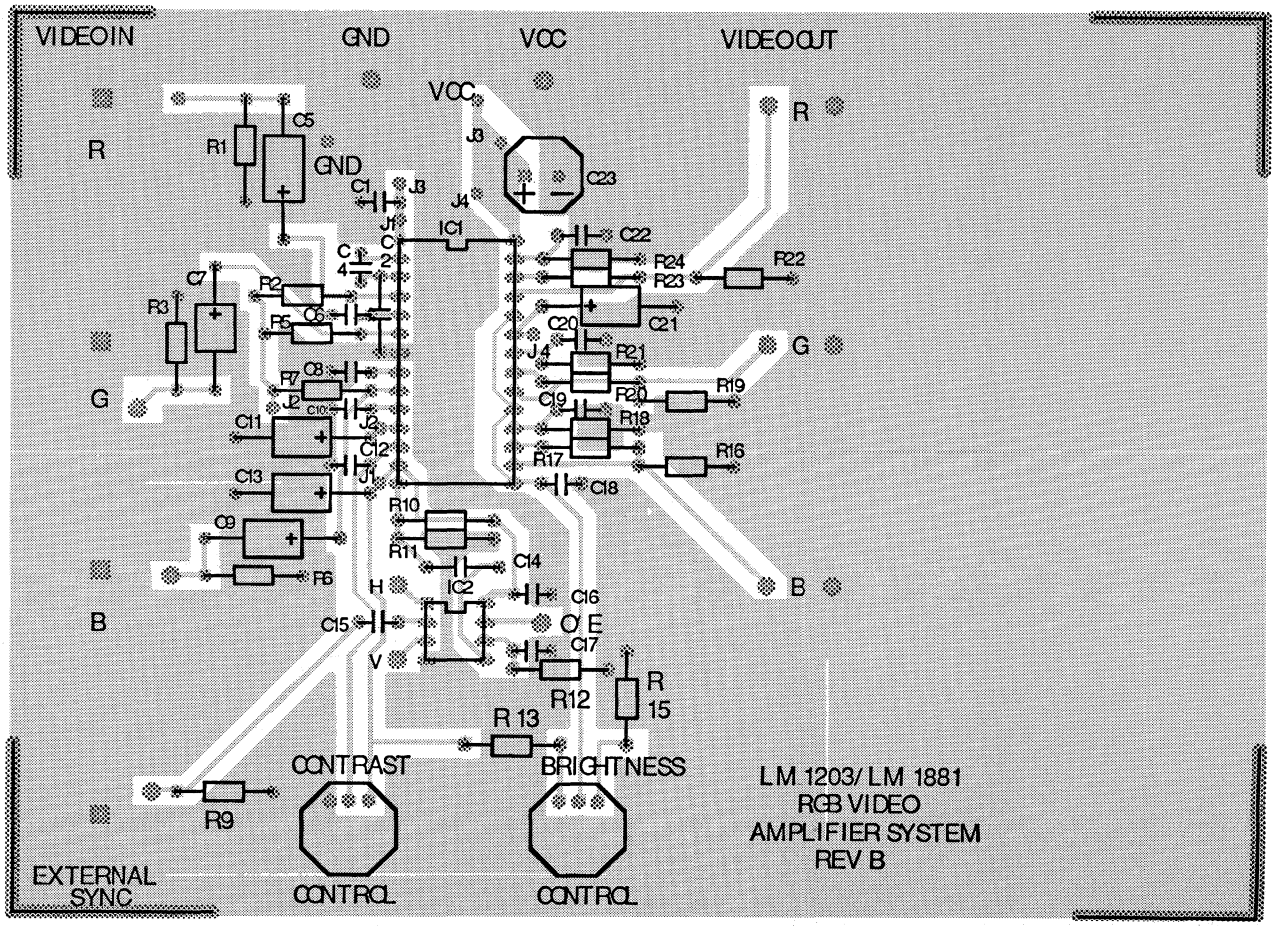
FIGURE 11. LM1203/LM1881 Application Circuit for PC Board

PC Board with Components



TL/H/9178–17

National Semiconductor

LM1203A
150 MHz RGB Video Amplifier System

General Description

The LM1203A is an improved version of the popular LM1203 wideband video amplifier system. The device is intended for high resolution RGB CRT monitors. In addition to three matched video amplifiers, the LM1203A contains three gated differential input black level clamp comparators for brightness control and three matched attenuator circuits for contrast control. Each video amplifier contains a gain set or "Drive" node for setting maximum system gain or providing gain trim capability for white balance. The LM1203A also contains a voltage reference for the video inputs. The LM1203A is pin and function compatible with the LM1203.

Features

- Three wideband video amplifiers 150 MHz @ −3 dB
- Matched (±0.1 dB or 1.2%) attenuators for contrast control
- Three externally gated comparators for brightness control
- Provisions for individual gain control (Drive) of each video amplifier
- Video input voltage reference
- Low impedance output driver

Improvements over LM1203

- 150 MHz vs 70 MHz bandwidth
- V_{OUT} low: 0.15V vs 0.9V
- t_r, t_f: 4 ns vs 7 ns
- Built in power down spot killer

Applications

- High resolution RGB CRT monitors
- Video AGC amplifiers
- Wideband amplifiers with gain and DC offset controls

Block and Connection Diagrams

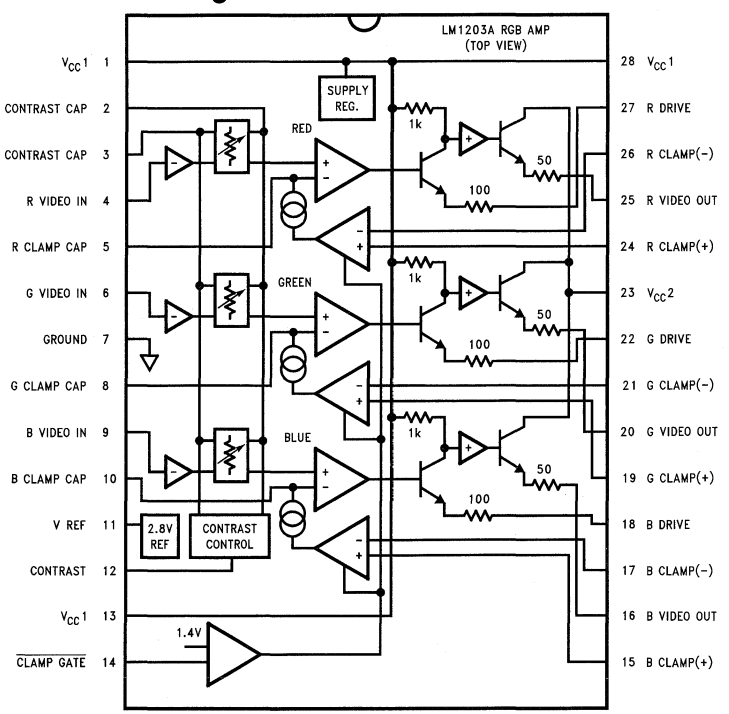


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FIGURE 1

Order Number LM1203AN
See NS Package Number N28B

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})
Pins 1, 13, 23, 28 (Note 3) 13.5V

Peak Video Output Source Current
(Any One Amp) Pins 16, 20 or 25 28 mA

Voltage at Any Input Pin (V_{IN}) $V_{CC} \geq V_{IN} \geq$ GND

Power Dissipation, (P_D) (Above 25°C derate based on θ_{JA} and T_J) 2.5W

Thermal Resistance (θ_{JA}) 50°C/W

Junction Temperature (T_J) 150°C

ESD Susceptibility (Note 4) 2 kV

Storage Temperature −65°C to 150°C

Lead Temperature (Soldering, 10 sec.) 265°C

Operating Ratings (Note 2)

Temperature Range −20°C to +80°C

Supply Voltage (V_{CC}) 10.8V ≤ V_{CC} ≤ 13.2V

DC Electrical Characteristics

See Test Circuit *(Figure 2)*, T_A = 25°C; V_{CC1} = V_{CC2} = 12V. S17, 21, 26 Open; V12 = 6V; V14 = 0V; V15 = 2.0V unless otherwise stated.

Symbol	Parameter	Conditions	Typical (Note 5)	Limit (Note 6)	Units
I_S	Supply Current	V_{CC1} + V_{CC2}, R_L = ∞ (Note 7)	70	95	mA (max)
V11	Video Input Reference Voltage		2.8	2.5	V (min)
				3.1	V (max)
I_B	Video Input Bias Current	Any One Amplifier	7	20	μA (max)
V_{14L}	Clamp Gate Low Input Voltage	Clamp Comparators On	1.2	0.8	V (max)
V_{14H}	Clamp Gate High Input Voltage	Clamp Comparators Off	1.6	2.0	V (min)
I_{14L}	Clamp Gate Low Input Current	V14 = 0V	−1	−5.0	μA (max)
I_{14H}	Clamp Gate High Input Current	V14 = 12V	0.07	0.2	μA (max)
I_{CLAMP+}	Clamp Cap Charge Current	V5, 8 or 10 = 0V	750	500	μA (min)
I_{CLAMP-}	Clamp Cap Discharge Current	V5, 8 or 10 = 5V	−750	−500	μA (min)
V_{OL}	Video Output Low Voltage	V5, 8 or 10 = 0V	0.15	0.5	V (max)
V_{OH}	Video Output High Voltage	V5, 8 or 10 = 5V	7.5	7	V (min)
$\Delta V_{O(2V)}$	Video Output Offset Voltage	Between Any Two Amplifiers, V15 = 2V	2	±25	mV (max)
$\Delta V_{O(4V)}$	Video Output Offset Voltage	Between Any Two Amplifiers, V15 = 4V	2	±25	mV (max)

AC Electrical Characteristics

See Test Circuit *(Figure 2)*, $T_A = 25°C$; $V_{CC1} = V_{CC2} = 12V$. S17, 21, 26 Closed; V14 = 0V; V15 = 4V unless otherwise stated.

Symbol	Parameter	Conditions	Typical (Note 5)	Limit (Note 6)	Units
$A_{V\ max}$	Video Amplifier Gain	V12 = 12V, V_{IN} = 560 mV_{PP}	6.5	4.5	V/V (min)
$\Delta A_{V\ 5V}$	Attenuation @ 5V	Ref: A_V max, V12 = 5V	−8		dB
$\Delta A_{V\ 2V}$	Attenuation @ 2V	Ref: A_V max, V12 = 2V	−30		dB
$A_{V\ match}$	Absolute Gain Match @ A_V max	V12 = 12V (Note 8)	±0.3		dB
$\Delta A_{V\ track\ 1}$	Gain Change Between Amplifiers	V12 = 5V (Notes 8, 9)	±0.1		dB
$\Delta A_{V\ track\ 2}$	Gain Change Between Amplifiers	V12 = 5V (Notes 8, 9)	±0.3		dB
THD	Video Amplifier Distortion	V12 = 3V, V_O = 1 V_{PP}	1		%
f (−3 dB)	Video Amplifier Bandwidth (Notes 10, 11)	V12 = 12V, V_O = 4 V_{PP} (No External Peaking Capacitor)	100		MHz
f (−3 dB)	Video Amplifier Bandwidth (Notes 10, 11)	V12 = 12V, V_O = 4 V_{PP} With 18 pF Peaking Cap from Pins 18, 22 and 27 to GND	150		MHz
t_r	Output Rise Time (Note 10)	V_O = 4 V_{PP} (No External Peaking Capacitor)	3		ns
t_f	Output Fall Time (Note 10)	V_O = 4 V_{PP} (No External Peaking Capacitor)	4		ns
$V_{sep\ 10\ kHz}$	Video Amplifier 10 kHz Isolation	V12 = 12V (Note 12)	−70		dB
$V_{sep\ 10\ MHz}$	Video Amplifier 10 MHz Isolation	V12 = 12V (Notes 10, 12)	−50		dB

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur.

Note 2: Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

Note 3: V_{CC} supply pins 1, 13, 23, 28 must be externally wired together to prevent internal damage during V_{CC} power on/off cycles.

Note 4: Human body model, 100 pF discharged through a 1.5 kΩ resistor.

Note 5: Typical specifications are specified at +25°C and represent the most likely parametric norm.

Note 6: Tested limits are guaranteed to National's AOQL (Average Outgoing Quality Level).

Note 7: The supply current specified is the quiescent current for V_{CC1} and V_{CC2} with $R_L = \infty$, see *Figure 2's* test circuit. The supply current for V_{CC2} (pin 23) also depends on the output load. With video output at 2V DC, the additional current through V_{CC2} is 18 mA for *Figure 2's* test circuit.

Note 8: Measure gain difference between any two amplifiers. V_{IN} = 1 V_{PP}.

Note 9: $\Delta A_{V\ track}$ is a measure of the ability of any two amplifiers to track each other and quantifies the matching of the three attenuators. It is the difference in gain change between any two amplifiers with the contrast voltage (V12) at either 5V or 2V measured relative to an A_V max condition, V12 = 12V. For example, at A_V max the three amplifiers' gains might be 17.4 dB, 16.9 dB and 16.4 dB and change to 7.3 dB, 6.9 dB, and 6.5 dB respectively for V12 = 5V. This yields the measured typical ±0.1 dB channel tracking.

Note 10: When measuring video amplifier bandwidth or pulse rise and fall times, a double sided full ground plane printed circuit board without socket is recommended. Video amplifier 10 MHz isolation test also requires this printed circuit board.

Note 11: Adjust input frequency from 10 kHz (A_V max reference level) to the −3 dB corner frequency ($f_{-3\ dB}$).

Note 12: Measure output levels of the other two undriven amplifiers relative to the driven amplifier to determine channel separation. Terminate the undriven amplifier inputs to simulate generator loading. Repeat test at f_{IN} = 10 MHz for V_{sep} = 10 MHz.

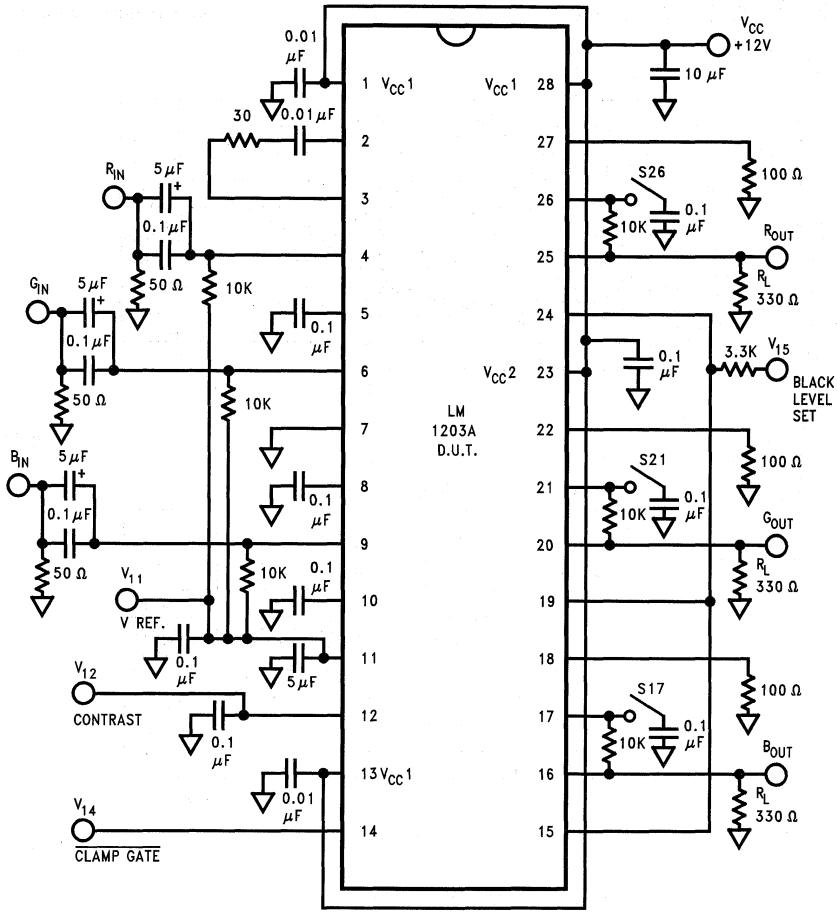

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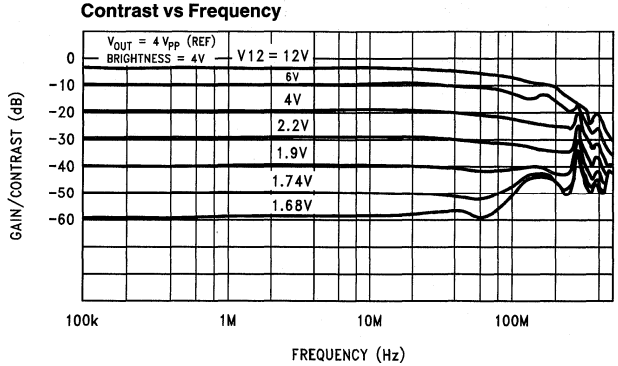
FIGURE 2. LM1203A Test Circuit

Typical Performance Characteristics V_{CC} = 12V, T_A = 25°C unless otherwise specified

Contrast vs Frequency



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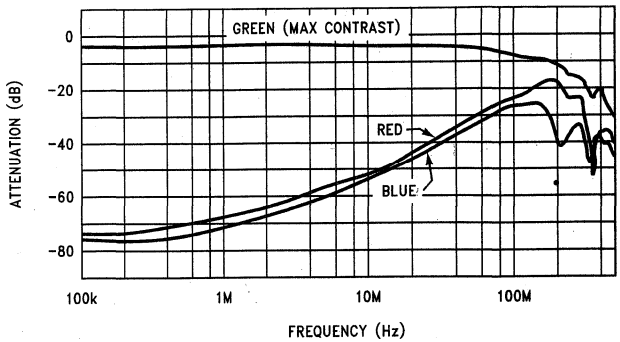
Typical Performance Characteristics V_{CC} = 12V, T_A = 25°C unless otherwise specified (Continued)

Crosstalk vs Frequency



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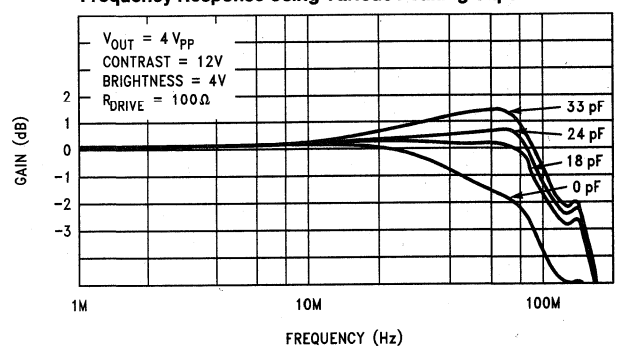
Frequency Response Using Various Peaking Caps



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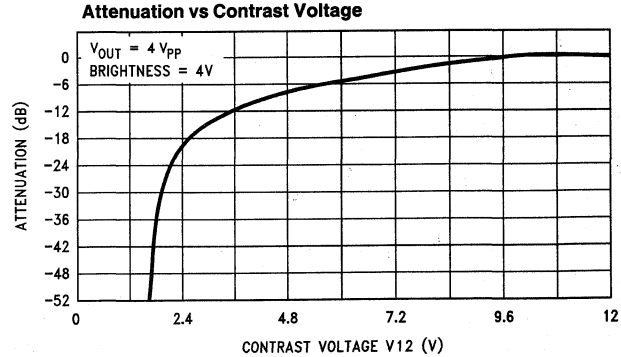
Attenuation vs Contrast Voltage



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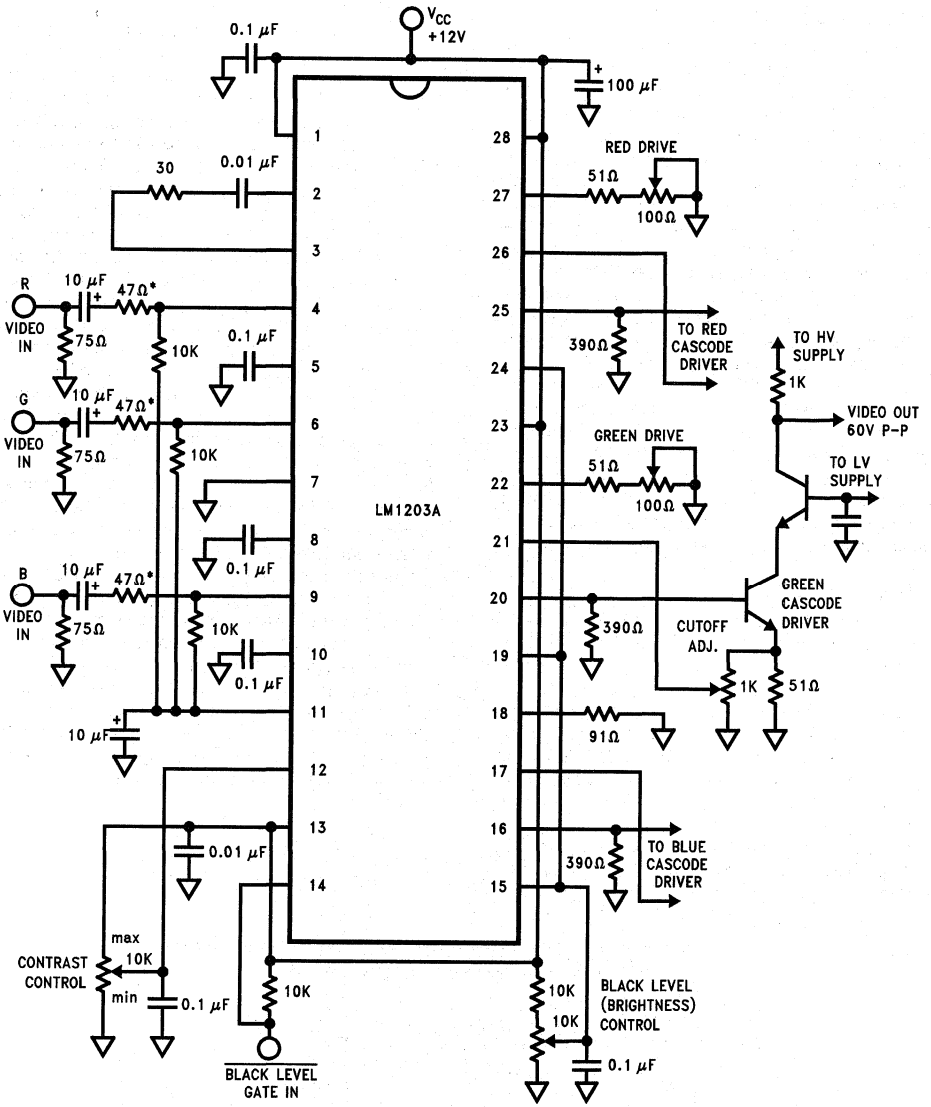

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*47Ω resistors are added to the input pins for protection against current surges coming from the 10 μF capacitors. By increasing these resistors to well over 100Ω the rise and fall times of the LM1203A can be increased for EMI considerations.

FIGURE 3. LM1203A Typical Application

Applications Information

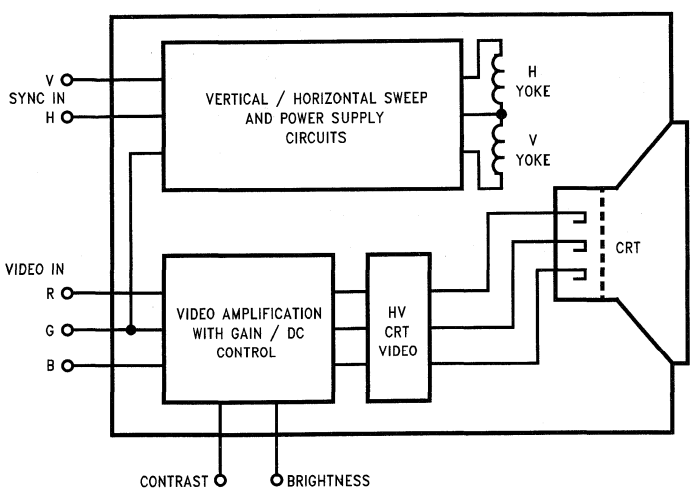
Figure 4 shows the block diagram of a typical analog RGB color monitor. The RGB monitor is used with CAD/CAM work stations, PC's, arcade games and in a wide range of other applications that benefit from the use of color display terminals. The RGB color monitor characteristics may differ in such ways as sweep rates, screen size, CRT color trio spacing (dot pitch), or in video amplifier bandwidths but will still be generally configured as shown in *Figure 4*. Separate horizontal and vertical sync signals may be required or they may be contained in the green video input signal. The video input signals are usually supplied by coax cable which is terminated in 75Ω at the monitor input and internally AC coupled to the video amplifiers. These input signals are approximately 1V peak to peak in amplitude and at the input of the high voltage video section, approximately 6V peak to peak. At the cathode of the CRT the video signals can be as high as 60V peak to peak. One important requirement of the three video amplifiers is that they match and track each other over the contrast and brightness control range. The *Figure 4* block labeled "VIDEO AMPLIFICATION WITH GAIN AND DC CONTROL" describes the function of the LM1203A which contains the three matched video amplifiers, contrast control and brightness control.

Circuit Description

Figure 5 is a block diagram of one of the video amplifiers along with the contrast and brightness controls. The contrast control is a DC-operated attenuator which varies the AC gain of all three amplifiers simultaneously while not introducing any signal distortions or tracking errors. The brightness control function requires a "sample and hold" circuit (black level clamp) which holds the DC bias of the video amplifiers and CRT cathodes constant during the black level reference portion of the video waveform. The clamp comparator, when gated on during this reference period, will charge or discharge the clamp capacitor until the plus input of the clamp comparator matches that of the minus input voltage which was set by the brightness control.

VIDEO AMPLIFIER SECTION

Figure 6 is a simplified schematic of one of the three video amplifiers along with the recommended external components. The IC pin numbers are circled and all external components are shown outside the dashed line. The video input is applied to pin 6 via a 10 μF coupling capacitor. DC bias for the video input is through the 10k resistor connected to the 2.8V reference at pin 11. The low frequency roll-off of the amplifier is set by these two components. Transistor Q1 buffers the video signal to the base of Q2. Q2's collector current is then directed to the V_{CC1} supply directly or through the 2k load resistor depending upon the differential DC voltage at the bases of Q3 and Q4. This differential DC voltage is generated by the contrast control circuit which is described in the following sections. A 0.01 μF decoupling capacitor in series with a 30Ω resistor is required between pins 2 and 3 to ensure high frequency isolation between the three video amplifiers which share these common connections. The video signal is buffered by Q5 and Q6 and DC level shifted by the voltage drop across R5. The magnitude of the current through R5 is determined by the voltage at pin 8. The voltage at pin 8 is set by the clamp comparator output current which charges or discharges the clamp hold capacitor during the black level period of the video waveform. Transistors Q9 and Q10 are Darlington connected to ensure a minimum discharge of the clamp hold capacitor during the time that the clamp capacitor is gated off. Q7, Q8 and R6 form a current mirror which sets a voltage at the base of Q11. Q11 buffers the video signal to the base of Q12 which provides additional signal gain. The "Drive" pin allows the user to trim the Q12 gain of each amplifier to correct for gain differences in the CRT and high voltage cathode driver gain stages. A small capacitor (several pico-Farads) from the "Drive" pin to ground will cause high frequency peaking and slightly improve the amplifier's bandwidth.

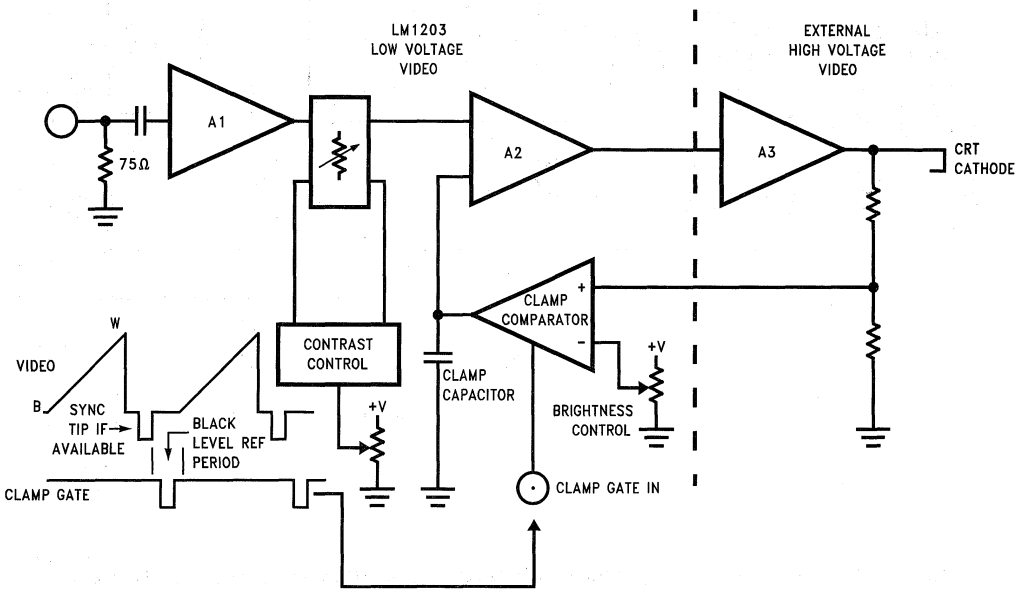


TL/H/11441–8

FIGURE 4. Typical RGB Color Monitor Block Diagram

Circuit Description (Continued)

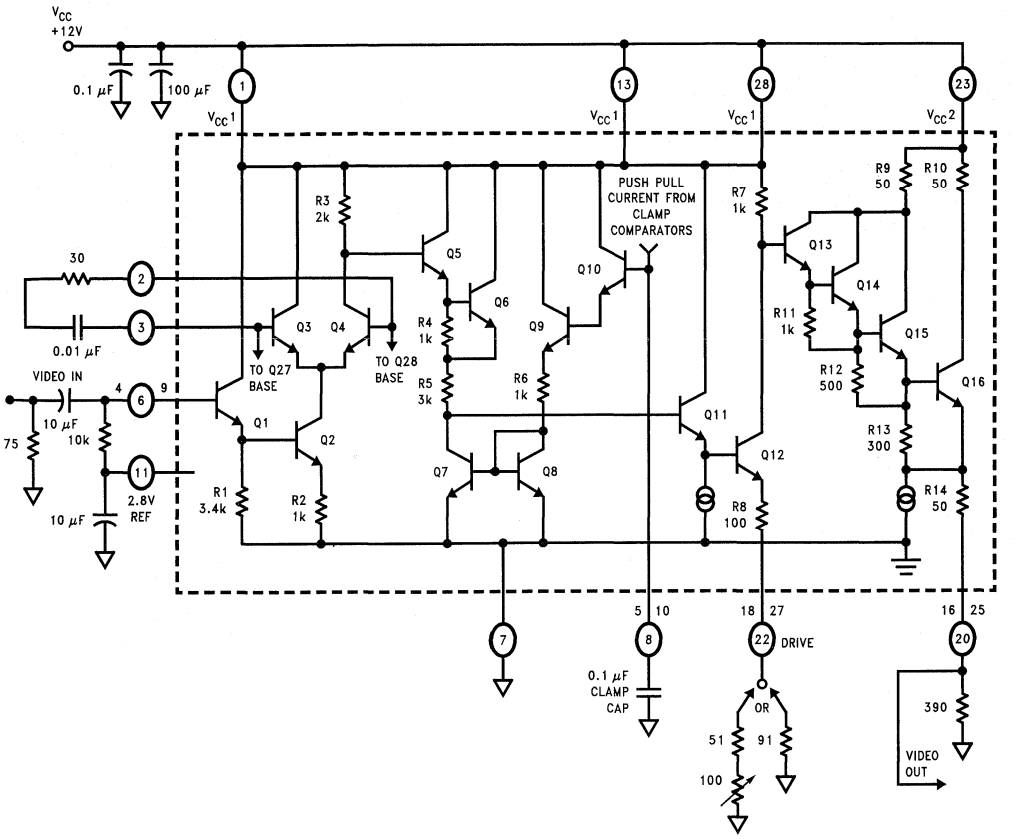
For individual gain adjustment of each video channel, a 51Ω resistor in series with a 100Ω potentiometer should be used with the red and green channel drive pins. A 91Ω resistor used with the blue channel drive pin sets the blue channel amplifier gain at approximately 6.2. The 100Ω potentiometer at the red and green channel drive pins allow a gain of 6.2 with ±25% gain adjustment. The video signal at the collector of Q12 is buffered and level shifted down by Q13, Q14 and Q15 to the base of the output emitter follower Q16. A 50Ω decoupling resistor is included in series with the emitter of Q16 and the video output pin so as to prevent oscillations when driving capacitive loads. An external resistor should be connected between the video output pin and ground. The value of this resistor should not be less than 390Ω or else package power limitations may be exceeded under worst case conditions (high supply voltage, maximum current, maximum temperature). The collector current from the video output transistor of each video channel is returned to the power supply at V_{CC2}, pin 23. When making power dissipation calculations note that the data sheet specifies only the V_{CC1} and V_{CC2} supply current at 12V supply voltage with no pull down resistor at the output (i.e., $R_L = \infty$, see test circuit *Figure 2*). The IC power dissipation due to V_{CC2} is dependant upon the external video output pull down resistor.



TL/H/11441–9

FIGURE 5. Block Diagram of LM1203A Video Amplifier with Contrast and Black Level Control

Circuit Description (Continued)



TL/H/11441–10

FIGURE 6. Simplified Schematic of LM1203A Video Amplifier Section with Recommended External Components

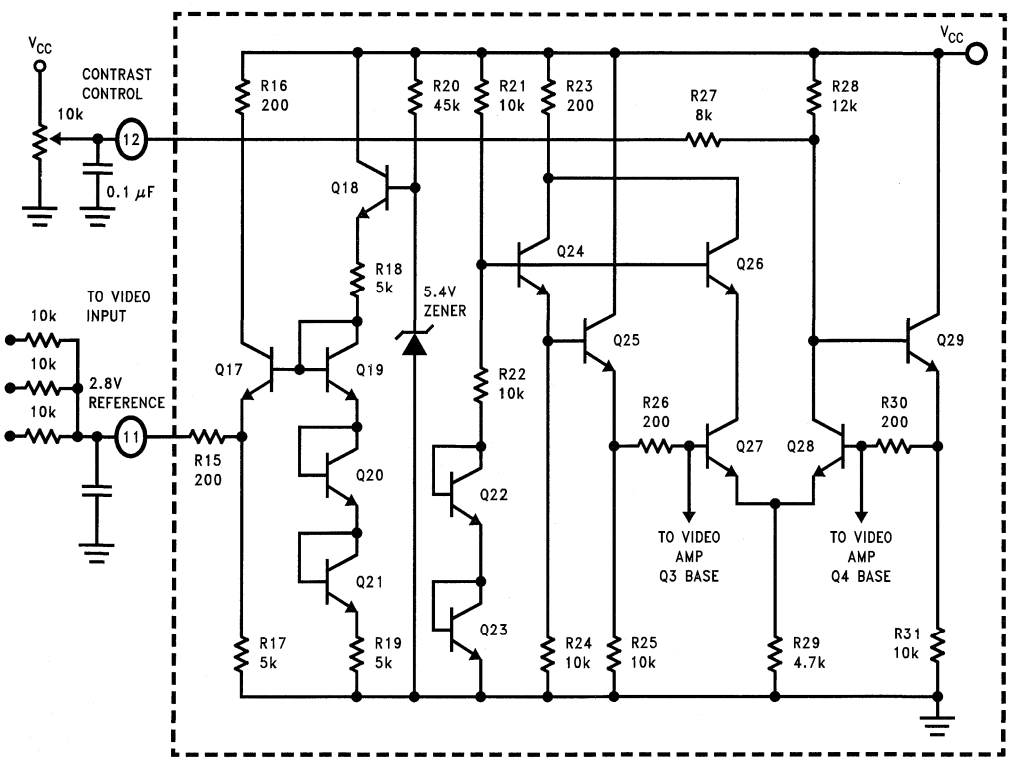
Circuit Description (Continued)

INPUT REFERENCE AND CONTRAST CONTROL SECTION

Figure 7 shows the input reference and contrast control circuitry. A temperature compensated 2.8V reference voltage is made available at pin 11. The external DC biasing resistors shown should not be larger than 10k because minor differences in input bias currents of the individual video amplifiers may cause offsets in gain. *Figure 7* also shows how the contrast control circuit is configured. R21, R22, Q22, Q23 and Q24 establish a low impedance zero TC half supply voltage reference at the base of Q25. The differential amplifier formed by Q27, Q28 and feedback transistor Q29 along with R28 and R29 establish a differential base voltage for Q3 and Q4 in *Figure 6*. When externally adding or subtracting current from the collector of Q28, a new differential voltage is generated that reflects the change in the ratio of currents in Q27 and Q28. To allow voltage control of the current through Q28, resistor R27 is added between the collector Q28 and pin 12. A capacitor should be connected from pin 12 to ground to prevent noise from the contrast control potentiometer from entering the IC.

CLAMP GATE AND CLAMP COMPARATOR SECTION

Figures 8 and *9* show simplified schematics of the clamp gate and clamp comparator circuits. The clamp gate circuit *(Figure 8)* consists of a PNP input buffer transistor (Q46), a PNP emitter coupled pair (Q47 and Q49) referenced on one side to 2.1V and an output switch transistor Q53. When the clamp gate input at pin 14 is high (>1.5V) the Q53 switch is on and shunts the 200 μA current from current source Q54 to ground. When pin 14 is low (<1.3V) the Q53 switch is off and the 200 μA current is mirrored by the current mirror comprised of Q55 and Q36 (see *Figure 9*). Consequently the clamp comparator comprised of the differential pair Q35 and Q37 is enabled. The input of each clamp comparator is similar to the clamp gate except than an NPN emitter coupled pair is used to control the current that will charge or discharge the clamp capacitors at pins 5, 8 and 10. PNP transistors are used at the inputs because they offer a number of advantages over NPNs. PNPs will operate with base voltages at or near ground and will usually have a greater emitter base breakdown voltage (BVebo). Because the differential input voltage to the clamp comparator during the video scan period could be greater than the BVebo of NPN transistors, a resistor (R37) with a value one half that of R36 or R39 is connected between the bases of Q34 and Q38. The clamp comparator's common mode range is from ground to approximately 9V and the maximum differential input voltage is V_{CC} and ground.



TL/H/11441–11

FIGURE 7. Simplified Schematic of LM1203A Video Input Reference and Contrast Control Circuits

Circuit Description (Continued)

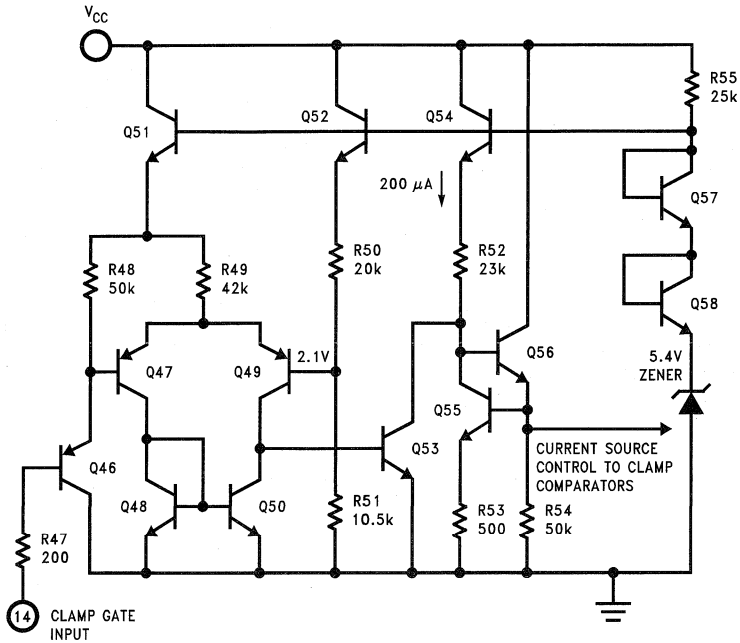


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FIGURE 8. Simplified Schematic of LM1203A Clamp Gate Circuit

Circuit Description (Continued)

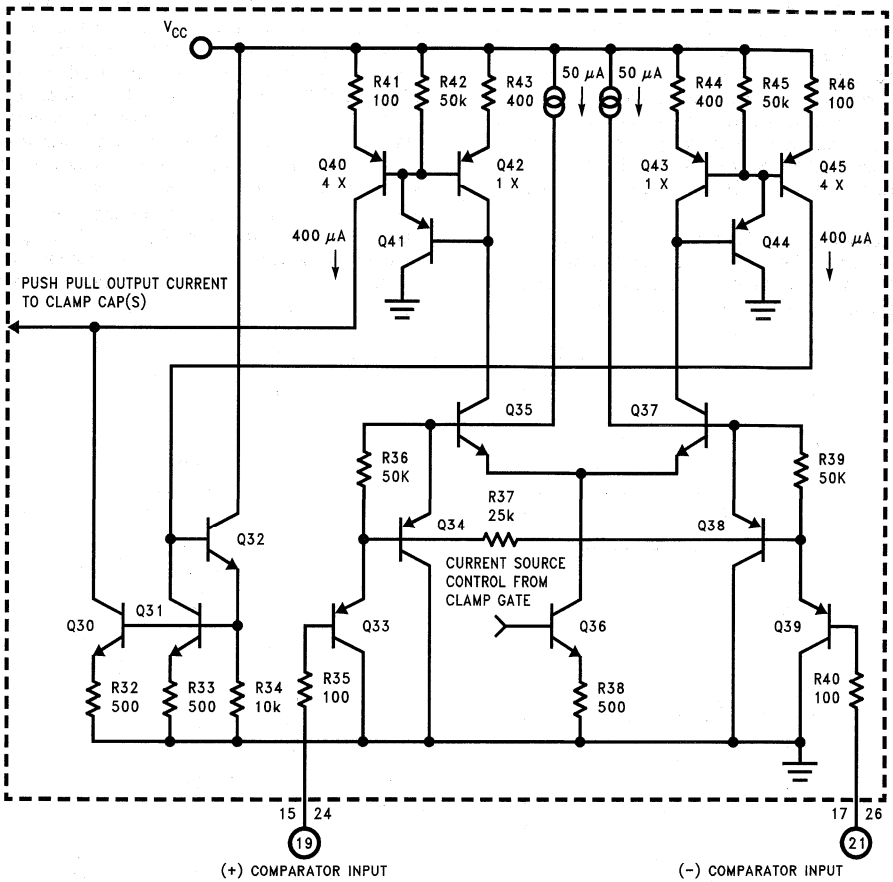

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FIGURE 9. Simplified Schematic of LM1203A Clamp Comparator Circuits

Additional Applications of the LM1203A

Figure 10 shows the configuration for a three channel high frequency amplifier with non gated DC feedback. Pin 14 is tied low to turn on the clamp comparators (feedback amplifiers). The inverting inputs (Pins 17, 21, 26) are connected to the amplifier outputs from a low pass filter. Additional low frequency filtering is provided by the clamp caps. The drive resistors can be made variable or fixed at values between 0Ω and 300Ω. Maximum output swings are achieved when the DC output is set to approximately 4V. The high frequency response will be dependent upon external peaking at the drive pins.

Figure 11 shows a complete RGB video preamplifier circuit using the LM1203A. A quad Exclusive-OR gate (MM74HC86) is used to generate the back porch clamp signal from the composite sync input signal. The composite H Sync input signal may have either polarity. The back porch clamp signal applied to LM1203A's pin 14 allows clamping the video output signals to the black reference level, thereby providing DC restoration. The back porch clamp pulse width is determined by the time constant due to the product of R11 and C15. For fast horizontal scan rates, the back porch clamp pulse width can be made narrower by decreasing the value of R11 or C15 or both. Note that an MM74C86 Exclusive-OR gate may also be used, however, the pin out is different than that of the MM74HC86.

For optimum performance and maximum bandwidth, high speed buffer transistors (Q1, Q2 and Q3 in *Figure 11*) are recommended. The 2N5770 NPN transistors maintain high speed at high currents when driving the inputs of high voltage CRT drivers.

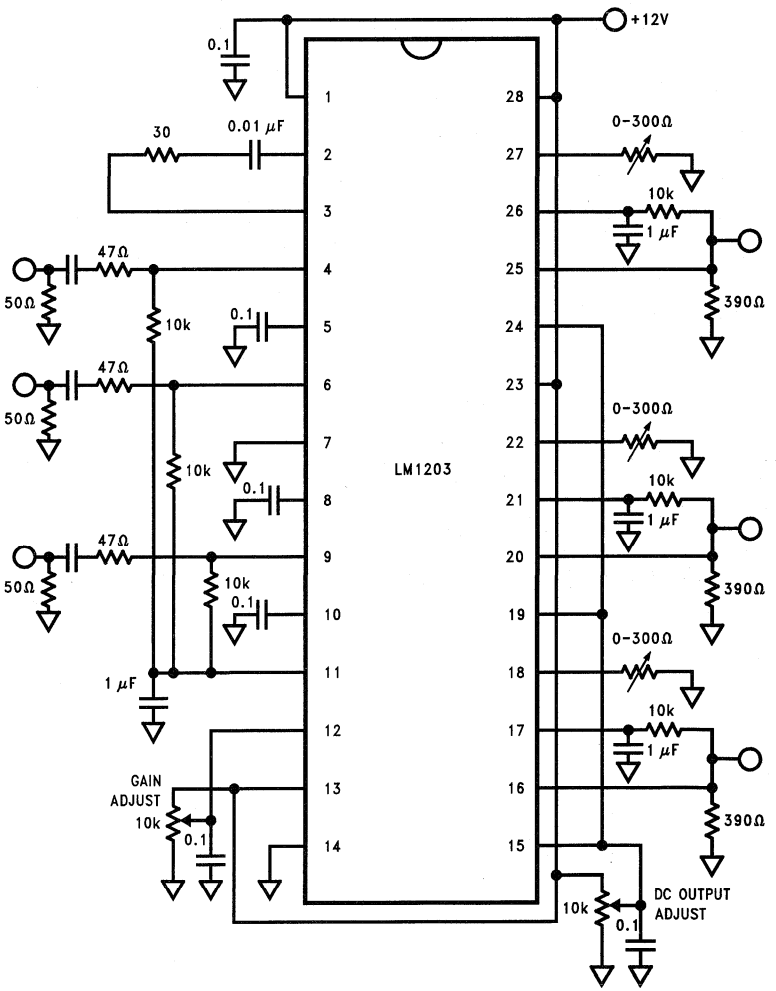

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FIGURE 10. Three Channel High Frequency Amplifier with Non-gated DC Feedback (Non-video Application)

Additional Applications of the LM1203A (Continued)

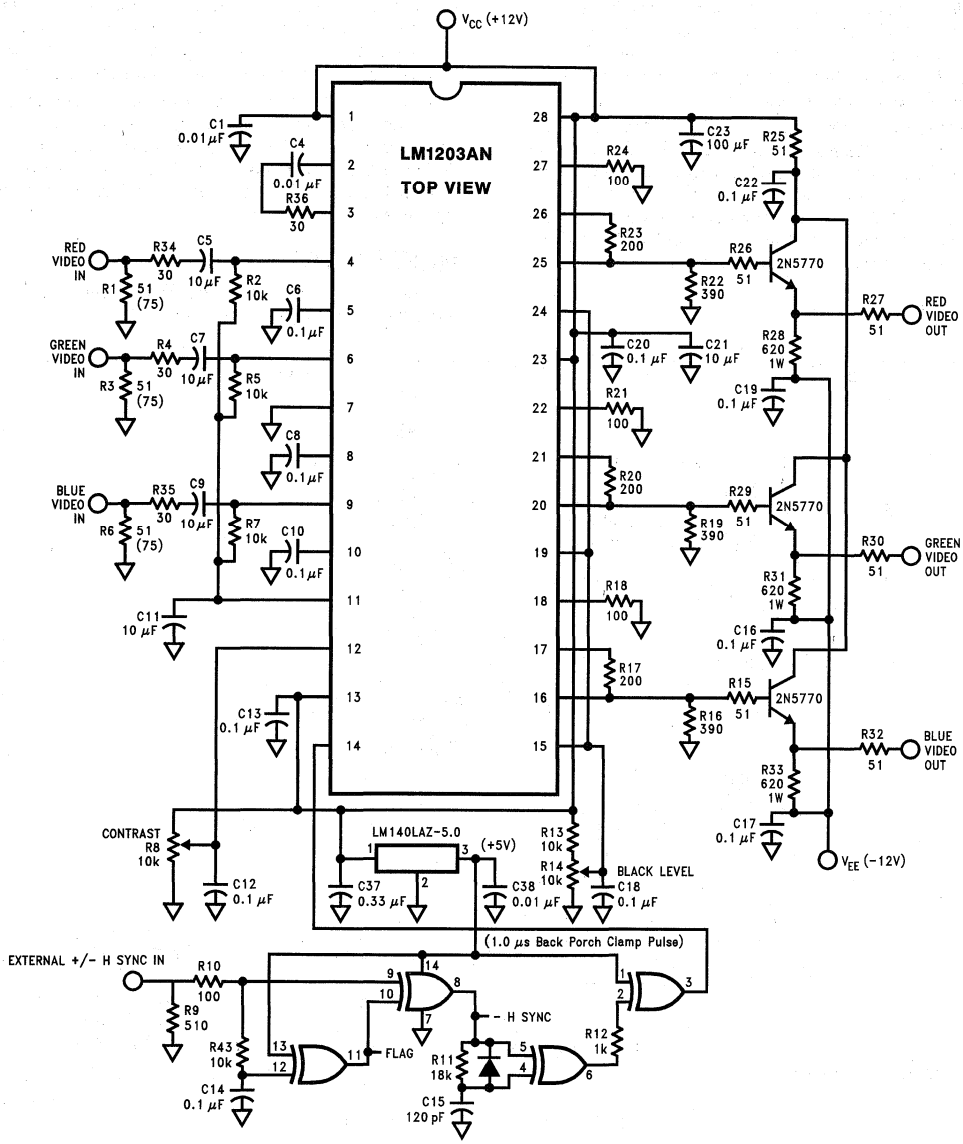

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FIGURE 11. LM1203A Applications Circuit

LM1203A vs LM1203

LM1203A is an improved version of the LM1203 RGB video amplifier system and is pin and function compatible with the LM1203. LM1203A's output voltage can swing as low as 0.15V as opposed to 0.9V for the LM1203. This eliminates the need for a level shift stage between the preamplifier and the CRT driver in most applications.

The LM1203A also offers faster rise and fall times of 4 ns vs 7 ns for the LM1203 and 100 MHz bandwidth vs 70 MHz for LM1203. With a peaking capacitor across the drive resistor, LM1203A's bandwidth can be extended to 150 MHz. Because of LM1203A's wide bandwidth, the device may oscillate if plugged directly into an existing LM1203 board. For optimum performance and stable operation, a double sided printed circuit board with adequate ground plane and power supply decoupling as close to the V_{CC} pins as possible is recommended. *Figure 12* shows the layout of the PC board for *Figure 11's* circuit. For suggestions on optimum PC board layout, please see the reference section below.

The LM1203A also includes a built-in power down spot killer to prevent a flash on the screen upon power down. In some preamplifiers, the video output signal may go high as the device is being powered down. This may cause a whiter than white level at the output of the CRT driver, thus causing a flash on the screen.

REFERENCE

Ott, Henry W. *Noise Reduction Techniques in Electronic Systems,* John Wiley & Sons, New York, 1976.

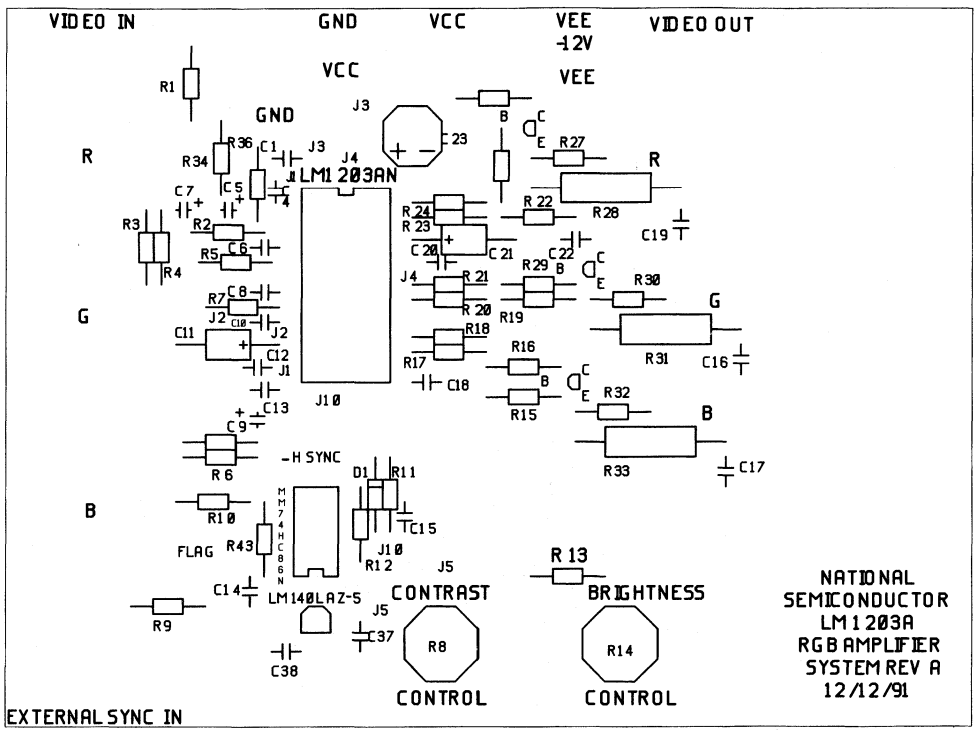

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FIGURE 12(a). PC Board Silk Screen

Additional Applications of the LM1203A (Continued)

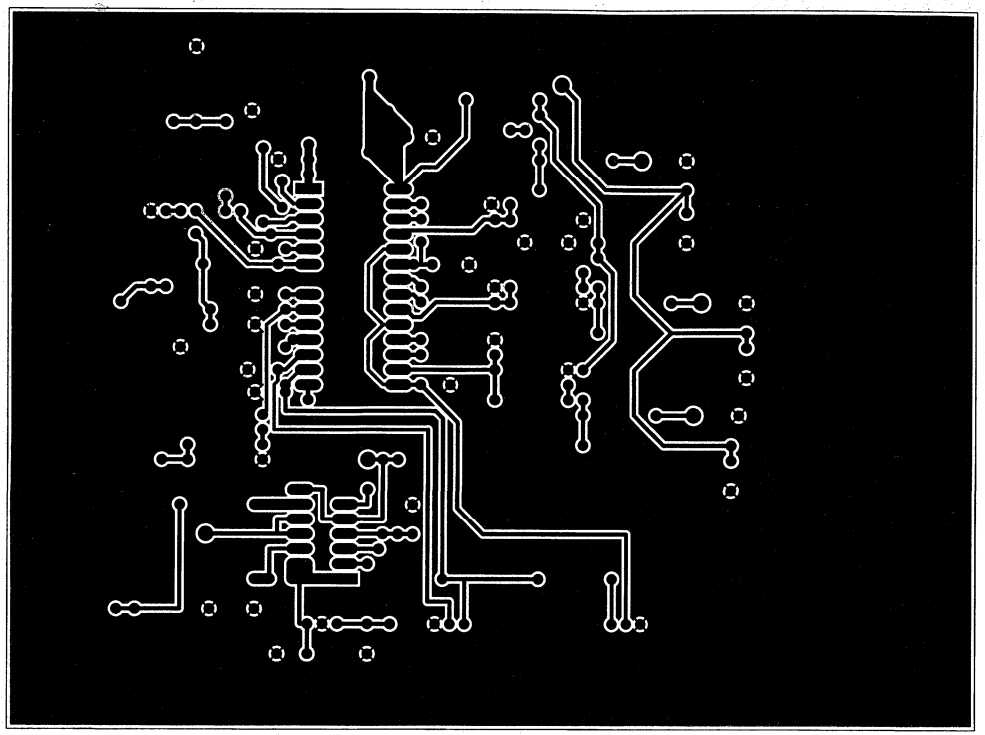

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FIGURE 12(b). PC board layout of bottom side. Top side of PC board (not shown) is full ground plane.

National Semiconductor

LM1558/LM1458 Dual Operational Amplifier

General Description

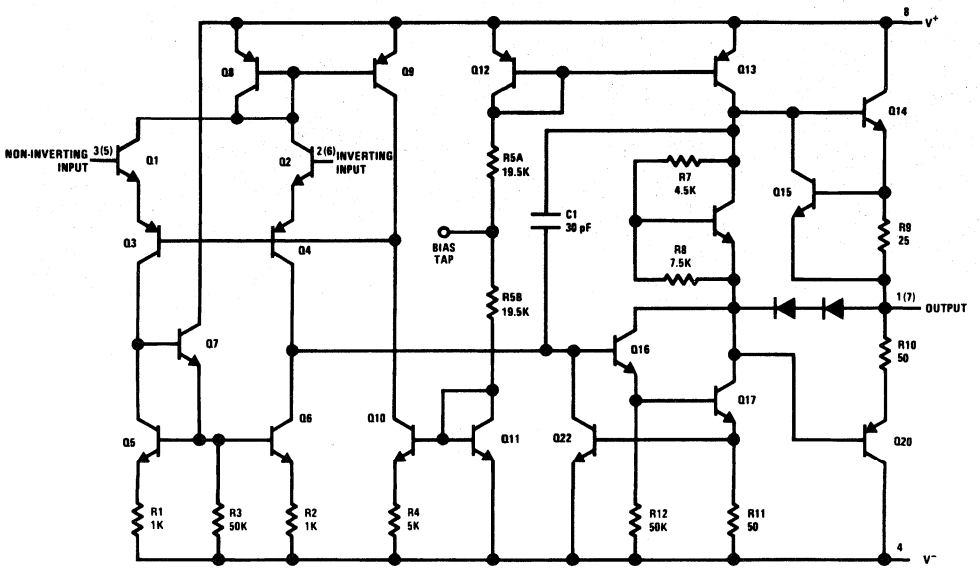
The LM1558 and the LM1458 are general purpose dual operational amplifiers. The two amplifiers share a common bias network and power supply leads. Otherwise, their operation is completely independent.

The LM1458 is identical to the LM1558 except that the LM1458 has its specifications guaranteed over the temperature range from 0°C to +70°C instead of −55°C to +125°C.

Features

- No frequency compensation required
- Short-circuit protection
- Wide common-mode and differential voltage ranges
- Low-power consumption
- 8-lead can and 8-lead mini DIP
- No latch up when input common mode range is exceeded

Schematic and Connection Diagrams



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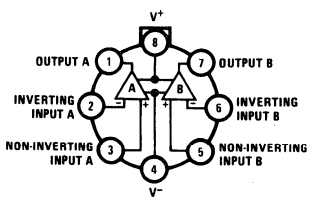
Note: Numbers in parentheses are pin numbers for amplifier B.

Metal Can Package

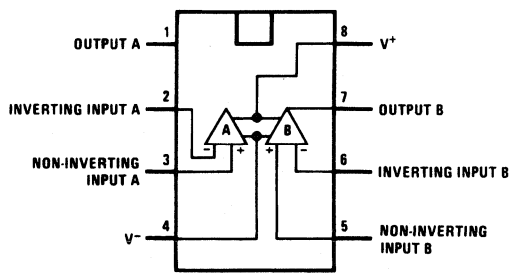


TL/H/7886–2

Top View

Order Number LM1558H, LM1558H/883 or LM1458H
See NS Package Number H08C

Dual-In-Line Package



TL/H/7886–3

Top View

Order Number LM1558J, LM1558J/883, LM1458J, LM1458M or LM1458N
See NS Package Number J08A, M08A or N08E

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications. (Note 4)

Supply Voltage
- LM1558 ±22V
- LM1458 ±18V

Power Dissipation (Note 1)
- LM1558H/LM1458H 500 mW
- LM1458N 400 mW

Differential Input Voltage ±30V

Input Voltage (Note 2) ±15V

Output Short-Circuit Duration Continuous

Operating Temperature Range
- LM1558 −55°C to +125°C
- LM1458 0°C to +70°C

Storage Temperature Range −65°C to +150°C

Lead Temperature (Soldering, 10 sec.) 260°C

Soldering Information
- Dual-In-Line Package
  - Soldering (10 seconds) 260°C
- Small Outline Package
  - Vapor Phase (60 seconds) 215°C
  - Infrared (15 seconds) 220°C

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

ESD tolerance (Note 5) 300V

Electrical Characteristics (Note 3)

Parameter	Conditions	LM1558			LM1458			Units
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	$T_A = 25°C$, $R_S \leq 10\ k\Omega$		1.0	5.0		1.0	6.0	mV
Input Offset Current	$T_A = 25°C$		80	200		80	200	nA
Input Bias Current	$T_A = 25°C$		200	500		200	500	nA
Input Resistance	$T_A = 25°C$	0.3	1.0		0.3	1.0		MΩ
Supply Current Both Amplifiers	$T_A = 25°C$, $V_S = \pm 15V$		3.0	5.0		3.0	5.6	mA
Large Signal Voltage Gain	$T_A = 25°C$, $V_S = \pm 15V$ $V_{OUT} = \pm 10V$, $R_L \geq 2\ k\Omega$	50	160		20	160		V/mV
Input Offset Voltage	$R_S \leq 10\ k\Omega$			6.0			7.5	mV
Input Offset Current				500			300	nA
Input Bias Current				1.5			0.8	μA
Large Signal Voltage Gain	$V_S = \pm 15V$, $V_{OUT} = \pm 10V$ $R_L \geq k\Omega$	25			15			V/mV
Output Voltage Swing	$V_S = \pm 15V$, $R_L = 10\ k\Omega$	±12	±14		±12	±14		V
	$R_L = 2\ k\Omega$	±10	±13		±10	±13		V
Input Voltage Range	$V_S = \pm 15V$	±12			±12			V
Common Mode Rejection Ratio	$R_S \leq 10\ k\Omega$	70	90		70	90		dB
Supply Voltage Rejection Ratio	$R_S \leq 10\ k\Omega$	77	96		77	96		dB

Note 1: The maximum junction temperature of the LM1558 is 150°C, while that of the LM1458 is 100°C. For operating at elevated temperatures, devices in the H08 package must be derated based on a thermal resistance of 150°C/W, junction to ambient or 20°C/W, junction to case. For the DIP the device must be derated based on a thermal resistance of 187°C/W, junction to ambient.

Note 2: For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

Note 3: These specifications apply for $V_S = \pm 15V$ and $-55°C \leq T_A \leq 125°C$, unless otherwise specified. With the LM1458, however, all specifications are limited to $0°C \leq T_A \leq 70°C$ and $V_S = \pm 15V$.

Note 4: Refer to RETS 1558V for LM1558J and LM1558H military specifications.

Note 5: Human body model, 1.5 kΩ in series with 100 pF.

National Semiconductor

LM1875 20 Watt Power Audio Amplifier

General Description

The LM1875 is a monolithic power amplifier offering very low distortion and high quality performance for consumer audio applications.

The LM1875 delivers 20 watts into a 4Ω or 8Ω load on ±25V supplies. Using an 8Ω load and ±30V supplies, over 30 watts of power may be delivered. The amplifier is designed to operate with a minimum of external components. Device overload protection consists of both internal current limit and thermal shutdown.

The LM1875 design takes advantage of advanced circuit techniques and processing to achieve extremely low distortion levels even at high output power levels. Other outstanding features include high gain, fast slew rate and a wide power bandwidth, large output voltage swing, high current capability, and a very wide supply range. The amplifier is internally compensated and stable for gains of 10 or greater.

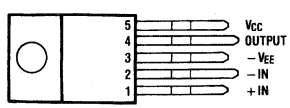
Features

- Up to 30 watts output power
- A_{VO} typically 90 dB
- Low distortion: 0.015%, 1 kHz, 20 W
- Wide power bandwidth: 70 kHz
- Protection for AC and DC short circuits to ground
- Thermal protection with parole circuit
- High current capability: 4A
- Wide supply range 16V-60V
- Internal output protection diodes
- 94 dB ripple rejection
- Plastic power package TO-220

Applications

- High performance audio systems
- Bridge amplifiers
- Stereo phonographs
- Servo amplifiers
- Instrument systems

Connection Diagram



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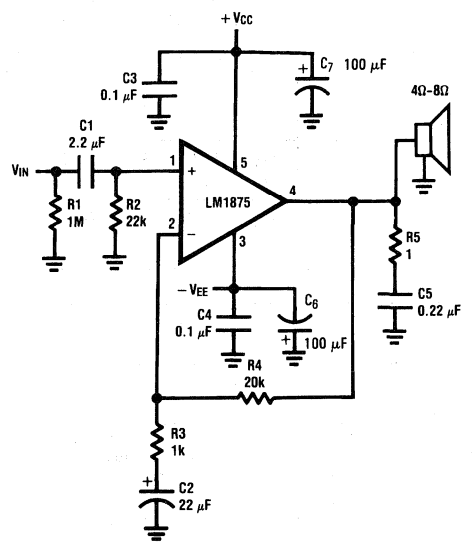
Front View

Order Number LM1875T
See NS Package Number T05B

Typical Applications



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Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	60V
Input Voltage	$-V_{EE}$ to V_{CC}
Storage Temperature	−65°C to + 150°C
Junction Temperature	150°C
Lead Temperature (Soldering, 10 seconds)	260°C

Electrical Characteristics

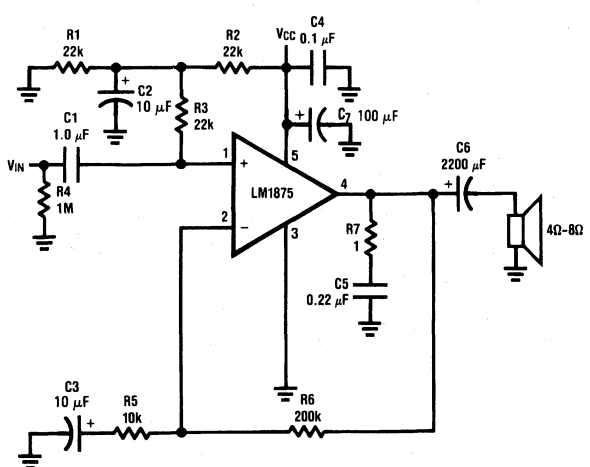
V_{CC} = +25V, $-V_{EE}$ = −25V, $T_{AMBIENT}$ = 25°C, R_L = 8Ω, A_V = 20 (26 dB), f_o = 1 kHz, unless otherwise specified.

Parameter	Conditions	Typical	Tested Limits	Units
Supply Current	P_{OUT} = 0W	70	100	mA
Output Power (Note 1)	THD = 1%	25		W
THD (Note 1)	P_{OUT} = 20W, f_o = 1 kHz	0.015		%
	P_{OUT} = 20W, f_o = 20 kHz	0.05	0.4	%
	P_{OUT} = 20W, R_L = 4Ω, f_o = 1 kHz	0.022		%
	P_{OUT} = 20W, R_L = 4Ω, f_o = 20 kHz	0.07	0.6	%
Offset Voltage		±1	±15	mV
Input Bias Current		±0.2	±2	μA
Input Offset Current		0	±0.5	μA
Gain-Bandwidth Product	f_o = 20 kHz	5.5		MHz
Open Loop Gain	DC	90		dB
PSRR	V_{CC}, 1 kHz, 1 Vrms	95	52	dB
	V_{EE}, 1 kHz, 1 Vrms	83	52	dB
Max Slew Rate	20W, 8Ω, 70 kHz BW	8		V/μs
Current Limit	V_{OUT} = V_{SUPPLY} −10V	4	3	A
Equivalent Input Noise Voltage	R_S = 600Ω, CCIR	3		μVrms

Note 1: Assumes the use of a heat sink having a thermal resistance of 1°C/W and no insulator with an ambient temperature of 25°C. Because the output limiting circuitry has a negative temperature coefficient, the maximum output power delivered to a 4Ω load may be slightly reduced when the tab temperature exceeds 55°C.

Typical Applications (Continued)

Typical Single Supply Operation



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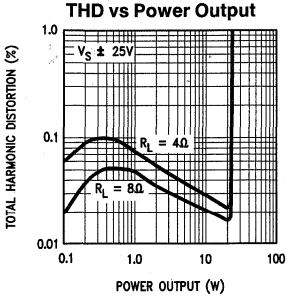
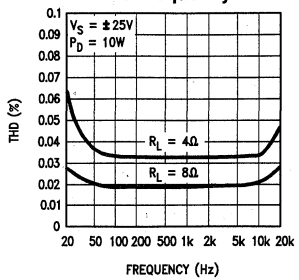
Typical Performance Characteristics

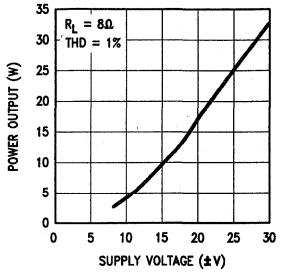
THD vs Power Output



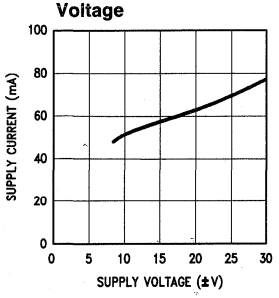
THD vs Frequency



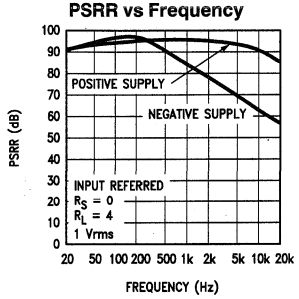
Power Output vs Supply Voltage



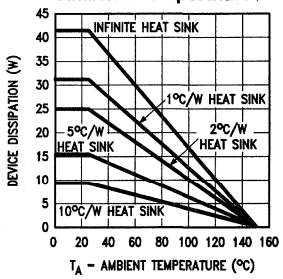
Supply Current vs Supply Voltage



PSRR vs Frequency

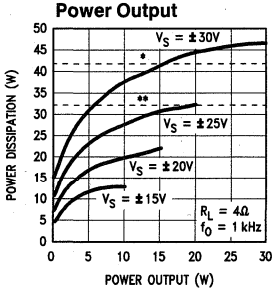


Device Dissipation vs Ambient Temperature†

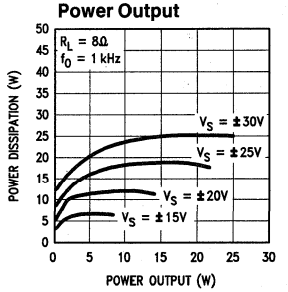


†ϕINTERFACE = 1°C/W.
See Application Hints.

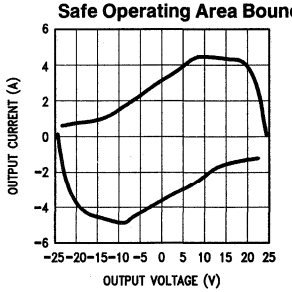
Power Dissipation vs Power Output



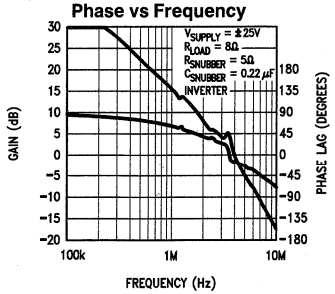
Power Dissipation vs Power Output



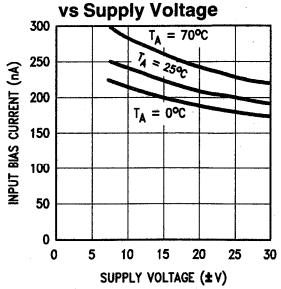
I_{OUT} vs V_{OUT}-Current Limit/ Safe Operating Area Boundary



Open Loop Gain and Phase vs Frequency



Input Bias Current vs Supply Voltage

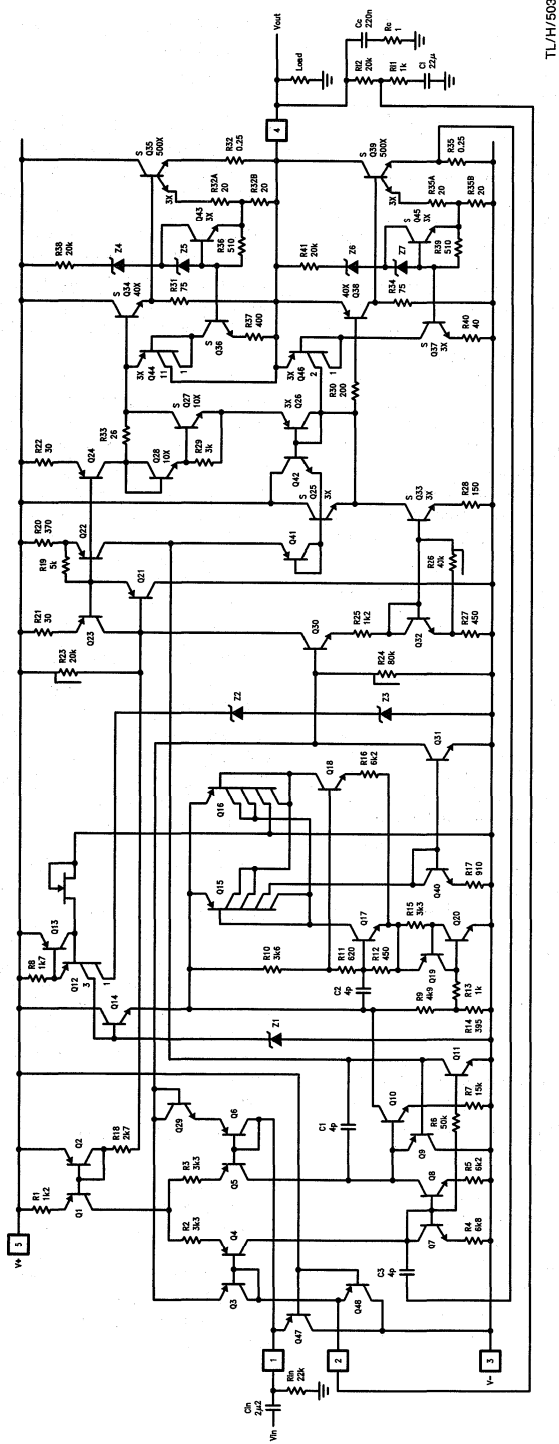


TL/H/5030–4

*Thermal shutdown with infinite heat sink

**Thermal shutdown with 1°C/W heat sink

Schematic Diagram



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Application Hints

STABILITY

The LM1875 is designed to be stable when operated at a closed-loop gain of 10 or greater, but, as with any other high-current amplifier, the LM1875 can be made to oscillate under certain conditions. These usually involve printed circuit board layout or output/input coupling.

Proper layout of the printed circuit board is very important. While the LM1875 will be stable when installed in a board similar to the ones shown in this data sheet, it is sometimes necessary to modify the layout somewhat to suit the physical requirements of a particular application. When designing a different layout, it is important to return the load ground, the output compensation ground, and the low level (feedback and input) grounds to the circuit board ground point through separate paths. Otherwise, large currents flowing along a ground conductor will generate voltages on the conductor which can effectively act as signals at the input, resulting in high frequency oscillation or excessive distortion. It is advisable to keep the output compensation components and the 0.1 μF supply decoupling capacitors as close as possible to the LM1875 to reduce the effects of PCB trace resistance and inductance. For the same reason, the ground return paths for these components should be as short as possible.

Occasionally, current in the output leads (which function as antennas) can be coupled through the air to the amplifier input, resulting in high-frequency oscillation. This normally happens when the source impedance is high or the input leads are long. The problem can be eliminated by placing a small capacitor (on the order of 50 pF to 500 pF) across the circuit input.

Most power amplifiers do not drive highly capacitive loads well, and the LM1875 is no exception. If the output of the LM1875 is connected directly to a capacitor with no series resistance, the square wave response will exhibit ringing if the capacitance is greater than about 0.1 μF. The amplifier can typically drive load capacitances up to 2 μF or so without oscillating, but this is not recommended. If highly capacitive loads are expected, a resistor (at least 1Ω) should be placed in series with the output of the LM1875. A method commonly employed to protect amplifiers from low impedances at high frequencies is to couple to the load through a 10Ω resistor in parallel with a 5 μH inductor.

DISTORTION

The preceding suggestions regarding circuit board grounding techniques will also help to prevent excessive distortion levels in audio applications. For low THD, it is also necessary to keep the power supply traces and wires separated from the traces and wires connected to the inputs of the LM1875. This prevents the power supply currents, which are large and nonlinear, from inductively coupling to the LM1875 inputs. Power supply wires should be twisted together and separated from the circuit board. Where these wires are soldered to the board, they should be perpendicular to the plane of the board at least to a distance of a couple of inches. With a proper physical layout, THD levels at 20 kHz with 10W output to an 8Ω load should be less than 0.05%, and less than 0.02% at 1 kHz.

CURRENT LIMIT AND SAFE OPERATING AREA (SOA) PROTECTION

A power amplifier's output transistors can be damaged by excessive applied voltage, current flow, or power dissipation. The voltage applied to the amplifier is limited by the design of the external power supply, while the maximum current passed by the output devices is usually limited by internal circuitry to some fixed value. Short-term power dissipation is usually not limited in monolithic audio power amplifiers, and this can be a problem when driving reactive loads, which may draw large currents while high voltages appear on the output transistors. The LM1875 not only limits current to around 4A, but also reduces the value of the limit current when an output transistor has a high voltage across it.

When driving nonlinear reactive loads such as motors or loudspeakers with built-in protection relays, there is a possibility that an amplifier output will be connected to a load whose terminal voltage may attempt to swing beyond the power supply voltages applied to the amplifier. This can cause degradation of the output transistors or catastrophic failure of the whole circuit. The standard protection for this type of failure mechanism is a pair of diodes connected between the output of the amplifier and the supply rails. These are part of the internal circuitry of the LM1875, and needn't be added externally when standard reactive loads are driven.

THERMAL PROTECTION

The LM1875 has a sophisticated thermal protection scheme to prevent long-term thermal stress to the device. When the temperature on the die reaches 170°C, the LM1875 shuts down. It starts operating again when the die temperature drops to about 145°C, but if the temperature again begins to rise, shutdown will occur at only 150°C. Therefore, the device is allowed to heat up to a relatively high temperature if the fault condition is temporary, but a sustained fault will limit the maximum die temperature to a lower value. This greatly reduces the stresses imposed on the IC by thermal cycling, which in turn improves its reliability under sustained fault conditions.

Since the die temperature is directly dependent upon the heat sink, the heat sink should be chosen for thermal resistance low enough that thermal shutdown will not be reached during normal operation. Using the best heat sink possible within the cost and space constraints of the system will improve the long-term reliability of any power semiconductor device.

POWER DISSIPATION AND HEAT SINKING

The LM1875 must always be operated with a heat sink, even when it is not required to drive a load. The maximum idling current of the device is 100 mA, so that on a 60V power supply an unloaded LM1875 must dissipate 6W of power. The 54°C/W junction-to-ambient thermal resistance of a TO-220 package would cause the die temperature to rise 324°C above ambient, so the thermal protection circuitry will shut the amplifier down if operation without a heat sink is attempted.

Application Hints (Continued)

In order to determine the appropriate heat sink for a given application, the power dissipation of the LM1875 in that application must be known. When the load is resistive, the maximum average power that the IC will be required to dissipate is approximately:

$$P_{D(MAX)} \approx \frac{V_S^2}{2\pi^2 R_L} + P_Q$$

where V_S is the total power supply voltage across the LM1875, R_L is the load resistance, and P_Q is the quiescent power dissipation of the amplifier. The above equation is only an approximation which assumes an "ideal" class B output stage and constant power dissipation in all other parts of the circuit. The curves of "Power Dissipation vs Power Output" give a better representation of the behavior of the LM1875 with various power supply voltages and resistive loads. As an example, if the LM1875 is operated on a 50V power supply with a resistive load of 8Ω, it can develop up to 19W of internal power dissipation. If the die temperature is to remain below 150°C for ambient temperatures up to 70°C, the total junction-to-ambient thermal resistance must be less than

$$\frac{150°C - 70°C}{19W} = 4.2°C/W.$$

Using $\theta_{JC} = 2°C/W$, the sum of the case-to-heat-sink interface thermal resistance and the heat-sink-to-ambient thermal resistance must be less than 2.2°C/W. The case-to-heat-sink thermal resistance of the TO-220 package varies with the mounting method used. A metal-to-metal interface will be about 1°C/W if lubricated, and about 1.2°C/W if dry.

If a mica insulator is used, the thermal resistance will be about 1.6°C/W lubricated and 3.4°C/W dry. For this example, we assume a lubricated mica insulator between the LM1875 and the heat sink. The heat sink thermal resistance must then be less than

4.2°C/W − 2°C/W − 1.6°C/W = 0.6°C/W.

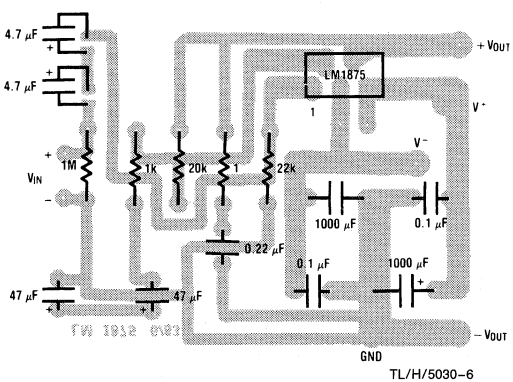
This is a rather large heat sink and may not be practical in some applications. If a smaller heat sink is required for reasons of size or cost, there are two alternatives. The maximum ambient operating temperature can be reduced to 50°C (122°F), resulting in a 1.6°C/W heat sink, or the heat sink can be isolated from the chassis so the mica washer is not needed. This will change the required heat sink to a 1.2°C/W unit if the case-to-heat-sink interface is lubricated.

Note: When using a single supply, maximum transfer of heat away from the LM1875 can be achieved by mounting the device directly to the heat sink (tab is at ground potential); this avoids the use of a mica or other type insulator.

The thermal requirements can become more difficult when an amplifier is driving a reactive load. For a given magnitude of load impedance, a higher degree of reactance will cause a higher level of power dissipation within the amplifier. As a general rule, the power dissipation of an amplifier driving a 60° reactive load (usually considered to be a worst-case loudspeaker load) will be roughly that of the same amplifier driving the resistive part of that load. For example, a loudspeaker may at some frequency have an impedance with a magnitude of 8Ω and a phase angle of 60°. The real part of this load will then be 4Ω, and the amplifier power dissipation will roughly follow the curve of power dissipation with a 4Ω load.

Component Layouts

Split Supply



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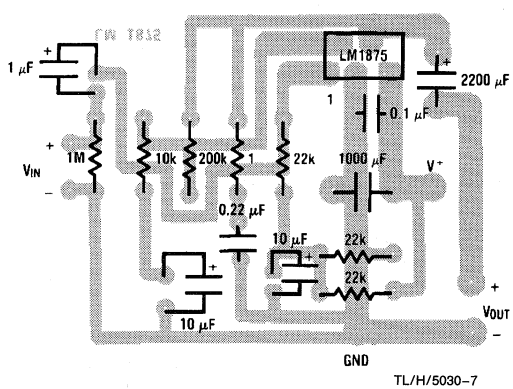
Single Supply



TL/H/5030–7

National Semiconductor

LM1877 Dual Power Audio Amplifier

General Description

The LM1877 is a monolithic dual power amplifier designed to deliver 2W/channel continuous into 8Ω loads. The LM1877 is designed to operate with a low number of external components, and still provide flexibility for use in stereo phonographs, tape recorders and AM-FM stereo receivers, etc. Each power amplifier is biased from a common internal regulator to provide high power supply rejection, and output Q point centering. The LM1877 is internally compensated for all gains greater than 10.

Features

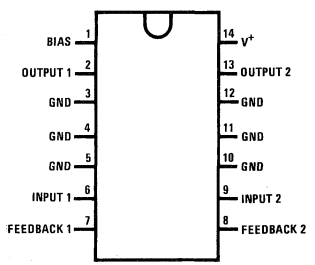
- 2W/channel
- −65 dB ripple rejection, output referred
- −65 dB channel separation, output referred
- Wide supply range, 6V–24V
- Very low cross-over distortion
- Low audio band noise
- AC short circuit protected
- Internal thermal shutdown

Applications

- Multi-channel audio systems
- Stereo phonographs
- Tape recorders and players
- AM-FM radio receivers
- Servo amplifiers
- Intercom systems
- Automotive products

Connection Diagram

Dual-In-Line Package
or Surface Mount Package



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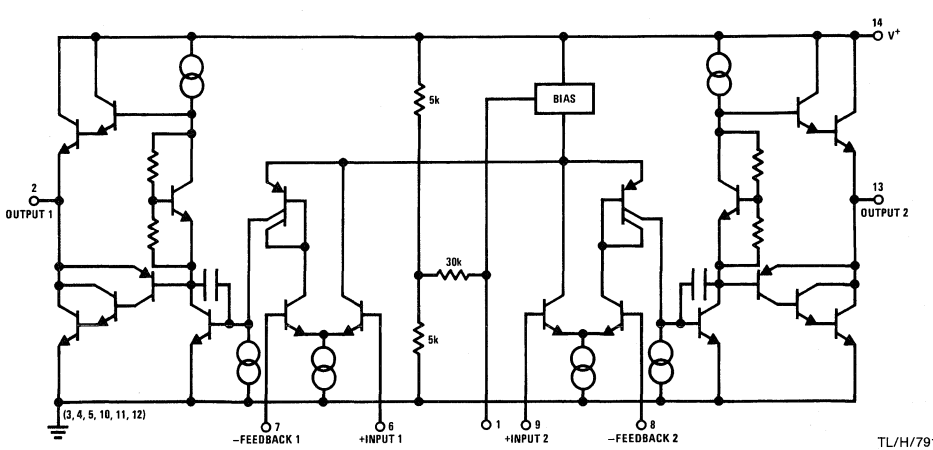
Top View

Order Number LM1877M-9 or LM1877N-9
See NS Package Number M14B or N14A

Equivalent Schematic Diagram



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Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	26V
Input Voltage	±0.7V
Operating Temperature	0°C to +70°C
Storage Temperature	−65°C to +150°C
Junction Temperature	150°C

Lead Temperature

N-Package Soldering (10 sec.)	260°C
M-Package Infared (15 sec.)	220°C
M-Package Vapor Phase (60 sec.)	215°C

Thermal Resistance, θ_{JA}

M-Package	106°C/W
N-Package	76°C/W

Electrical Characteristics

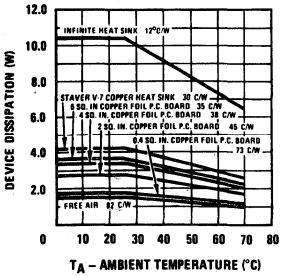
V_S = 20V, T_A = 25°C, (See Note 1) R_L = 8Ω, A_V = 50 (34 dB) unless otherwise specified

Parameter	Conditions	Min	Typ	Max	Units
Total Supply Current	P_O = 0W		25	50	mA
Output Power LM1877	THD = 10% V_S = 20V, R_L = 8Ω	2.0			W/Ch
Total Harmonic Distortion LM1877	f = 1 kHz, V_S = 14V				
	P_O = 50 mW/Channel		0.075		%
	P_O = 500 mW/Channel		0.045		%
	P_O = 1 W/Channel		0.055		%
Output Swing	R_L = 8Ω		V_S −6		Vp-p
Channel Separation	C_F = 50 µF, C_{IN} = 0.1 µF, f = 1 kHz, Output Referred				
	V_S = 20V, V_O = 4 Vrms	−50	−70		dB
	V_S = 7V, V_O = 0.5 Vrms		−60		dB
PSRR Power Supply Rejection Ratio	C_F = 50 µF, C_{IN} = 0.1 µF, f = 120 Hz, Output Referred				
	V_S = 20V, V_{RIPPLE} = 1 Vrms	−50	−65		dB
	V_S = 7V, V_{RIPPLE} = 0.5 Vrms		−40		dB
Noise	Equivalent Input Noise				
	R_S = 0, C_{IN} = 0.1 µF, BW = 20 Hz–20 kHz, Output Noise Wideband		2.5		µV
	R_S = 0, C_N = 0.1 µF, A_V 200		0.80		mV
Open Loop Gain	R_S = 0, f = 100 kHz, R_L = 8Ω		70		dB
Input Offset Voltage			15		mV
Input Bias Current			50		nA
Input Impedance	Open Loop		4		MΩ
DC Output Level	V_S = 20V	9	10	11	V
Slew Rate			2.0		V/µs
Power Bandwidth			65		kHz
Current Limit			1.0		A

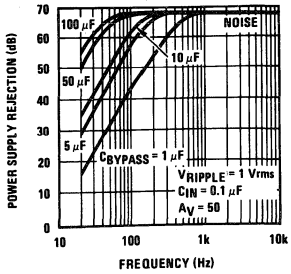
Note 1: For operation at ambient temperature greater than 25°C, the LM1877 must be derated based on a maximum 150°C junction temperature.

Typical Performance Characteristics

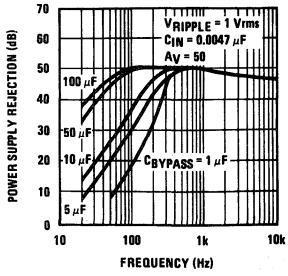
Device Dissipation vs Ambient Temperature



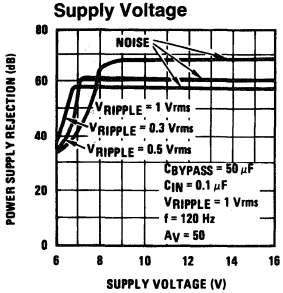
Power Supply Rejection Ratio (Referred to the Output) vs Frequency



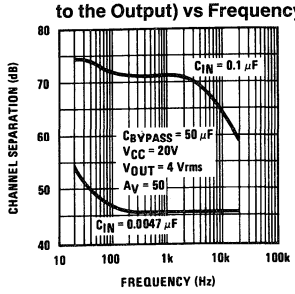
Power Supply Rejection Ratio (Referred to the Output) vs Frequency



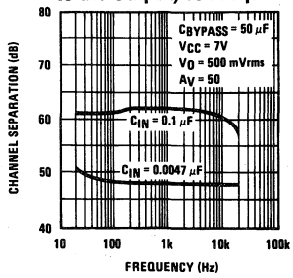
Power Supply Rejection Ratio (Referred to the Output) vs Supply Voltage



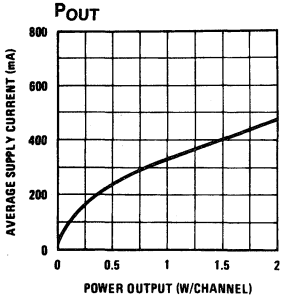
Channel Separation (Referred to the Output) vs Frequency



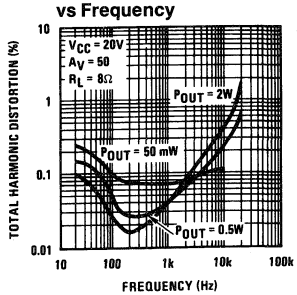
Channel Separation (Referred to the Output) vs Frequency



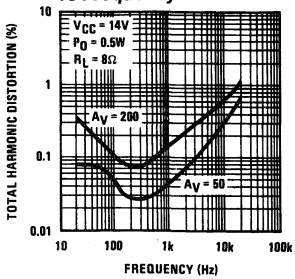
Average Supply Current vs POUT



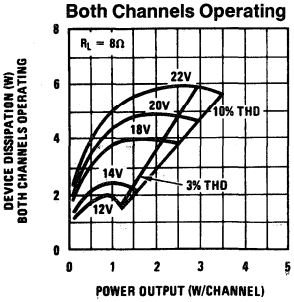
Total Harmonic Distortion vs Frequency



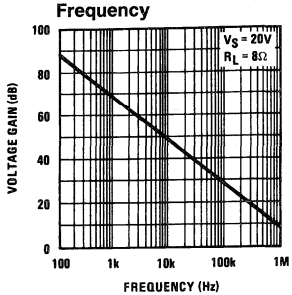
Total Harmonic Distortion vs Frequency



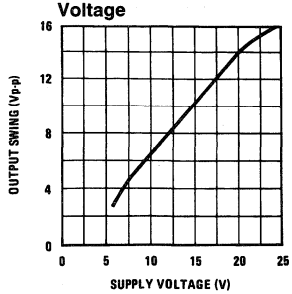
Power Dissipation (W) Both Channels Operating



Open Loop Gain vs Frequency



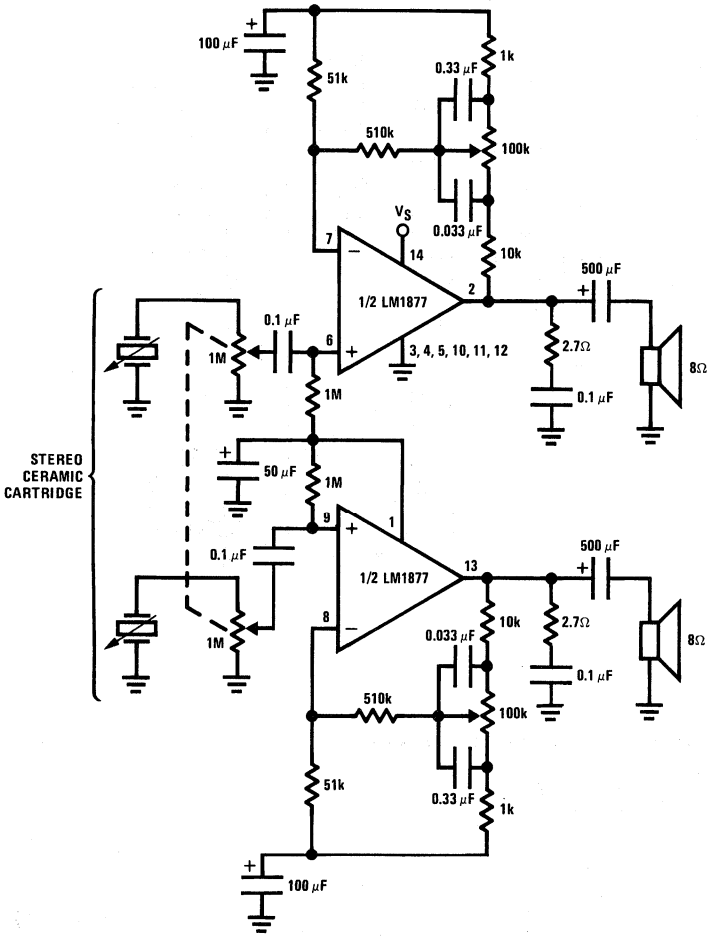
Output Swing vs Supply Voltage



TL/H/7913–3

Typical Applications

Stereo Phonograph Amplifier with Bass Tone Control



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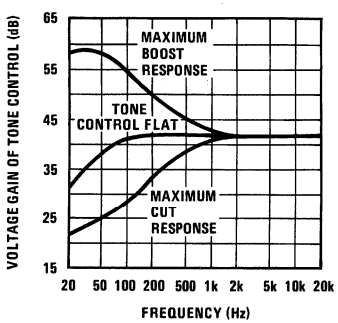
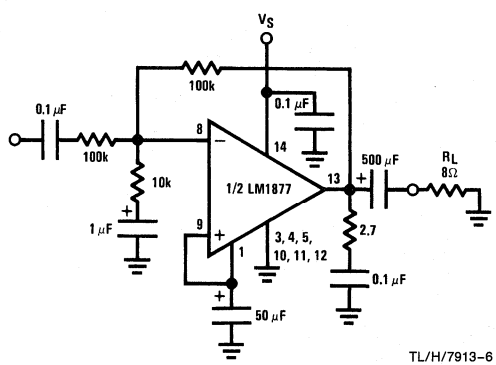
Frequency Response of Bass Tone Control



TL/H/7913–5

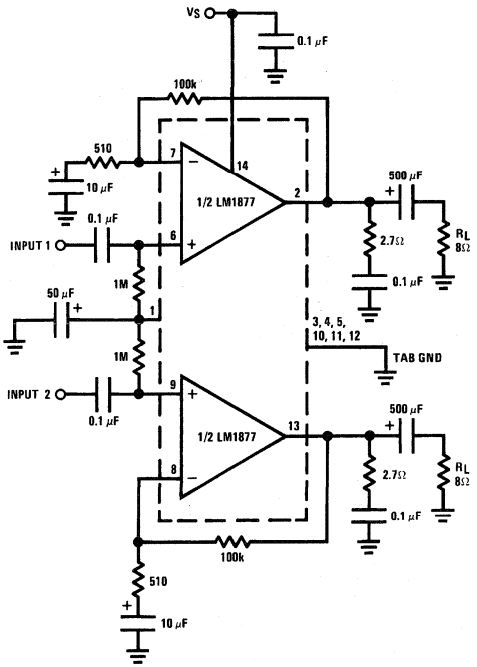
Inverting Unity Gain Amplifier



TL/H/7913–6

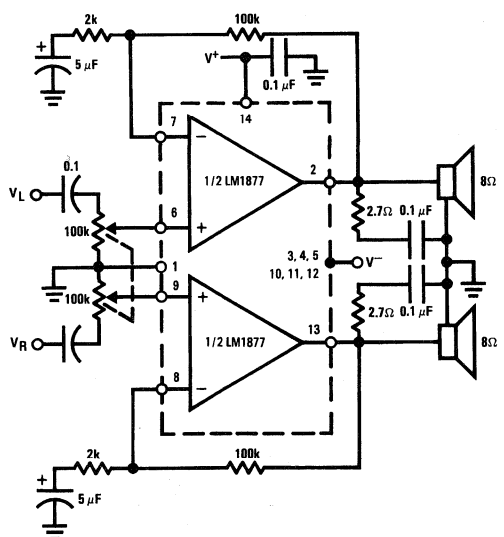
Typical Applications (Continued)

Stereo Amplifier with $A_V = 200$



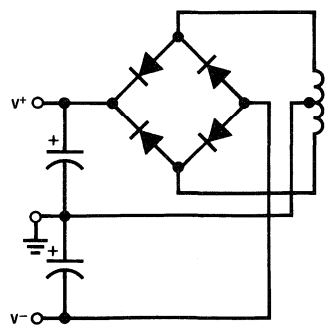
TL/H/7913–7

Non-Inverting Amplifier Using Split Supply



TL/H/7913–8

Typical Split Supply



TL/H/7913–9

National Semiconductor

LM2877 Dual 4-Watt Power Audio Amplifier

General Description

The LM2877 is a monolithic dual power amplifier designed to deliver 4W/channel continuous into 8Ω loads. The LM2877 is designed to operate with a low number of external components, and still provide flexibility for use in stereo phonographs, tape recorders and AM-FM stereo receivers, etc. Each power amplifier is biased from a common internal regulator to provide high power supply rejection and output Q point centering. The LM2877 is internally compensated for all gains greater than 10, and comes in an 11-lead single-in-line package.

Features

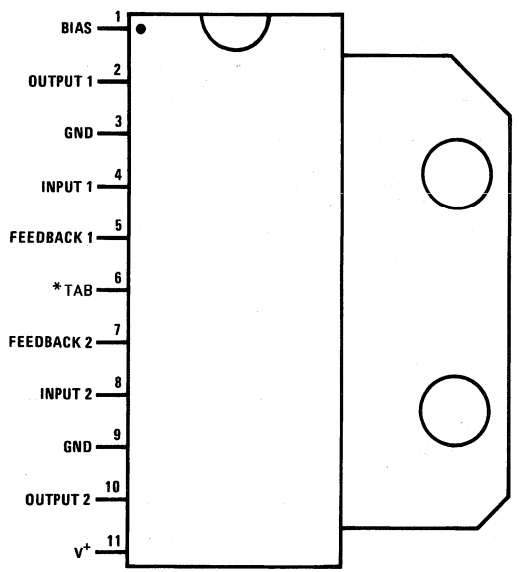
- 4W/channel
- −68 dB ripple rejection, output referred
- −70 dB channel separation, output referred
- Wide supply range, 6-24V
- Very low cross-over distortion
- Low audio band noise
- AC short circuit protected
- Internal thermal shutdown

Applications

- Multi-channel audio systems
- Stereo phonographs
- Tape recorders and players
- AM-FM radio receivers
- Servo amplifiers
- Intercom systems
- Automotive products

Connection Diagram

(Single-In-Line Package)



TL/H/7933–1

Top View

Order Number LM2877P
See NS Package Number P11A

*Pin 6 must be connected to GND.

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

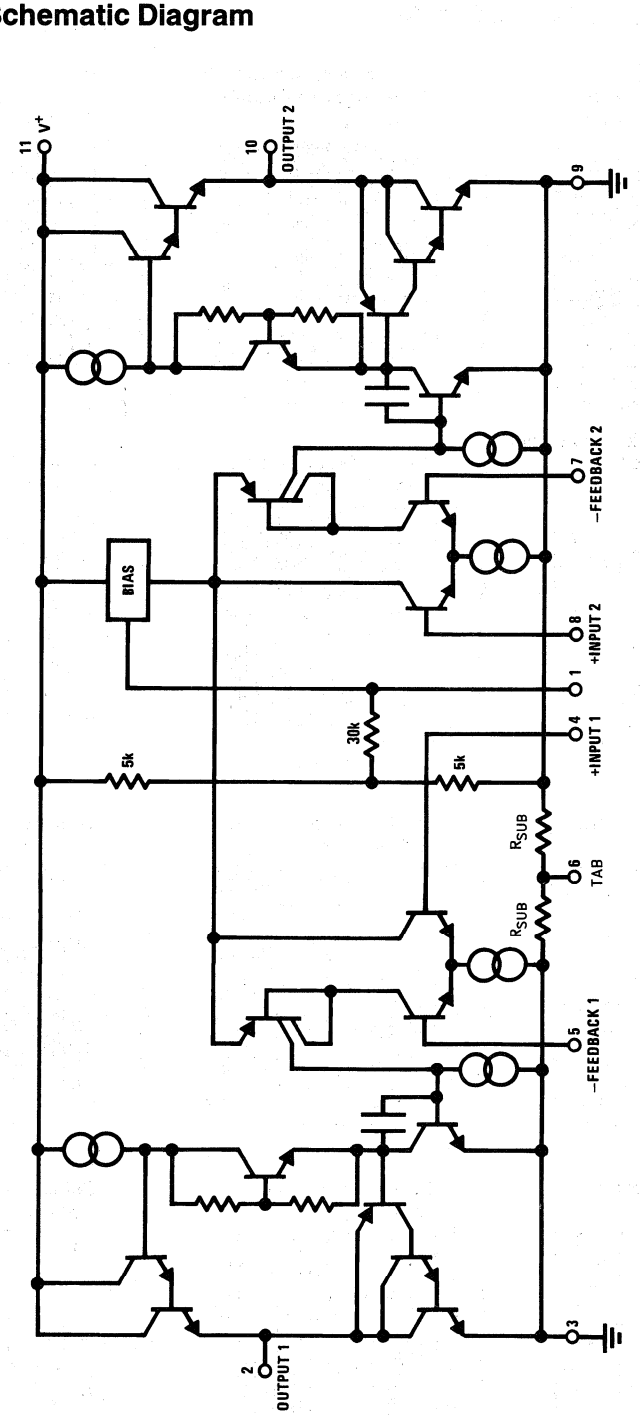
Supply Voltage	26V
Input Voltage	±0.7V
Operating Temperature	0°C to +70°C
Storage Temperature	−65°C to +150°C
Junction Temperature	150°C
Lead Temperature (Soldering, 10 sec.)	260°C

Electrical Characteristics V_S = 20V, T_{TAB} = 25°C, R_L = 8Ω, A_V = 50 (34 dB) unless otherwise specified.

Parameter	Conditions	Min	Typ	Max	Units
Total Supply Current	P_O = 0W		25	50	mA
Operating Supply Voltage		6		24	V
Output Power/Channel	f = 1 kHz, THD = 10%, T_{TAB} = 25°C				
	V_S = 20V	4.0	4.5		W
	V_S = 18V		3.6		W
	V_S = 12V, R_L = 4Ω	1.5	1.9		W
Distortion, THD	f = 1 kHz, V_S = 20V				
	P_O = 50 mW/Channel		0.1		%
	P_O = 1W/Channel		0.07	1	%
	P_O = 2W/Channel		0.07		%
	f = 1 kHz, V_S = 12V, R_L = 4Ω				
	P_O = 50 mW/Channel		0.25		%
	P_O = 500 mW/Channel		0.20		%
	P_O = 1W/Channel		0.15	1	%
Output Swing	R_L = 8Ω		V_S−4		V_{p-p}
Channel Separation	C_F = 50 μF, C_{IN} = 0.1 μF, f = 1 kHz, Output Referred				
	V_S = 20V, V_O = 4 Vrms	−50	−70		dB
	V_S = 7V, V_O = 0.5 Vrms		−60		dB
PSRR Power Supply	C_F = 50 μF, C_{IN} = 0.1 μF, f = 120 Hz				
Rejection Ratio	Output Referred				
	V_S = 20V, V_{RIPPLE} = 1 Vrms	−50	−68		dB
	V_S = 7V, V_{RIPPLE} = 0.5 Vrms		−40		dB
Noise	Equivalent Input Noise				
	R_S = 0, C_{IN} = 0.1 μF, BW = 20 Hz–20 kHz		2.5		μV
	Output Noise Wideband				
	R_S = 0, C_{IN} = 0.1 μF, A_V = 200		0.80		mV
Open Loop Gain	R_S = 0, f = 1 kHz, R_L = 8Ω		70		dB
Input Offset Voltage			15		mV
Input Bias Current			50		nA
Input Impedance	Open Loop		4		MΩ
DC Output Level	V_S = 20V	9	10	11	V
Slew Rate			2.0		V/μs
Power Bandwidth			65		kHz
Current Limit			1.0		A

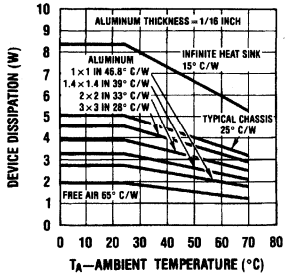
Note 1: For operation at ambient temperature greater than 25°C, the LM2877 must be derated based on a maximum 150°C junction temperature using a thermal resistance which depends upon device mounting techniques.

Equivalent Schematic Diagram

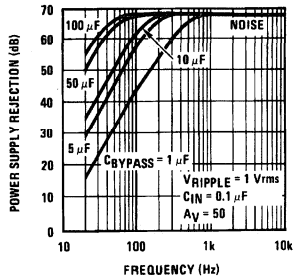


Typical Performance Characteristics

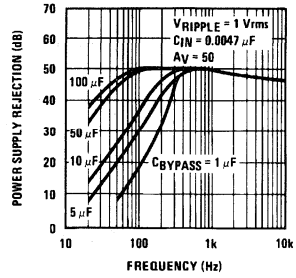
Device Dissipation vs Ambient Temperature



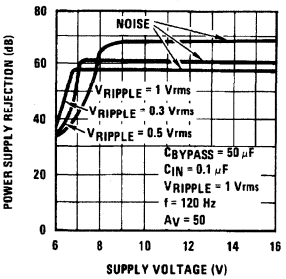
Power Supply Rejection Ratio (Referred to the Output) vs Frequency



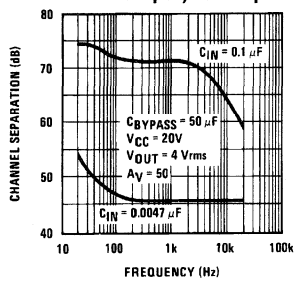
Power Supply Rejection Ratio (Referred to the Output) vs Frequency



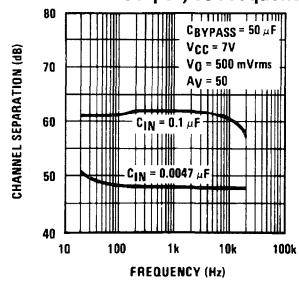
Power Supply Rejection Ratio (Referred to the Output) vs Supply Voltage



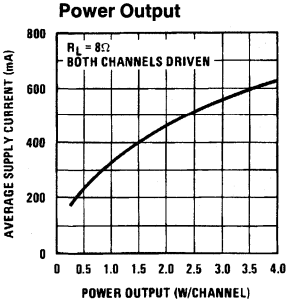
Channel Separation (Referred to the Output) vs Frequency



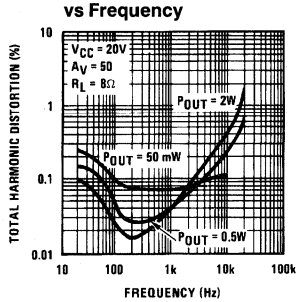
Channel Separation (Referred to the Output) vs Frequency



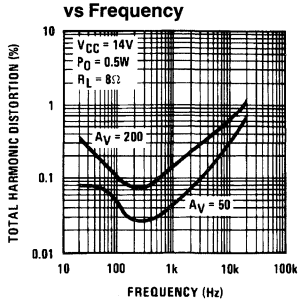
Average Supply Current vs Power Output



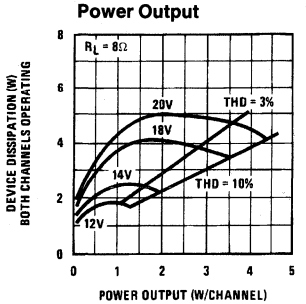
Total Harmonic Distortion vs Frequency



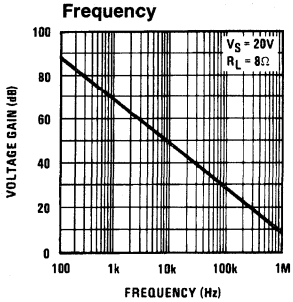
Total Harmonic Distortion vs Frequency



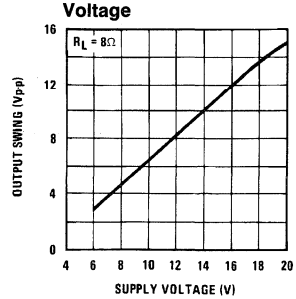
Power Dissipation vs Power Output



Open Loop Gain vs Frequency



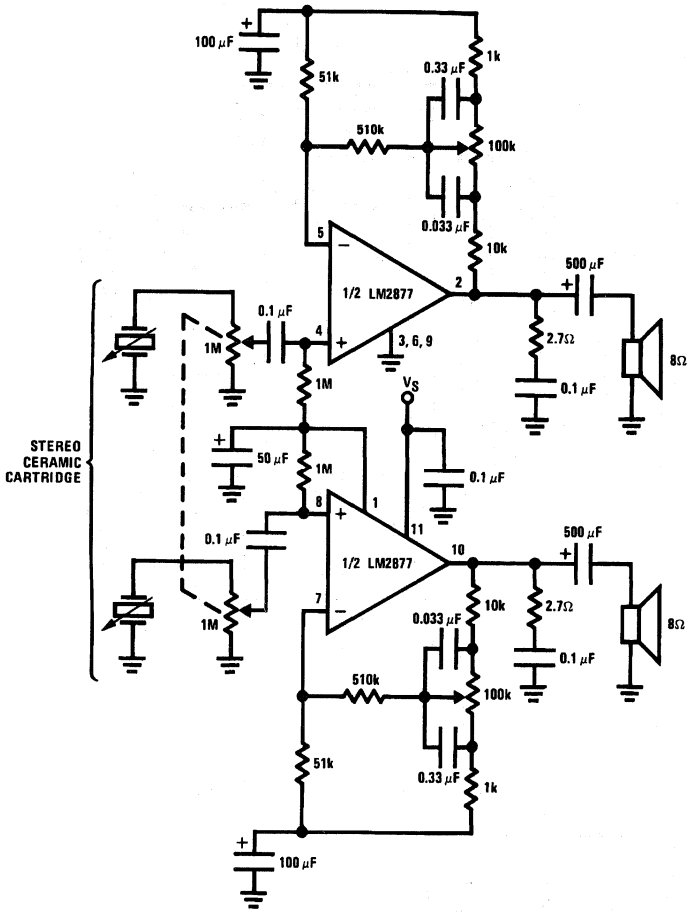
Output Swing vs Supply Voltage



TL/H/7933–3

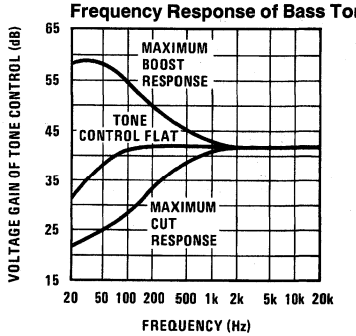
Typical Applications

Stereo Phonograph Amplifier with Bass Tone Control



TL/H/7933–4

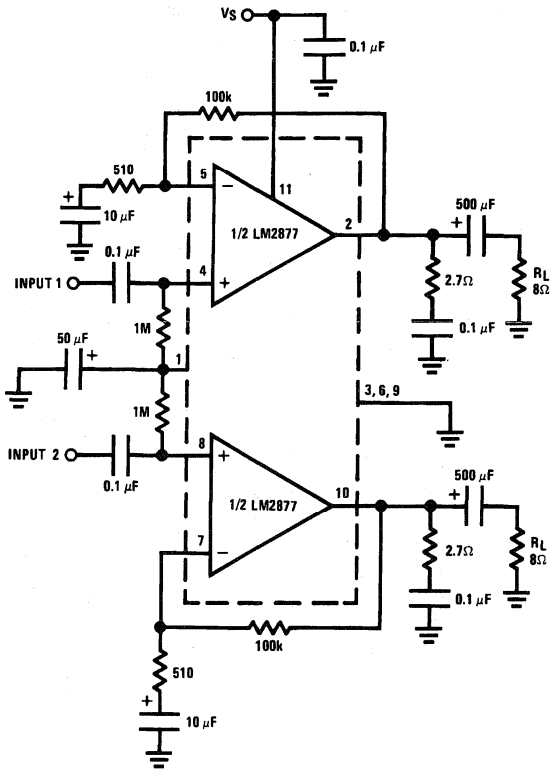
Frequency Response of Bass Tone Control



TL/H/7933–5

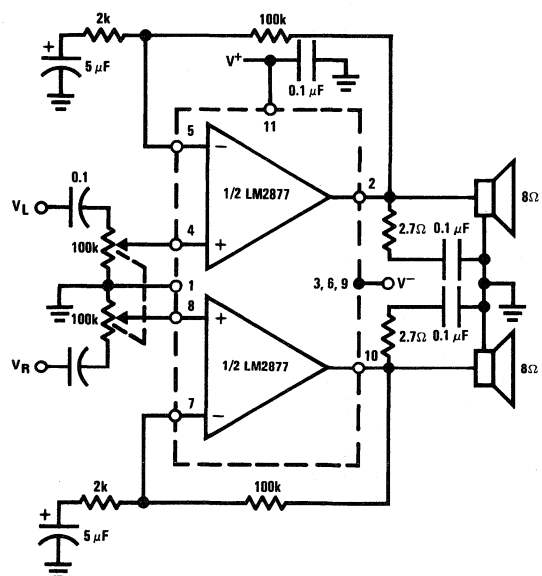
Typical Applications (Continued)

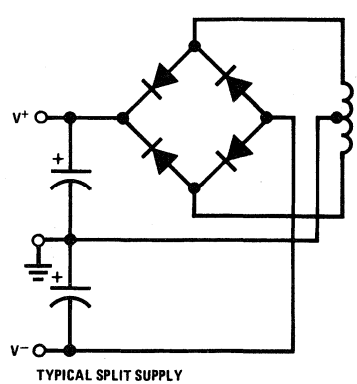
Stereo Amplifier with $A_V = 200$



TL/H/7933–6

Non-Inverting Amplifier Using Split Supply



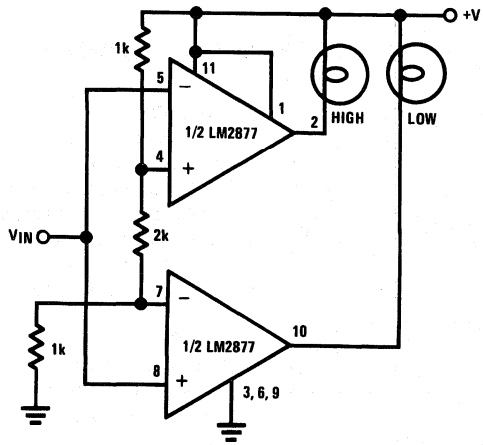


TYPICAL SPLIT SUPPLY

TL/H/7933–7

Typical Applications (Continued)

Window Comparator Driving High, Low Lamps



TL/H/7933–8

Truth Table

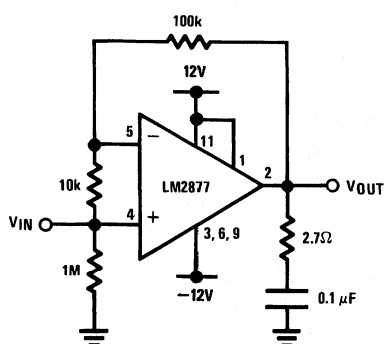
V_{IN}	High	Low
$<1/4\ V^+$	Off	On
$1/4\ V^+$ to $3/4\ V^+$	Off	Off
$>3/4\ V^+$	On	Off

Application Hints

The LM2877 is an improved LM377 in typical audio applications. In the LM2877, the internal voltage regulator for the input stage is generated from the voltage on pin 1. Normally, the input common-mode range is within ±0.7V of this pin 1 voltage. Nevertheless, the common-mode range can be increased by externally forcing the voltage on pin 1. One way to do this is to short pin 1 to the positive supply, pin 11.

The only special care required with the LM2877 is to limit the maximum input differential voltage to ±7V. If this differential voltage is exceeded, the input characteristics may change.

Figure 1 shows a power op amp application with $A_V = 1$. The 100k and 10k resistors set a noise gain of 10 and are dictated by amplifier stability. The 10k resistor is bootstrapped by the feedback so the input resistance is dominated by the 1 MΩ resistor.



TL/H/7933–9

FIGURE 1

National Semiconductor

LM2878 Dual 5 Watt Power Audio Amplifier

General Description

The LM2878 is a high voltage stereo power amplifier designed to deliver 5W/channel continuous into 8Ω loads. The amplifier is ideal for use with low regulation power supplies due to the absolute maximum rating of 35V and its superior power supply rejection. The LM2878 is designed to operate with a low number of external components, and still provide flexibility for use in stereo phonographs, tape recorders, and AM-FM stereo receivers. The flexibility of the LM2878 allows it to be used as a power operational amplifier, power comparator or servo amplifier. The LM2878 is internally compensated for all gains greater than 10, and comes in an 11-lead single-in-line package (SIP). The package has been redesigned, resulting in the slightly degraded thermal characteristics shown in the figure Device Dissipation vs Ambient Temperature.

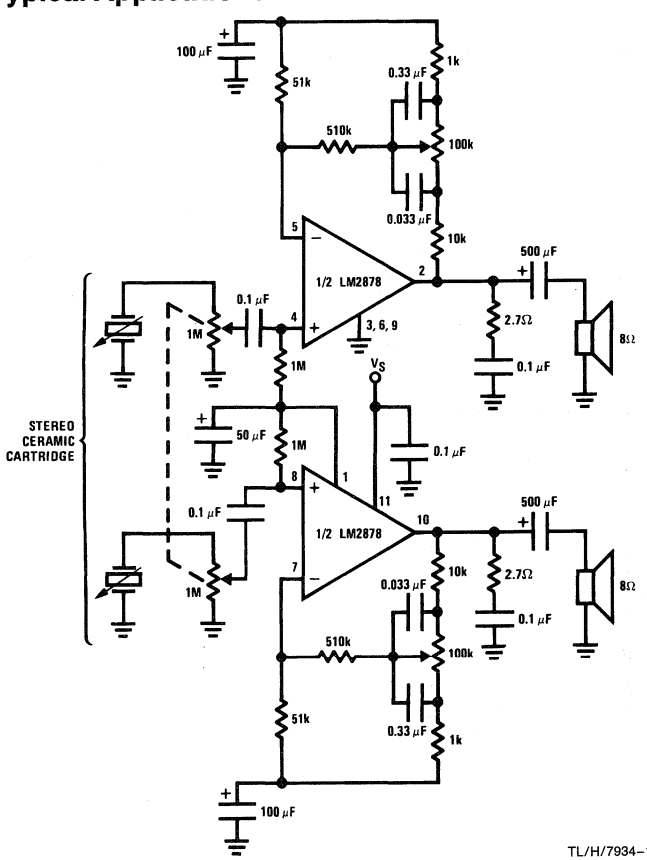
Features

- Wide operating range 6V–32V
- 5W/channel output
- 60 dB ripple rejection, output referred
- 70 dB channel separation, output referred
- Low crossover distortion
- AC short circuit protected
- Internal thermal shutdown

Applications

- Stereo phonographs
- AM-FM radio receivers
- Power op amp, power comparator
- Servo amplifiers

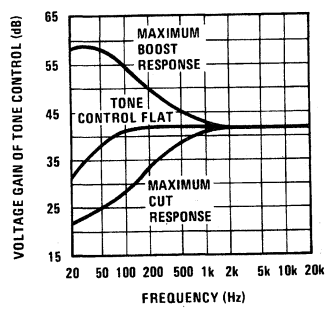
Typical Applications



TL/H/7934–1

FIGURE 1. Stereo Phonograph Amplifier with Bass Tone Control

Frequency Response of Bass Tone Control



TL/H/7934–2

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	35V
Input Voltage (Note 1)	±0.7V
Operating Temperature (Note 2)	0°C to +70°C
Storage Temperature	−65°C to +150°C
Junction Temperature	+150°C
Lead Temperature (Soldering, 10 sec.)	+260°C

Electrical Characteristics V_S = 22V, T_{TAB} = 25°C, R_L = 8Ω, A_V = 50 (34 dB) unless otherwise specified.

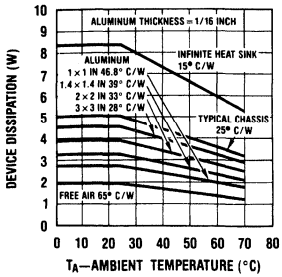
Parameter	Conditions	Min	Typ	Max	Units
Total Supply Current	P_O = 0W		10	50	mA
Operating Supply Voltage		6		32	V
Output Power/Channel	f = 1 kHz, THD = 10%, T_{TAB} = 25°C	5	5.5		W
Distortion	f = 1 kHz, R_L = 8Ω P_O = 50 mW		0.20		%
	P_O = 0.5W		0.15		%
	P_O = 2W		0.14		%
Output Swing	R_L = 8Ω		V_S − 6V		Vp-p
Channel Separation	C_{BYPASS} = 50 μF, C_{IN} = 0.1 μF f = 1 kHz, Output Referred V_O = 4 Vrms	−50	−70		dB
PSRR Power Supply Rejection Ratio	C_{BYPASS} = 50 μF, C_{IN} = 0.1 μF f = 120 Hz, Output Referred V_{ripple} = 1 Vrms	−50	−60		dB
PSRR Negative Supply	Measured at DC, Input Referred		−60		dB
Common-Mode Range	Split Supplies ±15V, Pin 1 Tied to Pin 11		±13.5		V
Input Offset Voltage			10		mV
Noise	Equivalent Input Noise R_S = 0, C_{IN} = 0.1 μF BW = 20 − 20 kHz		2.5		μV
	CCIR•ARM		3.0		μV
	Output Noise Wideband R_S = 0, C_{IN} = 0.1 μF, A_V = 200		0.8		mV
Open Loop Gain	R_S = 51Ω, f = 1 kHz, R_L = 8Ω		70		dB
Input Bias Current			100		nA
Input Impedance	Open Loop		4		MΩ
DC Output Voltage	V_S = 22V	10	11	12	V
Slew Rate			2		V/μS
Power Bandwidth	3 dB Bandwidth at 2.5W		65		kHz
Current Limit			1.5		A

Note 1: ±0.7V applies to audio applications; for extended range, see Application Hints.

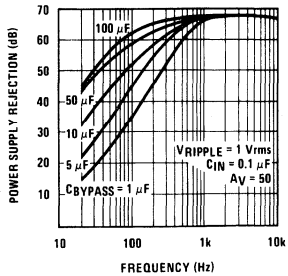
Note 2: For operation at ambient temperature greater than 25°C, the LM2878 must be derated based on a maximum 150°C junction temperature using a thermal resistance which depends upon device mounting techniques.

Typical Performance Characteristics

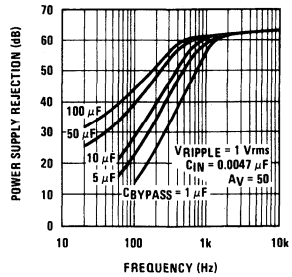
Device Dissipation vs Ambient Temperature



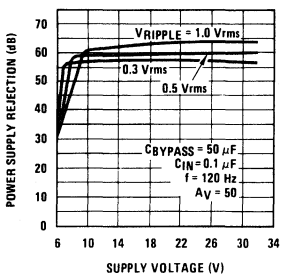
Power Supply Rejection Ratio (Referred to the Output) vs Frequency



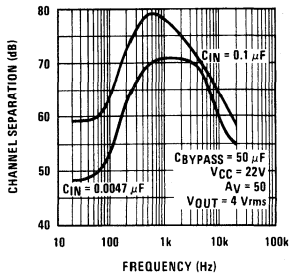
Power Supply Rejection Ratio (Referred to the Output) vs Frequency



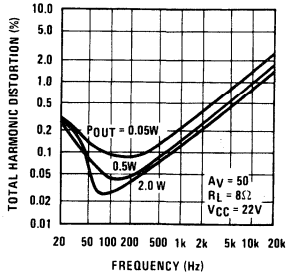
Power Supply Rejection Ratio (Referred to the Output) vs Supply Voltage



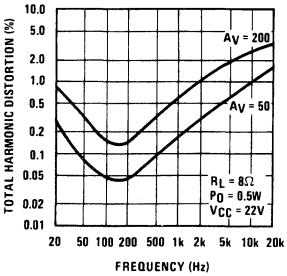
Channel Separation (Referred to the Output) vs Frequency



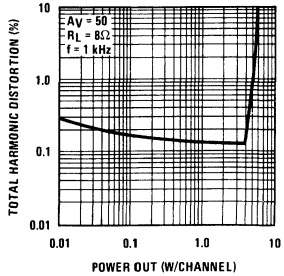
Total Harmonic Distortion vs Frequency



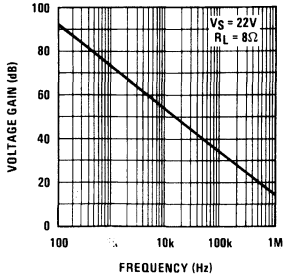
Total Harmonic Distortion vs Frequency



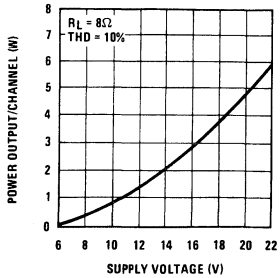
Total Harmonic Distortion vs Power Out



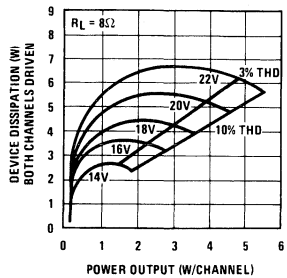
Open Loop Gain vs Frequency



Power Output/Channel vs Supply Voltage

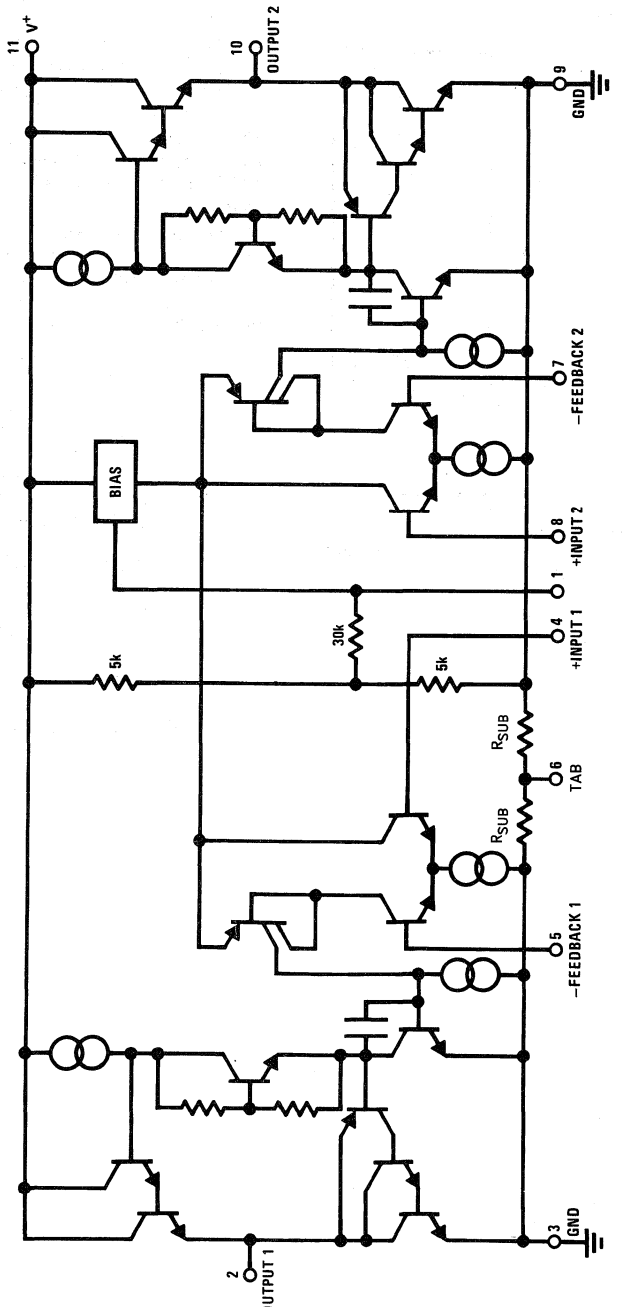


Power Dissipation vs Power Out



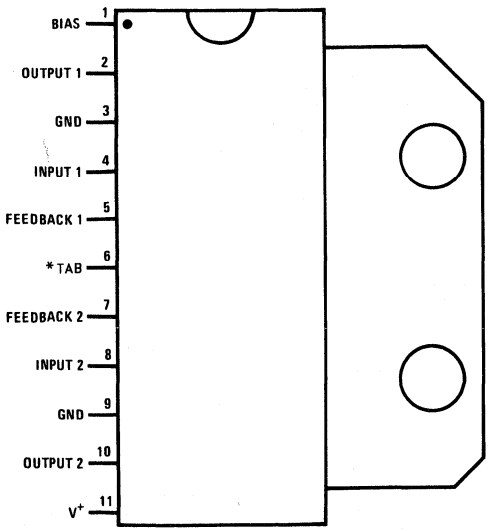
TL/H/7934–3

Equivalent Schematic Diagram



Connection Diagram

Single-In-Line Package



TL/H/7934–5

Top View

*Pin 6 must be connected to GND.

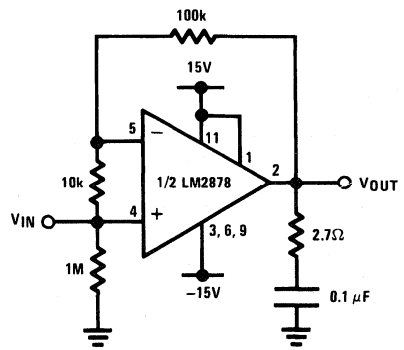
Order Number LM2878P
See NS Package Number P11A

Application Hints

The LM2878 is an improved LM378 in typical audio applications. In the LM2878, the internal voltage regulator for the input stage is generated from the voltage on pin 1. Normally, the input common-mode range is within ±0.7V of this pin 1 voltage. Nevertheless the common-mode range can be increased by externally forcing the voltage on pin 1. One way to do this is to short pin 1 to the positive supply, pin 11.

The only special care required with the LM2878 is to limit the maximum input differential voltage to ±7V. If this differential voltage is exceeded, the input characteristics may change.

Figure 2 shows a power op amp application with $A_V = 1$. The 100k and 10k resistors set a noise gain of 10 and are dictated by amplifier stability. The 10k resistor is bootstrapped by the feedback so the input resistance is dominated by the 1 MΩ resistor.



TL/H/7934–6

FIGURE 2. Operational Power Amplifier, $A_V = 1$

External Components *(Figure 3)*

1. R2, R5, R7, R10 Sets voltage gain $A_V = 1 + R2/R5$ for one channel and $A_V = 1 + R10/R7$ for the other channel.
2. R4, R8 Resistors set input impedance and supply bias current for the positive input.
3. R_O Works with C_O to stabilize output stage.
4. C1 Improves power supply rejection (see Typical Performance Characteristics).
5. C11 Stabilizes amplifier, may need to be larger depending on power supply filtering.
6. C4, C8 Input coupling capacitor. Pins 4 and 8 are at a DC potential of $V_S/2$. Low frequency pole set by:

$$f_L = \frac{1}{2\pi R4C4}$$

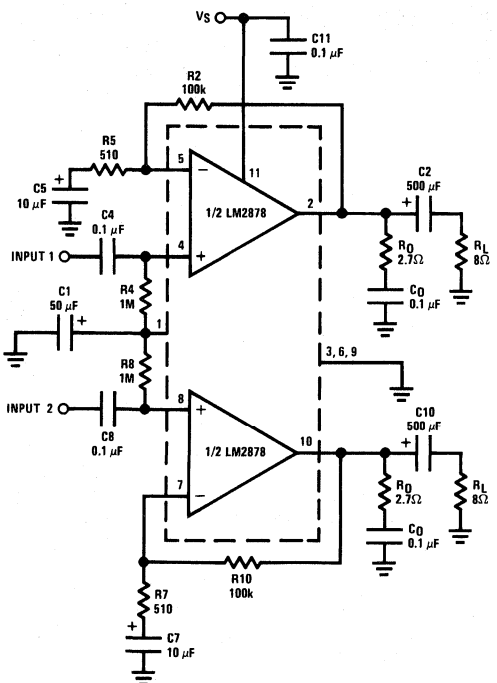
7. C5, C7 Feedback capacitors. Ensure unity gain at DC. Also low frequency pole at:

$$f_L = \frac{1}{2\pi R5C5}$$

8. C_O Works with R_O to stabilize output stage.
9. C2, C10 Output coupling capacitor. Low frequency pole given by:

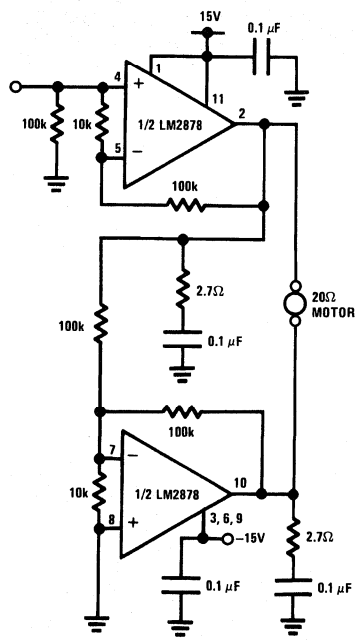
$$f_L = \frac{1}{R\pi RLC2}$$

Typical Applications (Continued)



TL/H/7934–7

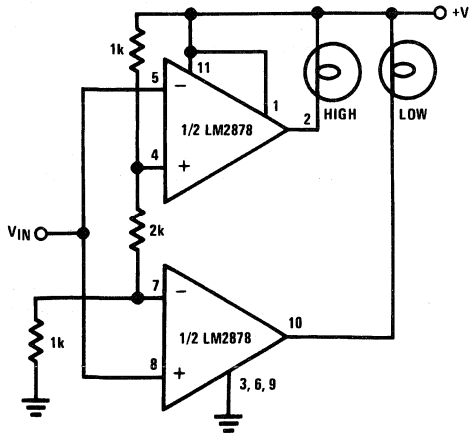
FIGURE 3. Stereo Amplifier with $A_V = 200$



TL/H/7934–8

FIGURE 4. LM2878 Servo Amplifier in Bridge Configuration

Typical Applications (Continued)



TL/H/7934–9

FIGURE 5. Window Comparator Driving High, Low Lamps

Truth Table

V_{IN}	High	Low
$<1/4V^+$	Off	On
$1/4V^+$ to $3/4V^+$	Off	Off
$>3/4V^+$	On	Off

National Semiconductor

LM2879 Dual 8-Watt Audio Amplifier

General Description

The LM2879 is a monolithic dual power amplifier which offers high quality performance for stereo phonographs, tape players, recorders, AM-FM stereo receivers, etc.

The LM2879 will deliver 8W/channel to an 8Ω load. The amplifier is designed to operate with a minimum of external components and contains an internal bias regulator to bias each amplifier. Device overload protection consists of both internal current limit and thermal shutdown.

Features

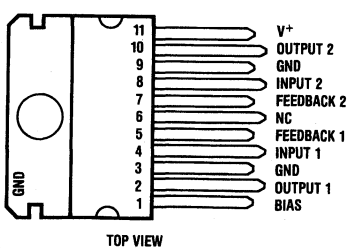
- A_{VO} typical 90 dB
- 9W per channel (typical)
- 60 dB ripple rejection
- 70 dB channel separation
- Self-centering biasing
- 4 MΩ input impedance
- Internal current limiting
- Internal thermal protection

Applications

- Multi-channel audio systems
- Tape recorders and players
- Movie projectors
- Automotive systems
- Stereo phonographs
- Bridge output stages
- AM-FM radio receivers
- Intercoms
- Servo amplifiers
- Instrument systems

Connection Diagram and Typical Application

Plastic Package

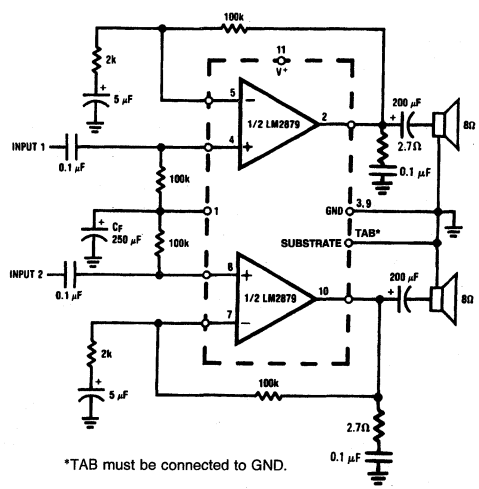


TOP VIEW

TL/H/5291–1

Order Number LM2879T
See NS Package Number TA11B

Stereo Amplifier



*TAB must be connected to GND.

TL/H/5291–2

FIGURE 1

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	35V
Input Voltage (Note 1)	±0.7V
Operating Temperature (Note 2)	0°C to + 70°C
Storage Temperature	−65°C to +150°C
Junction Temperature	150°C
Lead Temp. (Soldering, 10 seconds)	260°C
ESD rating to be determined.	

Electrical Characteristics $V_S = 28V$, $T_{TAB} = 25°C$, $R_L = 8\Omega$, $A_V = 50$ (34 dB), unless otherwise specified.

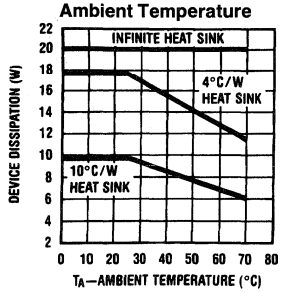
Parameter	Conditions	Min	Typ	Max	Units
Total Supply Current	$P_O = 0W$		12	65	mA
Operating Supply Voltage		6		32	V
Output Power/Channel	f = 1 kHz, THD = 10%, $T_{TAB} = 25°C$	6	8		W
Distortion	f = 1 kHz, $R_L = 8\Omega$ $P_O = 1$ W/Channel		0.05	1	%
Output Swing	$R_L = 8\Omega$		$V_S - 6V$		Vp-p
Channel Separation	$C_{BYPASS} = 50\ \mu F$, $C_{IN} = 0.1\ \mu F$ f = 1 kHz, Output Referred $V_O = 4$ Vrms	−50	−70		dB
PSRR Positive Supply	$C_{BYPASS} = 50\ \mu F$, $C_{IN} = 0.1\ \mu F$ f = 120 Hz, Output Referred $V_{ripple} = 1$ Vrms	−50	−60		dB
PSRR Negative Supply	Measured at DC, Input Referred		−60		dB
Common-Mode Range	Split Supplies ±15V, Pin 1 Tied to Pin 11		±13.5		V
Input Offset Voltage			10		mV
Noise	Equivalent Input Noise $R_S = 0$, $C_{IN} = 0.1\ \mu F$ BW = 20 − 20 kHz CCIR•ARM Output Noise Wideband $R_S = 0$, $C_{IN} = 0.1\ \mu F$, $A_V = 200$		 2.5 3.0 0.8		 μV μV mV
Open Loop Gain	$R_S = 51\Omega$, f = 1 kHz, $R_L = 8\Omega$		70		dB
Input Bias Current			100		nA
Input Impedance	Open Loop		4		MΩ
DC Output Voltage	$V_S = 28V$		14		V
Slew Rate			2		V/μs
Power Bandwidth	3 dB Bandwidth at 2.5W		65		kHz
Current Limit			1.5		A

Note 1: The input voltage range is normally limited to ±0.7V with respect to pin 1. This range may be extended by shorting pin 1 to the positive supply.

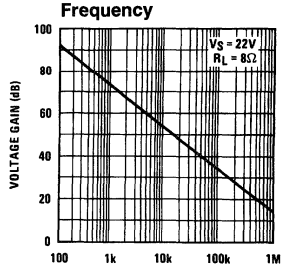
Note 2: For operation at ambient temperature greater than 25°C, the LM2879 must be derated based on a maximum 150°C junction temperature. Thermal resistance, junction to case, is 3°C/W. Thermal resistance, case to ambient, is 40°C/W.

Typical Performance Characteristics

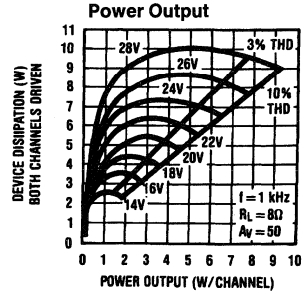
Device Dissipation vs Ambient Temperature



Open Loop Gain vs Frequency



Power Dissipation vs Power Output



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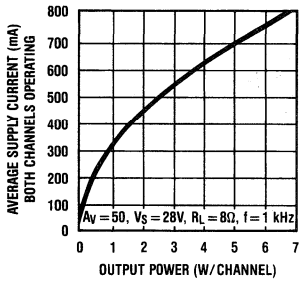
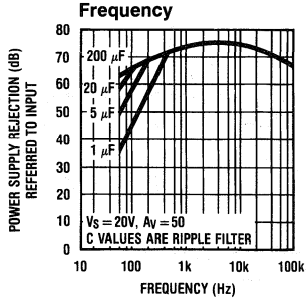
Typical Performance Characteristics (Continued)

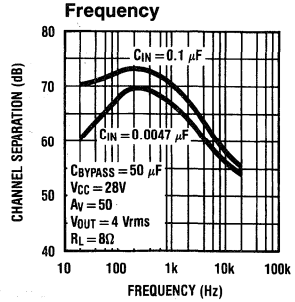
Supply Current vs Output Power



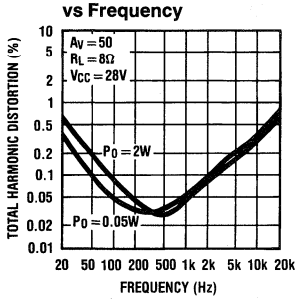
Supply Rejection vs Frequency



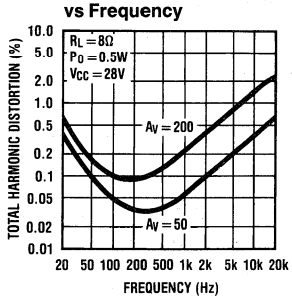
Channel Separation (Referred to the Output) Frequency



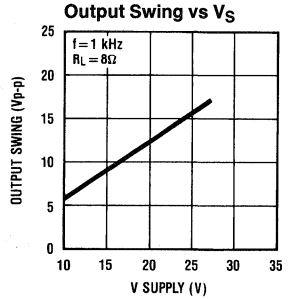
Total Harmonic Distortion vs Frequency



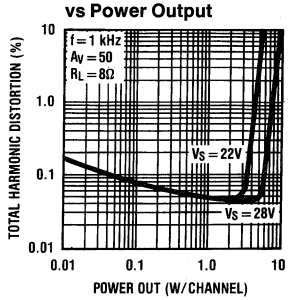
Total Harmonic Distortion vs Frequency



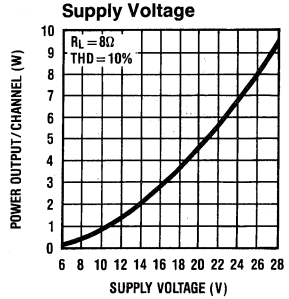
Output Swing vs V_S



Total Harmonic Distortion vs Power Output

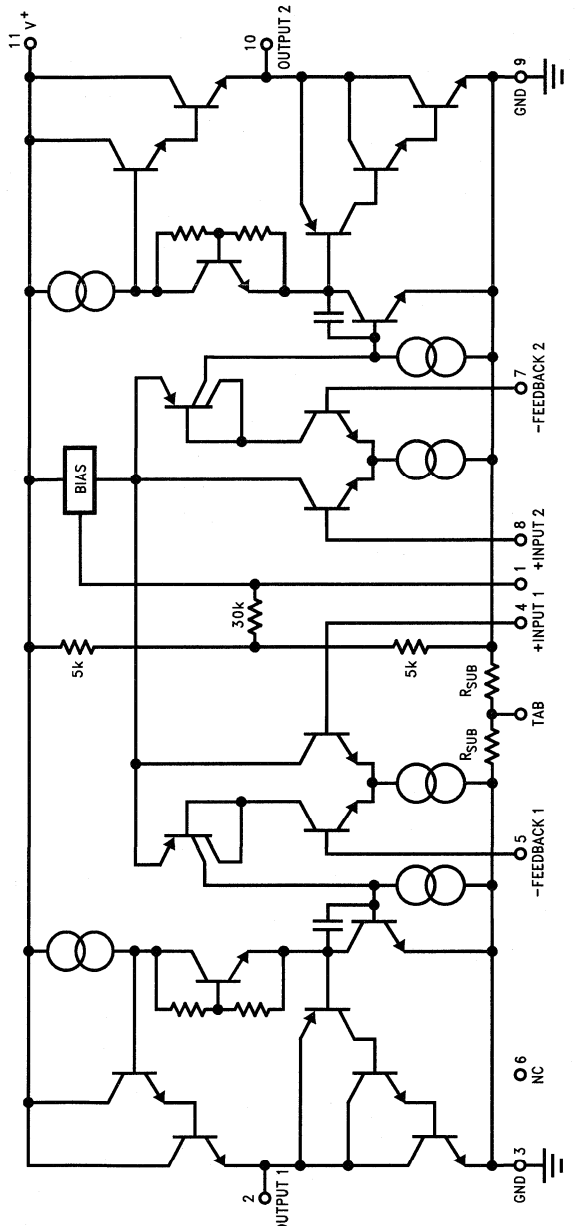


Power Output/Channel vs Supply Voltage



TL/H/5291–4

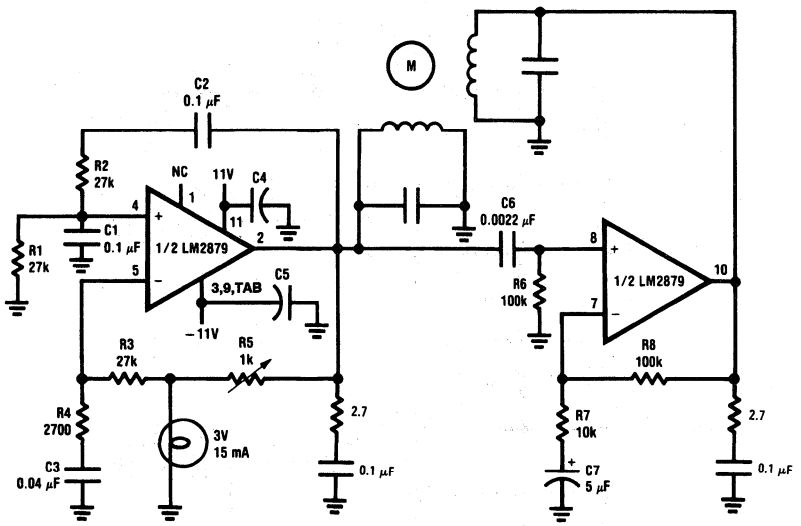
Equivalent Schematic Diagram



TL/H/5291–5

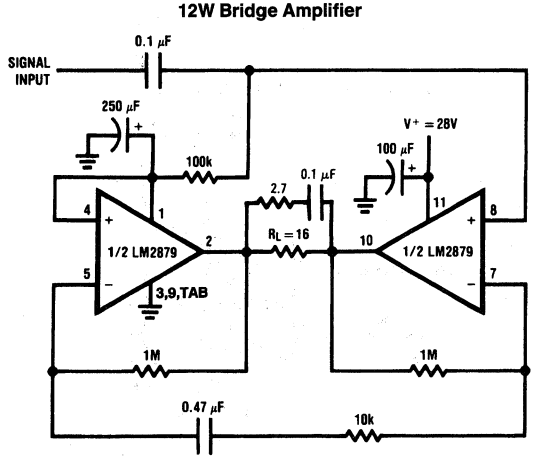
Typical Applications

Two-Phase Motor Drive



TL/H/5291–6

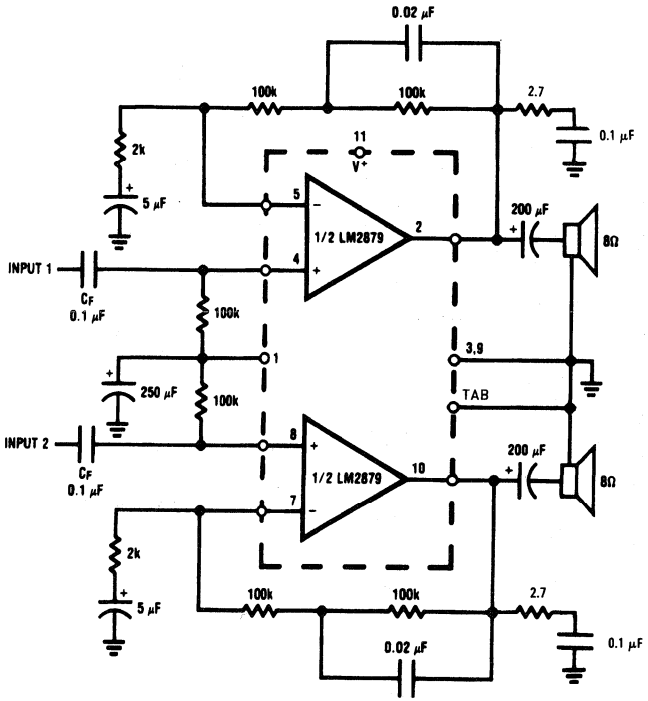
12W Bridge Amplifier



TL/H/5291–7

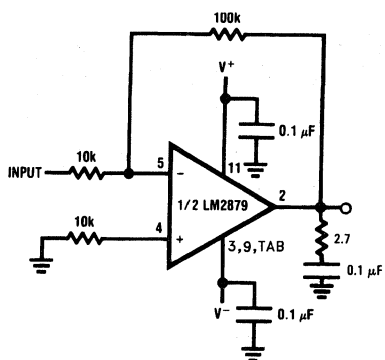
Typical Applications (Continued)

Simple Stereo Amplifier with Bass Boost



TL/H/5291–8

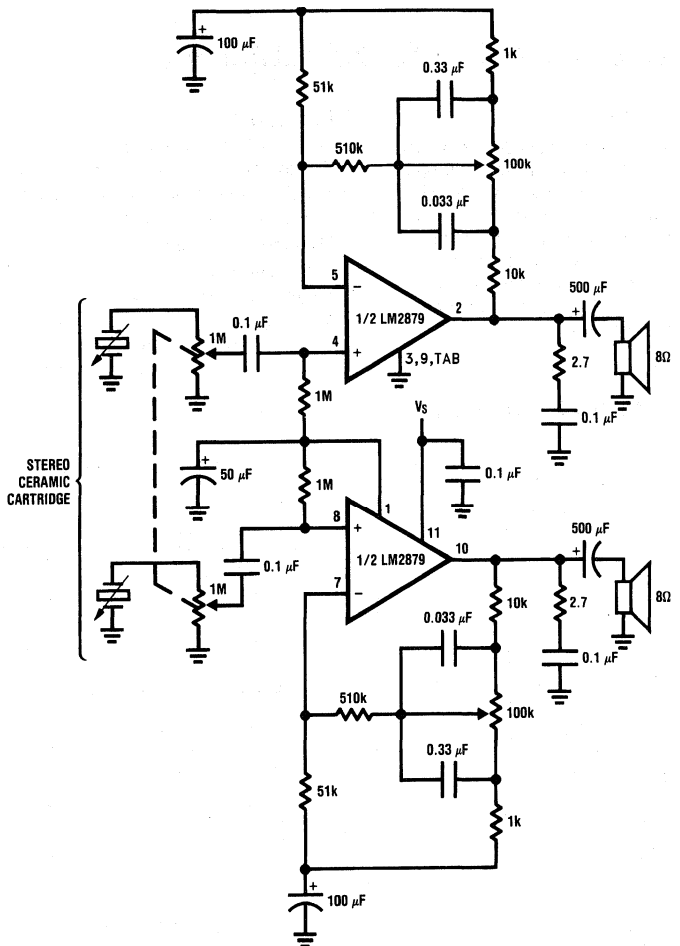
Power Op Amp (Using Split Supplies)



TL/H/5291–9

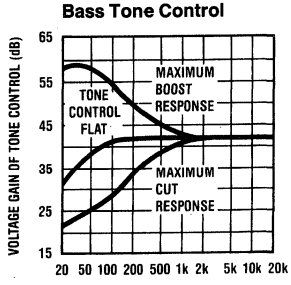
Typical Applications (Continued)

Stereo Phonograph Amplifier with Bass Tone Control



TL/H/5291–10

Frequency Response of Bass Tone Control



TL/H/5291–11

National Semiconductor

LM2900/LM3900/LM3301 Quad Amplifiers

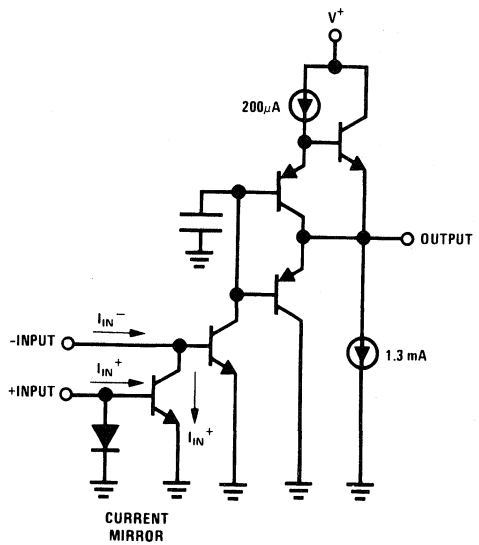
General Description

The LM2900 series consists of four independent, dual input, internally compensated amplifiers which were designed specifically to operate off of a single power supply voltage and to provide a large output voltage swing. These amplifiers make use of a current mirror to achieve the non-inverting input function. Application areas include: ac amplifiers, RC active filters, low frequency triangle, squarewave and pulse waveform generation circuits, tachometers and low speed, high voltage digital logic gates.

Features

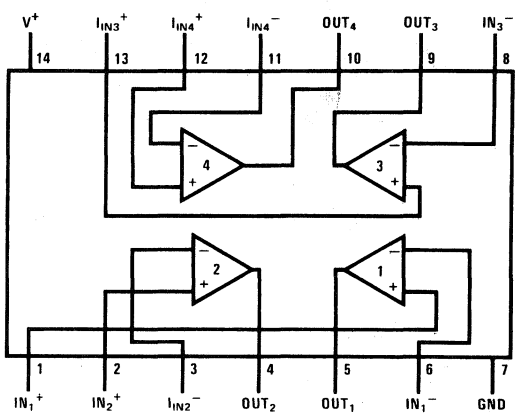
- Wide single supply voltage — 4 V_{DC} to 32 V_{DC}
  Range or dual supplies — ±2 V_{DC} to ±16 V_{DC}
- Supply current drain independent of supply voltage
- Low input biasing current — 30 nA
- High open-loop gain — 70 dB
- Wide bandwidth — 2.5 MHz (unity gain)
- Large output voltage swing — (V^+ − 1) Vp-p
- Internally frequency compensated for unity gain
- Output short-circuit protection

Schematic and Connection Diagrams



TL/H/7936–1

Dual-In-Line and S.O.



TL/H/7936–2

Top View

Order Number LM2900N, LM3900M, LM3900N or LM3301N
See NS Package Number M14A or N14A

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

	LM2900/LM3900	LM3301
Supply Voltage	32 V_{DC} ±16 V_{DC}	28 V_{DC} ±14 V_{DC}
Power Dissipation (T_A = 25°C) (Note 1)		
Molded DIP	1080 mW	1080 mW
S.O. Package	765 mW	
Input Currents, I_{IN}^+ or I_{IN}^-	20 mA_{DC}	20 mA_{DC}
Output Short-Circuit Duration—One Amplifier T_A = 25°C (See Application Hints)	Continuous	Continuous
Operating Temperature Range		−40°C to +85°C
LM2900	−40°C to +85°C	
LM3900	0°C to +70°C	
Storage Temperature Range	−65°C to +150°C	−65°C to +150°C
Lead Temperature (Soldering, 10 sec.)	260°C	260°C
Soldering Information		
Dual-In-Line Package		
Soldering (10 sec.)	260°C	260°C
Small Outline Package		
Vapor Phase (60 sec.)	215°C	215°C
Infrared (15 sec.)	220°C	220°C

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

ESD tolerance (Note 7)	2000V	2000V

Electrical Characteristics T_A = 25°C, V^+ = 15 V_{DC}, unless otherwise stated

Parameter		Conditions		LM2900			LM3900			LM3301			Units
				Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Open Loop	Voltage Gain	Over Temp.											V/mV
	Voltage Gain	ΔV_O = 10 V_{DC} Inverting Input		1.2	2.8		1.2	2.8		1.2	2.8		
	Input Resistance				1			1			1		MΩ
	Output Resistance				8			8			9		kΩ
Unity Gain Bandwidth		Inverting Input			2.5			2.5			2.5		MHz
Input Bias Current		Inverting Input, V^+ = 5 V_{DC} Inverting Input			30	200		30	200		30	300	nA
Slew Rate		Positive Output Swing			0.5			0.5			0.5		V/μs
		Negative Output Swing			20			20			20		
Supply Current		R_L = ∞ On All Amplifiers			6.2	10		6.2	10		6.2	10	mA_{DC}
Output Voltage Swing	V_{OUT} High	R_L = 2k, V^+ = 15.0 V_{DC}	I_{IN}^- = 0, I_{IN}^+ = 0	13.5			13.5			13.5			V_{DC}
	V_{OUT} Low		I_{IN}^- = 10 μA, I_{IN}^+ = 0		0.09	0.2		0.09	0.2		0.09	0.2	
	V_{OUT} High	V^+ = Absolute Maximum Ratings	I_{IN}^- = 0, I_{IN}^+ = 0 R_L = ∞,	29.5			29.5			26.0			
Output Current Capability	Source			6	18		6	10		5	18		mA_{DC}
	Sink	(Note 2)		0.5	1.3		0.5	1.3		0.5	1.3		
	I_{SINK}	V_{OL} = 1V, I_{IN}^- = 5 μA			5			5			5		

Electrical Characteristics (Note 6), $V^+ = 15\ V_{DC}$, unless otherwise stated (Continued)

Parameter	Conditions	LM2900			LM3900			LM3301			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Power Supply Rejection	$T_A = 25°C$, f = 100 Hz		70			70			70		dB
Mirror Gain	@ 20 μA (Note 3)	0.90	1.0	1.1	0.90	1.0	1.1	0.90	1	1.10	μA/μA
	@ 200 μA (Note 3)	0.90	1.0	1.1	0.90	1.0	1.1	0.90	1	1.10	
ΔMirror Gain	@ 20 μA to 200 μA (Note 3)		2	5		2	5		2	5	%
Mirror Current	(Note 4)		10	500		10	500		10	500	μA_{DC}
Negative Input Current	$T_A = 25°C$ (Note 5)		1.0			1.0			1.0		mA_{DC}
Input Bias Current	Inverting Input		300			300					nA

Note 1: For operating at high temperatures, the device must be derated based on a 125°C maximum junction temperature and a thermal resistance of 92°C/W which applies for the device soldered in a printed circuit board, operating in a still air ambient. Thermal resistance for the S.O. package is 131°C/W.

Note 2: The output current sink capability can be increased for large signal conditions by overdriving the inverting input. This is shown in the section on Typical Characteristics.

Note 3: This spec indicates the current gain of the current mirror which is used as the non-inverting input.

Note 4: Input V_{BE} match between the non-inverting and the inverting inputs occurs for a mirror current (non-inverting input current) of approximately 10 μA. This is therefore a typical design center for many of the application circuits.

Note 5: Clamp transistors are included on the IC to prevent the input voltages from swinging below ground more than approximately $-0.3\ V_{DC}$. The negative input currents which may result from large signal overdrive with capacitance input coupling need to be externally limited to values of approximately 1 mA. Negative input currents in excess of 4 mA will cause the output voltage to drop to a low voltage. This maximum current applies to any one of the input terminals. If more than one of the input terminals are simultaneously driven negative smaller maximum currents are allowed. Common-mode current biasing can be used to prevent negative input voltages; see for example, the "Differentiator Circuit" in the applications section.

Note 6: These specs apply for $-40°C \leq T_A \leq +85°C$, unless otherwise stated.

Note 7: Human body model, 1.5 kΩ in series with 100 pF.

Application Hints

When driving either input from a low-impedance source, a limiting resistor should be placed in series with the input lead to limit the peak input current. Currents as large as 20 mA will not damage the device, but the current mirror on the non-inverting input will saturate and cause a loss of mirror gain at mA current levels—especially at high operating temperatures.

Precautions should be taken to insure that the power supply for the integrated circuit never becomes reversed in polarity or that the unit is not inadvertently installed backwards in a test socket as an unlimited current surge through the resulting forward diode within the IC could cause fusing of the internal conductors and result in a destroyed unit.

Output short circuits either to ground or to the positive power supply should be of short time duration. Units can be destroyed, not as a result of the short circuit current causing metal fusing, but rather due to the large increase in IC chip dissipation which will cause eventual failure due to excessive junction temperatures. For example, when operating from a well-regulated $+5\ V_{DC}$ power supply at $T_A = 25°C$ with a 100 kΩ shunt-feedback resistor (from the output to the inverting input) a short directly to the power supply will not cause catastrophic failure but the current magnitude will be approximately 50 mA and the junction temperature will be above T_J max. Larger feedback resistors will reduce the current, 11 MΩ provides approximately 30 mA, an open circuit provides 1.3 mA, and a direct connection from the output to the non-inverting input will result in catastrophic failure when the output is shorted to V^+ as this then places the base-emitter junction of the input transistor directly across the power supply. Short-circuits to ground will have magnitudes of approximately 30 mA and will not cause catastrophic failure at $T_A = 25°C$.

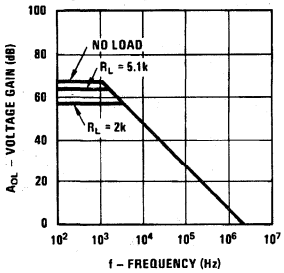
Unintentional signal coupling from the output to the non-inverting input can cause oscillations. This is likely only in breadboard hook-ups with long component leads and can be prevented by a more careful lead dress or by locating the non-inverting input biasing resistor close to the IC. A quick check of this condition is to bypass the non-inverting input to ground with a capacitor. High impedance biasing resistors used in the non-inverting input circuit make this input lead highly susceptible to unintentional AC signal pickup.

Operation of this amplifier can be best understood by noticing that input currents are differenced at the inverting-input terminal and this difference current then flows through the external feedback resistor to produce the output voltage. Common-mode current biasing is generally useful to allow operating with signal levels near ground or even negative as this maintains the inputs biased at $+V_{BE}$. Internal clamp transistors (see note 5) catch-negative input voltages at approximately $-0.3\ V_{DC}$ but the magnitude of current flow has to be limited by the external input network. For operation at high temperature, this limit should be approximately 100 μA.

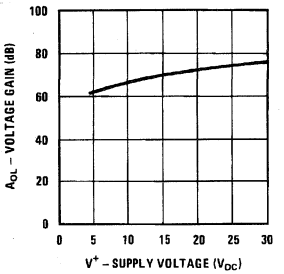
This new "Norton" current-differencing amplifier can be used in most of the applications of a standard IC op amp. Performance as a DC amplifier using only a single supply is not as precise as a standard IC op amp operating with split supplies but is adequate in many less critical applications. New functions are made possible with this amplifier which are useful in single power supply systems. For example, biasing can be designed separately from the AC gain as was shown in the "inverting amplifier," the "difference integrator" allows controlling the charging and the discharging of the integrating capacitor with positive voltages, and the "frequency doubling tachometer" provides a simple circuit which reduces the ripple voltage on a tachometer output DC voltage.

Typical Performance Characteristics

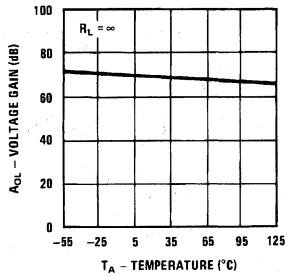
Open Loop Gain



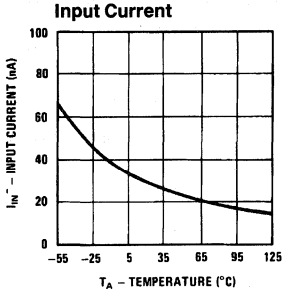
Voltage Gain



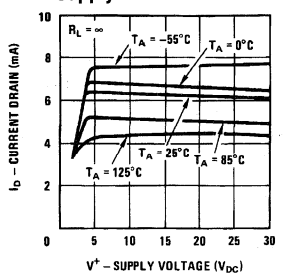
Voltage Gain



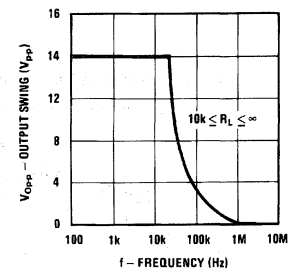
Input Current



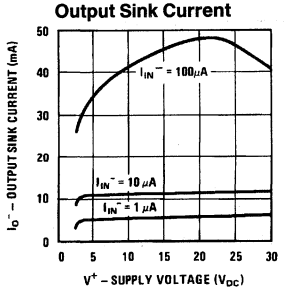
Supply Current



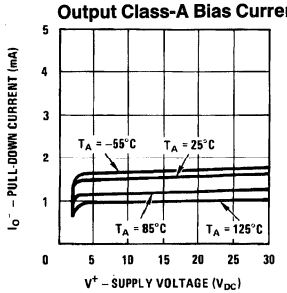
Large Signal Frequency Response



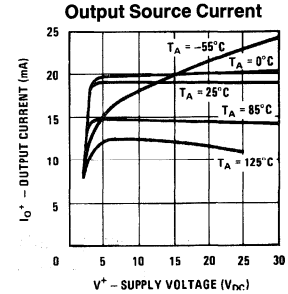
Output Sink Current



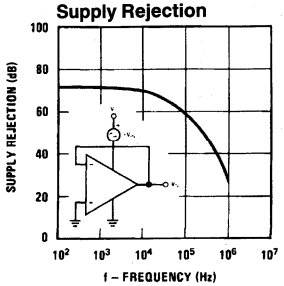
Output Class-A Bias Current



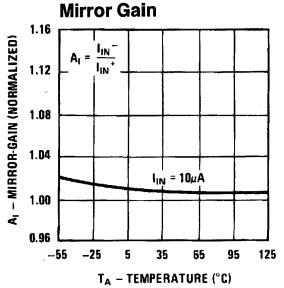
Output Source Current



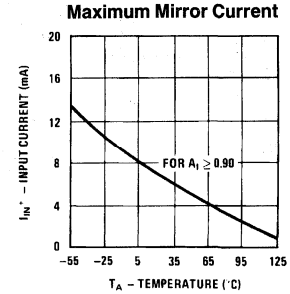
Supply Rejection



Mirror Gain



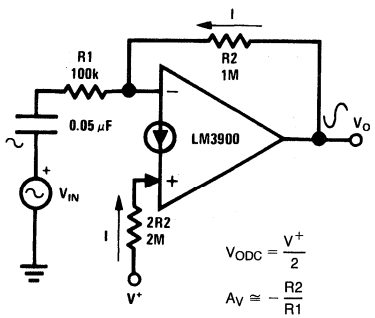
Maximum Mirror Current



TL/H/7936–9

Typical Applications ($V^+ = 15\ V_{DC}$)

Inverting Amplifier

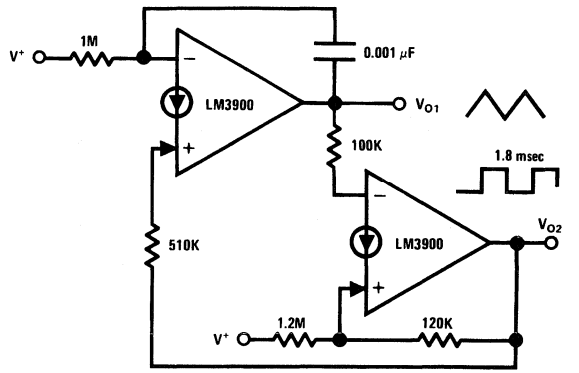


$$V_{ODC} = \frac{V^+}{2}$$

$$A_V \cong -\frac{R2}{R1}$$

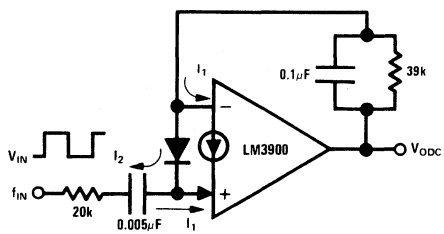
TL/H/7936-3

Triangle/Square Generator



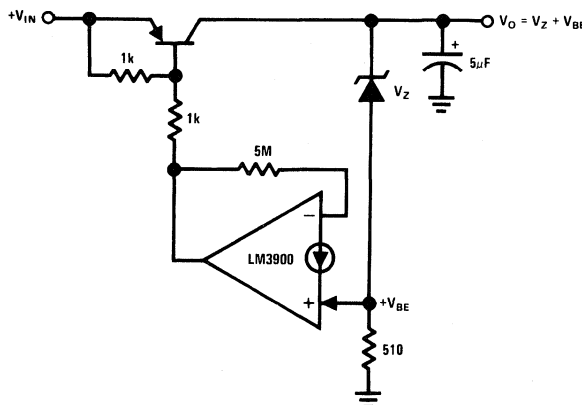
TL/H/7936-4

Frequency-Doubling Tachometer



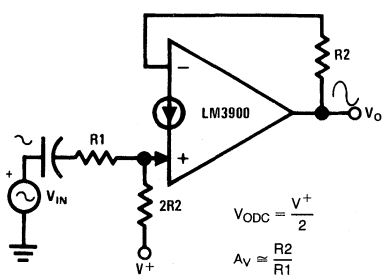
TL/H/7936-5

Low $V_{IN} - V_{OUT}$ Voltage Regulator



TL/H/7936-6

Non-Inverting Amplifier

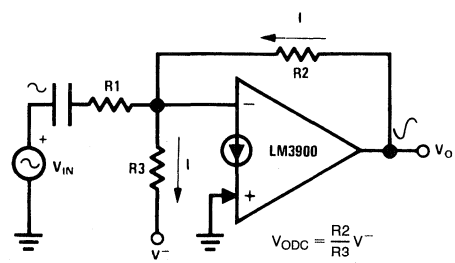


$$V_{ODC} = \frac{V^+}{2}$$

$$A_V \cong \frac{R2}{R1}$$

TL/H/7936-7

Negative Supply Biasing



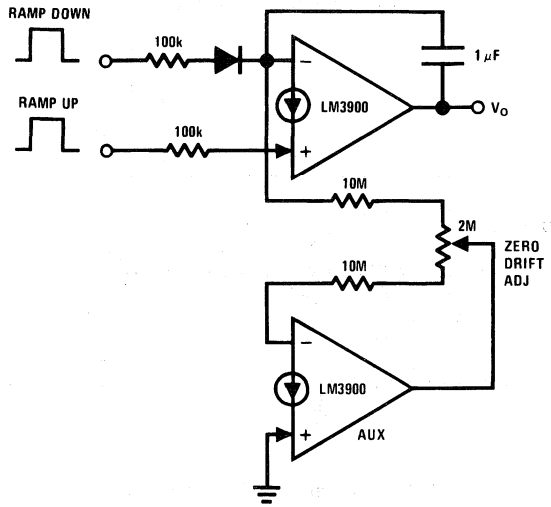
$$V_{ODC} = \frac{R2}{R3} V^-$$

$$A_V \cong \frac{R2}{R1}$$

TL/H/7936-8

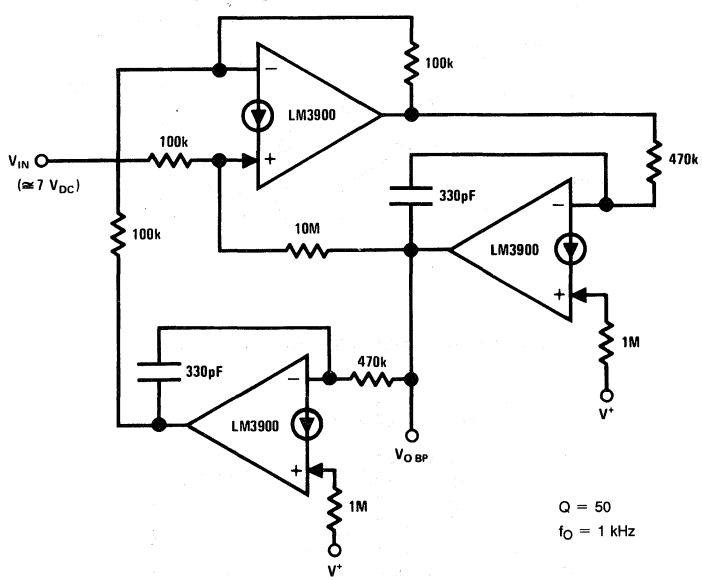
Typical Applications (V^+ = 15 V_{DC}) (Continued)

Low-Drift Ramp and Hold Circuit



TL/H/7936–10

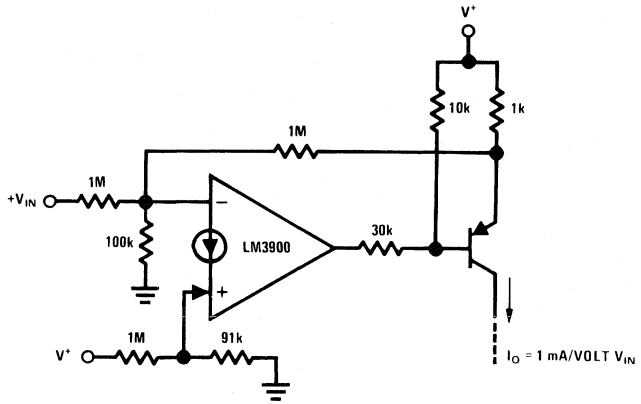
Bi-Quad Active Filter
(2nd Degree State-Variable Network)



TL/H/7936–11

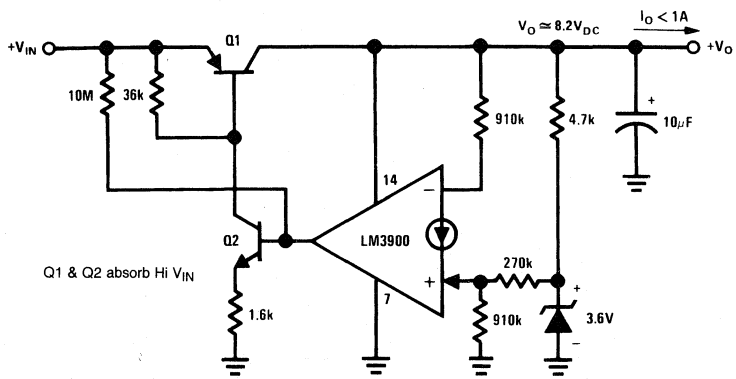
Typical Applications (V^+ = 15 V_{DC}) (Continued)

Voltage-Controlled Current Source (Transconductance Amplifier)



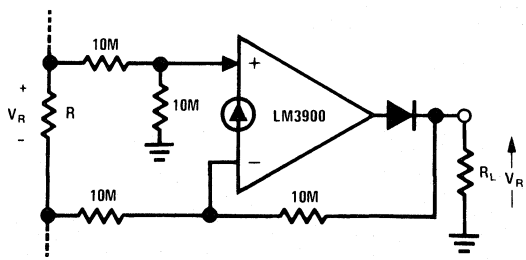
TL/H/7936–12

Hi V_{IN}, Lo (V_{IN} − V_O) Self-Regulator



TL/H/7936–13

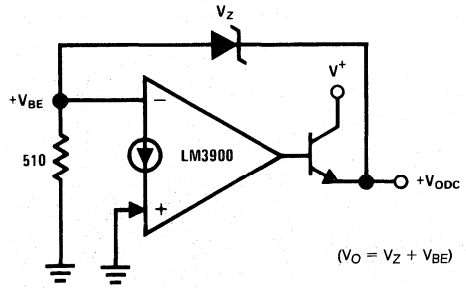
Ground-Referencing a Differential Input Signal



TL/H/7936–14

Typical Applications (V^+ = 15 V_{DC}) (Continued)

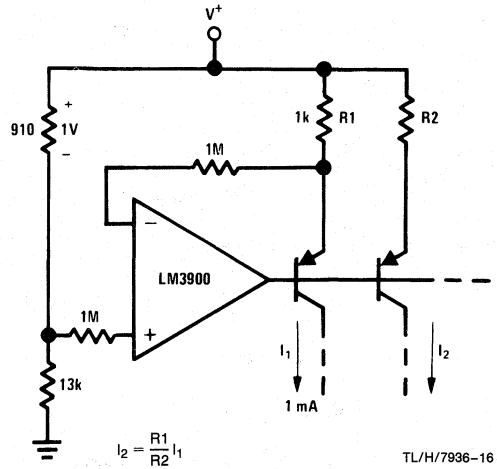
Voltage Regulator



$(V_O = V_Z + V_{BE})$

TL/H/7936–15

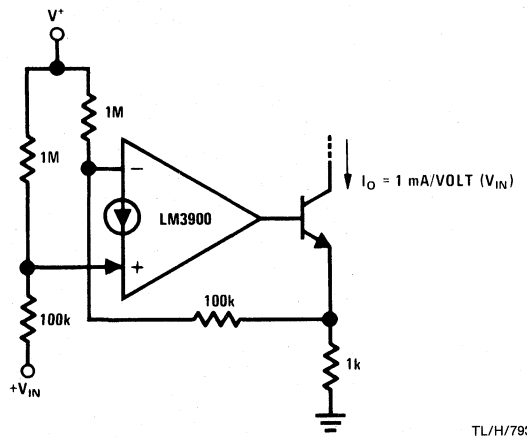
Fixed Current Sources



$I_2 = \frac{R1}{R2} I_1$

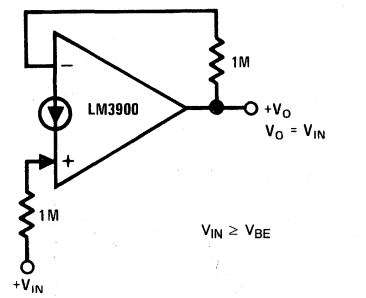
TL/H/7936–16

Voltage-Controlled Current Sink (Transconductance Amplifier)



TL/H/7936–17

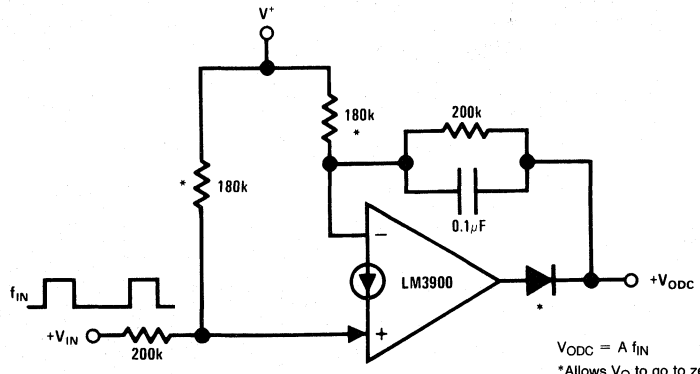
Buffer Amplifier



$V_{IN} \geq V_{BE}$

TL/H/7936–18

Tachometer



V_{ODC} = A f_{IN}

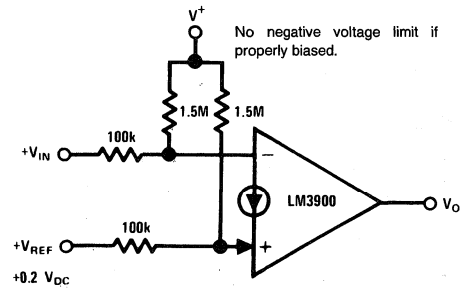
*Allows V_O to go to zero.

TL/H/7936–19

1

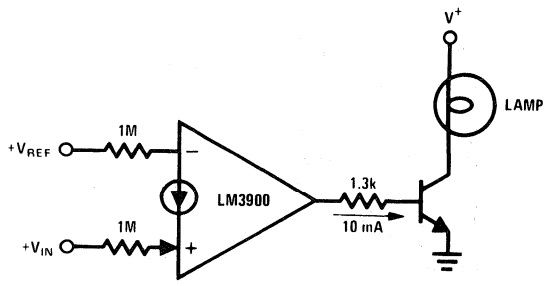
Typical Applications (V^+ = 15 V_{DC}) (Continued)

Low-Voltage Comparator



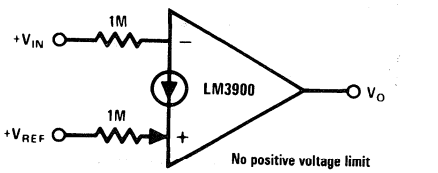
TL/H/7936–20

Power Comparator



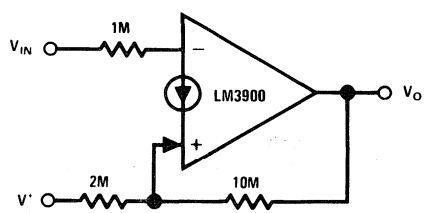
TL/H/7936–21

Comparator



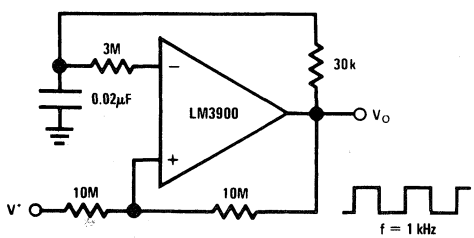
TL/H/7936–22

Schmitt-Trigger



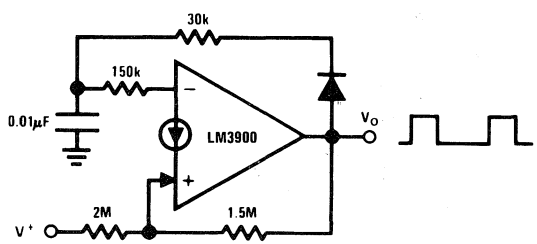
TL/H/7936–23

Square-Wave Oscillator



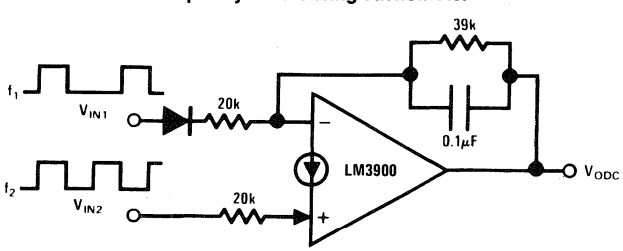
TL/H/7936–24

Pulse Generator



TL/H/7936–25

Frequency Differencing Tachometer

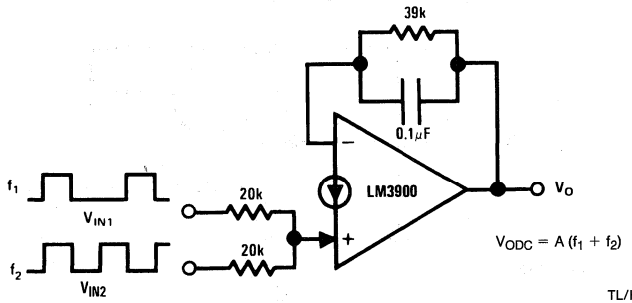


$V_{ODC} = A (f_1 - f_2)$

TL/H/7936–26

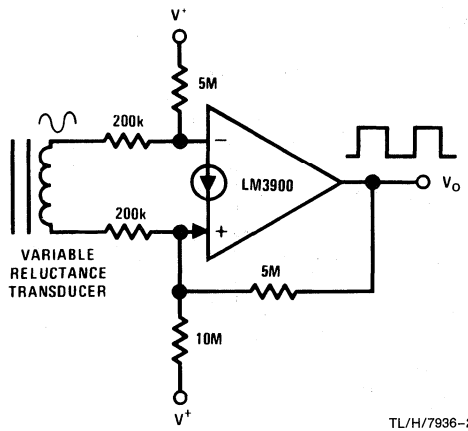
Typical Applications (V^+ = 15 V_{DC}) (Continued)

Frequency Averaging Tachometer



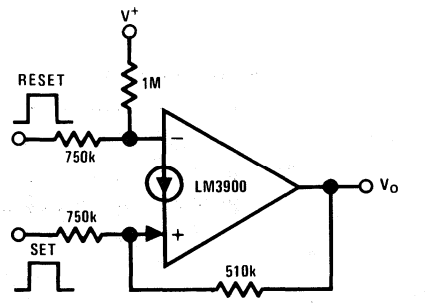
TL/H/7936–27

Squaring Amplifier (W/Hysteresis)



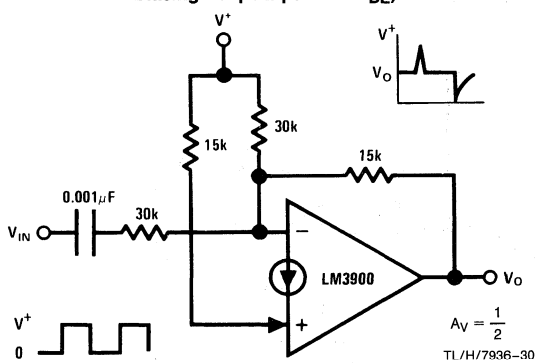
TL/H/7936–28

Bi-Stable Multivibrator



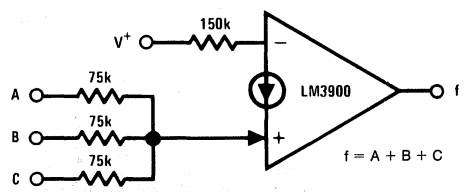
TL/H/7936–29

Differentiator (Common-Mode Biasing Keeps Input at $+V_{BE}$)



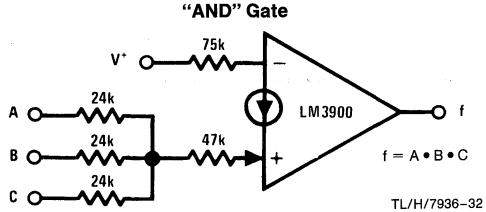
TL/H/7936–30

"OR" Gate



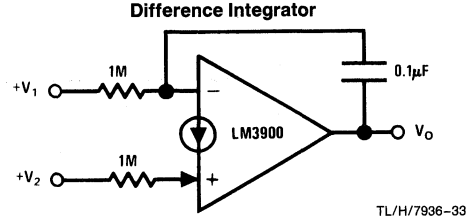
TL/H/7936–31

"AND" Gate



TL/H/7936–32

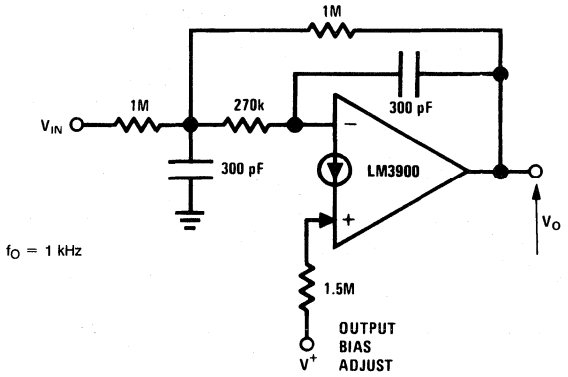
Difference Integrator



TL/H/7936–33

Typical Applications (V^+ = 15 V_{DC}) (Continued)

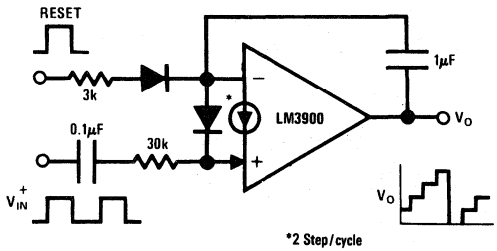
Low Pass Active Filter



f_O = 1 kHz

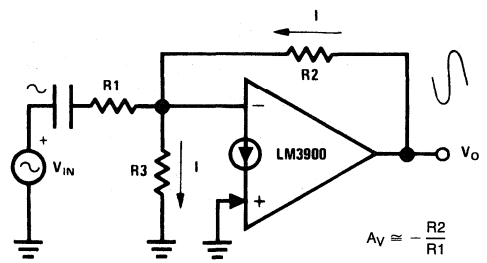
TL/H/7936–34

Staircase Generator



TL/H/7936–35

V_{BE} Biasing

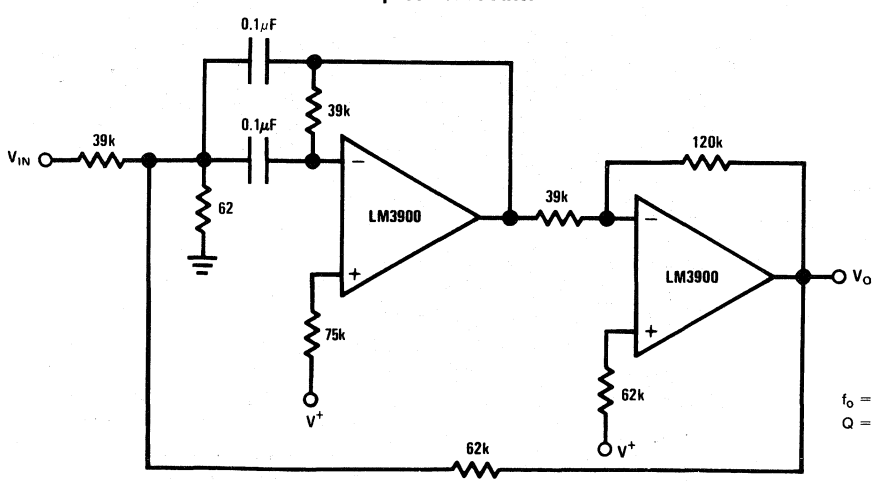


V_{BE} = 0.5 V_{DC}

$V_{ODC} = V_{BE}\left(1 + \frac{R2}{R3}\right)$

TL/H/7936–36

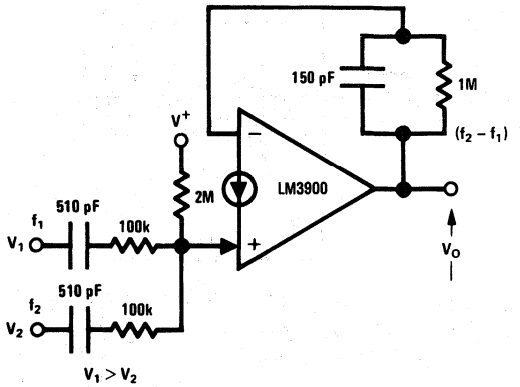
Bandpass Active Filter



TL/H/7936–37

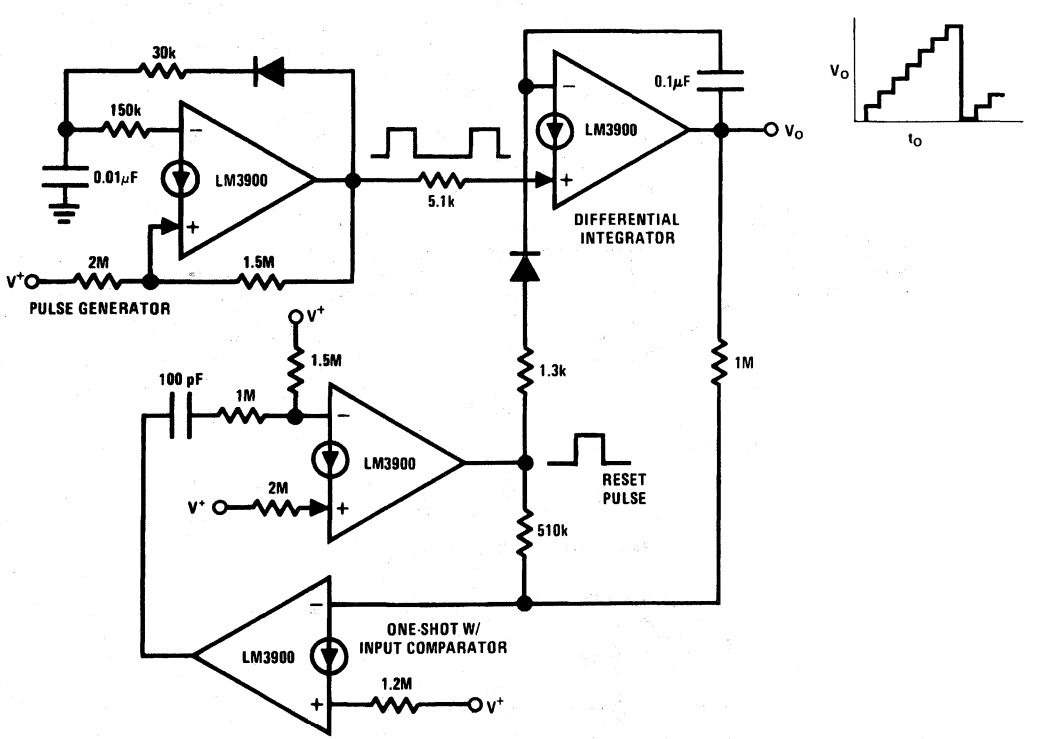
Typical Applications ($V^+ = 15\ V_{DC}$) (Continued)

Low-Frequency Mixer



TL/H/7936-38

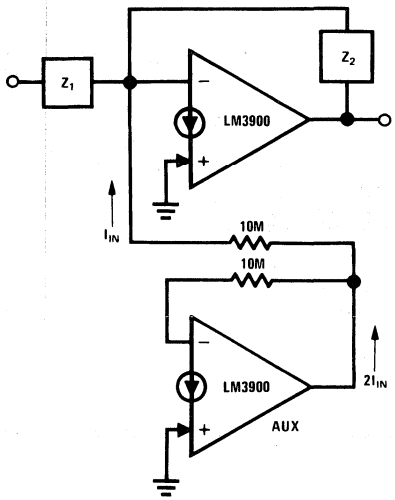
Free-Running Staircase Generator/Pulse Counter



TL/H/7936-39

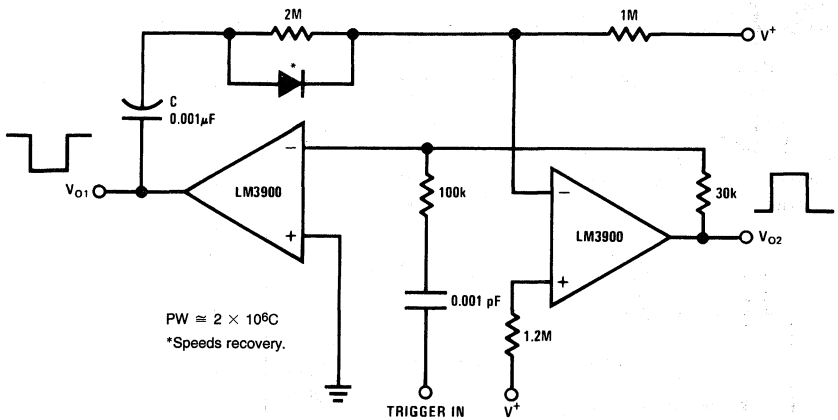
Typical Applications (V^+ = 15 V_{DC}) (Continued)

Supplying I_{IN} with Aux. Amp (to Allow Hi-Z Feedback Networks)



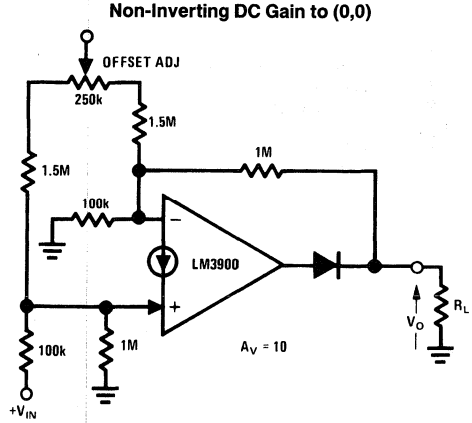
TL/H/7936–40

One-Shot Multivibrator



TL/H/7936–41

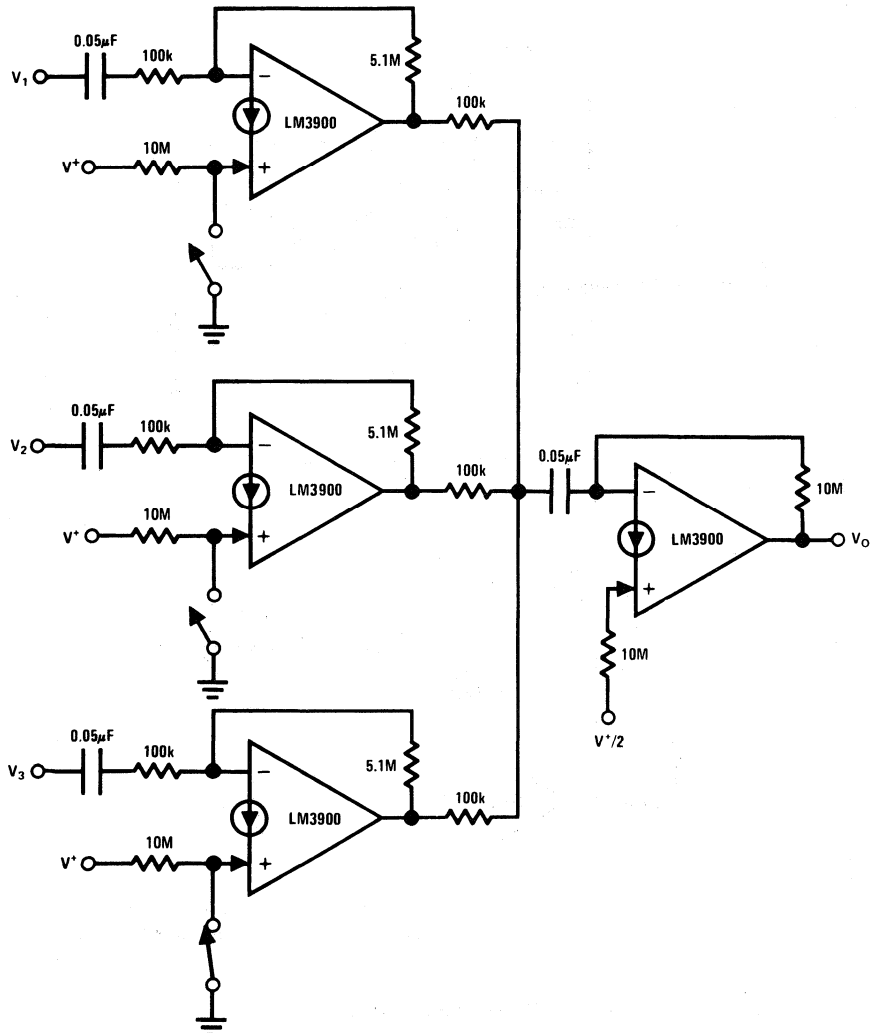
Non-Inverting DC Gain to (0,0)



TL/H/7936–42

Typical Applications (V^+ = 15 V_{DC}) (Continued)

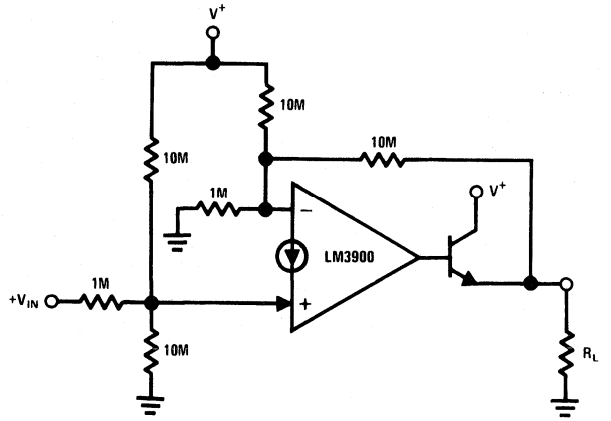
Channel Selection by DC Control (or Audio Mixer)



TL/H/7936–43

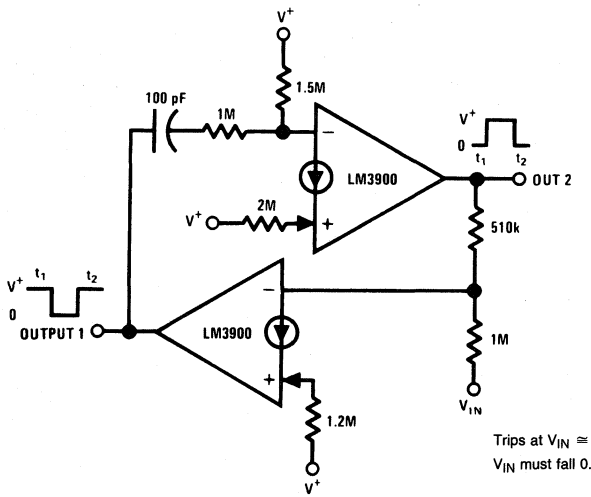
Typical Applications (V^+ = 15 V_{DC}) (Continued)

Power Amplifier



TL/H/7936–44

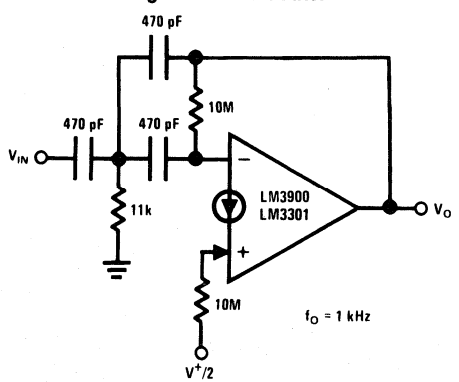
One-Shot with DC Input Comparator



Trips at $V_{IN} \cong 0.8\ V^+$
V_{IN} must fall 0.8 V^+ prior to t_2

TL/H/7936–45

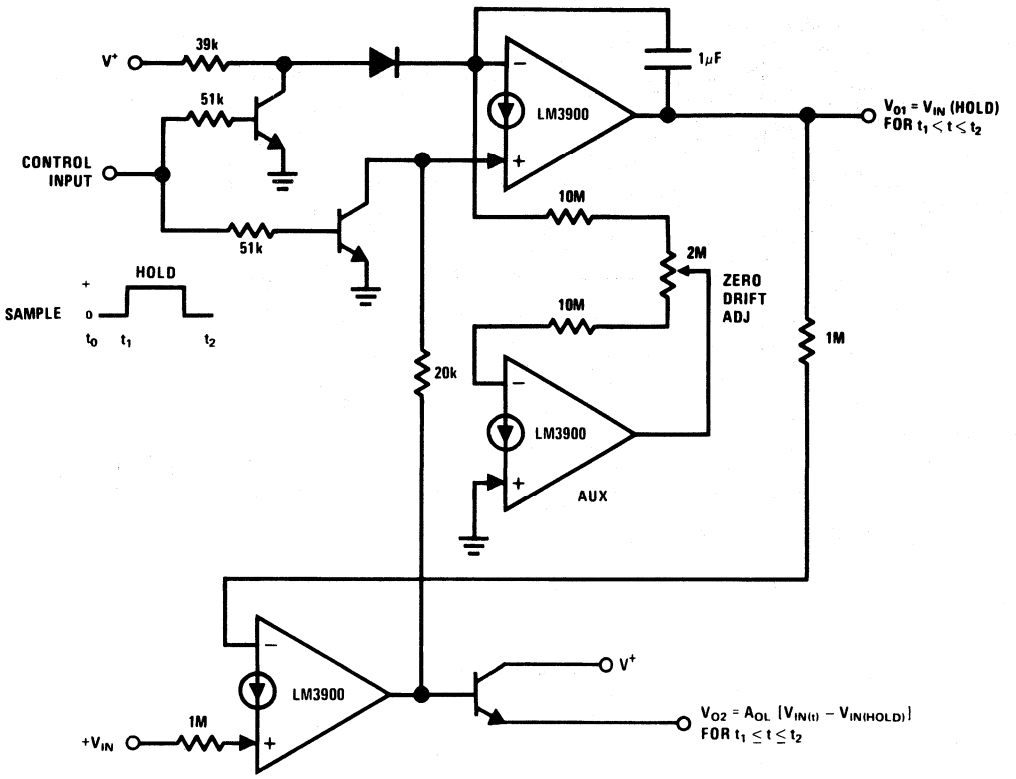
High Pass Active Filter



TL/H/7936–46

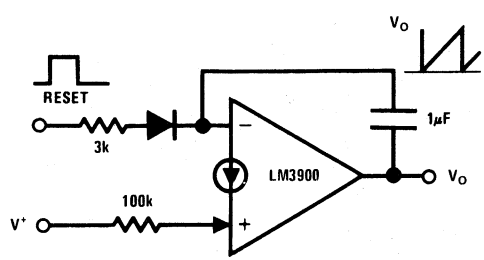
Typical Applications ($V^+ = 15\ V_{DC}$) (Continued)

Sample-Hold and Compare with New $+V_{IN}$



TL/H/7936–47

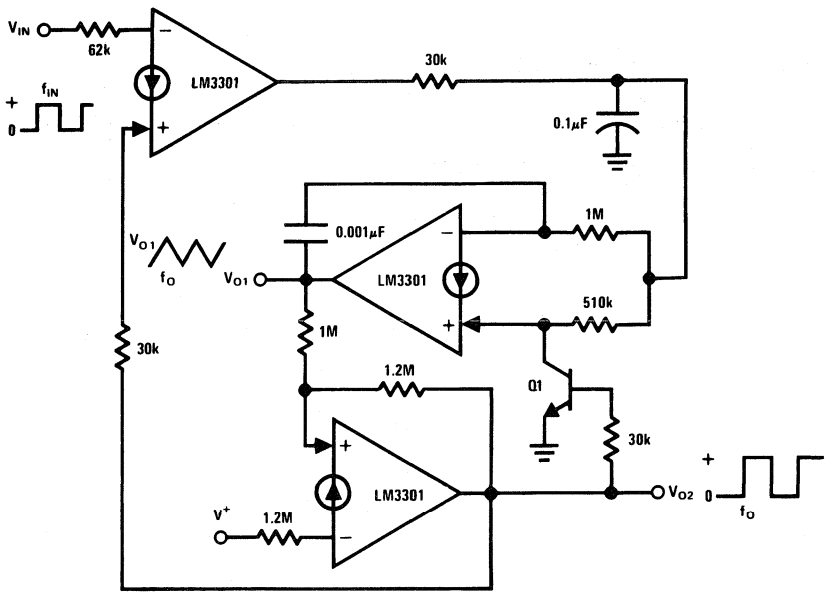
Sawtooth Generator



TL/H/7936–48

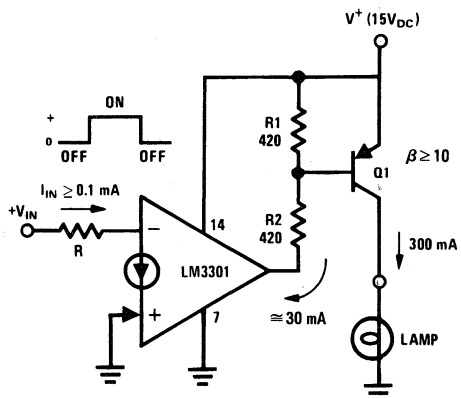
Typical Applications ($V^+ = 15\ V_{DC}$) (Continued)

Phase-Locked Loop



TL/H/7936–49

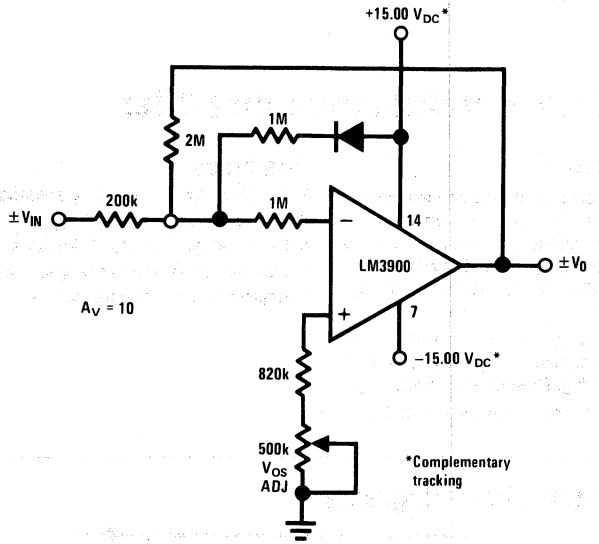
Boosting to 300 mA Loads



TL/H/7936–50

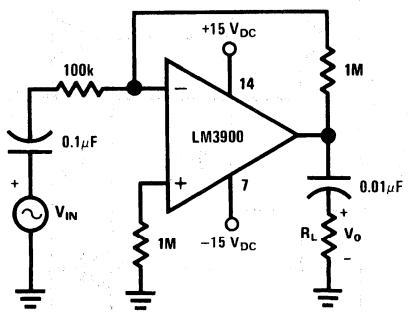
Split-Supply Applications ($V^+ = +15\ V_{DC}$ & $V^- = -15\ V_{DC}$)

Non-Inverting DC Gain



TL/H/7936–51

AC Amplifier



TL/H/7936–52

National Semiconductor

LM3080
Operational Transconductance Amplifier

General Description

The LM3080 is a programmable transconductance block intended to fulfill a wide variety of variable gain applications. The LM3080 has differential inputs and high impedance push-pull outputs. The device has high input impedance and its transconductance (g_m) is directly proportional to the amplifier bias current (I_{ABC}).

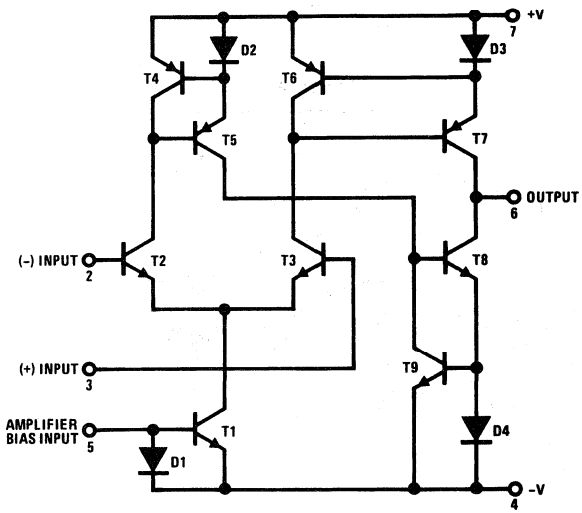
High slew rate together with programmable gain make the LM3080 an ideal choice for variable gain applications such as sample and hold, multiplexing, filtering, and multiplying.

The LM3080N and LM3080AN are guaranteed from 0°C to +70°C.

Features

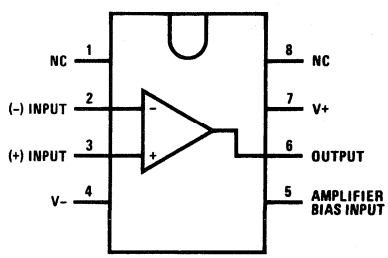
- Slew rate (unity gain compensated): 50 V/μs
- Fully adjustable gain: 0 to $g_m \bullet R_L$ limit
- Extended g_m linearity: 3 decades
- Flexible supply voltage range: ±2V to ±18V
- Adjustable power consumption

Schematic and Connection Diagrams



TL/H/7148–1

Dual-In-Line Package



TL/H/7148–2

Top View

Order Number LM3080AN, LM3080M or LM3080N
See NS Package Number M08A or N08E

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (Note 2)
- LM3080 ±18V
- LM3080A ±22V

Power Dissipation 250 mW

Differential Input Voltage ±5V

Amplifier Bias Current (I_{ABC}) 2 mA

DC Input Voltage $+V_S$ to $-V_S$

Output Short Circuit Duration Indefinite

Operating Temperature Range
- LM3080N or LM3080AN 0°C to +70°C

Storage Temperature Range −65°C to +150°C

Lead Temperature (Soldering, 10 sec.) 260°C

Electrical Characteristics (Note 1)

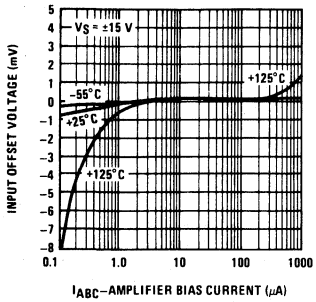
Parameter	Conditions	LM3080			LM3080A			Units
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage			0.4	5		0.4	2	mV
	Over Specified Temperature Range			6			5	mV
	I_{ABC} = 5 μA		0.3			0.3	2	mV
Input Offset Voltage Change	5 μA ≤ I_{ABC} ≤ 500 μA		0.1			0.1	3	mV
Input Offset Current			0.1	0.6		0.1	0.6	μA
Input Bias Current			0.4	5		0.4	5	μA
	Over Specified Temperature Range		1	7		1	8	μA
Forward Transconductance (g_m)		6700	9600	13000	7700	9600	12000	μmho
	Over Specified Temperature Range	5400			4000			μmho
Peak Output Current	R_L = 0, I_{ABC} = 5 μA		5		3	5	7	μA
	R_L = 0	350	500	650	350	500	650	μA
	R_L = 0 Over Specified Temperature Range	300			300			μA
Peak Output Voltage								
Positive	R_L = ∞, 5 μA ≤ I_{ABC} ≤ 500 μA	+12	+14.2		+12	+14.2		V
Negative	R_L = ∞, 5 μA ≤ I_{ABC} ≤ 500 μA	−12	−14.4		−12	−14.4		V
Amplifier Supply Current			1.1			1.1		mA
Input Offset Voltage Sensitivity								
Positive	$\Delta V_{OFFSET}/\Delta V+$		20	150		20	150	μV/V
Negative	$\Delta V_{OFFSET}/\Delta V-$		20	150		20	150	μV/V
Common Mode Rejection Ratio		80	110		80	110		dB
Common Mode Range		±12	±14		±12	±14		V
Input Resistance		10	26		10	26		kΩ
Magnitude of Leakage Current	I_{ABC} = 0		0.2	100		0.2	5	nA
Differential Input Current	I_{ABC} = 0, Input = ±4V		0.02	100		0.02	5	nA
Open Loop Bandwidth			2			2		MHz
Slew Rate	Unity Gain Compensated		50			50		V/μs

Note 1: These specifications apply for V_S = ±15V and T_A = 25°C, amplifier bias current (I_{ABC}) = 500 μA, unless otherwise specified.

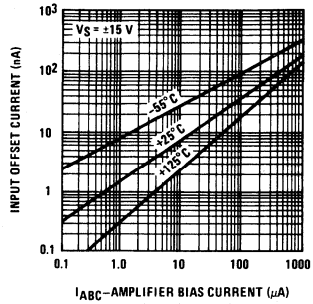
Note 2: Selection to supply voltage above ±22V, contact the factory.

Typical Performance Characteristics

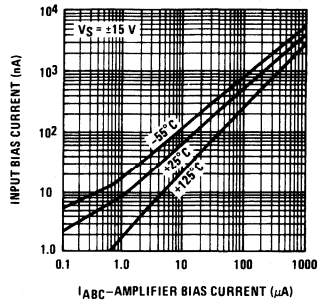
Input Offset Voltage



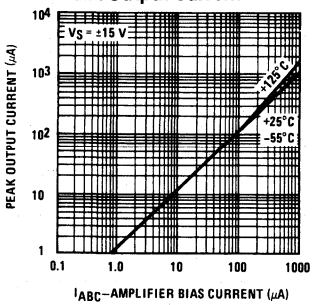
Input Offset Current



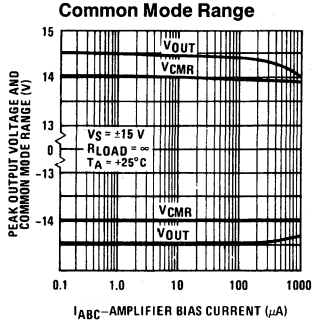
Input Bias Current



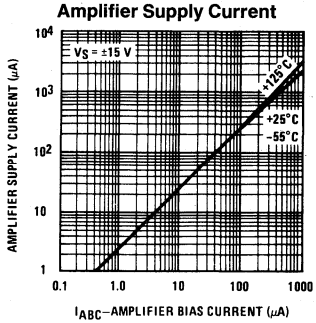
Peak Output Current



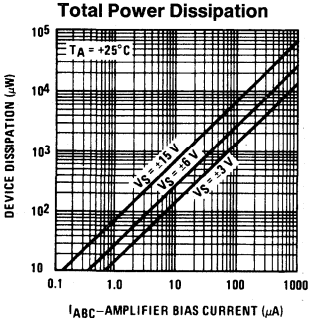
Peak Output Voltage and Common Mode Range



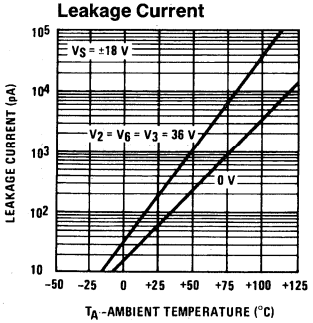
Amplifier Supply Current



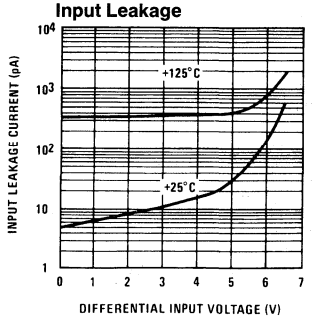
Total Power Dissipation



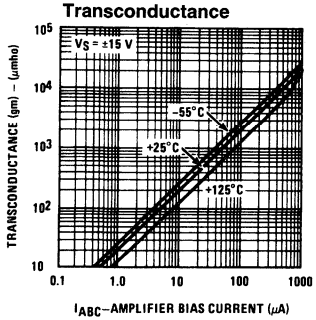
Leakage Current



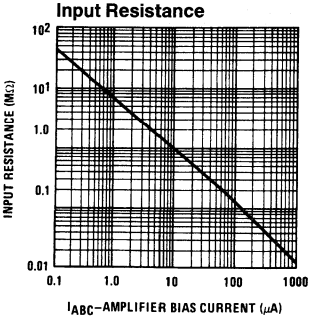
Input Leakage



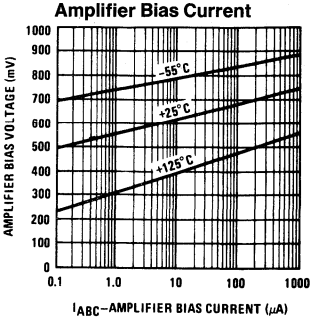
Transconductance



Input Resistance



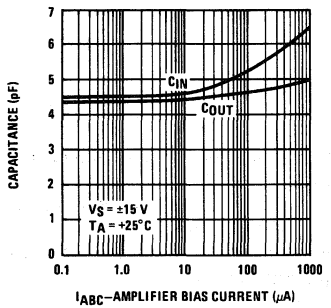
Amplifier Bias Voltage vs Amplifier Bias Current



TL/H/7148–3

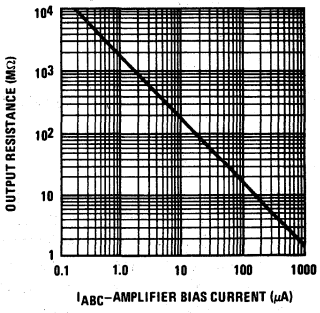
Typical Performance Characteristics (Continued)

Input and Output Capacitance



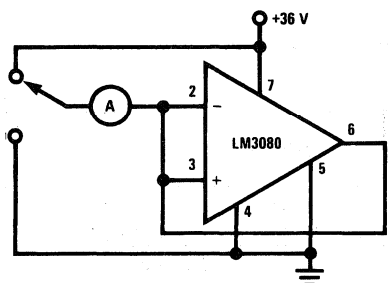
TL/H/7148–4

Output Resistance



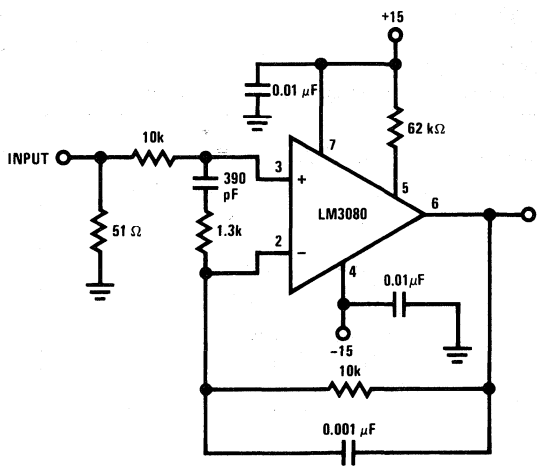
TL/H/7148–5

Leakage Current Test Circuit



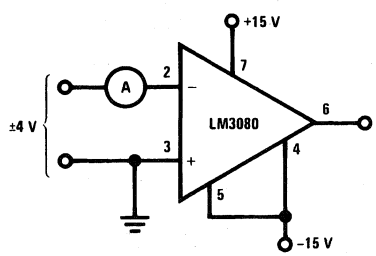
TL/H/7148–6

Unity Gain Follower



TL/H/7148–8

Differential Input Current Test Circuit



TL/H/7148–7

National Semiconductor

LM3303/LM3403
Quad Operational Amplifiers

General Description

The LM3303 and LM3403 are monolithic quad operational amplifiers consisting of four independent high gain, internally frequency compensated, operational amplifiers designed to operate from a single power supply or dual power supplies over a wide range of voltages. The common mode input range includes the negative supply, thereby eliminating the necessity for external biasing components in many applications.

Features

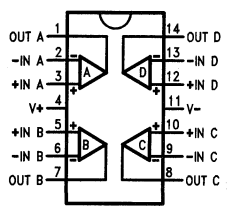
- Input common mode voltage range includes ground or negative supply
- Output voltage can swing to ground or negative supply
- Four internally compensated operational amplifiers in a single package
- Wide power supply range single supply of 3.0V to 36V dual supply of ±1.5V to ±18V
- Class AB output stage for minimal crossover distortion
- Short circuit protected outputs
- High open loop gain 200k
- LM741 operational amplifier type performance

Applications

- Filters
- Voltage controlled oscillators

Connection Diagram

14-Lead DIP and SO-14 Package



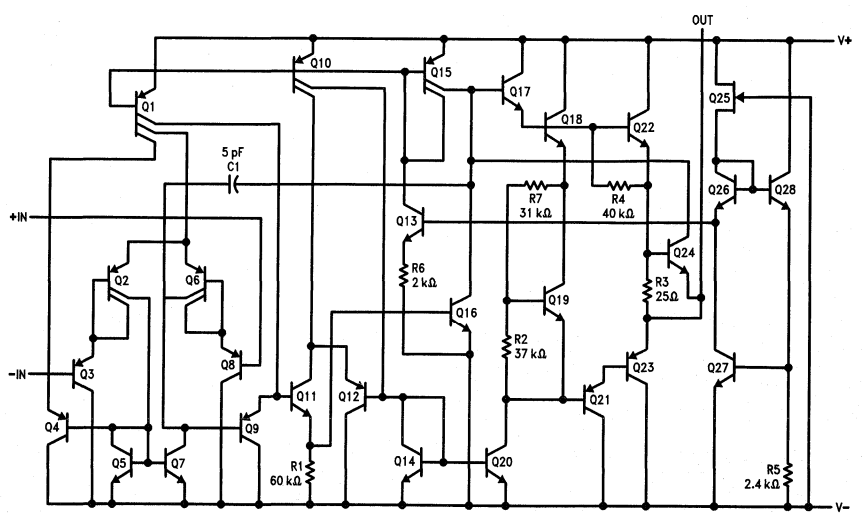
TL/H/10064–1

Top View

Order Information

Device Code	Package Code	Package Description
LM3303J	J14A	Ceramic DIP
LM3303N	N14A	Molded DIP
LM3303M	M14A	Molded Surface Mount
LM3403J	J14A	Ceramic DIP
LM3403N	N14A	Molded DIP
LM3403M	M14A	Molded Surface Mount

Equivalent Circuit (¼ of Circuit)



TL/H/10064–2

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature Range
- Ceramic DIP: −65°C to +175°C
- Molded DIP and SO-14: −65°C to +150°C

Operating Temperature Range
- Industrial (LM3303): −40°C to +85°C
- Commercial (LM3403): 0°C to +70°C

Lead Temperature
- Ceramic DIP (Soldering, 60 sec.): 300°C
- Molded DIP and SO-14 (Soldering, 10 sec.): 265°C

Internal Power Dissipation (Notes 1, 2)
- 14L-Ceramic DIP: 1.36W
- 14L-Molded DIP: 1.04W
- SO-14: 0.93W

Supply Voltage between V+ and V−: 36V

Differential Input Voltage (Note 3): ±30V

Input Voltage: (V−) − 0.3V to V+

ESD Tolerance: (To Be Determined)

LM3303 and LM3403 Electrical Characteristics

T_A = 25°C, V_{CC} = ±15V, unless otherwise specified

Symbol	Parameter		Conditions	LM3303			LM3403			Units
				Min	Typ	Max	Min	Typ	Max	
V_{IO}	Input Offset Voltage				2.0	8.0		2.0	8.0	mV
I_{IO}	Input Offset Current				30	75		30	50	nA
I_{IB}	Input Bias Current				200	500		200	500	nA
Z_I	Input Impedance			0.3	1.0		0.3	1.0		MΩ
I_{CC}	Supply Current		V_O = 0V, R_L = ∞		2.8	7.0		2.8	7.0	mA
CMR	Common Mode Rejection		R_S ≤ 10 kΩ	70	90		70	90		dB
V_{IR}	Input Voltage Range			+12V to V−	+12.5V to V−		+13V to V−	+13.5V to V−		V
PSRR	Power Supply Rejection Ratio				30	150		30	150	μV/V
I_{OS}	Output Short Circuit Current (Per Amplifier) (Note 4)			±10	±30	±45	±10	±30	±45	mA
A_{VS}	Large Signal Voltage Gain		V_O = ±10V, R_L ≥ 2.0 kΩ	20	200		20	200		V/mV
V_{OP}	Output Voltage Swing		R_L = 10 kΩ	±12	12.5		±12	+13.5		V
			R_L = 2.0 kΩ	±10	12		±10	±13		
TR	Transient Response	Rise Time/ Fall Time	V_O = 50 mV, A_V = 1.0, R_L = 10 kΩ		0.3			0.3		μs
		Overshoot	V_O = 50 mV, A_V = 1.0, R_L = 10 kΩ		5.0			5.0		%
BW	Bandwidth		V_O = 50 mV, A_V = 1.0, R_L = 10 kΩ		1.0			1.0		MHz
SR	Slew Rate		V_I = −10V to +10V, A_V = 1.0		0.6			0.6		V/μs

LM3303 and LM3403 (Continued)

Electrical Characteristics $T_A = 25°C$, $V_{CC} = \pm 15V$, unless otherwise specified

The following specifications apply for $-40°C \leq T_A \leq +85°C$ for the LM3303, and $0°C \leq T_A \leq +70°C$ for the LM3403

Symbol	Parameter	Conditions	LM3303			LM3403			Units
			Min	Typ	Max	Min	Typ	Max	
V_{IO}	Input Offset Voltage				10			10	mV
$\Delta V_{IO}/\Delta T$	Input Offset Voltage Temperature Sensitivity			10			10		μV/°C
I_{IO}	Input Offset Current				250			200	nA
$\Delta I_{IO}/\Delta T$	Input Offset Current Temperature Sensitivity			50			50		pA/°C
I_{IB}	Input Bias Current				1000			800	nA
A_{VS}	Large Signal Voltage Gain	$V_O = \pm 10V$, $R_L \geq 2.0\ k\Omega$	15			15			V/mV
V_{OP}	Output Voltage Swing	$R_L = 2.0\ k\Omega$	±10			±10			V

LM3303 and LM3403 Electrical Characteristics $T_A = 25°C$, V+ = 5.0V, V− = GND, unless otherwise specified

Symbol	Parameter	Conditions	LM3303			LM3403			Units
			Min	Typ	Max	Min	Typ	Max	
V_{IO}	Input Offset Voltage				8.0		2.0	8.0	mV
I_{IO}	Input Offset Current				75		30	50	nA
I_{IB}	Input Bias Current				500		200	500	nA
I_{CC}	Supply Current			2.5	7.0		2.5	7.0	mA
PSRR	Power Supply Rejection Ratio				150			150	μV/V
A_{VS}	Large Signal Voltage Gain	$R_L \geq 2.0\ k\Omega$	20	200		20	200		V/mV
V_{OP}	Output Voltage Swing (Note 5)	$R_L = 10\ k\Omega$	3.3			3.3			V
		5.0V ≤ V+ ≤ 30V, $R_L = 10\ k\Omega$	(V+) −2.0			(V+) −2.0			
CS	Channel Separation	1.0 Hz ≤ f ≤ 20 kHz (Input Referenced)		−120			−120		dB

Note 1: $T_{J\ Max} = 150°C$ for the Molded DIP and SO-14, and 175°C for the Ceramic DIP.

Note 2: Ratings apply to ambient temperature at 25°C. Above this temperature, derate the 14L-Ceramic DIP at 9.1 mW/°C, the 14L-Molded DIP at 8.3 mW/°C, and the SO-14 at 7.5 mW/°C.

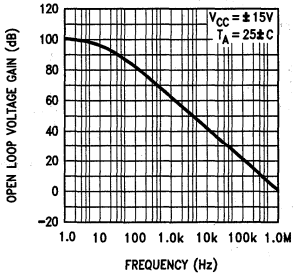
Note 3: For supply voltage less than 30V between V+ and V−, the absolute maximum input voltage is equal to the supply voltage.

Note 4: Not to exceed maximum package power dissipation.

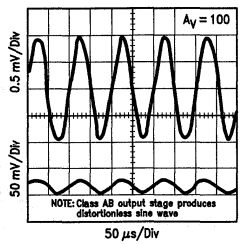
Note 5: Output will swing to ground.

Typical Performance Characteristics

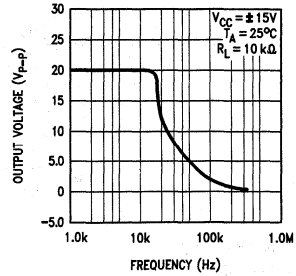
Open Loop Frequency Response



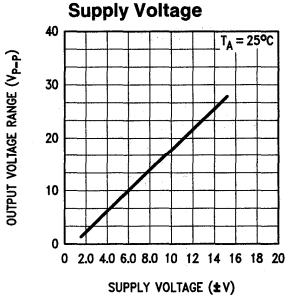
Sine Wave Response



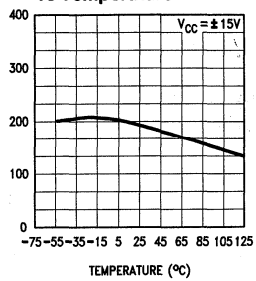
Output Voltage vs Frequency



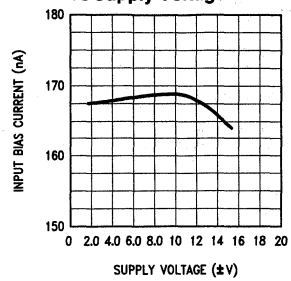
Output Swing vs Supply Voltage



Input Bias Current vs Temperature



Input Bias Current vs Supply Voltage

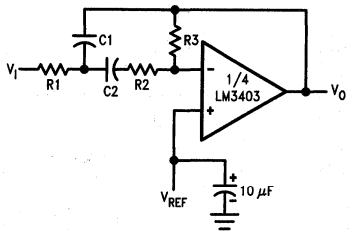


TL/H/10064–3

1

Typical Applications

Multiple Feedback Bandpass Filter



TL/H/10064–4

f_o = center frequency
BW = Bandwidth
R in kΩ
C in μF

$$Q = \frac{f_o}{BW} < 10$$

$$C1 = C2 = \frac{Q}{3}$$

$$R1 = R2 = 1\ R3 = 9Q^2 - 1$$ } Using scaling factors in these expressions.

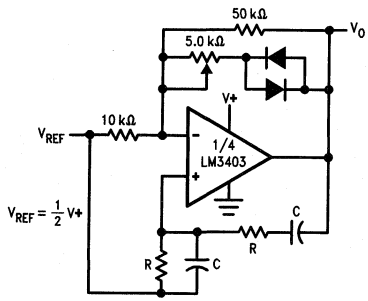
If source impedance is high or varies, filter may be preceded with voltage follower buffer to stabilize filter parameters.

Design example:

given: Q = 5, f_o = 1 kHz
Let R1 = R2 = 10 kΩ
then R3 = $9(5)^2 - 10$
R3 = 215 kΩ

$$C = \frac{5}{3} = 1.6\ nF$$

Wein Bridge Oscillator

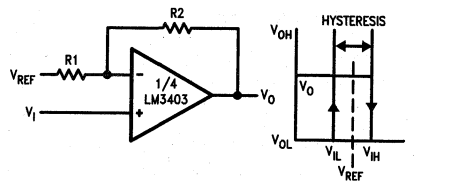


TL/H/10064–5

$$f_o = \frac{1}{2\pi RC} \text{ for } f_o = 1\ kHz$$

R = 16 kΩ
C = 0.01 μF

Comparator with Hysteresis



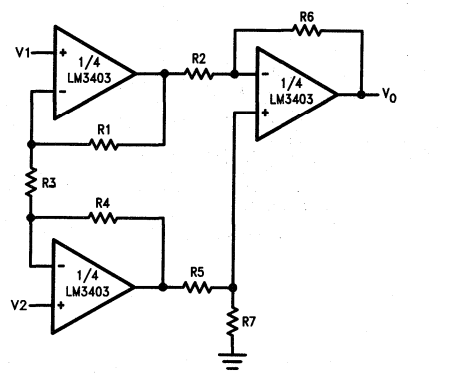
TL/H/10064–6

$$V_{IL} = \frac{R1}{R1 + R2}(V_{OL} - V_{REF}) + V_{REF}$$

$$V_{IH} = \frac{R1}{R1 + R2}(V_{OH} - V_{REF}) + V_{REF}$$

$$H = \frac{R1}{R1 + R2}(V_{OH} - V_{OL})$$

High Impedance Differential Amplifier



TL/H/10064–7

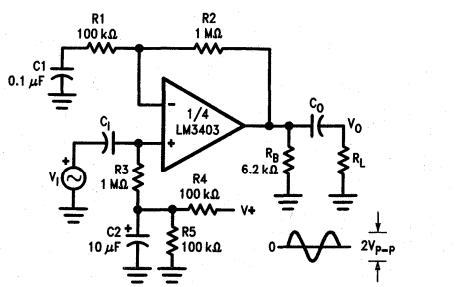
$$V_{OUT} = C(1 + a + b)(V2 - V1)$$

$$\frac{R2}{R5} \equiv \frac{R6}{R7} \text{ for best CMRR}$$

R1 = R4
R2 = R5

$$Gain = \frac{R6}{R5}\left(1 + \frac{2R1}{R3}\right) = C(1 + a + b)$$

AC Coupled Non-Inverting Amplifier



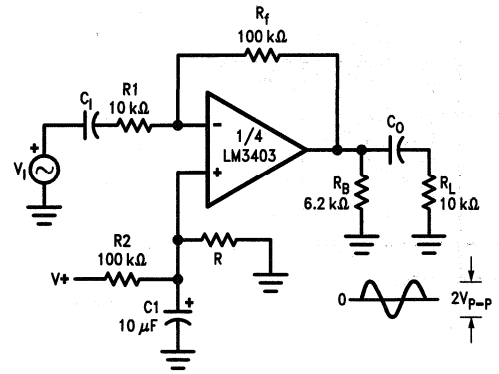
TL/H/10064–9

$$A_V = 1 + \frac{R2}{R1}$$

A_V = 11 (as shown)

Typical Applications (Continued)

AC Coupled Inverting Amplifier

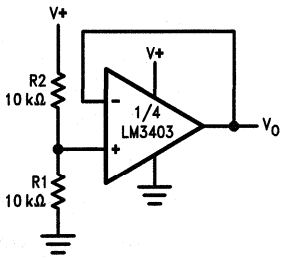


TL/H/10064–8

$$A_V = \frac{Rf}{R1}$$

A_V = 10 (as shown)

Voltage Reference

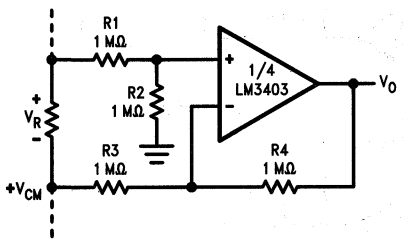


TL/H/10064–10

$$V_O = \frac{R1}{R1 + R2}\left(= \frac{V+}{2} \text{ as shown}\right)$$

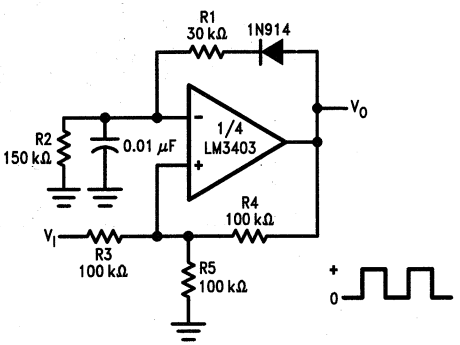
$$V_O = \frac{1}{2}V+$$

Ground Referencing a Differential Input Signal



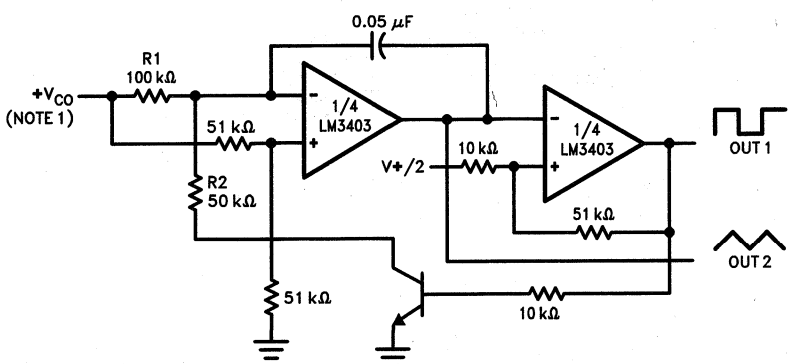
TL/H/10064–11

Pulse Generator



TL/H/10064–14

Voltage Controlled Oscillator

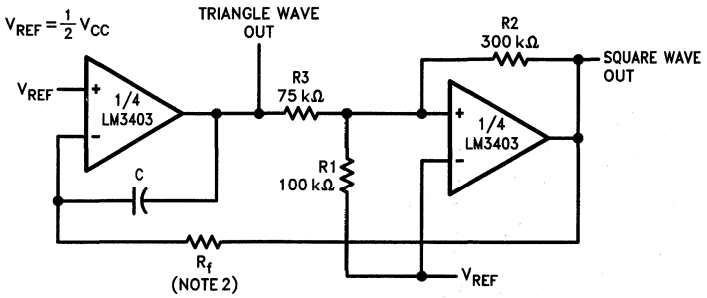


TL/H/10064–12

Note 1: Wide Control Voltage Range:
$0V \leq V_{CO} \leq 2\,(V \pm 1.5V)$

Typical Applications (Continued)

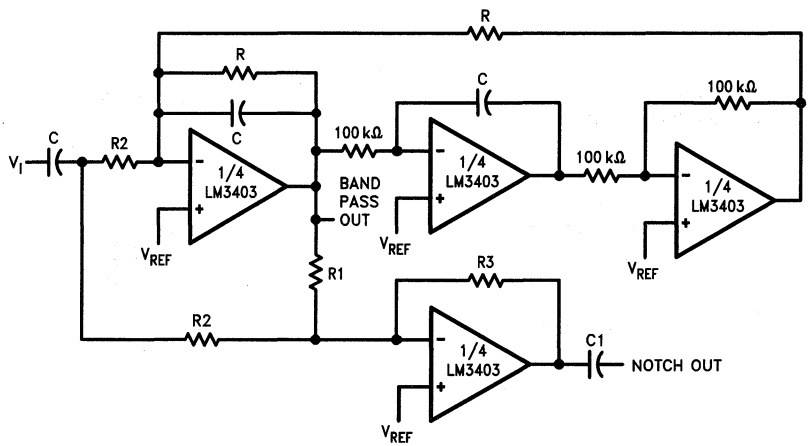
Function Generator



TL/H/10064–13

Note 2: $f = \frac{R1 + R2}{4CR_fR1}$ if $R3 = \frac{R2R1}{R2 + R1}$

Bi-Quad Filter



TL/H/10064–15

$Q = \frac{BW}{f_o}$

where:

T_{BP} = Center Frequency Gain
T_N = Bandpass Notch Gain

$f_o = \frac{1}{2\pi RC}$, $V_{REF} = \frac{1}{2} V_{CC}$

$R1 = QR$

$R2 = \frac{R1}{T_{BP}}$

$R3 = T_N R2$
$C1 = 10\ C$

Example:

f_o = 1000 Hz
BW = 100 Hz
T_{BP} = 1
T_N = 1
R = 160 kΩ
R1 = 1.6 MΩ
R2 = 1.6 MΩ
R3 = 1.6 MΩ
C = 0.001 μF

National Semiconductor

ADVANCE INFORMATION

LM3875
High Performance 40W Audio Power Amplifier

General Description

The LM3875 is a high-performance audio power amplifier. It is capable of delivering 40W to an 8Ω load. It is fully protected using circuit techniques similar to those found in the LM12.

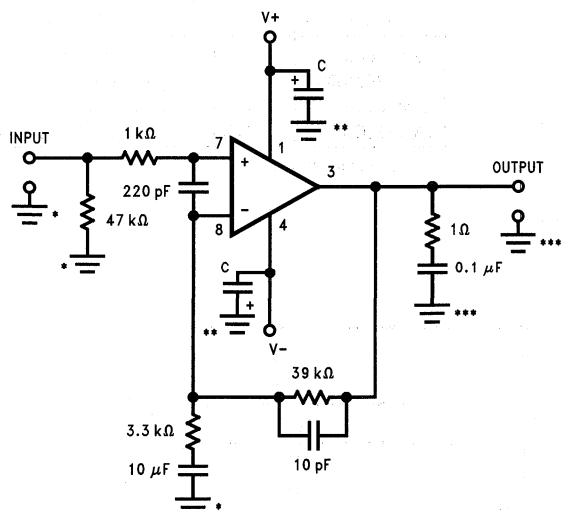
The output stage is protected from a short to ground or to the supplies. Protection against transients from inductive loads is provided at the output stage via internal clamp diodes. The LM3875 also contains thermal shutdown protection against operation outside its operating temperature range.

The LM3875 is internally compensated and stable for gains ≥10.

Features

- 40W output power into 8Ω
- Over-voltage protection
- Dynamic Safe Area Protection
- Fully protected from AC and DC short-circuits
- 11-lead TO-220 package
- Under-voltage shutdown

Typical Application



TL/H/11449-1

C—Power supply bypass using low ESR 680 μF electrolytic, 10 μF electrolytic, and 0.1 ceramic chip capacitor.

Ground Connections

*Input signal ground.

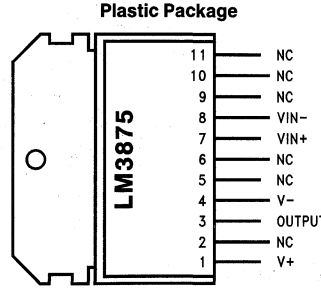
**Power supply bypass ground.

***Output signal ground.

These three ground connections should have separate return paths to the power supply ground ("star ground").

Connection Diagram

Plastic Package



TL/H/11449-2

Top View

Order Number LM3875CCT
See NS Package Number T11A

National Semiconductor

LM4136
Quad Operational Amplifier

General Description

The LM4136 monolithic quad operational amplifier consists of four independent high gain, internally frequency compensated operational amplifiers. The specifically designed low noise input transistors allow the LM4136 to be used in low noise signal processing applications such as audio preamplifiers and signal conditioners. The simplified output stage completely eliminates crossover distortion under any load conditions, has large source and sink capacity, and is short-circuit protected. A novel current source stabilizes output parameters over a wide power supply voltage range.

Features

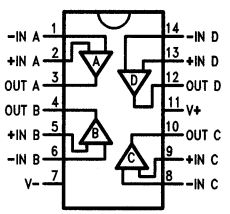
- Unity gain bandwidth—3.0 MHz
- Continuous short circuit protection
- No frequency compensation required
- No latch up
- Large common mode and differential voltage range
- LM741 operational amplifier type performance
- Parameter tracking over temperature range
- Gain and phase match between amplifiers

Applications

- Audio preamplifiers
- Signal conditioning

Connection Diagram

14-Lead DIP and SO-14 Package



TL/H/10065–1

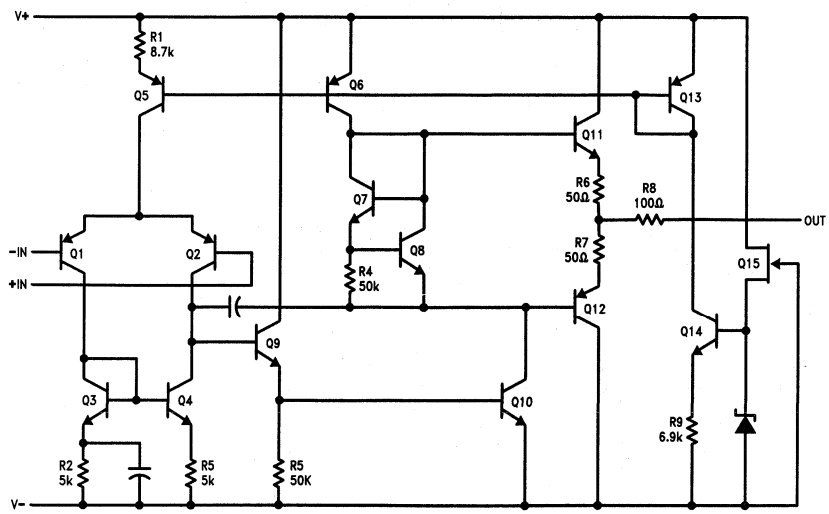
Top View

Ordering Information

Device Code	NS Package Number	Package Description
LM4136CJ	J14A	Ceramic DIP
LM4136J/883*	J14A	Ceramic DIP
LM4136CN	N14A	Molded DIP
LM4136CM	M14A	Molded Surface Mount

*Available per JM38510/11004

Equivalent Circuit (¼ of Circuit)



TL/H/10065–2

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature Range
- Ceramic DIP: −65°C to +175°C
- Molded DIP and SO-14: −65°C to +150°C

Operating Temperature Range: 0°C to +70°C

Lead Temperature
- Ceramic DIP (Soldering, 60 sec.): 300°C
- Molded DIP and SO-14 (Soldering, 10 sec.): 265°C

Internal Power Dissipation (Notes 1, 2)
- 14L-Ceramic DIP: 1.36W
- 14L-Molded DIP: 1.04W
- SO-14: 0.93W

Supply Voltage: ±18V

Differential Input Voltage (Note 3): ±30V

Input Voltage (Note 1): ±15V

Output Short Circuit Duration (Note 4): Indefinite

ESD Tolerance: 1000V

LM4136
Electrical Characteristics $T_A = 25°C$, $V_{CC} = \pm 15V$ unless otherwise specified

Symbol	Parameter		Conditions	Min	Typ	Max	Units
V_{IO}	Input Offset Voltage		$R_S \le 10\ k\Omega$		0.5	6.0	mV
I_{IO}	Input Offset Current				5.0	200	nA
I_{IB}	Input Bias Current				40	500	nA
Z_I	Input Impedance			0.3	5.0		MΩ
P_C	Power Consumption				210	340	mW
CMR	Common Mode Rejection		$R_S \le 10\ k\Omega$	70	90		dB
V_{IR}	Input Voltage Range			±12	±14		V
PSRR	Power Supply Rejection Ratio		$R_S \le 10\ k\Omega$		30	150	μV/V
A_{VS}	Large Signal Voltage Gain		$R_L \ge 2.0\ k\Omega$, $V_O = \pm 10V$	20	300		V/mV
V_{OP}	Output Voltage Swing		$R_L = 10\ k\Omega$	±12	±14		V
			$R_L = 2.0\ k\Omega$	±10	±13		
TR	Transient Response	Rise Time	$V_I = 20$ mV, $R_L = 2.0\ k\Omega$, $C_L = 100$ pF, $A_V = 1.0$		0.13		μs
		Overshoot			5.0		%
BW	Bandwidth		$A_V = 1.0$		3.0		MHz
SR	Slew Rate		$R_L = 2.0\ k\Omega$, $A_V = 1.0$		1.0		V/μs
CS	Channel Separation		f = 10 kHz, $R_S = 1.0\ k\Omega$ Open Loop		105		dB
			f = 10 kHz, $R_S = 1.0\ k\Omega$ $A_V = 100$		105		

The following specifications apply over the range of $0°C \le T_A \le +70°C$

V_{IO}	Input Offset Voltage	$R_S \le 10\ k\Omega$			7.5	mV
I_{IO}	Input Offset Current				300	nA
I_{IB}	Input Bias Current				800	nA
P_C	Power Consumption	$T_A = T_{A\ Max}$		180	300	mW
		$T_A = T_{A\ Min}$		240	400	
A_{VS}	Large Signal Voltage Gain	$R_L \ge 2.0\ k\Omega$, $V_O = \pm 10V$	15			V/mV
V_{OP}	Output Voltage Swing	$R_L = 2.0\ k\Omega$, $V_{CC} = \pm 15V$	±10			V

Note 1: $T_{J\ Max} = 150°C$ for the Molded DIP and SO-14, and 175°C for the Ceramic DIP.

Note 2: Ratings apply to ambient temperature at 25°C. Above this temperature, derate the 14L-Ceramic DIP at 9.1 mW/°C, the 14L-Molded DIP at 8.3 mW/°C, and the SO-14 at 7.5 mW/°C.

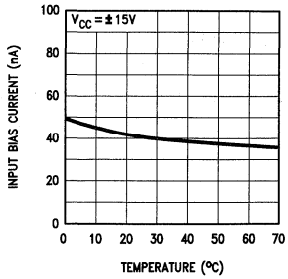
Note 3: For supply voltage less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

Note 4: Short circuit may be to ground, one amplifier only.

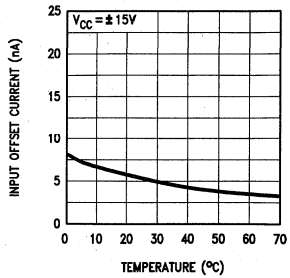
Note 5: For military specifications see RETS4136X for LM4136J.

Typical Performance Characteristics

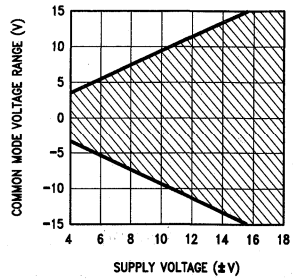
Input Bias Current vs Temperature



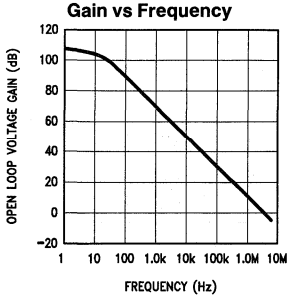
Input Offset Current vs Temperature



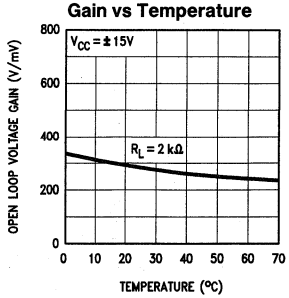
Common Mode Range vs Supply Voltage



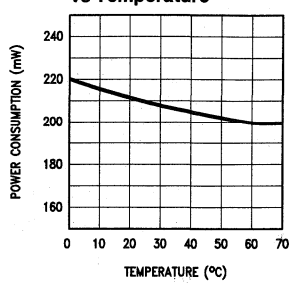
Open Loop Voltage Gain vs Frequency



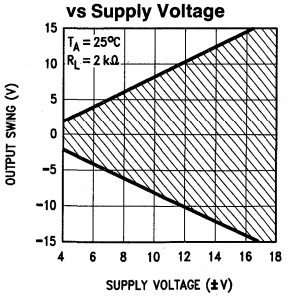
Open Loop Voltage Gain vs Temperature



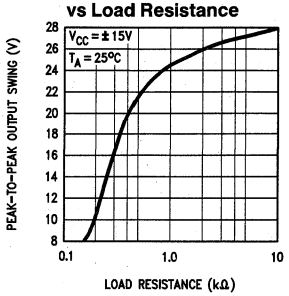
Power Consumption vs Temperature



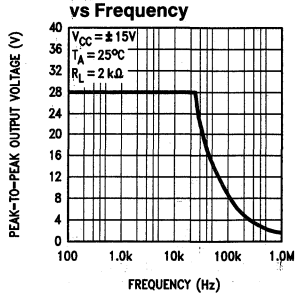
Typical Output Voltage vs Supply Voltage



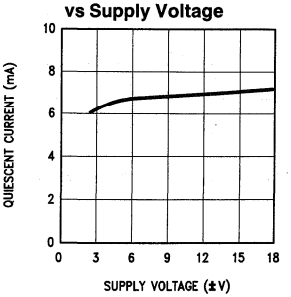
Output Voltage Swing vs Load Resistance



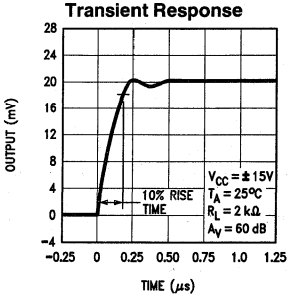
Output Voltage Swing vs Frequency



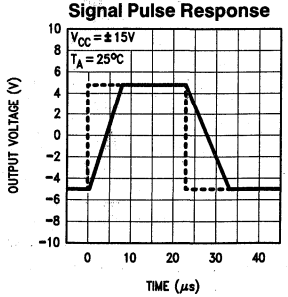
Quiescent Current vs Supply Voltage



Transient Response



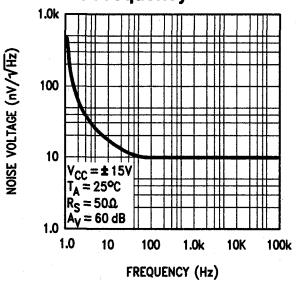
Voltage Follower Large Signal Pulse Response



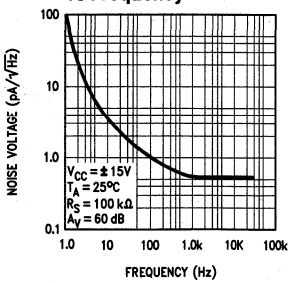
TL/H/10065–3

Typical Performance Characteristics (Continued)

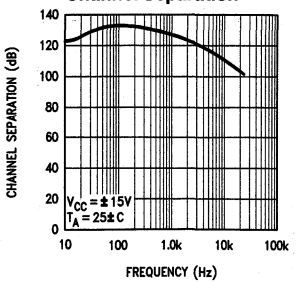
Input Noise Voltage vs Frequency



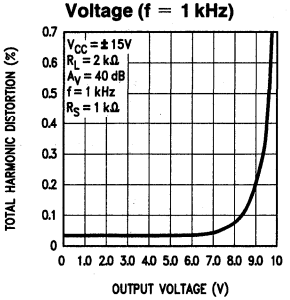
Input Noise Current vs Frequency



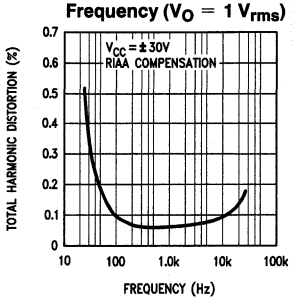
Channel Separation



Distortion vs Output Voltage (f = 1 kHz)



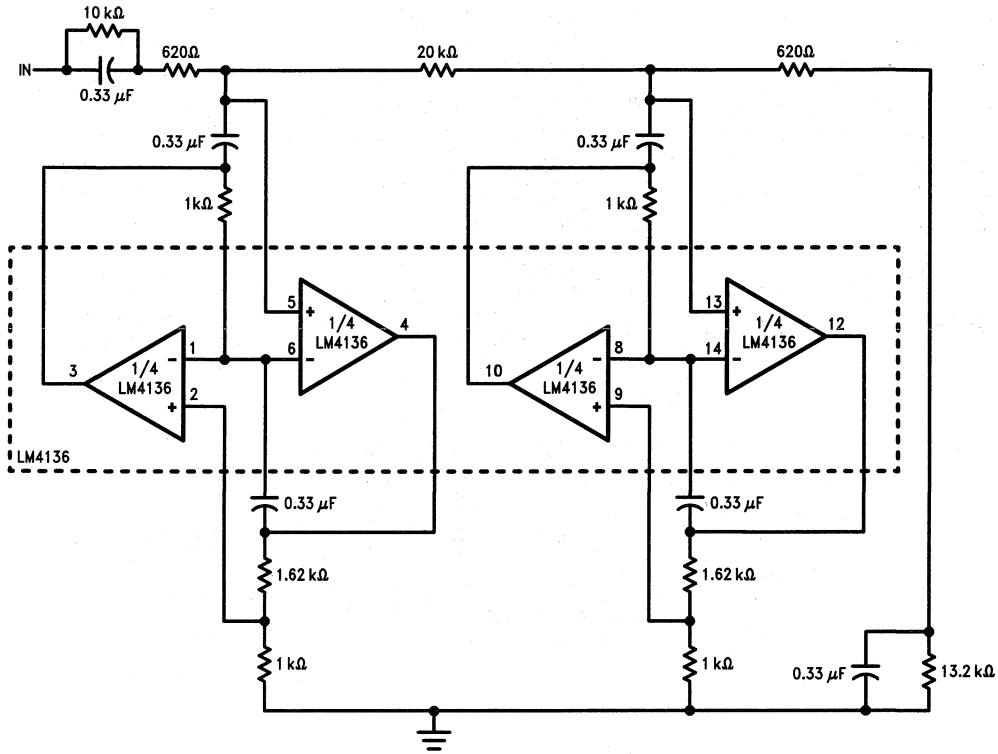
Distortion vs Frequency (V_O = 1 V_{rms})



TL/H/10065–4

Typical Applications

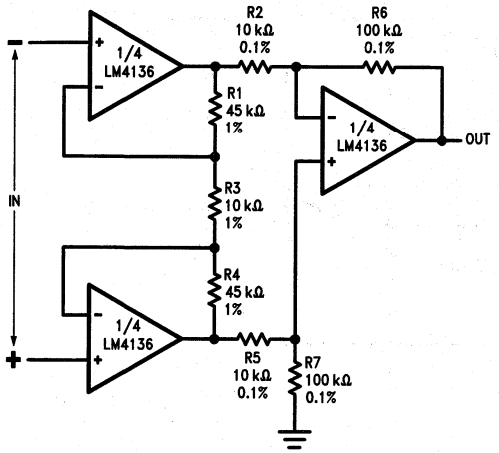
400 Hz Lowpass Butterworth Active Filter



TL/H/10065–5

Typical Applications (Continued)

Differential Input Instrumentation Amplifier with High Common Mode Rejection

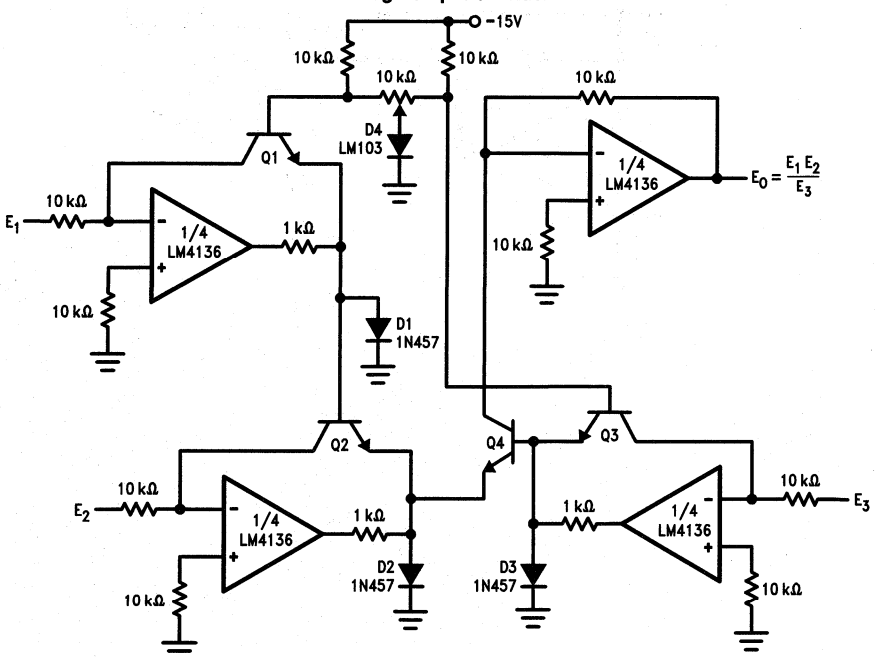


$$A_V = \frac{R6}{R2}\left(1 + \frac{2\,R1}{R3}\right)$$

Matching determines CMRR:
R1 = R4
R2 = R5
R6 = R7

TL/H/10065–6

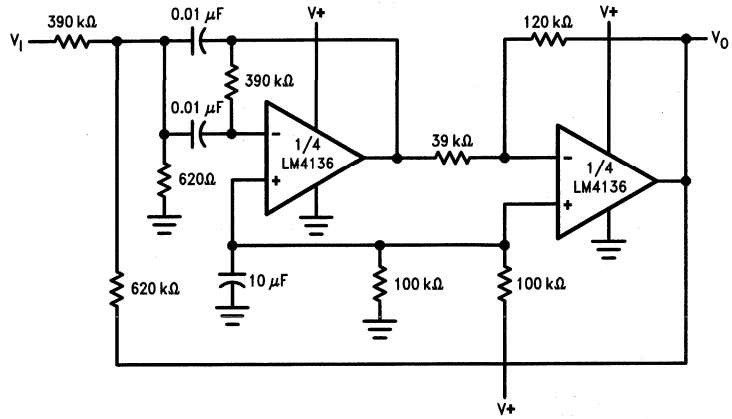
Analog Multiplier/Divider



TL/H/10065–7

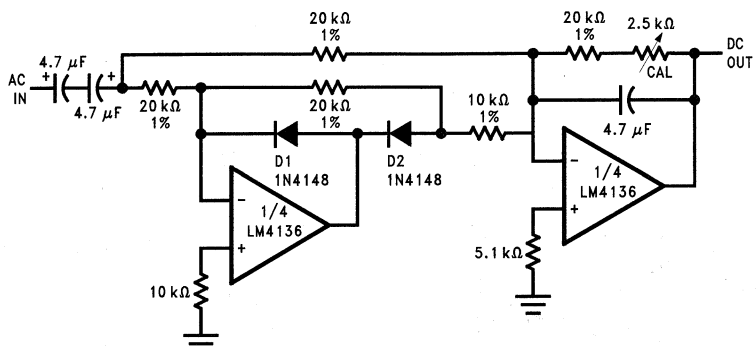
Typical Applications (Continued)

1 kHz Bandpass Active Filter



TL/H/10065–8

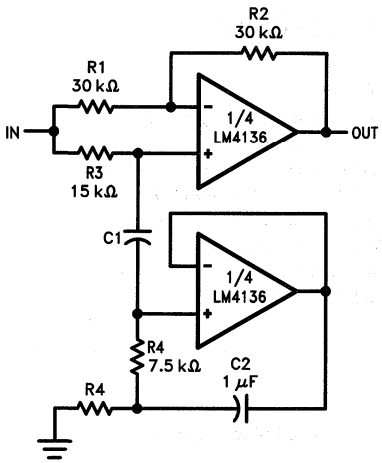
Full-Wave Rectifier and Averaging Filter



TL/H/10065–9

Typical Applications (Continued)

Notch Filter Using the LM4136 as a Gyrator

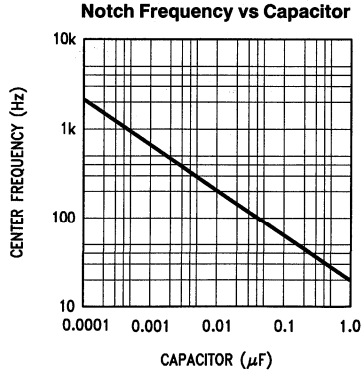


TL/H/10065–10

Trim R, Such That

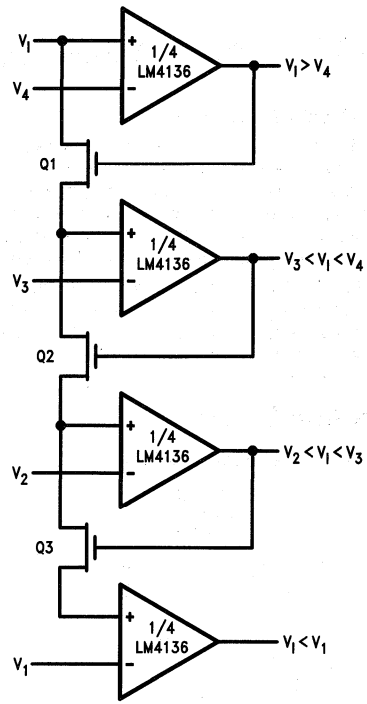
$$\frac{R1}{R2} = \frac{R3}{2\,R4}$$

Notch Frequency vs Capacitor



TL/H/10065–12

Multiple Aperture Window Discriminator



TL/H/10065–11

National Semiconductor

LM4250 Programmable Operational Amplifier

General Description

The LM4250 and LM4250C are extremely versatile programmable monolithic operational amplifiers. A single external master bias current setting resistor programs the input bias current, input offset current, quiescent power consumption, slew rate, input noise, and the gain-bandwidth product. The device is a truly general purpose operational amplifier.

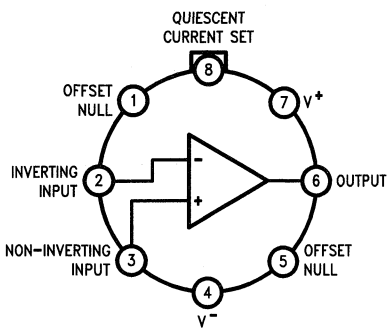
The LM4250C is identical to the LM4250 except that the LM4250C has its performance guaranteed over a 0°C to +70°C temperature range instead of the −55°C to +125°C temperature range of the LM4250.

Features

- ±1V to ±18V power supply operation
- 3 nA input offset current
- Standby power consumption as low as 500 nW
- No frequency compensation required
- Programmable electrical characteristics
- Offset voltage nulling capability
- Can be powered by two flashlight batteries
- Short circuit protection

Connection Diagrams

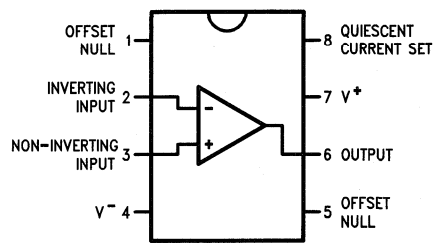
Metal Can Package



TL/H/9300–2

Top View

Dual-In-Line Package



TL/H/9300–5

Top View

Ordering Information

Temperature Range		Package	NSC Package Number
Military $-55°C \leq T_A \leq +125°C$	**Commercial** $0°C \leq T_A \leq +70°C$		
	LM4250CN	8-Pin Molded DIP	N08E
	LM4250CM	8-Pin Surface Mount	M08E
LM4250J LM4250J-MIL	LM4250CJ	8-Pin Ceramic DIP	J08E
LM4250H LM4250H-MIL	LM4250CH	8-Pin Metal Can	H08C

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.
(Note 2)

	LM4250	LM4250C
Supply Voltage	±18V	±18V
Operating Temp. Range	$-55°C \leq T_A \leq +125°C$	$0°C \leq T_A \leq +70°C$
Differential Input Voltage	±30V	±30V
Input Voltage (Note 1)	±15V	±15V
I_{SET} Current	150 nA	150 nA
Output Short Circuit Duration	Continuous	Continuous
T_{JMAX}		
H-Package	150°C	100°C
N-Package		100°C
J-Package	150°C	100°C
M-Package		100°C
Power Dissipation at $T_A = 25°C$		
H-Package (Still Air)	500 mW	300 mW
(400 LF/Min Air Flow)	1200 mW	1200 mW
N-Package		500 mW
J-Package	1000 mW	600 mW
M-Package		350 mW
Thermal Resistance (Typical) θ_{JA}		
H-Package (Still Air)	165°C/W	165°C/W
(400 LF/Min Air Flow)	65°C/W	65°C/W
N-Package		130°C/W
J-Package	108°C/W	108°C/W
M-Package		190°C/W
(Typical) θ_{JC}		
H-Package	21°C/W	21°C/W
Storage Temperature Range	−65°C to +150°C	−65°C to +150°C

Soldering Information

Dual-In-Line Package	
Soldering (10 seconds)	260°C
Small Outline Package	
Vapor Phase (60 seconds)	215°C
Infrared (15 seconds)	220°C

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

ESD tolerance (Note 3) 800V

Note 1: For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

Note 2: Refer to RETS4250X for military specifications.

Note 3: Human body model, 1.5 kΩ in series with 100 pF.

Resistor Biasing

Set Current Setting Resistor to V⁻

	I_{SET}				
V_S	0.1 μA	0.5 μA	1.0 μA	5 μA	10 μA
±1.5V	25.6 MΩ	5.04 MΩ	2.5 MΩ	492 kΩ	244 kΩ
±3.0V	55.6 MΩ	11.0 MΩ	5.5 MΩ	1.09 MΩ	544 kΩ
±6.0V	116 MΩ	23.0 MΩ	11.5 MΩ	2.29 MΩ	1.14 MΩ
±9.0V	176 MΩ	35.0 MΩ	17.5 MΩ	3.49 MΩ	1.74 MΩ
±12.0V	236 MΩ	47.0 MΩ	23.5 MΩ	4.69 MΩ	2.34 MΩ
±15.0V	296 MΩ	59.0 MΩ	29.5 MΩ	5.89 MΩ	2.94 MΩ

Electrical Characteristics LM4250 ($-55°C \le T_A \le +125°C$ unless otherwise specified.) $T_A = T_J$

Parameter	Conditions	$V_S = \pm 1.5V$			
		$I_{SET} = 1\ \mu A$		$I_{SET} = 10\ \mu A$	
		Min	Max	Min	Max
V_{OS}	$R_S \le 100\ k\Omega$, $T_A = 25°C$		3 mV		5 mV
I_{OS}	$T_A = 25°C$		3 nA		10 nA
I_{bias}	$T_A = 25°C$		7.5 nA		50 nA
Large Signal Voltage Gain	$R_L = 100\ k\Omega$, $T_A = 25°C$ $V_O = \pm 0.6V$, $R_L = 10\ k\Omega$	40k		50k	
Supply Current	$T_A = 25°C$		7.5 μA		80 μA
Power Consumption	$T_A = 25°C$		23 μW		240 μW
V_{OS}	$R_S \le 100\ k\Omega$		4 mV		6 mV
I_{OS}	$T_A = +125°C$ $T_A = -55°C$		5 nA 3 nA		10 nA 10 nA
I_{bias}			7.5 nA		50 nA
Input Voltage Range		±0.6V		±0.6V	
Large Signal Voltage Gain	$V_O = \pm 0.5V$, $R_L = 100\ k\Omega$ $R_L = 10\ k\Omega$	30k		30k	
Output Voltage Swing	$R_L = 100\ k\Omega$ $R_L = 10\ k\Omega$	±0.6V		±0.6V	
Common Mode Rejection Ratio	$R_S \le 10\ k\Omega$	70 dB		70 dB	
Supply Voltage Rejection Ratio	$R_S \le 10\ k\Omega$	76 dB		76 dB	
Supply Current			8 μA		90 μA
Power Consumption			24 μW		270 μW

Parameter	Conditions	$V_S = \pm 15V$			
		$I_{SET} = 1\ \mu A$		$I_{SET} = 10\ \mu A$	
		Min	Max	Min	Max
V_{OS}	$R_S \le 100\ k\Omega$, $T_A = 25°C$		3 mV		5 mV
I_{OS}	$T_A = 25°C$		3 nA		10 nA
I_{bias}	$T_A = 25°C$		7.5 nA		50 nA
Large Signal Voltage Gain	$R_L = 100\ k\Omega$, $T_A = 25°C$ $V_O = \pm 10V$, $R_L = 10\ k\Omega$	100k		100k	
Supply Current	$T_A = 25°C$		10 μA		90 μA
Power Consumption	$T_A = 25°C$		300 μW		2.7 mW
V_{OS}	$R_S \le 100\ k\Omega$		4 mV		6 mV
I_{OS}	$T_A = +125°C$ $T_A = -55°C$		25 nA 3 nA		25 nA 10 nA
I_{bias}			7.5 nA		50 nA
Input Voltage Range		±13.5V		±13.5V	
Large Signal Voltage Gain	$V_O = \pm 10V$, $R_L = 100\ k\Omega$ $R_L = 10\ k\Omega$	50k		50k	
Output Voltage Swing	$R_L = 100\ k\Omega$ $R_L = 10\ k\Omega$	±12V		±12V	
Common Mode Rejection Ratio	$R_S \le 10\ k\Omega$	70 dB		70 dB	
Supply Voltage Rejection Ratio	$R_S \le 10\ k\Omega$	76 dB		76 dB	
Supply Current			11 μA		100 μA
Power Consumption			330 μW		3 mW

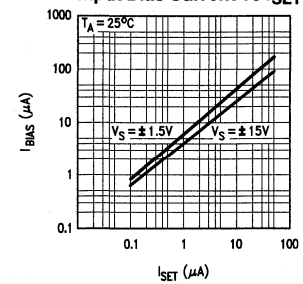
Electrical Characteristics LM4250C ($0°C \le T_A \le +70°C$ unless otherwise specified.) $T_A = T_J$

Parameter	Conditions	$V_S = \pm 1.5V$			
		$I_{SET} = 1\ \mu A$		$I_{SET} = 10\ \mu A$	
		Min	Max	Min	Max
V_{OS}	$R_S \le 100\ k\Omega$, $T_A = 25°C$		5 mV		6 mV
I_{OS}	$T_A = 25°C$		6 nA		20 nA
I_{bias}	$T_A = 25°C$		10 nA		75 nA
Large Signal Voltage Gain	$R_L = 100\ k\Omega$, $T_A = 25°C$ $V_O = \pm 0.6V$, $R_L = 10\ k\Omega$	25k		25k	
Supply Current	$T_A = 25°C$		8 μA		90 μA
Power Consumption	$T_A = 25°C$		24 μW		270 μW
V_{OS}	$R_S \le 10\ k\Omega$		6.5 mV		7.5 mV
I_{OS}			8 nA		25 nA
I_{bias}			10 nA		80 nA
Input Voltage Range		±0.6V		±0.6V	
Large Signal Voltage Gain	$V_O = \pm 0.5V$, $R_L = 100\ k\Omega$ $R_L = 10\ k\Omega$	25k		25k	
Output Voltage Swing	$R_L = 100\ k\Omega$ $R_L = 10\ k\Omega$	±0.6V		±0.6V	
Common Mode Rejection Ratio	$R_S \le 10\ k\Omega$	70 dB		70 dB	
Supply Voltage Rejection Ratio	$R_S \le 10\ k\Omega$	74 dB		74 dB	
Supply Current			8 μA		90 μA
Power Consumption			24 μW		270 μW

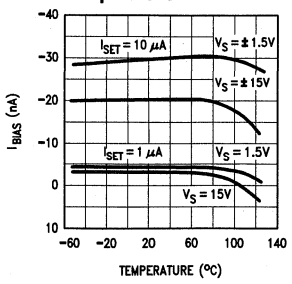
Parameter	Conditions	$V_S = \pm 15V$			
		$I_{SET} = 1\ \mu A$		$I_{SET} = 10\ \mu A$	
		Min	Max	Min	Max
V_{OS}	$R_S \le 100\ k\Omega$, $T_A = 25°C$		5 mV		6 mV
I_{OS}	$T_A = 25°C$		6 nA		20 nA
I_{bias}	$T_A = 25°C$		10 nA		75 nA
Large Signal Voltage Gain	$R_L = 100\ k\Omega$, $T_A = 25°C$ $V_O = \pm 10V$, $R_L = 10\ k\Omega$	60k		60k	
Supply Current	$T_A = 25°C$		11 μA		100 μA
Power Consumption	$T_A = 25°C$		330 μW		3 mW
V_{OS}	$R_S \le 100\ k\Omega$		6.5 mV		7.5 mV
I_{OS}			8 nA		25 nA
I_{bias}			10 nA		80 nA
Input Voltage Range		±13.5V		±13.5V	
Large Signal Voltage Gain	$V_O = \pm 10V$, $R_L = 100\ k\Omega$ $R_L = 10\ k\Omega$	50k		50k	
Output Voltage Swing	$R_L = 100\ k\Omega$ $R_L = 10\ k\Omega$	±12V		±12V	
Common Mode Rejection Ratio	$R_S \le 10\ k\Omega$	70 dB		70 dB	
Supply Voltage Rejection Ratio	$R_S \le 10\ k\Omega$	74 dB		74 dB	
Supply Current			11 μA		100 μA
Power Consumption			330 μW		3 mW

Typical Performance Characteristics

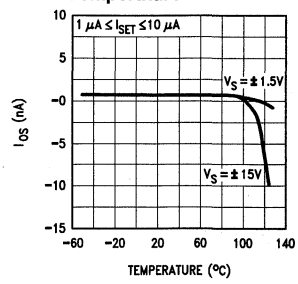
Input Bias Current vs I_{SET}



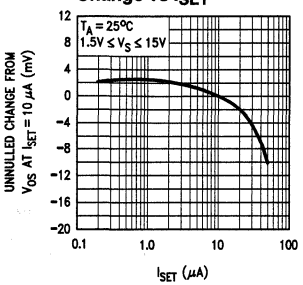
Input Bias Current vs Temperature



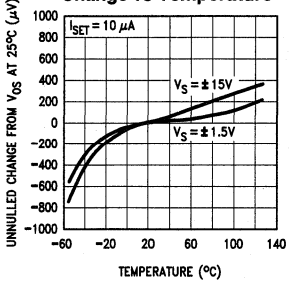
Input Offset Current vs Temperature



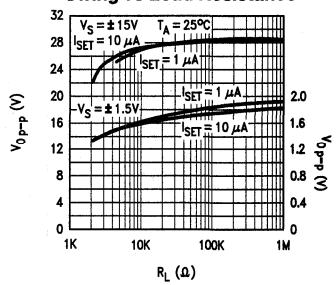
Unnulled Input Offset Voltage Change vs I_{SET}



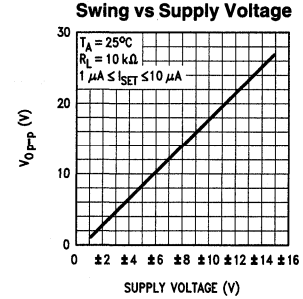
Unnulled Input Offset Voltage Change vs Temperature



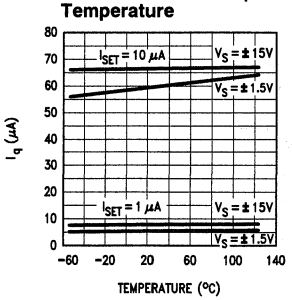
Peak to Peak Output Voltage Swing vs Load Resistance



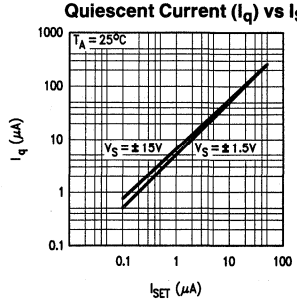
Peak to Peak Output Voltage Swing vs Supply Voltage



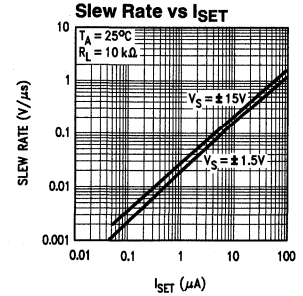
Quiescent Current (I_Q) vs Temperature



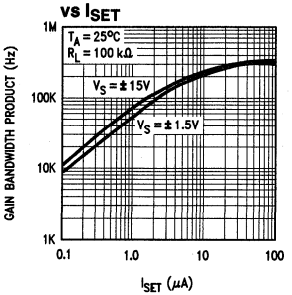
Quiescent Current (I_Q) vs I_{SET}



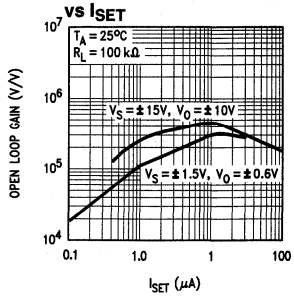
Slew Rate vs I_{SET}



Gain Bandwidth Product vs I_{SET}



Open Loop Voltage Gain vs I_{SET}



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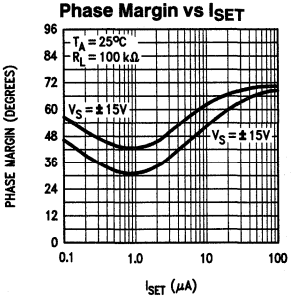
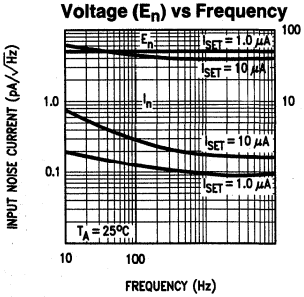
Typical Performance Characteristics (Continued)

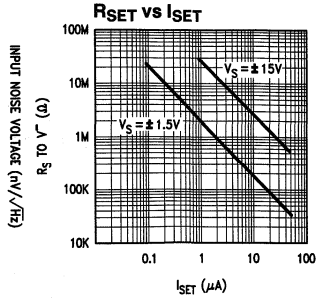
Phase Margin vs I_{SET}



Input Noise Current (I_n) and Voltage (E_n) vs Frequency



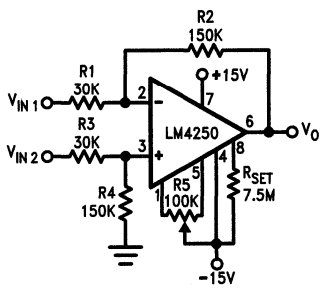
R_{SET} vs I_{SET}



TL/H/9300–7

Typical Applications

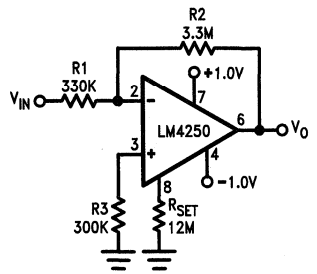
X5 Difference Amplifier



Quiescent P_D = 0.6 mW

TL/H/9300–3

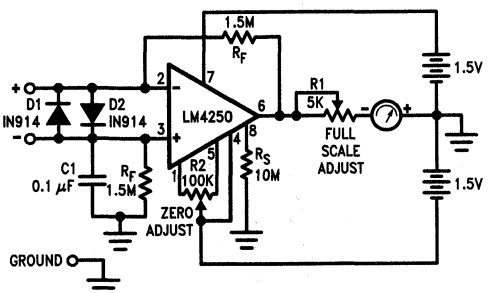
500 Nano-Watt X10 Amplifier



TL/H/9300–4

Quiescent P_D = 500 nW

Floating Input Meter Amplifier
100 nA Full Scale



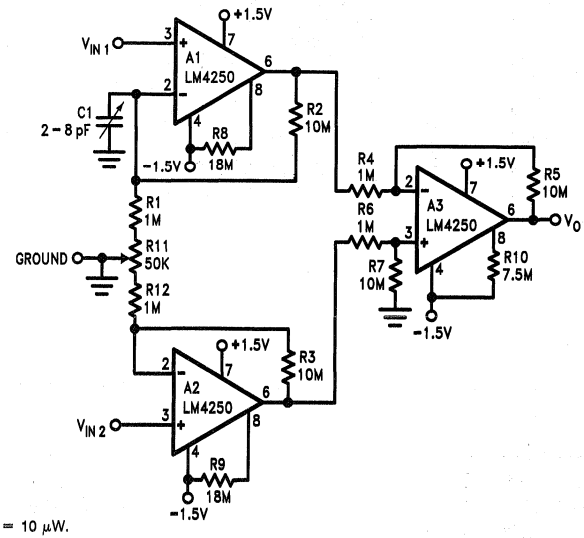
Quiescent P_D = 1.8 μW

*Meter movement (0–100 μA, 2 kΩ) marked for 0–100 nA full scale.

TL/H/9300–8

Typical Applications (Continued)

X100 Instrumentation Amplifier 10 μW



Note 1: Quiescent P_D = 10 μW.

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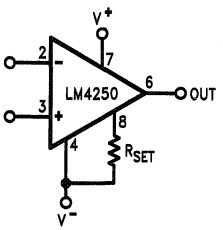
Note 2: R2, R3, R4, R5, R6 and R7 are 1% resistors.

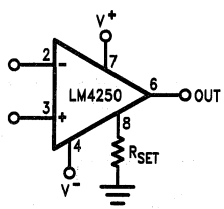
Note 3: R11 and C1 are for DC and AC common mode rejection adjustments.

R_{SET} Connected to V^-



TL/H/9300–10

R_{SET} Connected to Ground



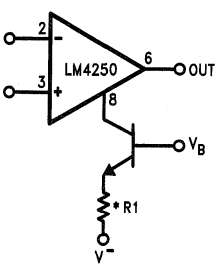
TL/H/9300–11

I_{SET} Equations:

$$I_{SET} \approx \frac{V^+ + |V^-| - 0.5}{R_{SET}}$$ where R_{SET} is connected to V^-

$$I_{SET} \approx \frac{V^+ - 0.5}{R_{SET}}$$ where R_{SET} is connected to ground.

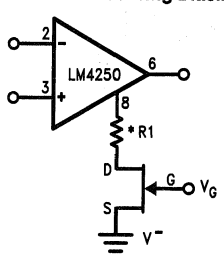
Transistor Current Sourcing Biasing



*R1 limits I_{SET} maximum

TL/H/9300–12

FET Current Sourcing Biasing



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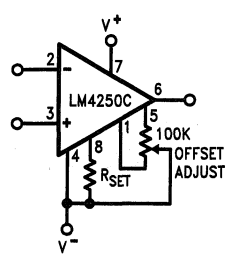
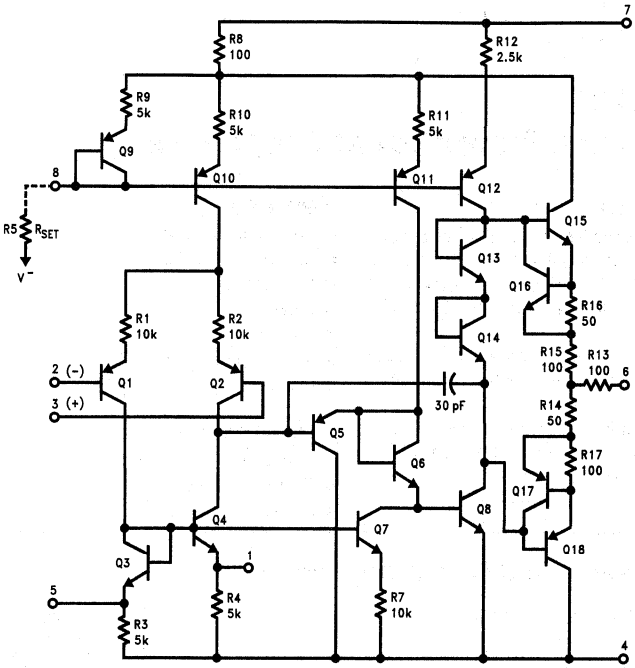
Offset Null Circuit



TL/H/9300–14

Schematic Diagram



TL/H/9300–1

National Semiconductor

LM6118/LM6218
Fast Settling Dual Operational Amplifiers

General Description

The LM6118 series are monolithic fast-settling unity-gain-compensated dual operational amplifiers with ±20 mA output drive capability. The PNP input stage has a typical bias current of 200 nA, and the operating supply voltage is ±5V to ±20V.

These dual op amps use slew enhancement with special mirror circuitry to achieve fast response and high gain with low total supply current.

The amplifiers are built on a junction-isolated VIP™ (Vertically Integrated PNP) process which produces fast PNP's that complement the standard NPN's.

Features

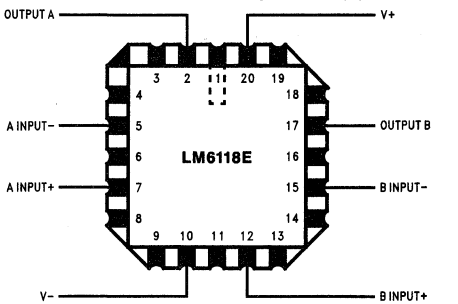
	Typical
■ Low offset voltage	0.2 mV
■ 0.01% settling time	400 ns
■ Slew rate $A_V = -1$	140 V/μs
■ Slew rate $A_V = +1$	75 V/μs
■ Gain bandwidth	17 MHz
■ Total supply current	5.5 mA
■ Output drives 50Ω load (±1V)	

Applications

- D/A converters
- Fast integrators
- Active filters

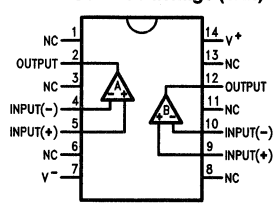
Connection Diagrams and Order Information

Ceramic Leadless Chip Carrier (E)



Order Number LM6118E/883*
See NS Package Number E20A

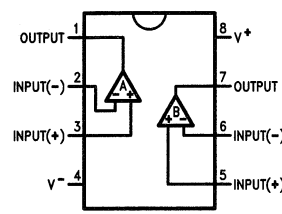
Small Outline Package (WM)



Top View

Order Number LM6218AWM or LM6218WM
See NS Package Number M14B

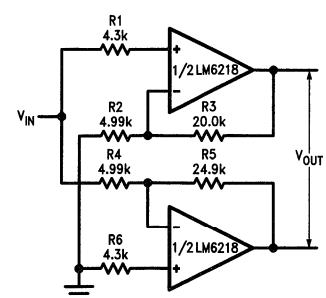
Dual-In-Line Package (J or N)



Top View

Order Number LM6118N, LM6118J/883*,
LM6218AN or LM6218N
See NS Package Number J08A or N08E

Typical Applications



Single ended input to differential output
A_V = 10, BW = 3.2 MHz
40 V_{PP} Response = 1.4 MHz
V_S = ±15V

Wide-Band, Fast-Settling
40 V_{PP} Amplifier

*Available per SMD #5962-9156501

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Total Supply Voltage	42V
Input Voltage	(Note 2)
Differential Input Current (Note 3)	±10 mA
Output Current (Note 4)	Internally Limited
Power Dissipation (Note 5)	500 mW
ESD Tolerance (C = 100 pF, R = 1.5 kΩ)	±2 kV
Junction Temperature	150°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec.)	300°C

Operating Temp. Range

LM6118	−55°C to +125°C
LM6218A	−40°C to +85°C
LM6218	−40°C to +85°C

Electrical Characteristics

$\pm 5V \le V_S \le \pm 20V$, $V_{CM} = 0V$, $V_{OUT} = 0V$, $I_{OUT} = 0A$, unless otherwise specified. Limits with standard type face are for $T_J = 25°C$, and **Bold Face Type** are for **Temperature Extremes.**

Parameter	Conditions	Typ 25°C	LM6118 Limits (Notes 6 & 7)	LM6218A Limits (Note 6)	LM6218 Limits (Note 6)	Units
Input Offset Voltage	$V_S = \pm 15V$	0.2	1 **2**	1 **2**	3 **4**	mV (max)
Input Offset Voltage	$V^- + 3V \le V_{CM} \le V^+ - 3.5V$	0.3	1.5 **2.5**	1.5 **2.5**	3.5 **4.5**	mV (max)
Input Offset Current	$V^- + 3V \le V_{CM} \le V^+ - 3.5V$	20	50 **250**	50 **100**	100 **200**	nA (max)
Input Bias Current	$V^- + 3V \le V_{CM} \le V^+ - 3.5V$	200	350 **950**	350 **950**	500 **1250**	nA (max)
Input Common Mode Rejection Ratio	$V^- + 3V \le V_{CM} \le V^+ - 3.5V$ $V_S = \pm 20V$	100	90 **85**	90 **85**	80 **75**	dB (min)
Positive Power Supply Rejection Ratio	$V^- = -15V$ $5V \le V^+ \le 20V$	100	90 **85**	90 **85**	80 **75**	dB (min)
Negative Power Supply Rejection Ratio	$V^+ = 15V$ $-20V \le V^- \le -5V$	100	90 **85**	90 **85**	80 **75**	dB (min)
Large Signal Voltage Gain	$V_{out} = \pm 17V$ $R_L = 10k$ $V_S = \pm 20V$	500	150 **100**	150 **100**	100 **70**	V/mV (min)
	$V_{out} = \pm 10V$ $R_L = 500$ $V_S = \pm 15V$ (±20 mA)	200	50 **30**	50 **30**	40 **25**	V/mV (min)
Total Supply Current	$V_S = \pm 15V$	5.5	7 **7.5**	7 **7.5**	7 **7.5**	mA (max)
Output Current Limit	$V_S = \pm 15V$, Pulsed	65	100	100	100	mA (max)
Slew Rate, Av = −1	$V_S = \pm 15V$, $V_{out} = \pm 10V$ $R_S = R_f = 2k$, $C_f = 10$ pF	140	100 **50**	100 **50**	100 **50**	V/μs (min)
Slew Rate, Av = +1	$V_S = \pm 15V$, $V_{out} = \pm 10V$ $R_S = R_f = 2k$, $C_f = 10$ pF	75	50 **30**	50 **30**	50 **30**	V/μs (min)
Gain-Bandwidth Product	$V_S = \pm 15V$, $f_o = 200$ kHz	17	14	14	13	MHz (min)
0.01% Settling Time $A_V = -1$	$\Delta V_{out} = 10V$, $V_S = \pm 15V$, $R_S = R_f = 2k$, $C_f = 10$ pF	400				ns
Input Capacitance	Inverter	5				pF
	Follower	3				pF

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its rated operating conditions.

Note 2: Input voltage range is ($V^+ - 1V$) to (V^-).

Note 3: The inputs are shunted with three series-connected diodes back-to-back for input differential clamping. Therefore differential input voltages greater than about 1.8V will cause excessive current to flow unless limited to less than 10 mA.

Note 4: Current limiting protects the output from a short to ground or any voltage less than the supplies. With a continuous overload, the package dissipation must be taken into account and heat sinking provided when necessary.

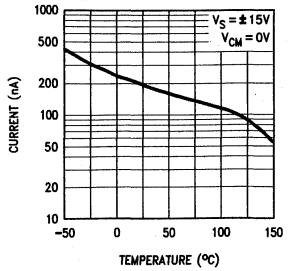
Note 5: Devices must be derated using a thermal resistance of 90°C/W for the N, J and WM packages.

Note 6: Limits are guaranteed by testing or correlation.

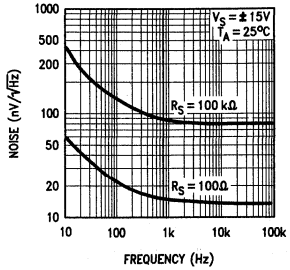
Note 7: A military RETS specification is available on request. At the time of printing, LM6118J/883 and LM6118E/883 RETS spec complied with the **Boldface** limits in this column.

Typical Performance Characteristics

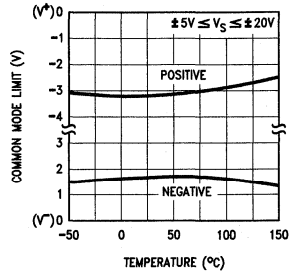
Input Bias Current



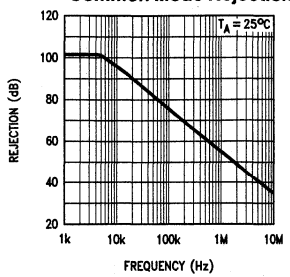
Input Noise Voltage



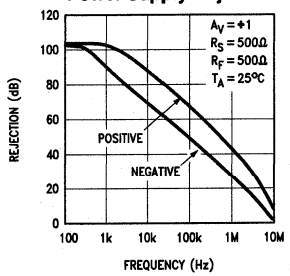
Common Mode Limits



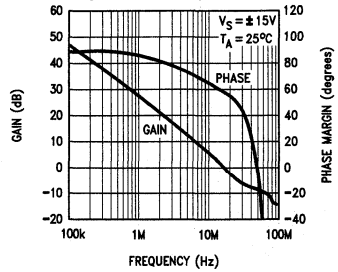
Common Mode Rejection



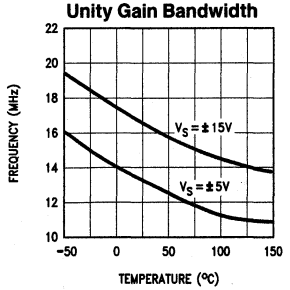
Power Supply Rejection



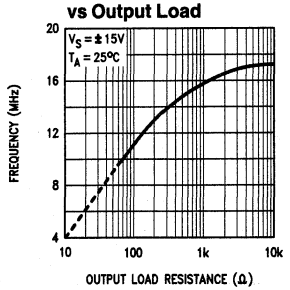
Frequency Response High Frequency



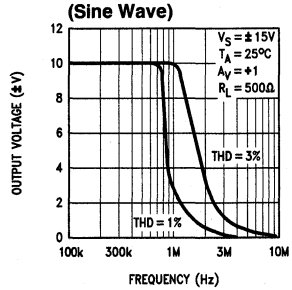
Unity Gain Bandwidth



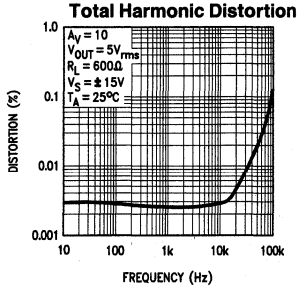
Unity Gain Bandwidth vs Output Load



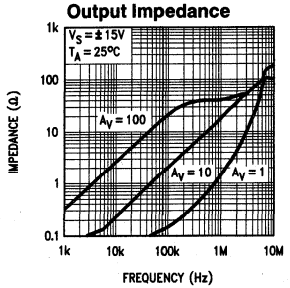
Large Signal Response (Sine Wave)



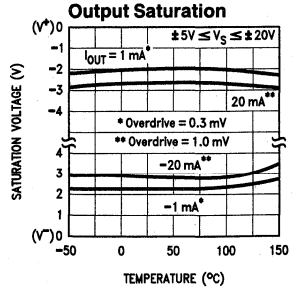
Total Harmonic Distortion



Output Impedance



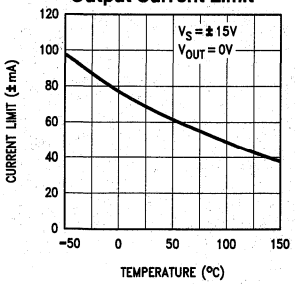
Output Saturation



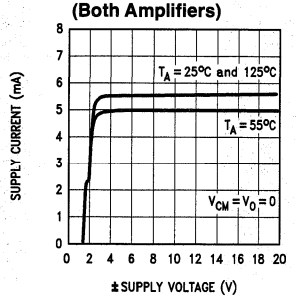
TL/H/10254–5

Typical Performance Characteristics (Continued)

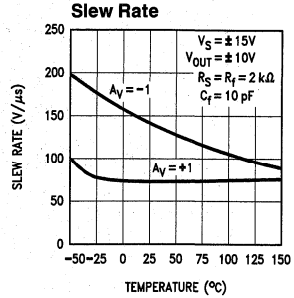
Output Current Limit



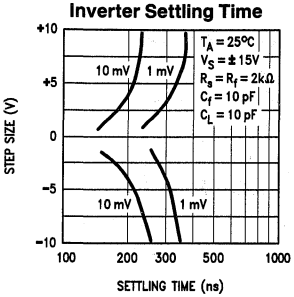
Supply Current (Both Amplifiers)



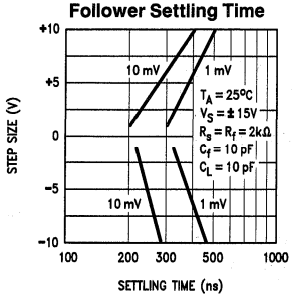
Slew Rate



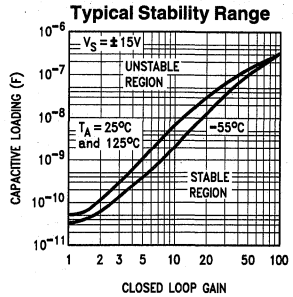
Inverter Settling Time



Follower Settling Time

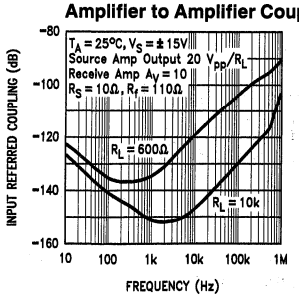


Typical Stability Range



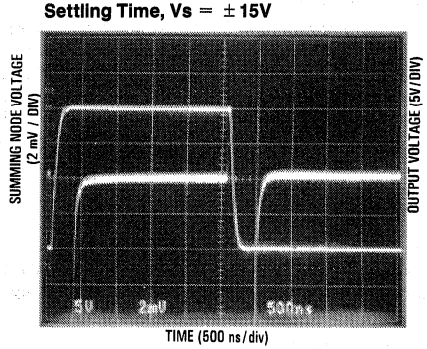
TL/H/10254–6

Amplifier to Amplifier Coupling



TL/H/10254–23

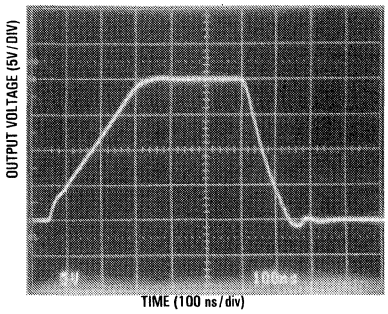
Settling Time, Vs = ±15V



TL/H/10254–7

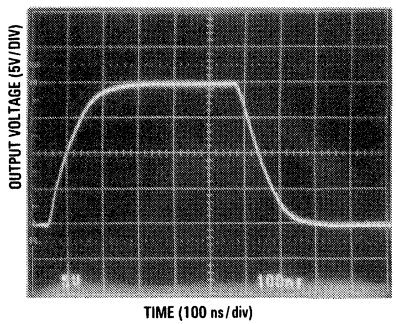
Typical Performance Characteristics (Continued)

Step Response, Av = +1, Vs = ±15V



TL/H/10254–8

Step Response, Av = −1, Vs = ±15V



TL/H/10254–9

Application Information

General

The LM6118 series are high-speed, fast-settling dual op-amps. To insure maximum performance, circuit board layout is very important. Minimizing stray capacitance at the inputs and reducing coupling between the amplifier's input and output will minimize problems.

Supply Bypassing

To assure stability, it is recommended that each power supply pin be bypassed with a 0.1 μF low inductance capacitor near the device. If high frequency spikes from digital circuits or switching supplies are present, additional filtering is recommended. To prevent these spikes from appearing at the output, R-C filtering of the supplies near the device may be necessary.

Power Dissipation

These amplifiers are specified to 20 mA output current. If accompanied with high supply voltages, relatively high power dissipation in the device will occur, resulting in high junction temperatures. In these cases the package thermal resistance must be taken into consideration. (See Note 5 under Electrical Characteristics.) For high dissipation, an N package with large areas of copper on the pc board is recommended.

Amplifier Shut Down

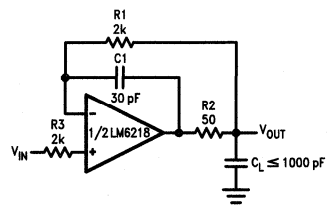
If one of the amplifiers is not used, it can be shut down by connecting both the inverting and non-inverting inputs to the V^- pin. This will reduce the power supply current by approximately 25%.

Capacitive Loading

Maximum capacitive loading is about 50 pF for a closed-loop gain of +1, before the amplifier exhibits excessive ringing and becomes unstable. A curve showing maximum capacitive loads, with different closed-loop gains, is shown in the Typical Performance Characteristics section.

To drive larger capacitive loads at low closed-loop gains, isolate the amplifier output from the capacitive load with 50Ω. Connect a small capacitor directly from the amplifier output to the inverting input. The feedback loop is closed from the isolated output with a series resistor to the inverting input.

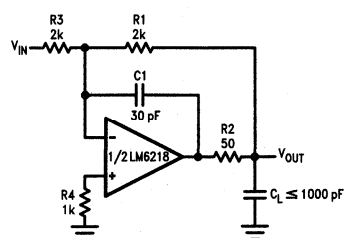
Voltage Follower



TL/H/10254–10

For C_L = 1000 pF, Small signal BW = 5 MHz
20 V_{p-p} BW = 500 kHz

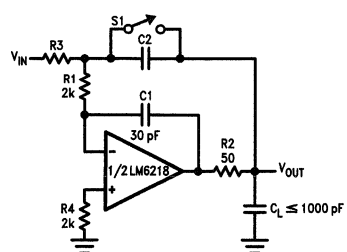
Inverter



TL/H/10254–11

Settling time to 0.01%, 10V Step
For C_L = 1000 pF, settling time ≈ 1500 ns
For C_L = 300 pF, settling time ≈ 500 ns

Integrator



TL/H/10254–12

Application Information (Continued)

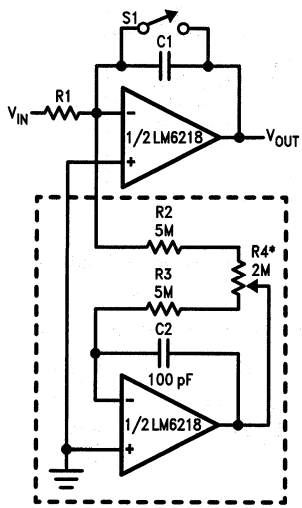
Examples of unity gain connections for a voltage follower, Inverter, and integrator driving capacitive loads up to 1000 pF are shown here. Different R1–C1 time constants and capacitive loads will have an effect on settling times.

Input Bias Current Compensation

Input bias current of the first op amp can be reduced or balanced out by the second op amp. Both amplifiers are laid out in mirror image fashion and in close proximity to each other, thus both input bias currents will be nearly identical and will track with temperature. With both op amp inputs at the same potential, a second op amp can be used to convert bias current to voltage, and then back to current feeding the first op amp using large value resistors to reduce the bias current to the level of the offset current.

Examples are shown here for an inverting application, (a) where the inputs are at ground potential, and a second circuit (b) for compensating bias currents for both inputs.

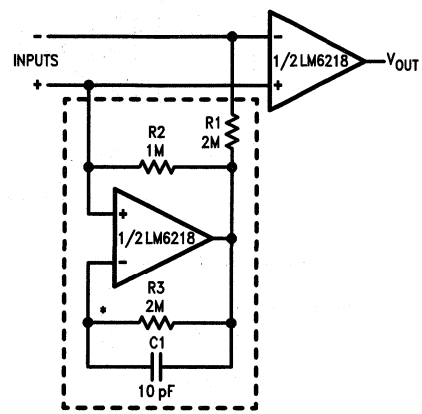
Bias Current Compensation



*adjust for zero integrator drift

TL/H/10254–13

(a) Inverting Input Bias Compensation for Integrator Application

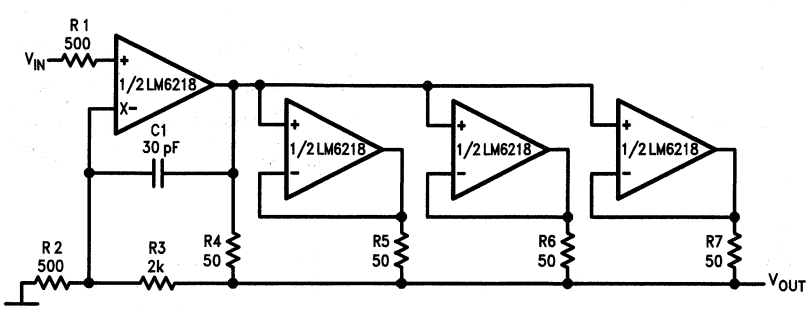


TL/H/10254–14

*mount resistor close to input pin to minimize stray capacitance

(b) Compensation to Both Inputs

Amplifier/Parallel Buffer

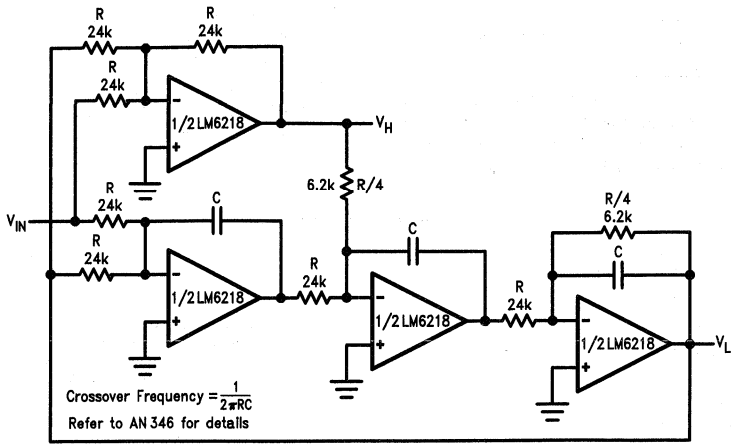


TL/H/10254–15

A_V = +5, $I_{OUT} \leq$ 80 mA
V_S = ±15V, $C_L \leq$ 0.01 μF
Large and small signal B.W. = 1.3 MHz (THD = 3%)

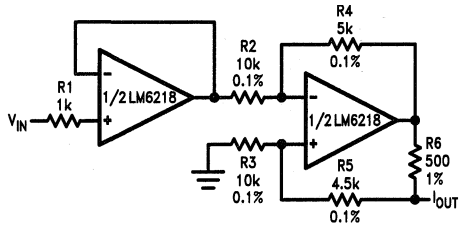
Application Information (Continued)

Constant-Voltage Crossover Network With 12 dB/Octave Slope



TL/H/10254–16

Bilateral Current Source



TL/H/10254–17

$V_S = \pm 15V, -10 \leq V_{IN} \leq 10V$

$$\frac{I_{OUT}}{V_{IN}} = \frac{R4}{R2\,R6} = \frac{1\,mA}{1V}$$

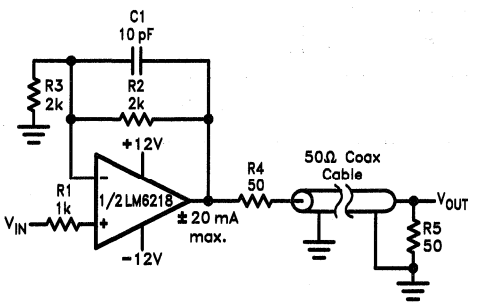
Output dynamic range = 10V − R6 $|I_{OUT}|$

R_L = 500Ω, small signal BW = 6 MHz

Large signal response = 800 kHz

$$C_{out}\ \text{equiv.} = \frac{R2 + R4}{2\pi f_O\, R2\, R6} = 32\ pF\ (f_O = 15\ MHz)$$

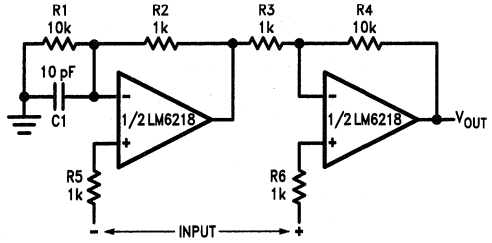
Coaxial Cable Driver



TL/H/10254–19

Small signal (200 mV_{p-p}) BW ≈ 5 MHz

Instrumentation Amplifier

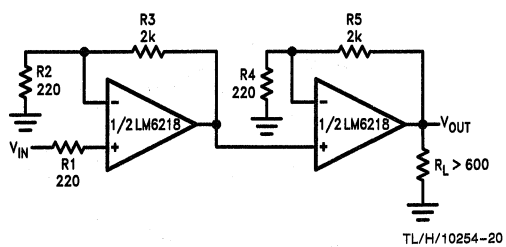


TL/H/10254–18

A_V = 10, V_S = ±15V, All resistors 0.01%

Small signal and large signal (20 V_{P-P}) B.W. ≈ 800 kHz

150 MHz Gain-Bandwidth Amplifier



TL/H/10254–20

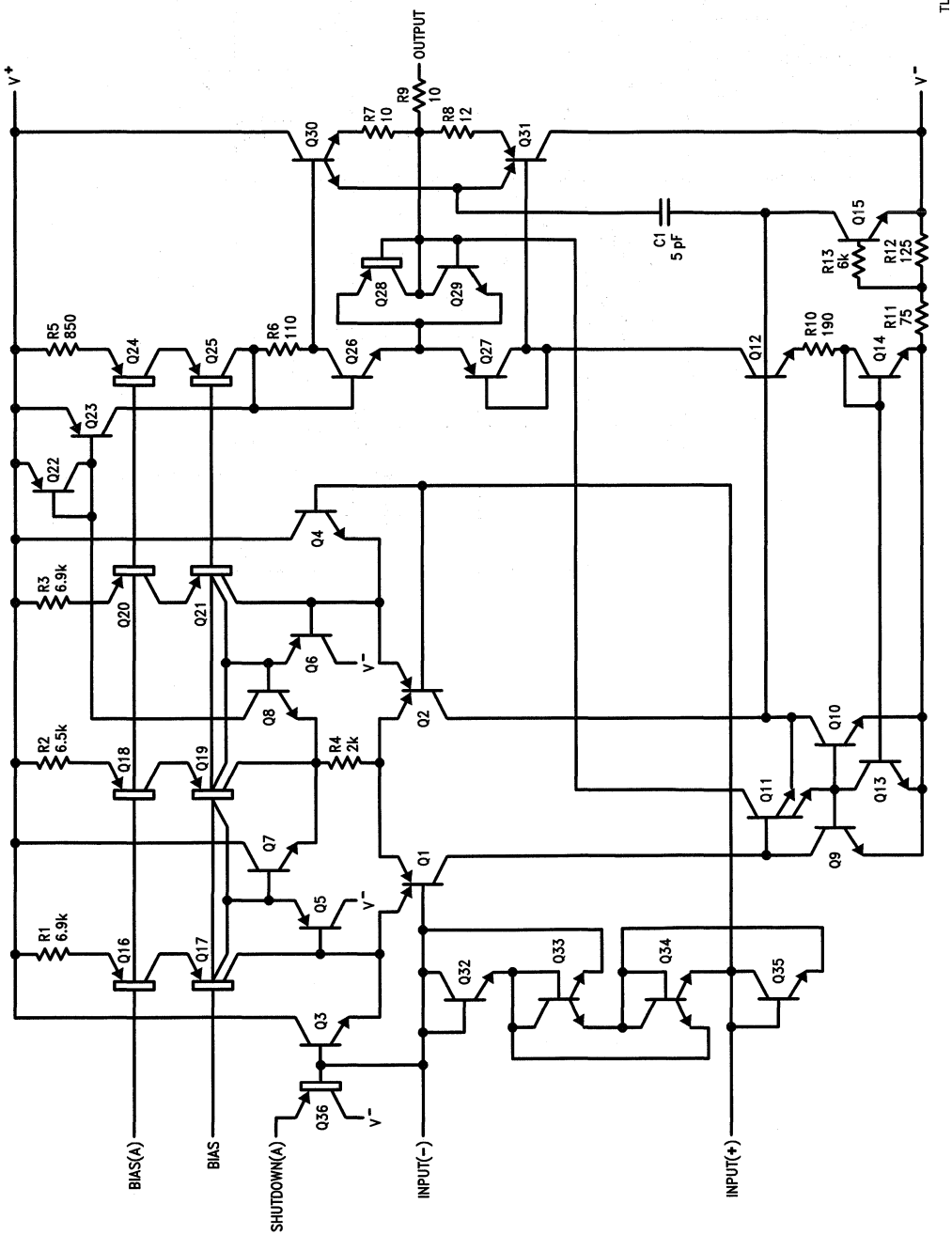
A_V = 100, V_S = ±15V,

Small signal BW ≈ 1.5 MHz

Large signal BW (20 V_{p-p}) ≈ 800 kHz

Schematic Diagram

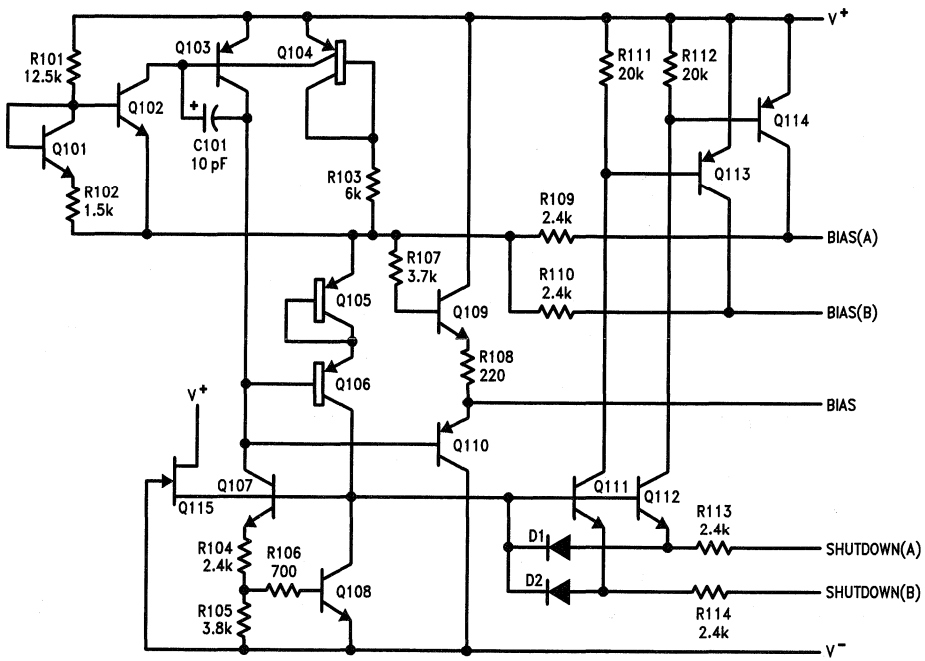
½ LM6116 (Op Amp A)



TL/H/10254–21

Schematic Diagram (Continued)

Bias Circuit



TL/H/10254–22

National Semiconductor

LM6161/LM6261/LM6361
High Speed Operational Amplifier

General Description

The LM6161 family of high-speed amplifiers exhibits an excellent speed-power product in delivering 300 V/μs and 50 MHz unity gain stability with only 5 mA of supply current. Further power savings and application convenience are possible by taking advantage of the wide dynamic range in operating supply voltage which extends all the way down to +5V.

These amplifiers are built with National's VIP™ (Vertically Integrated PNP) process which provides fast PNP transistors that are true complements to the already fast NPN devices. This advanced junction-isolated process delivers high speed performance without the need for complex and expensive dielectric isolation.

Features

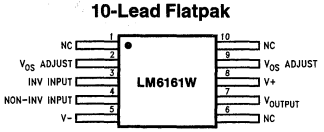
■ High slew rate	300 V/μs
■ High unity gain freq	50 MHz
■ Low supply current	5 mA
■ Fast settling	120 ns to 0.1%
■ Low differential gain	<0.1%
■ Low differential phase	0.1°
■ Wide supply range	4.75V to 32V
■ Stable with unlimited capacitive load	
■ Well behaved; easy to apply	

Applications

- Video amplifier
- High-frequency filter
- Wide-bandwidth signal conditioning
- Radar
- Sonar

Connection Diagrams

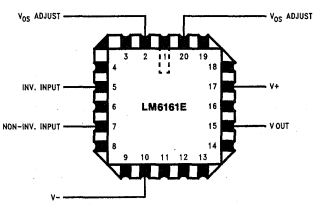
10-Lead Flatpak



TL/H/9057–13

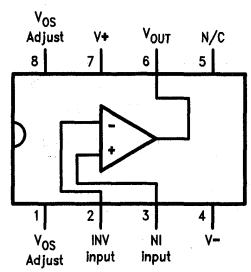
See NS Package Number W10A

20-Lead LCC



TL/H/9057–14

See NS Package Number E20A



TL/H/9057–5

See NS Package Number J08A, N08E or M08A

Temperature Range			Package	NSC Drawing
Military $-55°C \le T_A \le +125°C$	**Industrial** $-25°C \le T_A \le +85°C$	**Commercial** $0°C \le T_A \le +70°C$		
	LM6261N	LM6361N	8-Pin Molded DIP	N08E
LM6161J LM6161J/883 5962-8962101PA	LM6261J	LM6361J	8-Pin Ceramic DIP	J08A
	LM6261M	LM6361M	8-Pin Molded Surface Mt.	M08A
LM6161E/883 5962-89621012A			20-Lead LCC	E20A
LM6161W/883 5962-8962101HA			10-Pin Ceramic Flatpak	W10A

1

Absolute Maximum Ratings (Note 12)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage ($V^+ - V^-$)	36V
Differential Input Voltage (Note 8)	±8V
Common-Mode Voltage Range (Note 10)	$(V^+ - 0.7V)$ to $(V^- - 7V)$
Output Short Circuit to GND (Note 1)	Continuous
Soldering Information	
Dual-In-Line Package (N, J)	
Soldering (10 sec.)	260°C
Small Outline Package (M)	
Vapor Phase (60 sec.)	215°C
Infrared (15 sec.)	220°C

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

Storage Temp Range	−65°C to +150°C
Max Junction Temperature	150°C
ESD Tolerance (Notes 6 and 7)	±700V

Operating Ratings (Note 12)

Temperature Range (Note 2)	
LM6161	$-55°C \le T_J \le +125°C$
LM6261	$-25°C \le T_J \le +85°C$
LM6361	$0°C \le T_J \le +70°C$
Supply Voltage Range	4.75V to 32V

DC Electrical Characteristics

The following specifications apply for Supply Voltage = ±15V, $V_{CM} = 0$, $R_L \ge 100\ k\Omega$ and $R_S = 50\Omega$ unless otherwise noted. **Boldface** limits apply for $T_J = T_{MIN}$ to T_{MAX}; all other limits $T_J = 25°C$.

Symbol	Parameter	Conditions	Typ	LM6161 Limit (Notes 3, 11)	LM6261 Limit (Note 3)	LM6361 Limit (Note 3)	Units
V_{OS}	Input Offset Voltage		5	7 **10**	7 **9**	20 **22**	mV Max
V_{OS} Drift	Input Offset Voltage Average Drift		10				µV/°C
I_b	Input Bias Current		2	3 **6**	3 **5**	5 **6**	µA Max
I_{OS}	Input Offset Current		150	350 **800**	350 **600**	1500 **1900**	nA Max
I_{OS} Drift	Input Offset Current Average Drift		0.4				nA/°C
R_{IN}	Input Resistance	Differential	325				kΩ
C_{IN}	Input Capacitance	A_V = +1 @ 10 MHz	1.5				pF
A_{VOL}	Large Signal Voltage Gain	V_{OUT} = ±10V, R_L = 2 kΩ (Note 9)	750	550 **300**	550 **400**	400 **350**	V/V Min
		R_L = 10 kΩ (Note 9)	2900				V/V
V_{CM}	Input Common-Mode Voltage Range	Supply = ±15V	+14.0	+13.9 **+13.8**	+13.9 **+13.8**	+13.8 **+13.7**	Volts Min
			−13.2	−12.9 **−12.7**	−12.9 **−12.7**	−12.8 **−12.7**	Volts Min
		Supply = +5V (Note 4)	4.0	3.9 **3.8**	3.9 **3.8**	3.8 **3.7**	Volts Min
			1.8	2.0 **2.2**	2.0 **2.2**	2.1 **2.2**	Volts Max
CMRR	Common-Mode Rejection Ratio	$-10V \le V_{CM} \le +10V$	94	80 **74**	80 **76**	72 **70**	dB Min
PSRR	Power Supply Rejection Ratio	$\pm 10V \le V^{\pm} \le \pm 16V$	90	80 **74**	80 **76**	72 **70**	dB Min
V_O	Output Voltage Swing	Supply = ±15V and R_L = 2 kΩ	+14.2	+13.5 **+13.3**	+13.5 **+13.3**	+13.4 **+13.3**	Volts Min
			−13.4	−13.0 **−12.7**	−13.0 **−12.8**	−12.9 **−12.8**	Volts Min

DC Electrical Characteristics (Continued)

The following specifications apply for Supply Voltage = ±15V, V_{CM} = 0, $R_L \geq 100\ k\Omega$ and $R_S = 50\Omega$ unless otherwise noted. **Boldface** limits apply for $T_J = T_{MIN}$ to T_{MAX}; all other limits T_J = 25°C.

Symbol	Parameter	Conditions	Typ	LM6161 Limit (Notes 3, 11)	LM6261 Limit (Note 3)	LM6361 Limit (Note 3)	Units
V_O (Continued)	Output Voltage Swing (Continued)	Supply = +5V and R_L = 2 kΩ (Note 4)	4.2	3.5 **3.3**	3.5 **3.3**	3.4 **3.3**	Volts Min
			1.3	1.7 **2.0**	1.7 **1.9**	1.8 **1.9**	Volts Max
	Output Short Circuit Current	Source	65	30 **20**	30 **25**	30 **25**	mA Min
		Sink	65	30 **20**	30 **25**	30 **25**	mA Min
I_S	Supply Current		5.0	6.5 **6.8**	6.5 **6.7**	6.8 **6.9**	mA Max

AC Electrical Characteristics

The following specifications apply for Supply Voltage = ±15V, V_{CM} = 0, $R_L \geq 100\ k\Omega$ and $R_S = 50\Omega$ unless otherwise noted. **Boldface** limits apply for $T_J = T_{MIN}$ to T_{MAX}; all other limits T_J = 25°C.

Symbol	Parameter	Conditions	Typ	LM6161 Limit (Notes 3, 11)	LM6261 Limit (Note 3)	LM6361 Limit (Note 3)	Units
GBW	Gain-Bandwidth Product	@ f = 20 MHz	50	40 **30**	40 **35**	35 **32**	MHz Min
		Supply = ±5V	35				MHz
SR	Slew Rate	A_V = +1 (Note 8)	300	200 **180**	200 **180**	200 **180**	V/μs Min
		Supply = ±5V (Note 8)	200				V/μs
PBW	Power Bandwidth	V_{OUT} = 20 V_{PP}	4.5				MHz
t_S	Settling Time	10V Step to 0.1% A_V = −1, R_L = 2 kΩ	120				ns
ϕm	Phase Margin		45				Deg
A_D	Differential Gain	NTSC, A_V = +4	<0.1				%
ϕD	Differential Phase	NTSC, A_V = +4	0.1				Deg
e_{np-p}	Input Noise Voltage	f = 10 kHz	15				nV/√Hz
i_{np-p}	Input Noise Current	f = 10 kHz	1.5				pA/√Hz

Note 1: Continuous short-circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C.

Note 2: The typical junction-to-ambient thermal resistance of the molded plastic DIP (N) is 105°C/W, the molded plastic SO (M) package is 155°C/W, and the cerdip (J) package is 125°C/W. All numbers apply for packages soldered directly into a printed circuit board.

Note 3: Limits are guaranteed by testing or correlation.

Note 4: For single supply operation, the following conditions apply: V^+ = 5V, V^- = 0V, V_{CM} = 2.5V, V_{OUT} = 2.5V. Pin 1 & Pin 8 (Vos Adjust) are each connected to Pin 4 (V^-) to realize maximum output swing. This connection will degrade V_{OS}, V_{OS} Drift, and Input Voltage Noise.

Note 5: $C_L \leq 5$ pF.

Note 6: In order to achieve optimum AC performance, the input stage was designed without protective clamps. Exceeding the maximum differential input voltage results in reverse breakdown of the base-emitter junction of one of the input transistors and probable degradation of the input parameters (especially Vos, Ios, and Noise).

Note 7: The average voltage that the weakest pin combinations (those involving Pin 2 or Pin 3) can withstand and still conform to the datasheet limits. The test circuit used consists of the human body model of 100 pF in series with 1500Ω.

Note 8: V_{IN} = 8V step. For supply = ±5V, V_{IN} = 5V step.

Note 9: Voltage Gain is the total output swing (20V) divided by the input signal required to produce that swing.

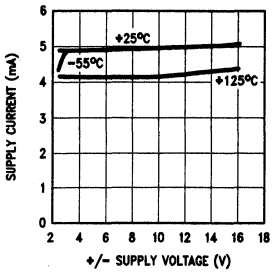
Note 10: The voltage between V^+ and either input pin must not exceed 36V.

Note 11: A military RETS electrical test specification is available on request. At the time of printing, the RETS6161X specs complied with all **Boldface** limits in this column.

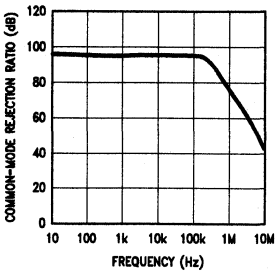
Note 12: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed.

Typical Performance Characteristics (R_L = 10 kΩ, T_A = 25°C unless otherwise specified)

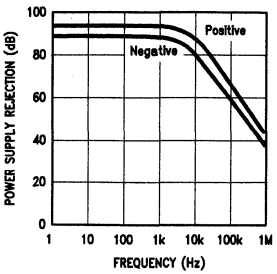
Supply Current vs Supply Voltage



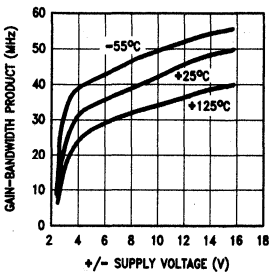
Common-Mode Rejection Ratio



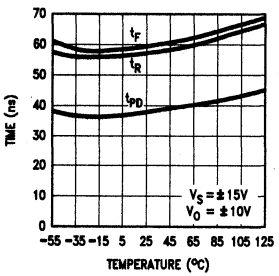
Power Supply Rejection Ratio



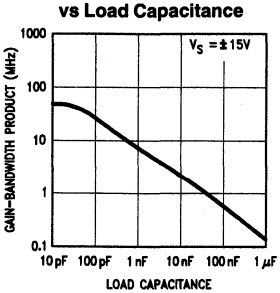
Gain-Bandwidth Product



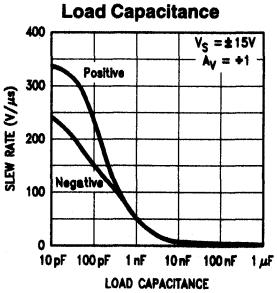
Propagation Delay Rise and Fall Times



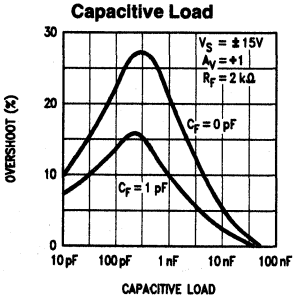
Gain-Bandwidth Product vs Load Capacitance



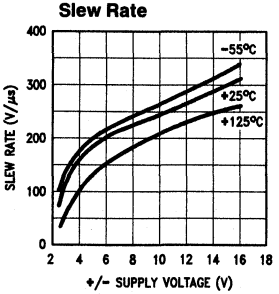
Slew Rate vs Load Capacitance



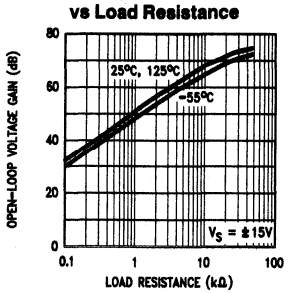
Overshoot vs Capacitive Load



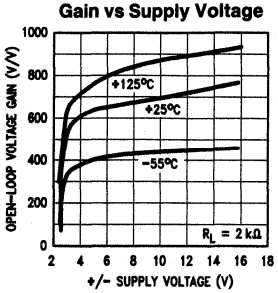
Slew Rate



Voltage Gain vs Load Resistance



Gain vs Supply Voltage

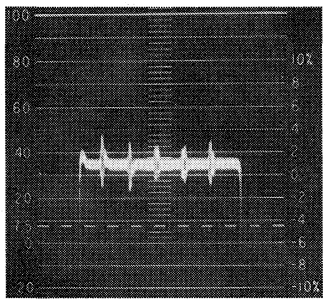


TL/H/9057–6

Typical Performance Characteristics

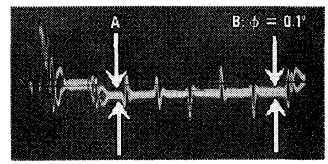
(R_L = 10 kΩ, T_A = 25°C unless otherwise specified) (Continued)

Differential Gain (Note)



TL/H/9057–7

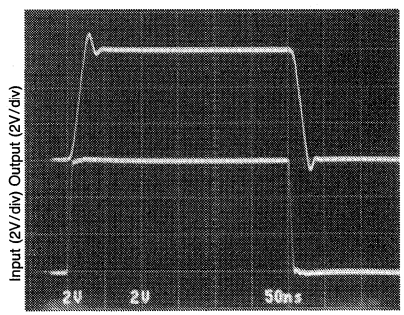
Differential Phase (Note)



TL/H/9057–8

Note: Differential gain and differential phase measured for four series LM6361 op amps configured as unity-gain followers, in series with an LM6321 buffer. Error added by LM6321 is negligible. Test performed using Tektronix Type 520 NTSC test system.

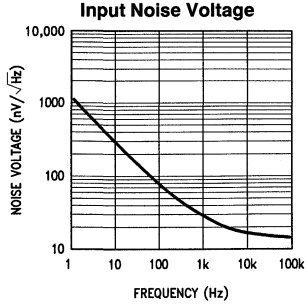
Step Response; Av = +1



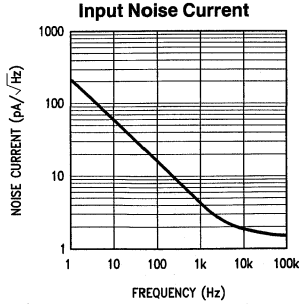
TL/H/9057–1

(50 ns/div)

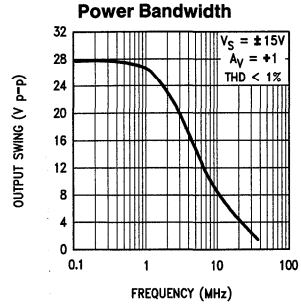
Input Noise Voltage



Input Noise Current



Power Bandwidth

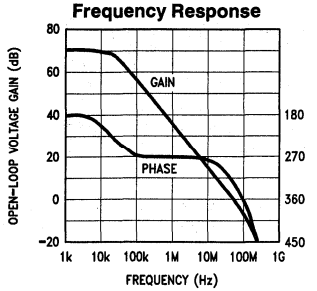


TL/H/9057–9

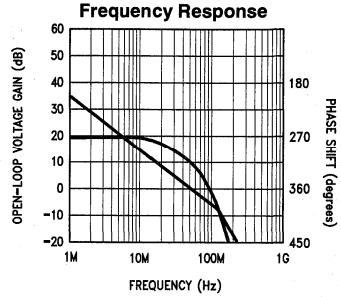
Typical Performance Characteristics

(R_L = 10 kΩ, T_A = 25°C unless otherwise specified) (Continued)

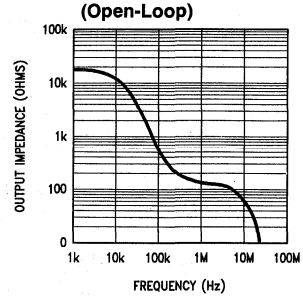
Open-Loop Frequency Response



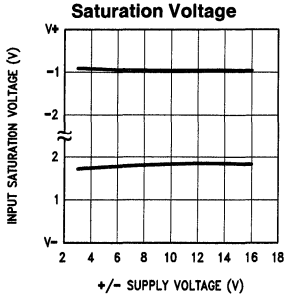
Open-Loop Frequency Response



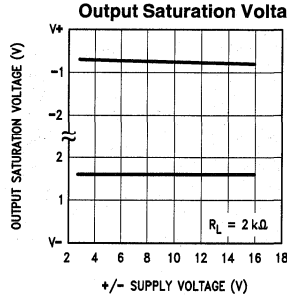
Output Impedence (Open-Loop)



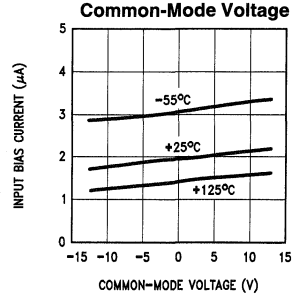
Common-Mode Input Saturation Voltage



Output Saturation Voltage

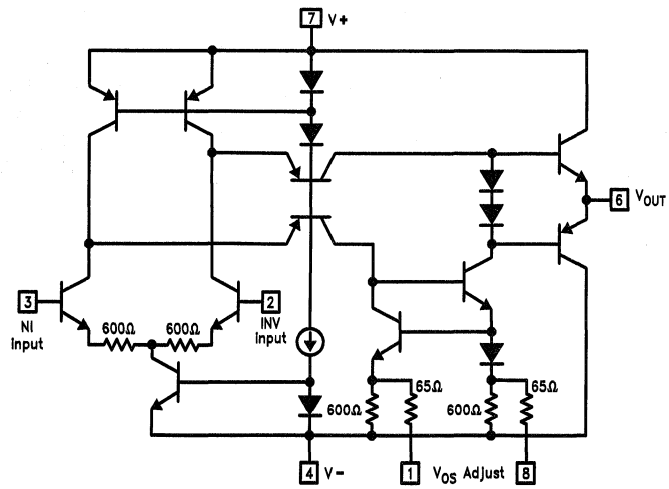


Bias Current vs Common-Mode Voltage



TL/H/9057–12

Simplified Schematic



TL/H/9057–3

Applications Tips

The LM6361 has been compensated for unity-gain operation. Since this compensation involved adding emitter-degeneration resistors to the op amp's input stage, the open-loop gain was reduced as the stability increased. Gain error due to reduced A_{VOL} is most apparent at high gains; thus, for gains between 5 and 25, the less-compensated LM6364 should be used, and the uncompensated LM6365 is appropriate for gains of 25 or more. The LM6361, LM6364, and LM6365 have the same high slew rate, regardless of their compensation.

The LM6361 is unusually tolerant of capacitive loads. Most op amps tend to oscillate when their load capacitance is greater than about 200 pF (especially in low-gain circuits). The LM6361's compensation is effectively increased with load capacitance, reducing its bandwidth and increasing its stability.

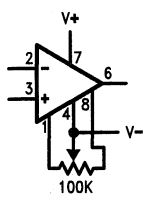
Power supply bypassing is not as critical for the LM6361 as it is for other op amps in its speed class. Bypassing will, however, improve the stability and transient response and is recommended for every design. 0.01 μF to 0.1 μF ceramic capacitors should be used (from each supply "rail" to ground); if the device is far away from its power supply source, an additional 2.2 μF to 10 μF of tantalum may provide extra noise reduction.

Keep all leads short to reduce stray capacitance and lead inductance, and make sure ground paths are low-impedance, especially where heavier currents will be flowing. Stray capacitance in the circuit layout can cause signal coupling across adjacent nodes and can cause gain to unintentionally vary with frequency.

Breadboarded circuits will work best if they are built using generic PC boards with a good ground plane. If the op amps are used with sockets, as opposed to being soldered into the circuit, the additional input capacitance may degrade circuit performance.

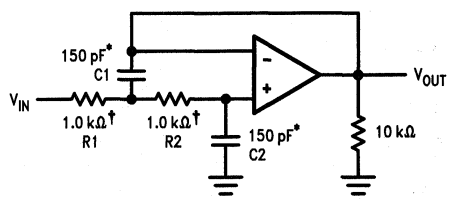
Typical Applications

Offset Voltage Adjustment



TL/H/9057–4

1 MHz Low-Pass Filter



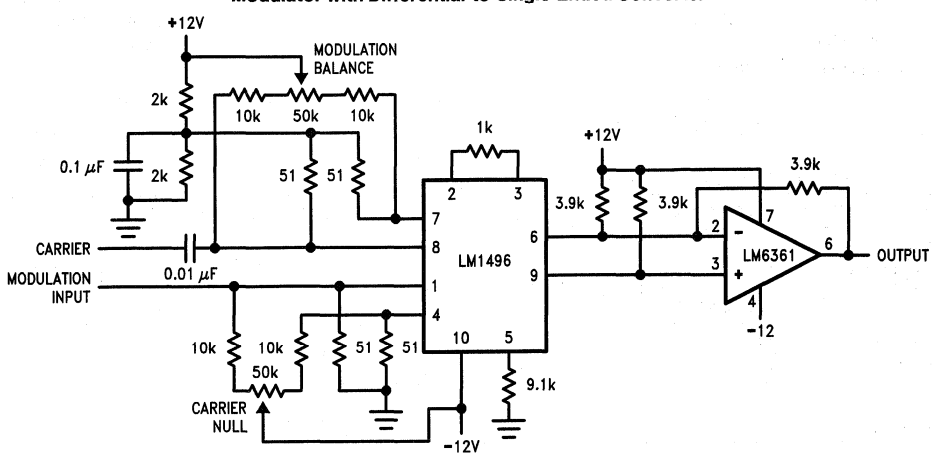
TL/H/9057–10

†1% tolerance

*Matching determines filter precision

$f_c = (2\pi\sqrt{(R1\ R2\ C1\ C2)})^{-1}$

Modulator with Differential-to-Single-Ended Converter



TL/H/9057–11

National Semiconductor

LM6162/LM6262/LM6362
High Speed Operational Amplifier

General Description

The LM6362 family of high-speed amplifiers exhibits an excellent speed-power product, delivering 300 V/μs and 100 MHz gain-bandwidth product (stable for gains as low as +2 or −1) with only 5 mA of supply current. Further power savings and application convenience are possible by taking advantage of the wide dynamic range in operating supply voltage which extends all the way down to +5V.

These amplifiers are built with National's VIP™ (Vertically Integrated PNP) process which provides fast transistors that are true complements to the already fast NPN devices. This advanced junction-isolated process delivers high speed performance without the need for complex and expensive dielectric isolation.

- Low supply current — 5 mA
- Fast settling time — 120 ns to 0.1%
- Low differential gain — <0.1%
- Low differential phase — <0.1°
- Wide supply range — 4.75V to 32V
- Stable with unlimited capacitive load
- Well behaved; easy to apply

Features

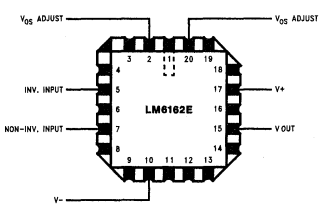
- High slew rate — 300 V/μs
- High gain-bandwidth product — 100 MHz

Applications

- Video amplifier
- Wide-bandwidth signal conditioning for image processing (FAX, scanners, laser printers)
- Hard disk drive preamplifier
- Error amplifier for high-speed switching regulator

Connection Diagrams

20-Lead LCC

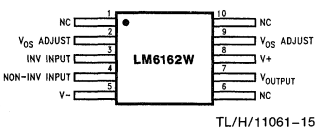


TL/H/11061–14

Top View

See NS Package Number E20A

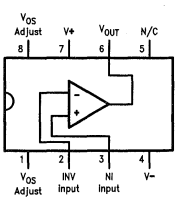
10-Pin Ceramic Flatpak



TL/H/11061–15

Top View

See NS Package Number W10A



TL/H/11061–2

See NS Package Number N08E, M08A or J08A

Temperature Range			Package	NSC Drawing
Military $-55°C \le T_A \le +125°C$	**Industrial** $-25°C \le T_A \le +85°C$	**Commercial** $0°C \le T_A \le +70°C$		
LM6162N	LM6262N	LM6362N	8-Pin Molded DIP	N08E
LM6162J/883 5962-9216501PA			8-Pin Ceramic DIP	J08A
	LM6262M	LM6362M	8-Pin Molded Surface Mt.	M08A
LM6162E/883 5962-92165012A			20-Lead LCC	E20A
LM6162W/883 5962-9216501HA			10-Pin Ceramic Flatpak	W10A

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage ($V^+ - V^-$)	36V
Differential Input Voltage (Note 2)	±8V
Common-Mode Input Voltage (Note 3)	($V^+ - 0.7V$) to ($V^- - 0.3V$)
Output Short Circuit to GND (Note 4)	Continuous
Soldering Information	
Dual-In-Line Package (N)	
Soldering (10 seconds)	260°C
Small Outline Package (M)	
Vapor Phase (60 seconds)	215°C
Infrared (15 seconds)	220°C

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

Storage Temperature Range	$-65°C \le T_J \le +150°C$
Max Junction Temperature	150°C
ESD Tolerance (Note 5)	±1100V

Operating Ratings

Temperature Range (Note 6)	
LM6162	$-55°C \le T_J \le +125°C$
LM6262	$-25°C \le T_J \le +85°C$
LM6362	$0°C \le T_J \le +70°C$
Supply Voltage Range	4.75V to 32V

DC Electrical Characteristics

These limits apply for supply voltage = ±15V, V_{CM} = 0V, and $R_L \ge 100\ k\Omega$, unless otherwise specified. Limits in standard typeface are for $T_A = T_J = 25°C$; limits in **boldface type** apply over the **Operating Temperature Range.**

Symbol	Parameter	Conditions	Typical (Note 7)	LM6162 Limit (Note 8)	LM6262 Limit (Note 8)	LM6362 Limit (Note 8)	Units
V_{OS}	Input Offset Voltage		±3	±5 **±8**	±5 **±8**	±13 **±15**	mV max
$\frac{\Delta V_{OS}}{\Delta Temp}$	Input Offset Voltage Average Drift		7				µV/°C
I_{bias}	Input Bias Current		2.2	3 **6**	3 **5**	4 **6**	µA max
I_{OS}	Input Offset Current		±150	±350 **±800**	±350 **±600**	±1500 **±1900**	nA max
$\frac{\Delta I_{OS}}{\Delta Temp}$	Input Offset Current Average Drift		0.3				nA/°C
R_{IN}	Input Resistance	Differential	180				kΩ
C_{IN}	Input Capacitance		2.0				pF
A_{VOL}	Large Signal Voltage Gain	V_{OUT} = ±10V, R_L = 2 kΩ (Note 9)	1400	1000 **500**	1000 **700**	800 **650**	V/V min
		R_L = 10 kΩ	6500				V/V
V_{CM}	Input Common-Mode Voltage Range	Supply = ±15V	+14.0	+13.9 **+13.8**	+13.9 **+13.8**	+13.8 **+13.7**	V min
			−13.2	−12.9 **−12.7**	−12.9 **−12.7**	−12.9 **−12.8**	V max
		Supply = +5V (Note 10)	4.0	3.9 **3.8**	3.9 **3.8**	3.8 **3.7**	V min
			1.6	1.8 **2.0**	1.8 **2.0**	1.9 **2.0**	V max
CMRR	Common-Mode Rejection Ratio	$-10V \le V_{CM} \le +10V$	100	83 **79**	83 **79**	76 **74**	dB min
PSRR	Power Supply Rejection Ratio	$\pm 10V \le V_S \le \pm 16V$	93	83 **79**	83 **79**	76 **74**	dB min
V_O	Output Voltage Swing	Supply = ±15V, R_L = 2 kΩ	+14.2	+13.5 **+13.3**	+13.5 **+13.3**	+13.4 **13.3**	V min
			−13.4	−13.0 **−12.7**	−13.0 **−12.8**	−12.9 **−12.8**	V max

DC Electrical Characteristics (Continued)

These limits apply for supply voltage = ±15V, V_{CM} = 0V, and $R_L \geq 100\ k\Omega$, unless otherwise specified. Limits in standard typeface are for $T_A = T_J = 25°C$; limits in **boldface type** apply over the **Operating Temperature Range**.

Symbol	Parameter	Conditions	Typical (Note 7)	LM6162 Limit (Note 8)	LM6262 Limit (Note 8)	LM6362 Limit (Note 8)	Units
V_O	Output Voltage Swing	Supply = +5V and R_L = 2 kΩ (Note 10)	4.2	3.5 **3.3**	3.5 **3.3**	3.4 **3.3**	V min
			1.3	1.7 **2.0**	1.7 **1.9**	1.8 **1.9**	V max
I_{OSC}	Output Short Circuit Current	Sourcing	65	30 **20**	30 **25**	30 **25**	mA min
		Sinking	65	30 **20**	30 **25**	30 **25**	mA min
I_S	Supply Current		5.0	6.5 **6.8**	6.5 **6.7**	6.8 **6.9**	mA max

AC Electrical Characteristics

These limits apply for supply voltage = ±15V, V_{CM} = 0V, $R_L \geq 100\ k\Omega$, and $C_L \leq 5$ pF, unless otherwise specified. Limits in standard typeface are for $T_A = T_J = 25°C$; limits in **boldface type** apply over the **Operating Temperature Range**.

Symbol	Parameter	Conditions	Typical (Note 7)	LM6162 Limit (Note 8)	LM6262 Limit (Note 8)	LM6362 Limit (Note 8)	Units
GBW	Gain-Bandwidth Product	f = 20 MHz	100	80 **55**	80 **65**	75 **65**	MHz min
		Supply = ±5V	70				MHz
SR	Slew Rate	A_V = +2 (Note 11)	300	200 **180**	200 **180**	200 **180**	V/μs min
		Supply = ±5V	200				V/μs
PBW	Power Bandwidth	V_{OUT} = 20 V_{PP}	4.5				MHz
t_s	Settling Time	10V step, to 0.1% A_V = −1, R_L = 2 kΩ	100				ns
ϕ_m	Phase Margin	A_V = +2	45				deg
	Differential Gain	NTSC, A_V = +2	<0.1				%
	Differential Phase	NTSC, A_V = +2	<0.1				deg
e_n	Input Noise Voltage	f = 10 kHz	10				nV/√Hz
i_n	Input Noise Current	f = 10 kHz	1.2				pA/√Hz

Note 1: Absolute maximum ratings indicate limits beyond which damage to the component may occur. Electrical specifications do not apply when operating the device beyond its rated operating conditions.

Note 2: The ESD protection circuitry between the inputs will begin to conduct when the differential input voltage reaches 8V.

Note 3: a) In addition, the voltage between the V^+ pin and either input pin must not exceed 36V.
b) When the voltage applied to an input pin is driven more than 0.3V below the negative supply pin voltage, a substrate diode begins to conduct. Current through this pin must then be kept less than 20 mA to limit damage from self-heating.

Note 4: Although the output current is internally limited, continuous short-circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C.

Note 5: This value is the average voltage that the weakest pin combinations can withstand and still conform to the datasheet limits. The test circuit used consists of the human body model, 100 pF in series with 1500Ω.

Note 6: The typical thermal resistance, junction-to-ambient, of the molded plastic DIP (N package) is 105°C/W. For the molded plastic SO (M package), use 155°C/W. All numbers apply for packages soldered directly into a printed circuit board.

Note 7: Typical values are for $T_J = 25°C$, and represent the most likely parametric norm.

Note 8: Limits are guaranteed, by testing or correlation.

Note 9: Voltage Gain is the total output swing (20V) divided by the magnitude of the input signal required to produce that swing.

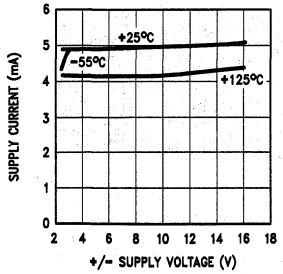
Note 10: For single-supply operation, the following conditions apply: $V^+ = 5V$, $V^- = 0V$, $V_{CM} = 2.5V$, $V_{OUT} = 2.5V$. Pin 1 and Pin 8 (V_{OS} Adjust pins) are each connected to pin 4 (V^-) to realize maximum output swing. This connection will increase the offset voltage.

Note 11: V_{IN} = 10V step. For ±5V supplies, V_{IN} = 1V step.

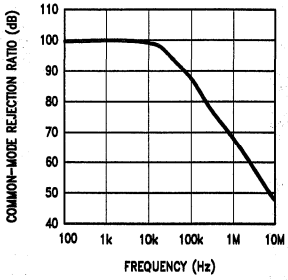
Note 12: A military RETS electrical test specification is available on request.

Typical Performance Characteristics $R_L = 10\ k\Omega$, $T_A = 25°C$ unless otherwise noted

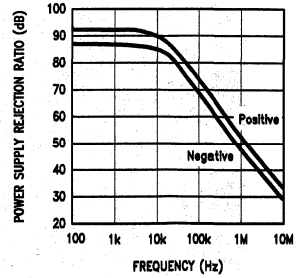
Supply Current vs Supply Voltage



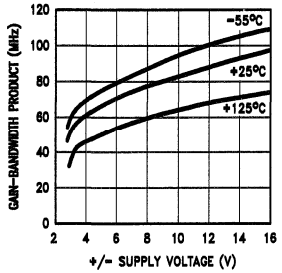
Common-Mode Rejection Ratio



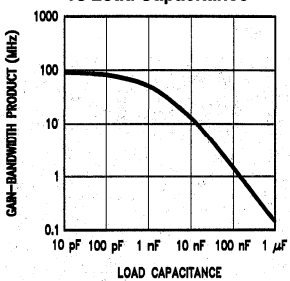
Power Supply Rejection Ratio



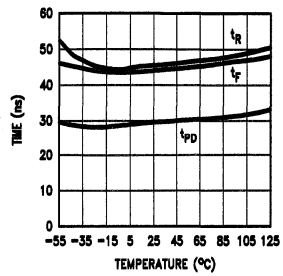
Gain-Bandwidth Product vs Supply Voltage



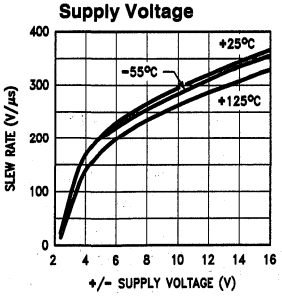
Gain-Bandwidth Product vs Load Capacitance



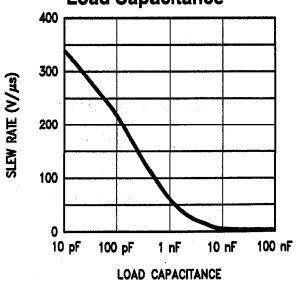
Propagation Delay, Rise and Fall Times



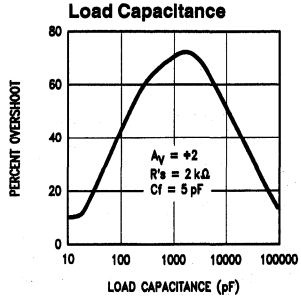
Slew Rate vs Supply Voltage



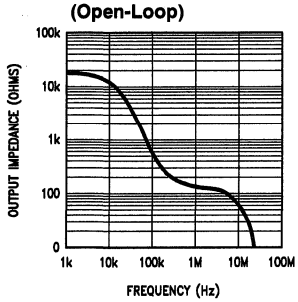
Slew Rate vs Load Capacitance



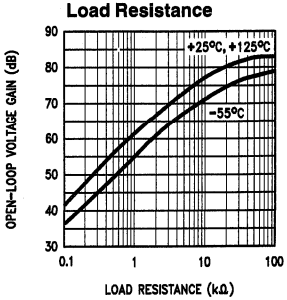
Overshoot vs Load Capacitance



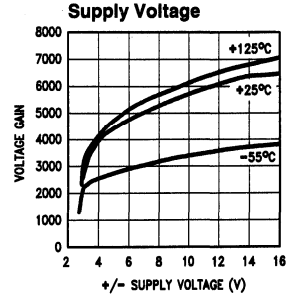
Output Impedance (Open-Loop)



Voltage Gain vs Load Resistance



Voltage Gain vs Supply Voltage

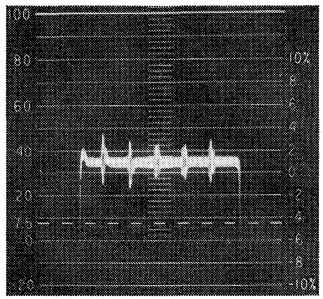


TL/H/11061–3

Typical Performance Characteristics (Continued)

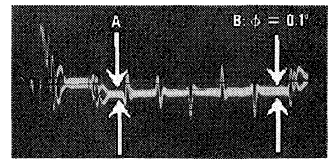
R_L = 10 kΩ, T_A = 25°C unless otherwise noted

Differential Gain (Note)



TL/H/11061–4

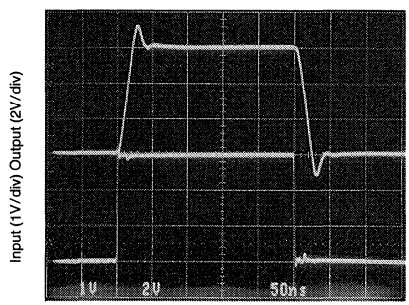
Differential Phase (Note)



TL/H/11061–5

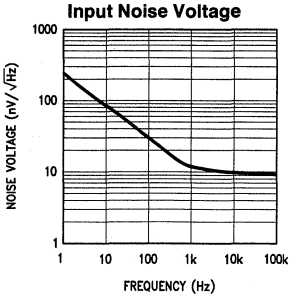
Note: Differential gain and differential phase measured for four series LM6362 op amps configured with gain of +2 each, in series with a 1:16 attenuator and an LM6321 buffer. Error added by LM6321 is negligible. Test performed using Tektronix Type 520 NTSC test system.

Step Response; Av = +2

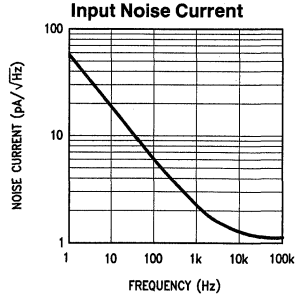


TL/H/11061–6

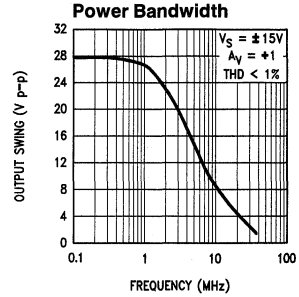
Input Noise Voltage



Input Noise Current



Power Bandwidth

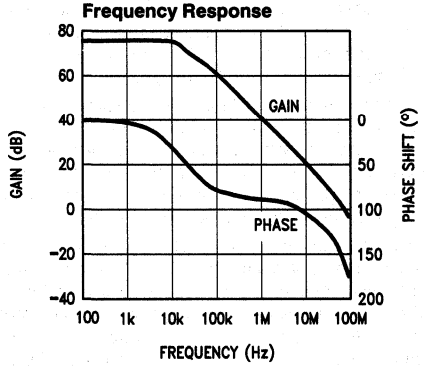


TL/H/11061–7

Typical Performance Characteristics (Continued)

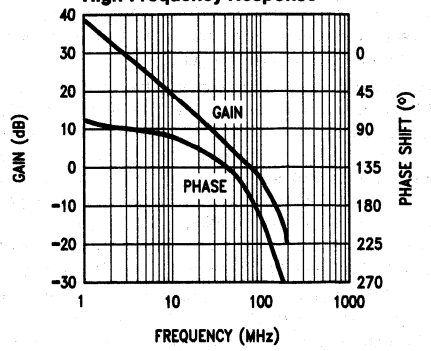
R_L = 10 kΩ, T_A = 25°C unless otherwise noted

Open-Loop Frequency Response



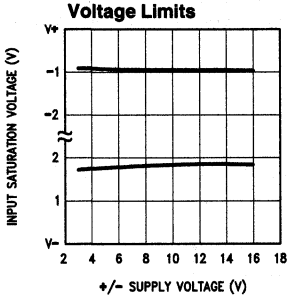
TL/H/11061–8

Open-Loop High-Frequency Response

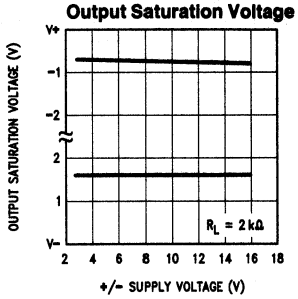


TL/H/11061–9

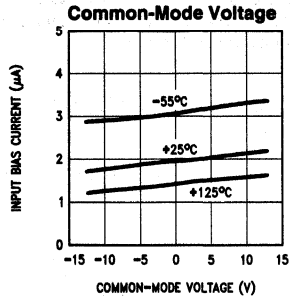
Common-Mode Input Voltage Limits



Output Saturation Voltage

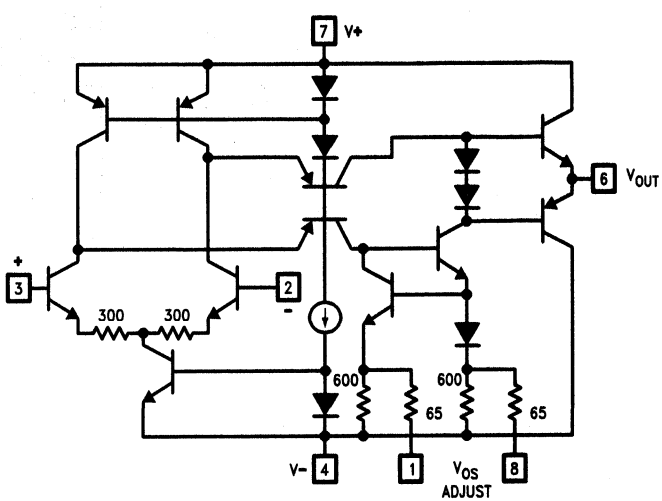


Bias Current vs Common-Mode Voltage



TL/H/11061–10

Simplified Schematic



TL/H/11061–1

Application Tips

The LM6362 has been decompensated for a wider gain-bandwidth product than the LM6361. However, the LM6362 still offers stability at gains of 2 (and −1) or greater over the specified ranges of temperature, power supply voltage, and load. Since this decompensation involved reducing the emitter-degeneration resistors in the op amp's input stage, the DC precision has been increased in the form of lower offset voltage and higher open-loop gain.

Other op amps in this family include the LM6361, LM6364, and LM6365. If unity-gain stability is required, the LM6361 should be used. The LM6364 has been decompensated for operation at gains of 5 or more, with corresponding greater gain-bandwidth product (125 MHz, typical) and DC precision. The fully-uncompensated LM6365 offers gain-bandwidth product of 725 MHz, typical, and is stable for gains of 25 or more. All parts in this family, regardless of compensation, have the same high slew rate of 300 V/μs (typ).

The LM6362 is unusually tolerant of capacitive loads. Most op amps tend to oscillate when their load capacitance is greater than about 200 pF (in low-gain circuits). However, load capacitance on the LM6362 effectively increases its compensation capacitance, thus slowing the op amp's response and reducing its bandwidth. The compensation is not ideal, though, and ringing may occur in low-gain circuits with large capacitive loads.

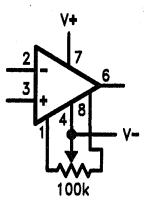
Power supply bypassing is not as critical for LM6362 as it is for other op amps in its speed class. However, bypassing will improve the stability and transient response of the LM6362, and is recommended for every design. 0.01 μF to 0.1 μF ceramic capacitors should be used (from each supply "rail" to ground); if the device is far away from its power supply source, an additional 2.2 μF to 10 μF of tantalum may be required for extra noise reduction.

Keep all leads short to reduce stray capacitance and lead inductance, and make sure ground paths are low-impedance, especially where heavier currents will be flowing. Stray capacitance in the circuit layout can cause signal coupling from one pin, input or lead to another, and can cause circuit gain to unintentionally vary with frequency.

Breadboarded circuits will work best if they are built using generic PC boards with a good ground plane. If the op amps are used with sockets, as opposed to being soldered into the circuit, the additional input capacitance may degrade circuit frequency response. At low gains (+2 or −1), a feedback capacitor C_f from output to inverting input will compensate for the phase lag caused by capacitance at the inverting input. Typically, values from 2 pF to 5 pF work well; however, best results can be obtained by observing the amplifier pulse response and optimizing C_f for the particular layout.

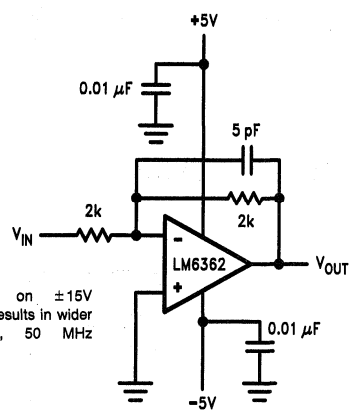
Typical Applications

Offset Voltage Adjustment



TL/H/11061–11

Inverting Amplifier, 30 MHz Bandwidth

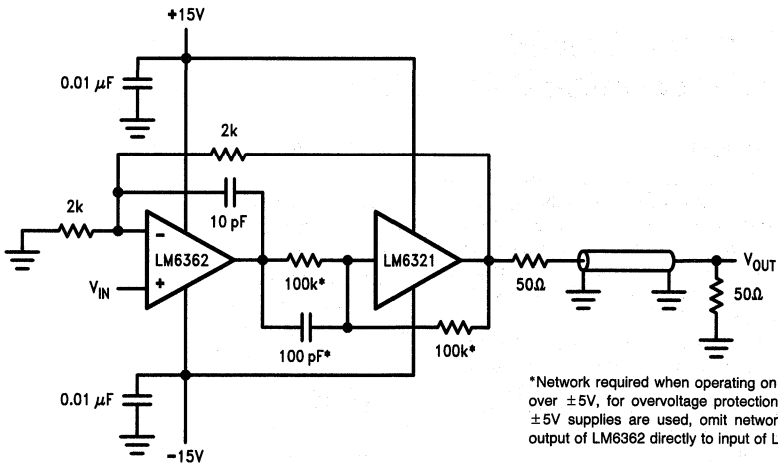


Operation on ±15V supplies results in wider bandwidth, 50 MHz (typ).

TL/H/11061–12

Typical Applications (Continued)

Video Cable Driver



*Network required when operating on supply voltage over ±5V, for overvoltage protection of LM6321. If ±5V supplies are used, omit network and connect output of LM6362 directly to input of LM6321.

TL/H/11061–13

National Semiconductor

LM6164/LM6264/LM6364
High Speed Operational Amplifier

General Description

The LM6164 family of high-speed amplifiers exhibits an excellent speed-power product in delivering 300V per μs and 175 MHz GBW (stable down to gains as low as +5) with only 5 mA of supply current. Further power savings and application convenience are possible by taking advantage of the wide dynamic range in operating supply voltage which extends all the way down to +5V.

These amplifiers are built with National's VIP™ (Vertically Integrated PNP) process which produces fast PNP transistors that are true complements to the already fast NPN devices. This advanced junction-isolated process delivers high speed performance without the need for complex and expensive dielectric isolation.

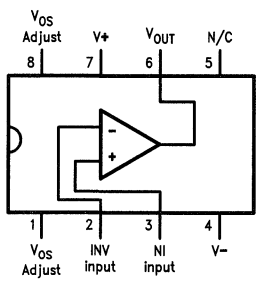
Features

- High slew rate — 300 V/μs
- High GBW product — 175 MHz
- Low supply current — 5 mA
- Fast settling — 100 ns to 0.1%
- Low differential gain — <0.1%
- Low differential phase — <0.1°
- Wide supply range — 4.75V to 32V
- Stable with unlimited capacitive load

Applications

- Video amplifier
- Wide-bandwidth signal conditioning
- Radar
- Sonar

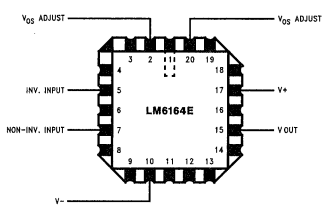
Connection Diagrams



TL/H/9153–8

NS Package Number J08A, M08A or N08E

20-Lead LCC

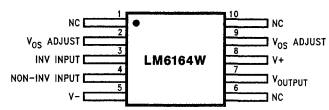


TL/H/9153–14

Top View

NS Package Number E20A

10-Lead Flatpak



TL/H/9153–15

Top View

NS Package Number W10A

Temperature Range			Package	NSC Drawing
Military $-55°C \le T_A \le +125°C$	**Industrial** $-25°C \le T_A \le +85°C$	**Commercial** $0°C \le T_A \le +70°C$		
	LM6264N	LM6364N	8-Pin Molded DIP	N08E
LM6164J LM6164J/883 5962-8962401PA	LM6264J		8-Pin Ceramic DIP	J08A
		LM6364M	8-Pin Molded Surface Mt.	M08A
LM6164E/883 5962-89624012A			20-Lead LCC	E20A
LM6164W/883 5962-8962401HA			10-Pin Ceramic Flatpak	W10A

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage ($V^+ - V^-$)	36V
Differential Input Voltage (Note 6)	±8V
Common-Mode Input Voltage (Note 10)	($V^+ - 0.7V$) to ($V^- - 7V$)
Output Short Circuit to Gnd (Note 1)	Continuous
Soldering Information	
Dual-In-Line Package (N, J)	
Soldering (10 sec.)	260°C
Small Outline Package (M)	
Vapor Phase (60 sec.)	215°C
Infrared (15 sec.)	220°C

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

Storage Temperature Range	−65°C to +150°C
Max Junction Temperature (Note 2)	150°C
ESD Tolerance (Notes 6 & 7)	±700V

Operating Ratings

Temperature Range (Note 2)	
LM6164	$-55°C \le T_J \le +125°C$
LM6264	$-25°C \le T_J \le +85°C$
LM6364	$0°C \le T_J \le +70°C$
Supply Voltage Range	4.75V to 32V

DC Electrical Characteristics

The following specifications apply for Supply Voltage = ±15V, V_{CM} = 0, $R_L \ge 100\ k\Omega$ and $R_S = 50\Omega$ unless otherwise noted. **Boldface** limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX}; all other limits $T_A = T_J = 25°C$.

Symbol	Parameter	Conditions	Typ	LM6164 Limit (Notes 3, 11)	LM6264 Limit (Note 3)	LM6364 Limit (Note 3)	Units
V_{OS}	Input Offset Voltage		2	4 **6**	4 **6**	9 **11**	mV max
V_{OS} Drift	Input Offset Voltage Average Drift		6				µV/°C
I_b	Input Bias Current		2.5	3 **6**	3 **5**	3 **6**	µA max
I_{OS}	Input Offset Current		150	350 **800**	350 **600**	1500 **1900**	mA max
I_{OS} Drift	Input Offset Current Average Drift		0.3				nA/°C
R_{IN}	Input Resistance	Differential	100				kΩ
C_{IN}	Input Capacitance		3.0				pF
A_{VOL}	Large Signal Voltage Gain	V_{OUT} = ±10V, R_L = 2 kΩ (Note 9)	2.5	1.8 **0.9**	1.8 **1.2**	1.3 **1.1**	V/mV min
		R_L = 10 kΩ	9				
V_{CM}	Input Common-Mode Voltage Range	Supply = ±15V	+14.0	+13.9 **+13.8**	+13.9 **+13.8**	+13.8 **+13.7**	V min
			−13.5	−13.3 **−13.1**	−13.3 **−13.1**	−13.2 **−13.1**	V min
		Supply = +5V (Note 4)	4.0	3.9 **3.8**	3.9 **3.8**	3.8 **3.7**	V min
			1.5	1.7 **1.9**	1.7 **1.9**	1.8 **1.9**	V max
CMRR	Common-Mode Rejection Ratio	$-10V \le V_{CM} \le +10V$	105	86 **80**	86 **82**	80 **78**	dB min
PSRR	Power Supply Rejection Ratio	$\pm 10V \le V\pm \le \pm 16V$	96	86 **80**	86 **82**	80 **78**	dB min

DC Electrical Characteristics

The following specifications apply for Supply Voltage = ±15V, V_{CM} = 0, $R_L \geq 100\ k\Omega$ and $R_S = 50\Omega$ unless otherwise noted. **Boldface** limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX}; all other limits $T_A = T_J = 25°C$. (Continued)

Symbol	Parameter	Conditions	Typ	LM6164 Limit (Notes 3, 11)	LM6264 Limit (Note 3)	LM6364 Limit (Note 3)	Units
V_O	Output Voltage Swing	Supply = +5V and R_L = 2 kΩ	+14.2	+13.5 **+13.3**	+13.5 **+13.3**	+13.4 **+13.3**	V min
			−13.4	−13.0 **−12.7**	−13.0 **−12.8**	−12.9 **−12.8**	V min
		Supply = +5V and R_L = 2 kΩ (Note 9)	4.2	3.5 **3.3**	3.5 **3.3**	3.4 **3.3**	V min
			1.3	1.7 **2.0**	1.7 **1.9**	1.8 **1.9**	V max
	Output Short Circuit Current	Source	65	30 **20**	30 **25**	30 **25**	mA min
		Sink	65	30 **20**	30 **25**	30 **25**	mA min
I_S	Supply Current		5.0	6.5 **6.8**	6.5 **6.7**	6.8 **6.9**	mA min

AC Electrical Characteristics

The following specifications apply for Supply Voltage = ±15V, V_{CM} = 0, $R_L \geq 100\ k\Omega$ and $R_S = 50\Omega$ unless otherwise noted. **Boldface** limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX}; all other limits $T_A = T_J = 25°C$.

Symbol	Parameter	Conditions	Typ	LM6164 Limit (Notes 3, 11)	LM6264 Limit (Note 3)	LM6364 Limit (Note 3)	Units
GBW	Gain-Bandwidth Product	F = 20 MHz	175	140 **100**	140 **120**	120 **100**	MHz min
		Supply = ±5V	120				
SR	Slew Rate	A_V = +5 (Note 8)	300	200 **180**	200 **180**	200 **180**	V/μs min
		Supply = ±5V	200				
PBW	Power Bandwidth	V_{OUT} = 20 V_{PP}	4.5				MHz
T_S	Settling Time	10V Step to 0.1% A_V = −4, R_L = 2 kΩ	100				ns
ϕ_m	Phase Margin	A_V = +5	45				Deg
A_D	Differential Gain	NTSC, A_V = +10	<0.1				%
ϕ_D	Differential Phase	NTSC, A_V = +10	<0.1				Deg
e_{np-p}	Input Noise Voltage	F = 10 kHz	8				nV/√Hz
i_{np-p}	Input Noise Current	F = 10 kHz	1.5				pA/√Hz

Note 1: Continuous short-circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C.

Note 2: The typical junction-to-ambient thermal resistance of the molded plastic DIP (N) is 105°C/Watt, the molded plastic SO (M) package is 155°C/Watt, and the cerdip (J) package is 125°C/Watt. All numbers apply for packages soldered directly into a printed circuit board.

Note 3: Limits are guaranteed by testing or correlation.

Note 4: For single supply operation, the following conditions apply: V+ = 5V, V− = 0V, V_{CM} = 2.5V, V_{OUT} = 2.5V. Pin 1 & Pin 8 (V_{OS} Adjust) are each connected to Pin 4 (V−) to realize maximum output swing. This connection will degrade V_{OS}.

Note 5: $C_L \leq 5$ pF.

Note 6: In order to achieve optimum AC performance, the input stage was designed without protective clamps. Exceeding the maximum differential input voltage results in reverse breakdown of the base-emitter junction of one of the input transistors and probable degradation of the input parameters (especially V_{OS}, I_{OS}, and Noise).

Note 7: The average voltage that the weakest pin combinations (those involving Pin 2 or Pin 3) can withstand and still conform to the datasheet limits. The test circuit used consists of the human body model of 100 pF in series with 1500Ω.

Note 8: V_{IN} = 4V step. For supply = ±5V, V_{IN} = 1V step.

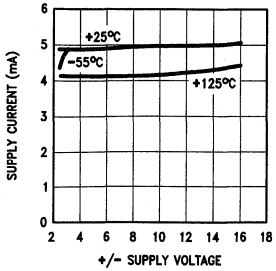
Note 9: Voltage Gain is the total output swing (20V) divided by the input signal required to produce that swing.

Note 10: The voltage between V^+ and either input pin must not exceed 36V.

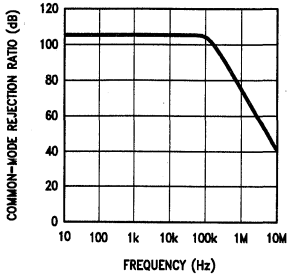
Note 11: A military RETS electrical test specification is available on request. At the time of printing, the LM6164J/883 RETS spec complied with the **Boldface** limits in this column. The LM6164J/883 may also be procured as Standard Military Drawing #5962-8962401PA.

Typical Performance Characteristics (R_L = 10 kΩ, T_A = 25°C unless otherwise specified)

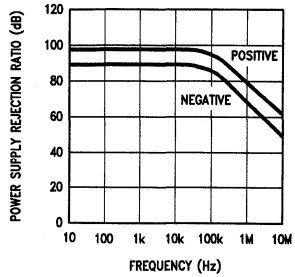
Supply Current vs Supply Voltage



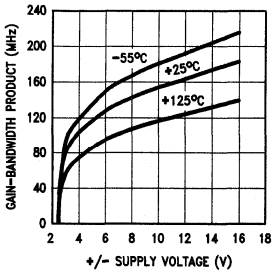
Common-Mode Rejection Ratio



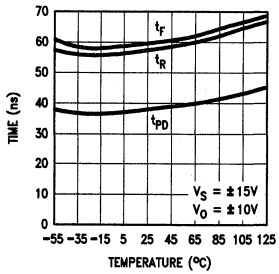
Power Supply Rejection Ratio



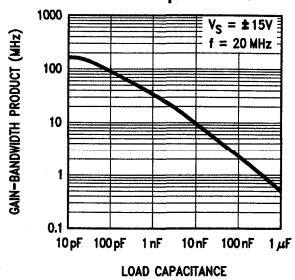
Gain-Bandwidth Product



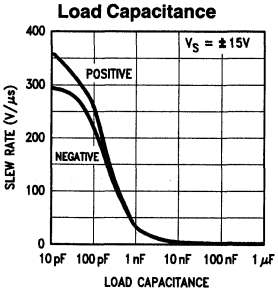
Propagation Delay Rise and Fall Time



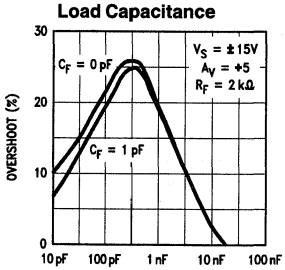
Gain-Bandwidth Product vs Load Capacitance



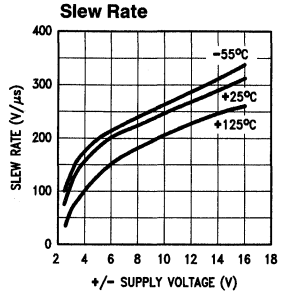
Slew Rate vs Load Capacitance



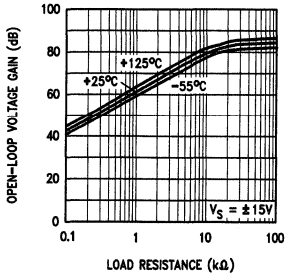
Overshoot vs Load Capacitance



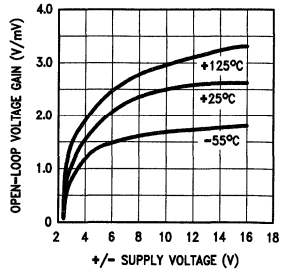
Slew Rate



Voltage Gain vs Load Resistance



Gain vs Supply Voltage

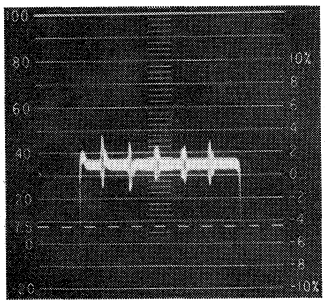


TL/H/9153-5

Typical Performance Characteristics

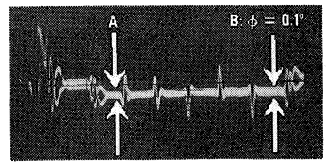
(R_L = 10 kΩ, T_A = 25°C unless otherwise specified) (Continued)

Differential Gain (Note)



TL/H/9153–6

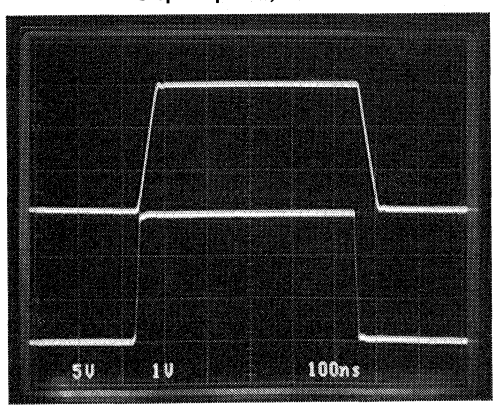
Differential Phase (Note)



TL/H/9153–7

Note: Differential gain and differential phase measured for four series LM6364 op amps in series with an LM6321 buffer. Error added by LM6321 is negligible. Test performed using Tektronix Type 520 NTSC test system. Configured with a gain of +5 (each output attenuated by 80%)

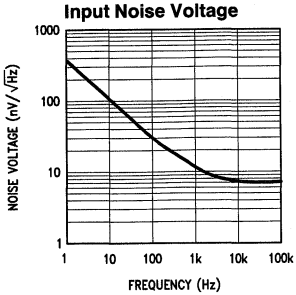
Step Response; Av = +5



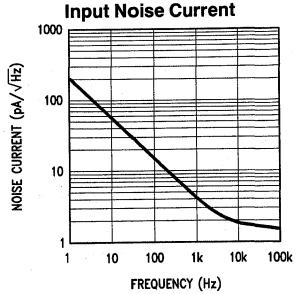
TL/H/9153–1

TIME (50 ns/div)

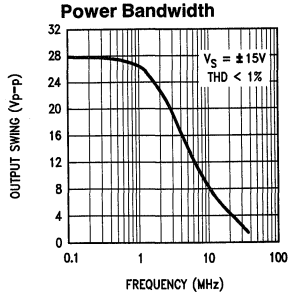
Input Noise Voltage



Input Noise Current



Power Bandwidth

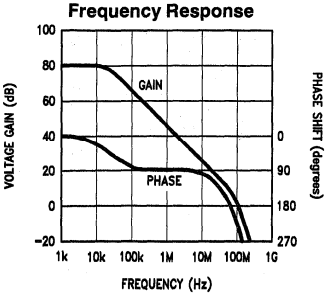


TL/H/9153–9

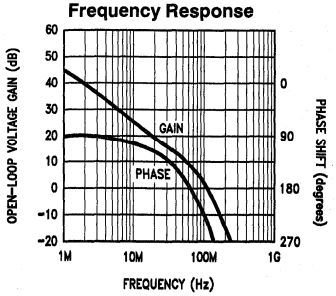
Typical Performance Characteristics

(R_L = 10 kΩ, T_A = 25°C unless otherwise specified) (Continued)

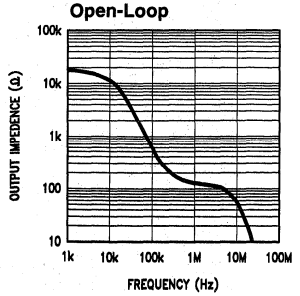
Open-Loop Frequency Response



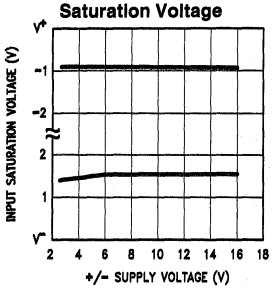
Open-Loop Frequency Response



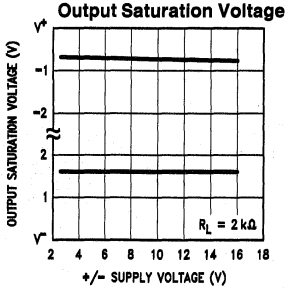
Output Resistance Open-Loop



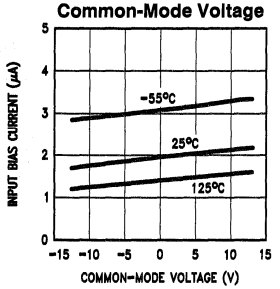
Common-Mode Input Saturation Voltage



Output Saturation Voltage

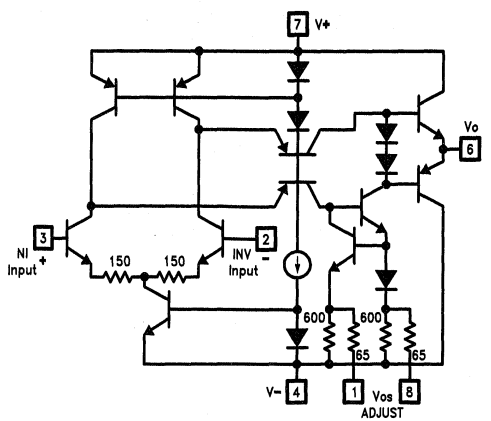


Bias Current vs Common-Mode Voltage



TL/H/9153-13

Simplified Schematic



TL/H/9153-3

Applications Tips

The LM6364 has been compensated for gains of 5 or greater (over specified ranges of temperature, power supply voltage, and load). Since this compensation involved adding emitter-degeneration resistors in the op amp's input stage, the open-loop gain was reduced as the stability increased. Gain error due to reduced A_{VOL} is most apparent at high gains; thus, the uncompensated LM6365 is appropriate for gains of 25 or more. If unity-gain operation is desired, the LM6361 should be used. The LM6361, LM6364, and LM6365 have the same high slew rate (typically 300 V/μs), regardless of their compensation.

The LM6364 is unusually tolerant of capacitive loads. Most op amps tend to oscillate when their load capacitance is greater than about 200 pF (in low-gain circuits). However, load capacitance on the LM6364 effectively increases its compensation capacitance, thus slowing the op amp's response and reducing its bandwidth. The compensation is not ideal, though, and ringing or oscillation may occur in low-gain circuits with large capacitive loads. To overcompensate the LM6364 for operation at gains less than 5, a series resistor-capacitor network should be added between the input pins (as shown in the Typical Applications, Noise Gain Compensation) so that the high-frequency noise gain rises to at least 5.

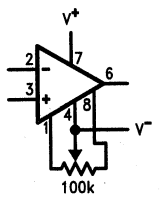
Power supply bypassing will improve the stability and transient response of the LM6364, and is recommended for every design. 0.01 μF to 0.1 μF ceramic capacitors should be used (from each supply "rail" to ground); if the device is far away from its power supply source, an additional 2.2 μF to 10 μF (tantalum) may be required for extra noise reduction.

Keep all leads short to reduce stray capacitance and lead inductance, and make sure ground paths are low-impedance, especially where heavier currents will be flowing. Stray capacitance in the circuit layout can cause signal coupling between adjacent nodes, so that circuit gain unintentionally varies with frequency.

Breadboarded circuits will work best if they are built using generic PC boards with a good ground plane. If the op amps are used with sockets, as opposed to being soldered into the circuit, the additional input capacitance may degrade circuit performance.

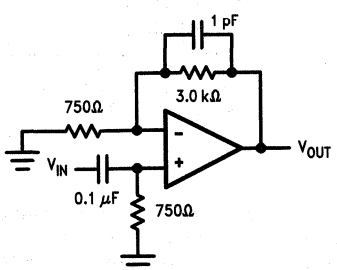
Typical Applications

Offset Voltage Adjustment



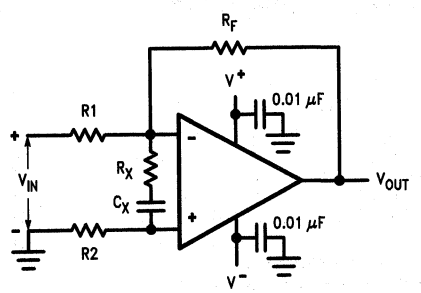
TL/H/9153–10

Video-Bandwidth Amplifier



TL/H/9153–12

Noise-Gain Compensation for Gains ≤5



TL/H/9153–11

$R_XC_X \geq (2\pi \cdot 25\ MHz)^{-1}$

$5\ R_X = R_1 + R_F(1 + R_1/R_2)$

National Semiconductor

LM6165/LM6265/LM6365
High Speed Operational Amplifier

General Description

The LM6165 family of high-speed amplifiers exhibits an excellent speed-power product in delivering 300 V/μs and 725 MHz GBW (stable for gains as low as +25) with only 5 mA of supply current. Further power savings and application convenience are possible by taking advantage of the wide dynamic range in operating supply voltage which extends all the way down to +5V.

These amplifiers are built with National's VIP™ (Vertically Integrated PNP) process which produces fast PNP transistors that are true complements to the already fast NPN devices. This advanced junction-isolated process delivers high speed performance without the need for complex and expensive dielectric isolation.

Features

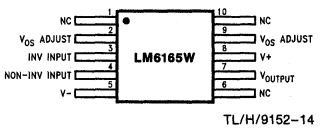
- High slew rate — 300 V/μs
- High GBW product — 725 MHz
- Low supply current — 5 mA
- Fast settling — 80 ns to 0.1%
- Low differential gain — <0.1%
- Low differential phase — <0.1°
- Wide supply range — 4.75V to 32V
- Stable with unlimited capacitive load

Applications

- Video amplifier
- Wide-bandwidth signal conditioning
- Radar
- Sonar

Connection Diagrams

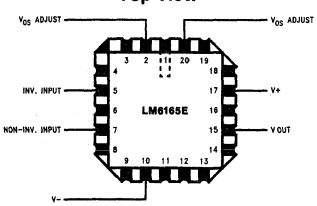
10-Lead Flatpak
Top View



TL/H/9152–14

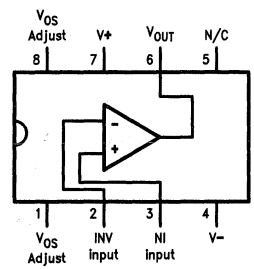
Order Number LM6165W/883
See NS Package Number W10A

20-Lead LCC
Top View



TL/H/9152–15

Order Number LM6165E/883
See NS Package Number E20A



TL/H/9152–8

Temperature Range			Package	NSC Drawing
Military −55°C ≤ T_A ≤ +125°C	Industrial −40°C ≤ T_A ≤ +85°C	Commercial 0°C ≤ T_A ≤ +70°C		
	LM6265N	LM6365N	8-Pin Molded DIP	N08E
LM6165J LM6165J/883 5962-8962501PA	LM6265J		8-Pin Ceramic DIP	J08A
		LM6365M	8-Pin Molded Surface Mt.	M08A
LM6165E/883 5962-89625012A			20-Lead LCC	E20A
LM6165W883 5962-8962501HA			10-Pin Ceramic Flatpak	W10A

Order Number LM6165J, LM6265J or LM6165J/883
See NS Package Number J08A

Order Number LM6365M
See NS Package Number M08A

Order Number LM6265N or LM6365N
See NS Package Number N08E

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage ($V^+ - V^-$)	36V
Differential Input Voltage (Note 6)	±8V
Common-Mode Voltage Range (Note 10)	$(V^+ - 0.7V)$ to $(V^- - 7V)$
Output Short Circuit to GND (Note 1)	Continuous
Soldering Information	
Dual-In-Line Package (N, J)	
Soldering (10 sec.)	260°C
Small Outline Package (M)	
Vapor Phase (60 sec.)	215°C
Infrared (15 sec.)	220°C

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

Storage Temp Range	−65°C to +150°C
Max Junction Temperature (Note 2)	150°C
ESD Tolerance (Notes 6 and 7)	±700V

Operating Ratings

Temperature Range (Note 2)	
LM6165, LM6165J/883	$-55°C \le T_J \le +125°C$
LM6265	$-25°C \le T_J \le +85°C$
LM6365	$0°C \le T_J \le +70°C$
Supply Voltage Range	4.75V to 32V

DC Electrical Characteristics

The following specifications apply for Supply Voltage = ±15V, $V_{CM} = 0$, $R_L \ge 100\ k\Omega$ and $R_S = 50\Omega$ unless otherwise noted. **Boldface** limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX}; all other limits $T_A = T_J = 25°C$.

Symbol	Parameter	Conditions	Typ	LM6165 Limit (Notes 3, 11)	LM6265 Limit (Note 3)	LM6365 Limit (Note 3)	Units
V_{OS}	Input Offset Voltage		1	3 **4**	3 **4**	6 **7**	mV Max
V_{OS} Drift	Input Offset Voltage Average Drift		3				µV/°C
I_b	Input Bias Current		2.5	3 **6**	3 **5**	5 **6**	µA Max
I_{OS}	Input Offset Current		150	350 **800**	350 **600**	1500 **1900**	nA Max
I_{OS} Drift	Input Offset Current Average Drift		0.3				nA/°C
R_{IN}	Input Resistance	Differential	20				kΩ
C_{IN}	Input Capacitance		6.0				pF
A_{VOL}	Large Signal Voltage Gain (Note 9)	$V_{OUT} = \pm 10V$, $R_L = 2\ k\Omega$	10.5	7.5 **5.0**	7.5 **6.0**	5.5 **5.0**	V/mV Min
		$R_L = 10\ k\Omega$	38				
V_{CM}	Input Common-Mode Voltage Range	Supply = ±15V	+14.0	+13.9 **+13.8**	+13.9 **+13.8**	+13.8 **+13.7**	V Min
			−13.6	−13.4 **−13.2**	−13.4 **−13.2**	−13.3 **−13.2**	V Min
		Supply = +5V (Note 4)	4.0	3.9 **3.8**	3.9 **3.8**	3.8 **3.7**	V Min
			1.4	1.6 **1.8**	1.6 **1.8**	1.7 **1.8**	V Max
CMRR	Common-Mode Rejection Ratio	$-10V \le V_{CM} \le +10V$	102	88 **82**	88 **84**	80 **78**	dB Min
PSRR	Power Supply Rejection Ratio	$\pm 10V \le V^{\pm} \le \pm 16V$	104	88 **82**	88 **84**	80 **78**	dB Min
V_O	Output Voltage Swing	Supply = ±15V, $R_L = 2\ k\Omega$	+14.2	+13.5 **+13.3**	+13.5 **+13.3**	+13.4 **+13.3**	V Min
			−13.4	−13.0 **−12.7**	−13.0 **−12.8**	−12.9 **−12.8**	V Min

DC Electrical Characteristics (Continued)

The following specifications apply for Supply Voltage = ±15V, V_{CM} = 0, $R_L \geq 100\ k\Omega$ and $R_S = 50\Omega$ unless otherwise noted. **Boldface** limits apply for $T_A = T_J = T_{MIN}$ to T_{Max}; all other limits $T_A = T_J = 25°C$.

Symbol	Parameter	Conditions	Typ	LM6165 Limit (Notes 3, 11)	LM6265 Limit (Note 3)	LM6365 Limit (Note 3)	Units
V_O (Continued)	Output Voltage Swing (Continued)	Supply = +5V R_L = 2 kΩ (Note 4)	4.2	3.5 **3.3**	3.5 **3.3**	3.4 **3.3**	V Min
			1.3	1.7 **2.0**	1.7 **1.9**	1.8 **1.9**	V Max
	Output Short Circuit Current	Source	65	30 **20**	30 **25**	30 **25**	mA Min
		Sink	65	30 **20**	30 **25**	30 **25**	mA Min
I_S	Supply Current		5.0	6.5 **6.8**	6.5 **6.7**	6.8 **6.9**	mA Max

AC Electrical Characteristics

The following specifications apply for Supply Voltage = ±15V, V_{CM} = 0, $R_L \geq 100\ k\Omega$ and $R_S = 50\Omega$ unless otherwise noted. **Boldface** limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX}; all other limits $T_A = T_J = 25°C$. (Note 5)

Symbol	Parameter	Conditions	Typ	LM6165 Limit (Notes 3, 11)	LM6265 Limit (Note 3)	LM6365 Limit (Note 3)	Units
GBW	Gain Bandwidth Product	F = 20 MHz	725	575 **350**	575	500	MHz Min
		Supply = ±5V	500				
SR	Slew Rate	A_V = +25 (Note 8)	300	200 **180**	200	200	V/μs Min
		Supply = ±5V	200				
PBW	Power Bandwidth Product	V_{OUT} = 20 V_{PP}	4.5				MHz
t_S	Settling Time	10V Step to 0.1% A_V = −25, R_L = 2 kΩ	80				ns
ϕ_m	Phase Margin	A_V = +25	45				Deg
A_D	Differential Gain	NTSC, A_V = +25	<0.1				%
ϕ_D	Differential Phase	NTSC, A_V = +25	<0.1				Deg
e_{np-p}	Input Noise Voltage	F = 10 kHz	5				$nV/\sqrt{Hz}$
i_{np-p}	Input Noise Current	F = 10 kHz	1.5				$pA/\sqrt{Hz}$

Note 1: Continuous short-circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C.

Note 2: The typical junction-to-ambient thermal resistance of the molded plastic DIP (N) is 105°C/Watt, and the molded plastic SO (M) package is 155°C/Watt, and the cerdip (J) package is 125°C/Watt. All numbers apply for packages soldered directly into a printed circuit board.

Note 3: All limits guaranteed by testing or correlation.

Note 4: For single supply operation, the following conditions apply: V+ = 5V, V− = 0V, V_{CM} = 2.5C, V_{OUT} = 2.5V. Pin 1 & Pin 8 (V_{OS} Adjust) are each connected to Pin 4 (V−) to realize maximum output swing. This connection will degrade V_{OS}.

Note 5: $C_L \leq 5$ pF.

Note 6: In order to achieve optimum AC performance, the input stage was designed without protective clamps. Exeeding the maximum differential input voltage results in reverse breakdown of the base-emitter junction of one of the input transistors and probable degradation of the input parameters (especially V_{OS}, I_{OS}, and Noise).

Note 7: The average voltage that the weakest pin combinations (those involving Pin 2 or Pin 3) can withstand and still conform to the datasheet limits. The test circuit used consists of the human body model of 100 pF in series with 1500Ω.

Note 8: V_{IN} = 0.8V step. For supply = ±5V, V_{IN} = 0.2V step.

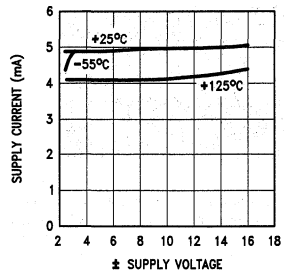
Note 9: Voltage Gain is the total output swing (20V) divided by the input signal required to produce that swing.

Note 10: The voltage between V^+ and either input pin must not exceed 36V.

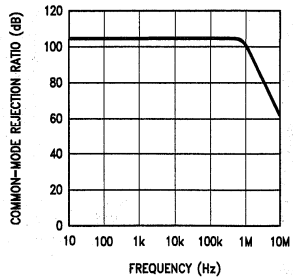
Note 11: A military RETS electrical test specification is available on request. At the time of printing, the LM6165J/883 RETS spec complied with the **Boldface** limits in this column. The LM6165J/883 may also be procured as Standard Military Drawing #5962-8962501PA.

Typical Performance Characteristics $R_L = 10\ k\Omega$, $T_A = 25°C$ unless otherwise specified

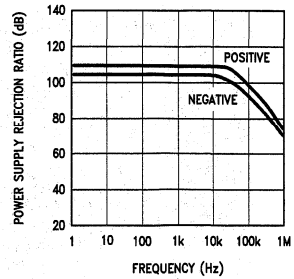
Supply Current vs Supply Voltage



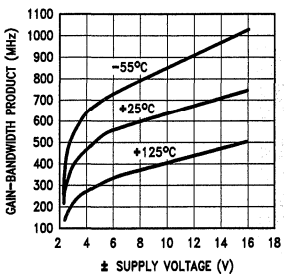
Common-Mode Rejection Ratio



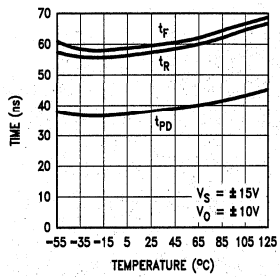
Power Supply Rejection Ratio



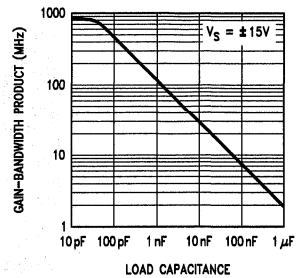
Gain-Bandwidth Product



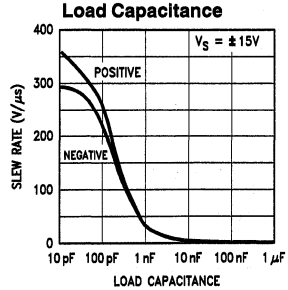
Propagation Delay, Rise and Fall Times



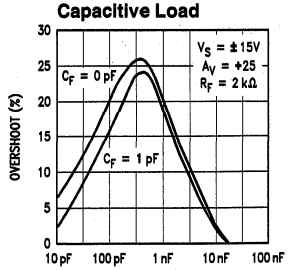
Gain-Bandwidth Product vs Load Capacitance



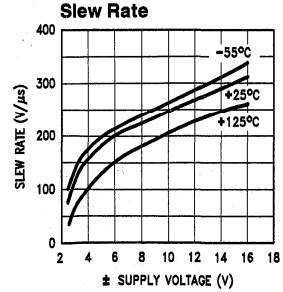
Slew Rate vs Load Capacitance



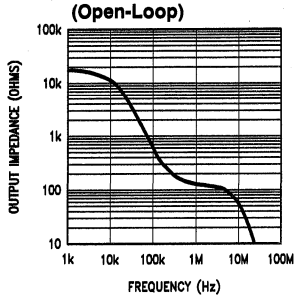
Overshoot vs Capacitive Load



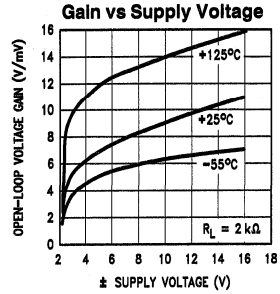
Slew Rate



Output Impedance (Open-Loop)



Gain vs Supply Voltage

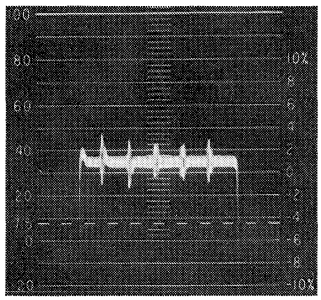


TL/H/9152–5

Typical Performance Characteristics (Continued)

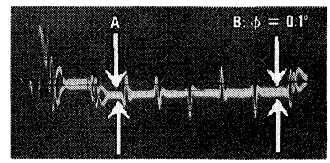
R_L = 10 kΩ, T_A = 25°C unless otherwise specified

Differential Gain (Note)



TL/H/9152-6

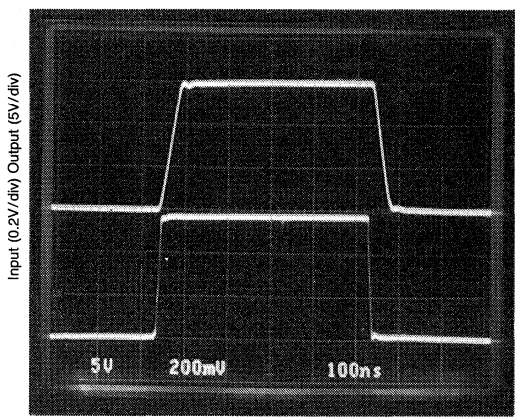
Differential Phase (Note)



TL/H/9152-7

Note: Differential gain and differential phase measured for four series LM6365 op amps configured with gain of +25 (each output attenuated by 96%), in series with an LM6321 buffer. Error added by LM6321 is negligible. Test performed using Tektronix Type 520 NTSC test system.

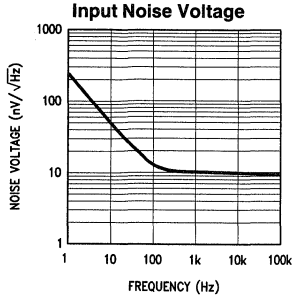
Step Response; Av = +25



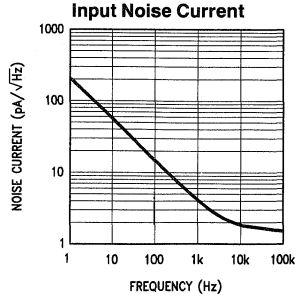
TL/H/9152-1

TIME (50 (ns/div)

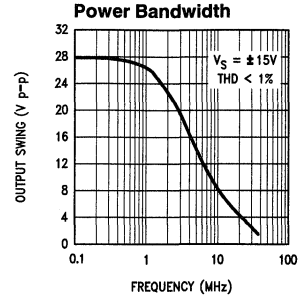
Input Noise Voltage



Input Noise Current



Power Bandwidth

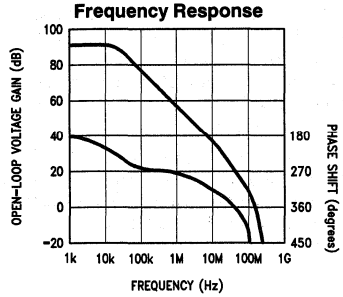


TL/H/9152-9

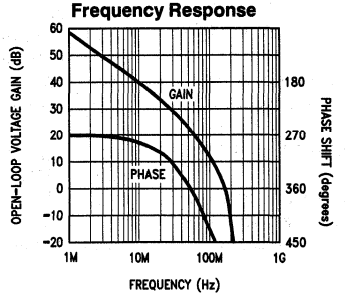
Typical Performance Characteristics (Continued)

R_L = 10 kΩ, T_A = 25°C unless otherwise specified

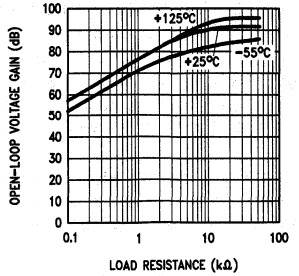
Open-Loop Frequency Response



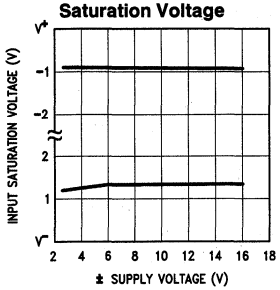
Open-Loop Frequency Response



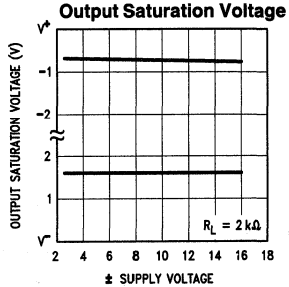
Voltage Gain vs Load Resistance



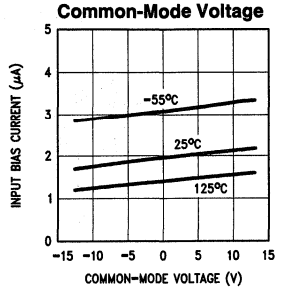
Common-Mode Input Saturation Voltage



Output Saturation Voltage

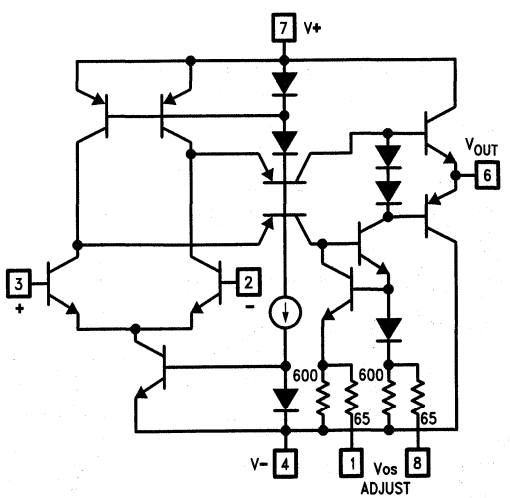


Bias Current vs Common-Mode Voltage



TL/H/9152–10

Simplified Schematic



TL/H/9152–3

Applications Tips

The LM6365 is stable for gains of 25 or greater. The LM6361 and LM6364, specified in separate datasheets, are compensated versions of the LM6365. The LM6361 is unity-gain stable, while the LM6364 is stable for gains as low as 5. The LM6361, and LM6364 have the same high slew rate as the LM6365, typically 300 V/μs.

To use the LM6365 for gains less than 25, a series resistor-capacitor network should be added between the input pins (as shown in the Typical Applications, Noise Gain Compensation) so that the high-frequency noise gain rises to at least 25.

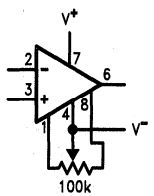
Power supply bypassing will improve stability and transient response of the LM6365, and is recommended for every design. 0.01 μF to 0.1 μF ceramic capacitors should be used (from each supply "rail" to ground); an additional 2.2 μF to 10 μF (tantalum) may be required for extra noise reduction.

Keep all leads short to reduce stray capacitance and lead inductance, and make sure ground paths are low-impedance, especially where heavier currents will be flowing. Stray capacitance in the circuit layout can cause signal coupling between adjacent nodes, and can cause circuit gain to unintentionally vary with frequency.

Breadboarded circuits will work best if they are built using generic PC boards with a good ground plane. If the op amps are used with sockets, as opposed to being soldered into the circuit, the additional input capacitance may degrade circuit performance.

Typical Applications

Offset Voltage Adjustment



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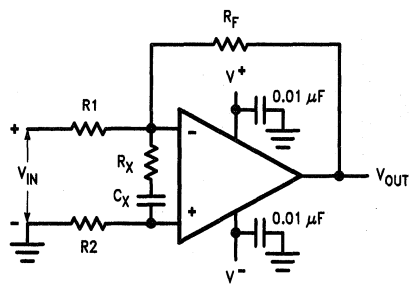
Noise-Gain Compensation



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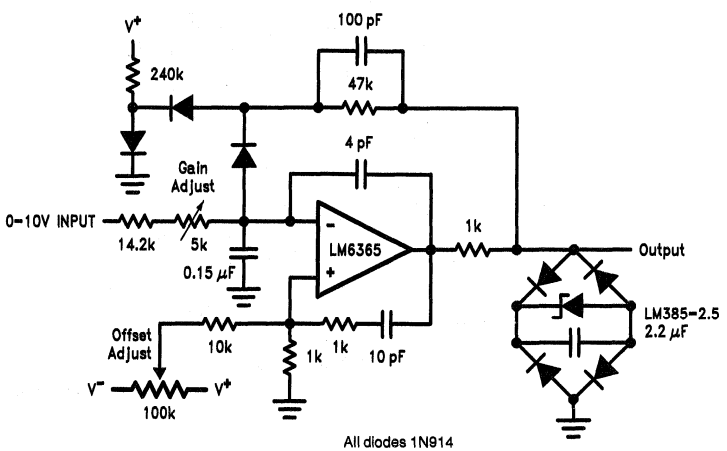
$R_X C_X \geq 1/(2\pi \bullet 25\ MHz)$

$[R1 + R_F (1 + R1/R2)] = 25\ R_X$

1 MHz Voltage-to-Frequency Converter
(f_{OUT} = 1 MHz for V_{IN} = 10V)



All diodes 1N914

TL/H/9152–13

National Semiconductor

LM6181 100 mA, 100 MHz Current Feedback Amplifier

General Description

The LM6181 current-feedback amplifier offers an unparalleled combination of bandwidth, slew-rate, and output current. The amplifier can directly drive up to 100 pF capacitive loads without oscillating and a 10V signal into a 50Ω or 75Ω back-terminated coax cable system over the full industrial temperature range. This represents a radical enhancement in output drive capability for an 8-pin high-speed amplifier making it ideal for video applications.

Built on National's advanced high-speed VIP™ II (Vertically Integrated PNP) process, the LM6181 employs current-feedback providing bandwidth that does not vary dramatically with gain; 100 MHz at $A_V = -1$, 60 MHz at $A_V = -10$. With a slew rate of 2000V/μs, 2nd harmonic distortion of −50 dBc at 10 MHz and settling time of 50 ns (0.1%) the LM6181 dynamic performance makes it ideal for data acquisition, high speed ATE, and precision pulse amplifier applications.

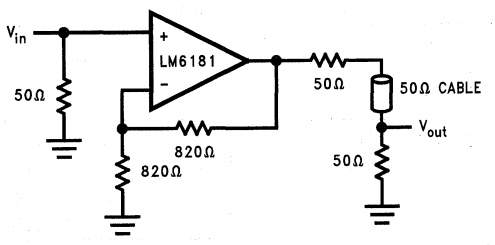
Features (Typical unless otherwise noted)

- Slew rate 2000 V/μs
- Settling time (0.1%) 50 ns
- Characterized for supply ranges ±5V and ±15V
- Low differential gain and phase error 0.05%, 0.04°
- High output drive ±10V into 100Ω
- Guaranteed bandwidth and slew rate
- Improved performance over EL2020, OP160, AD844, LT1223 and HA5004

Applications

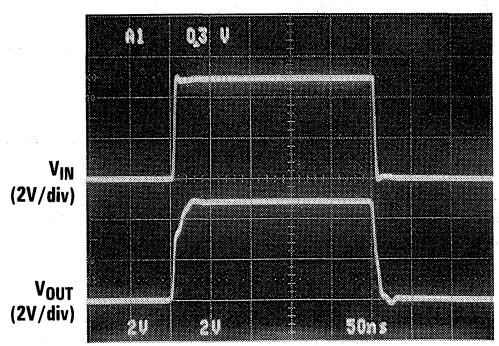
- Coax cable driver
- Video amplifier
- Flash ADC buffer
- High frequency filter

Typical Application



TL/H/11328–1

Cable Driver

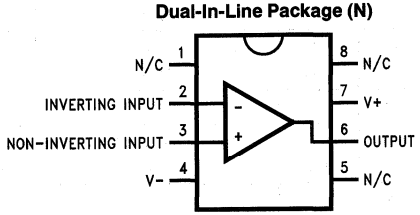


TIME (50ns/div)

TL/H/11328–2

Connection Diagrams (For Ordering Information See Back Page)

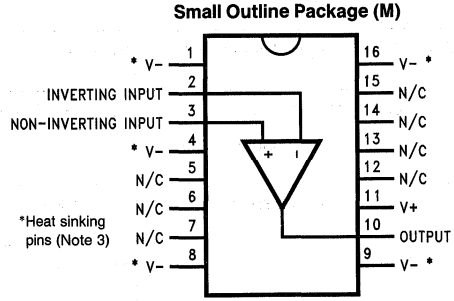
Dual-In-Line Package (N)



TL/H/11328–3

Order Number LM6181IN, LM6181AIN or LM6181AMN
See NS Package Number N08E

Small Outline Package (M)



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Order Number LM6181IM or LM6181AIM
See NS Package Number M16A

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	±18V
Differential Input Voltage	±6V
Input Voltage	±Supply Voltage
Inverting Input Current	15 mA
Soldering Information	
Dual-In-Line Package (N) Soldering (10 sec)	260°C
Small Outline Package (M)	
Vapor Phase (60 seconds)	215°C
Infrared (15 seconds)	220°C
Output Short Circuit	(Note 7)
Storage Temperature Range	$-65°C \le T_J \le +150°C$
Maximum Junction Temperature	150°C
ESD Rating (Note 2)	±3000V

Operating Ratings

Supply Voltage Range	7V to 32V
Junction Temperature Range (Note 3)	
LM6181AM	$-55°C \le T_J \le +125°C$
LM6181AI, LM6181I	$-40°C \le T_J \le +85°C$

DC Electrical Characteristics

The following specifications apply for **Supply Voltage** = ±**15V**, and R_L = 1 kΩ unless otherwise noted. **Boldface** limits apply at the temperature extremes; all other limits T_J = 25°C.

Symbol	Parameter	Conditions	LM6181AM		LM6181AI		LM6181I		Units
			Typical (Note 4)	Limit (Note 5)	Typical (Note 4)	Limit (Note 5)	Typical (Note 4)	Limit (Note 5)	
V_{OS}	Input Offset Voltage		2.0	5.0 **5.0**	2.0	5.0 **5.0**	3.5	7.0 **7.0**	mV max
TC V_{OS}	Input Offset Voltage Drift		5.0		5.0		5.0		µV/°C
I_B	Inverting Input Bias Current		2.0	5.0 **12.0**	2.0	5.0 **12.0**	5.0	10 **17.0**	µA max
	Non-Inverting Input Bias Current		0.5	1.5 **3.0**	0.5	1.5 **3.0**	2.0	3.0 **5.0**	
TC I_B	Inverting Input Bias Current Drift		30		30		30		nA/°C
	Non-Inverting Input Bias Current Drift		10		10		10		
I_B PSR	Inverting Input Bias Current Power Supply Rejection	V_S = ±4.5V, ±16V	0.3	0.5 **3.0**	0.3	0.5 **3.0**	0.3	0.75 **4.5**	µA/V max
	Non-Inverting Input Bias Current Power Supply Rejection	V_S = ±4.5V, ±16V	0.05	0.5 **1.5**	0.05	0.5 **1.5**	0.05	0.5 **3.0**	
I_B CMR	Inverting Input Bias Current Common Mode Rejection	$-10V \le V_{CM} \le +10V$	0.3	0.5 **0.75**	0.3	0.5 **0.75**	0.3	0.75 **1.0**	
	Non-Inverting Input Bias Current Common Mode Rejection	$-10V \le V_{CM} \le +10V$	0.1	0.5 **0.5**	0.1	0.5 **0.5**	0.1	0.5 **0.5**	
CMRR	Common Mode Rejection Ratio	$-10V \le V_{CM} \le +10V$	60	50 **50**	60	50 **50**	60	50 **50**	dB min
PSRR	Power Supply Rejection Ratio	V_S = ±4.5V, ±16V	80	70 **70**	80	70 **70**	80	70 **65**	dB min
R_O	Output Resistance	$A_V = -1$, f = 300 kHz	0.2		0.2		0.2		Ω
R_{IN}	Non-Inverting Input Resistance		10	5.0 **5.0**	10	5.0 **5.0**	10	2.5 **2.5**	MΩ min
V_O	Output Voltage Swing	R_L = 1 kΩ	12	11 **11**	12	11 **11**	12	11 **11**	V min
		R_L = 100Ω	11	10 **7.5**	11	10 **8.0**	11	10 **8.0**	
I_{SC}	Output Short Circuit Current		130	100 **75**	130	100 **85**	130	100 **85**	mA min

DC Electrical Characteristics (Continued)

The following specifications apply for **Supply Voltage** = ±**15V**, and R_L = 1 kΩ unless otherwise noted. **Boldface** limits apply at the temperature extremes; all other limits T_J = 25°C.

Symbol	Parameter	Conditions	LM6181AM		LM6181AI		LM6181I		Units
			Typical (Note 4)	Limit (Note 5)	Typical (Note 4)	Limit (Note 5)	Typical (Note 4)	Limit (Note 5)	
Z_T	Transimpedance	R_L = 1 kΩ	1.8	1.0 **0.6**	1.8	1.0 **0.6**	1.8	0.8 **0.6**	MΩ min
		R_L = 100Ω	1.4	0.8 **0.45**	1.4	0.8 **0.5**	1.4	0.7 **0.45**	
I_S	Supply Current	No Load, V_O = 0V	7.5	10 **10**	7.5	10 **10**	7.5	10 **10**	mA max
V_{CM}	Input Common Mode Voltage Range		$V^+ - 1.7V$ $V^- + 1.7V$		$V^+ - 1.7V$ $V^- + 1.7V$		$V^+ - 1.7V$ $V^- + 1.7V$		V

AC Electrical Characteristics

The following specifications apply for **Supply Voltage** = ±**15V**, R_L = 1 kΩ unless otherwise noted. **Boldface** limits apply at the temperature extremes; all other limits T_J = 25°C.

Symbol	Parameter	Conditions	LM6181AM		LM6181AI		LM6181I		Units
			Typical (Note 4)	Limit (Note 5)	Typical (Note 4)	Limit (Note 5)	Typical (Note 4)	Limit (Note 5)	
BW	Closed Loop Bandwidth −3 dB	A_V = +2	100		100		100		MHz min
		A_V = +10	80		80		80		
		A_V = −1	100	80	100	80	100	80	
		A_V = −10	60		60		60		
PBW	Power Bandwidth	A_V = −1, V_O = 5 V_{PP}	60		60		60		
SR	Slew Rate	Overdriven	2000		2000		2000		V/μs min
		A_V = −1, V_O = ±10V (Note 6)	1400	1000	1400	1000	1400	1000	
t_s	Settling Time (0.1%)	A_V = −1, V_O = ±5V R_L = 150Ω	50		50		50		ns
t_r, t_f	Rise and Fall Time	V_O = 1 V_{PP}	5		5		5		
t_p	Propagation Delay Time	V_O = 1 V_{PP}	6		6		6		
$i_{n(+)}$	Non-Inverting Input Noise Current Density	f = 1 kHz	3		3		3		pA/√Hz
$i_{n(-)}$	Inverting Input Noise Current Density	f = 1 kHz	16		16		16		pA/√Hz
e_n	Input Noise Voltage Density	f = 1 kHz	4		4		4		nV/√Hz
	Second Harmonic Distortion	2 V_{PP}, 10 MHz	−50		−50		−50		dBc
	Third Harmonic Distortion	2 V_{PP}, 10 MHz	−55		−55		−50		
	Differential Gain	R_L = 150Ω A_V = +2 NTSC	0.05		0.05		0.05		%
	Differential Phase	R_L = 150Ω A_V = +2 NTSC	0.04		0.04		0.04		Deg

DC Electrical Characteristics

The following specifications apply for **Supply Voltage** = ±**5V**, and R_L = 1 kΩ unless otherwise noted. **Boldface** limits apply at the temperature extremes; all other limits T_J = 25°C.

Symbol	Parameter	Conditions	LM6181AM		LM6181AI		LM6181I		Units
			Typical (Note 4)	Limit (Note 5)	Typical (Note 4)	Limit (Note 5)	Typical (Note 4)	Limit (Note 5)	
V_{OS}	Input Offset Voltage		1.5	3.0 **3.0**	1.5	3.0 **3.0**	3.0	5.0 **5.0**	mV max
TC V_{OS}	Input Offset Voltage Drift		2.5		2.5		2.5		µV/°C
I_B	Inverting Input Bias Current		5.0	10 **22**	5.0	10 **22**	5.0	17.5 **27.0**	µA max
	Non-Inverting Input Bias Current		0.25	1.5 **1.5**	0.25	1.5 **1.5**	0.25	3.0 **5.0**	µA max
TC I_B	Inverting Input Bias Current Drift		50		50		50		nA/°C
	Non-Inverting Input Bias Current Drift		3.0		3.0		3.0		nA/°C
I_B PSR	Inverting Input Bias Current Power Supply Rejection	V_S = ±4.0V, ±6.0V	0.3	0.5 **0.5**	0.3	0.5 **0.5**	0.3	1.0 **1.0**	µA/V max
	Non-Inverting Input Bias Current Power Supply Rejection	V_S = ±4.0V, ±6.0V	0.05	0.5 **0.5**	0.05	0.5 **0.5**	0.05	0.5 **0.5**	µA/V max
I_B CMR	Inverting Input Bias Current Common Mode Rejection	$-2.5V \le V_{CM} \le +2.5V$	0.3	0.5 **1.0**	0.3	0.5 **1.0**	0.3	1.0 **1.5**	µA/V max
	Non-Inverting Input Bias Current Common Mode Rejection	$-2.5V \le V_{CM} \le +2.5V$	0.12	0.5 **1.0**	0.12	0.5 **0.5**	0.12	0.5 **0.5**	µA/V max
CMRR	Common Mode Rejection Ratio	$-2.5V \le V_{CM} \le +2.5V$	57	50 **47**	57	50 **47**	57	50 **47**	dB min
PSRR	Power Supply Rejection Ratio	V_S = ±4.0V, ±6.0V	80	70 **70**	80	70 **70**	80	64 **64**	dB min
R_O	Output Resistance	A_V = −1, f = 300 kHz	0.25		0.25		0.25		Ω
R_{IN}	Non-Inverting Input Resistance		8	5 **2.5**	8	5 **2.5**	8	2.5 **2.0**	MΩ min
V_O	Output Voltage Swing	R_L = 1 kΩ	2.6	2.25 **2.2**	2.6	2.25 **2.25**	2.6	2.25 **2.25**	V min
		R_L = 100Ω	2.2	2.0 **2.0**	2.2	2.0 **2.0**	2.2	2.0 **2.0**	V min
I_{SC}	Output Short Circuit Current		100	75 **70**	100	75 **70**	100	75 **70**	mA min
Z_T	Transimpedance	R_L = 1 kΩ	1.4	0.75 **0.5**	1.4	0.75 **0.5**	1.0	0.6 **0.4**	MΩ min
		R_L = 100Ω	1.0	0.5 **0.25**	1.0	0.5 **0.3**	1.0	0.4 **0.25**	MΩ min
I_S	Supply Current	No Load, V_O = 0V	6.5	8.5 **8.5**	6.5	8.5 **8.5**	6.5	8.5 **8.5**	mA max
V_{CM}	Input Common Mode Voltage Range		$V^+ - 1.7V$ $V^- + 1.7V$		$V^+ - 1.7V$ $V^- + 1.7V$		$V^+ - 1.7V$ $V^- + 1.7V$		V

AC Electrical Characteristics

The following specifications apply for **Supply Voltage** = ±5V, R_L = 1 kΩ unless otherwise noted. **Boldface** limits apply at the temperature extremes; all other limits T_J = 25°C.

Symbol	Parameter	Conditions	LM6181AM		LM6181AI		LM6181I		Units
			Typical (Note 4)	Limit (Note 5)	Typical (Note 4)	Limit (Note 5)	Typical (Note 4)	Limit (Note 5)	
BW	Closed Loop Bandwidth −3 dB	A_V = +2	50		50		50		MHZ min
		A_V = +10	40		40		40		
		A_V = −1	55	35	55	35	55	35	
		A_V = −10	35		35		35		
PBW	Power Bandwidth	A_V = −1, V_O = 4 V_{PP}	40		40		40		
SR	Slew Rate	A_V = −1, V_O = ±2V (Note 6)	500	375	500	375	500	375	V/μs min
t_s	Settling Time (0.1%)	A_V = −1, V_O = ±2V R_L = 150Ω	50		50		50		ns
t_r, t_f	Rise and Fall Time	V_O = 1 V_{PP}	8.5		8.5		8.5		
t_p	Propagation Delay Time	V_O = 1 V_{PP}	8		8		8		
$i_{n(+)}$	Non-Inverting Input Noise Current Density	f = 1 kHz	3		3		3		pA/√Hz
$i_{n(-)}$	Inverting Input Noise Current Density	f = 1 kHz	16		16		16		pA/√Hz
e_n	Input Noise Voltage Density	f = 1 kHz	4		4		4		nV/√Hz
	Second Harmonic Distortion	2 V_{PP}, 10 MHz	−45		−45		−45		dBc
	Third Harmonic Distortion	2 V_{PP}, 10 MHz	−55		−55		−55		
	Differential Gain	R_L = 150Ω A_V = +2 NTSC	0.063		0.063		0.063		%
	Differential Phase	R_L = 150Ω A_V = +2 NTSC	0.16		0.16		0.16		Deg

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating ratings indicate conditions the device is intended to be functional, but device parameter specifications may not be guaranteed under these conditions. For guaranteed specifications and test conditions, see the Electrical Characteristics.

Note 2: Human body model 100 pF and 1.5 kΩ.

Note 3: The typical junction-to-ambient thermal resistance of the molded plastic DIP(N) package soldered directly into a PC board is 102°C/W. The junction-to-ambient thermal resistance of the S.O. surface mount (M) package mounted flush to the PC board is 70°C/W when pins 1, 4, 8, 9 and 16 are soldered to a total 2 in^2 1 oz. copper trace.

Note 4: Typical values represent the most likely parametric norm.

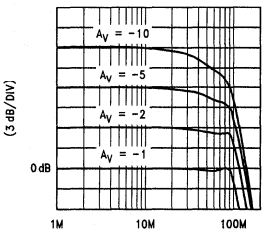
Note 5: All limits guaranteed at room temperature (standard type face) or at operating temperature extremes (**bold face type**).

Note 6: Measured from +25% to +75% of output waveform.

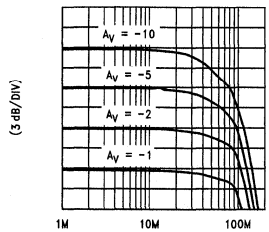
Note 7: Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C. Output currents in excess of ±130 mA over a long term basis may adversely affect reliability.

Typical Performance Characteristics T_A = 25°C unless otherwise noted

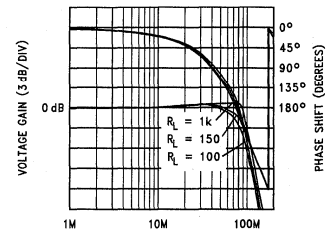
CLOSED-LOOP FREQUENCY RESPONSE
$V_S = \pm 15V$; $R_f = 820\Omega$; $R_L = 1\,k\Omega$



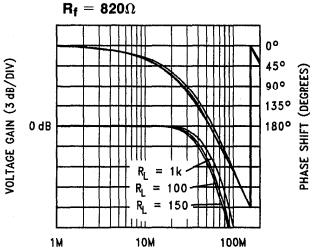
CLOSED-LOOP FREQUENCY RESPONSE
$V_S = \pm 15V$; $R_f = 820\Omega$; $R_L = 150\Omega$



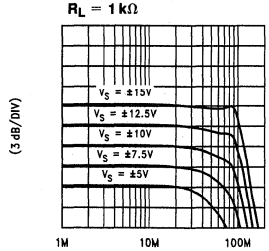
UNITY GAIN FREQUENCY RESPONSE
$V_S = \pm 15V$; $A_V = +1$; $R_f = 820\Omega$



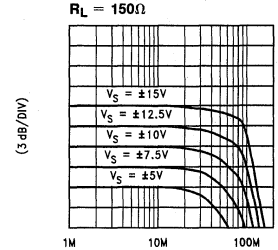
UNIT GAIN FREQUENCY RESPONSE
$V_S = \pm 5V$; $A_V = +1$; $R_f = 820\Omega$



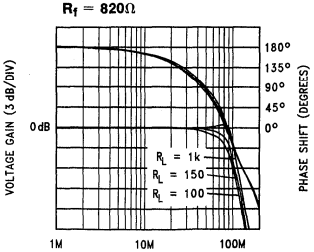
FREQUENCY RESPONSE vs SUPPLY VOLTAGE
$A_V = -1$; $R_f = 820\Omega$; $R_L = 1\,k\Omega$



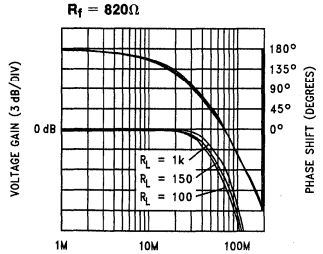
FREQUENCY RESPONSE vs SUPPLY VOLTAGE
$A_V = -1$; $R_f = 820\Omega$; $R_L = 150\Omega$



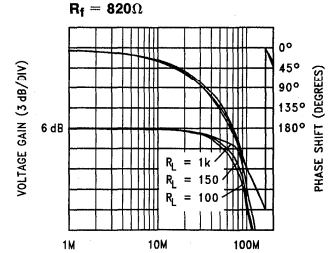
INVERTING GAIN FREQUENCY RESPONSE
$V_S = \pm 15V$; $A_V = -1$; $R_f = 820\Omega$



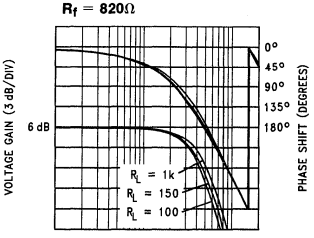
INVERTING GAIN FREQUENCY RESPONSE
$V_S = \pm 5V$; $A_V = -1$; $R_f = 820\Omega$



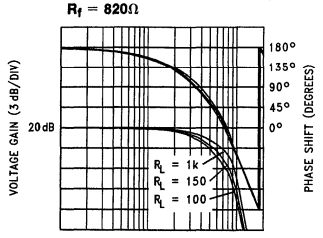
NON-INVERTING GAIN FREQUENCY RESPONSE
$V_S = \pm 15V$; $A_V = +2$; $R_f = 820\Omega$



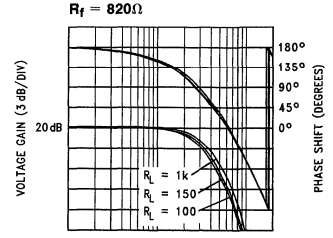
NON-INVERTING GAIN FREQUENCY RESPONSE
$V_S = \pm 5V$; $A_V = +2$; $R_f = 820\Omega$



INVERTING GAIN FREQUENCY RESPONSE
$V_S = \pm 15V$; $A_V = -10$; $R_f = 820\Omega$



INVERTING GAIN FREQUENCY RESPONSE
$V_S = \pm 5V$; $A_V = -10$; $R_f = 820\Omega$



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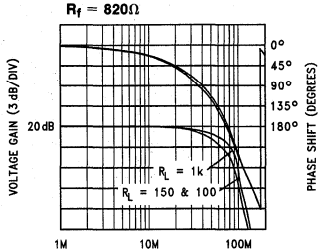
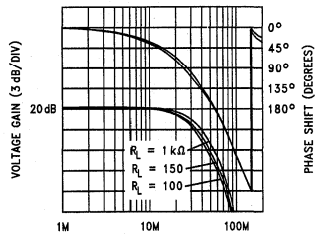
Typical Performance Characteristics $T_A = 25°C$ unless otherwise noted (Continued)

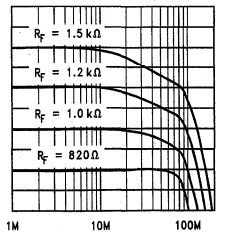
NON-INVERTING GAIN FREQUENCY RESPONSE
$V_S = \pm 15V$; $A_V = +10$;
$R_f = 820\Omega$



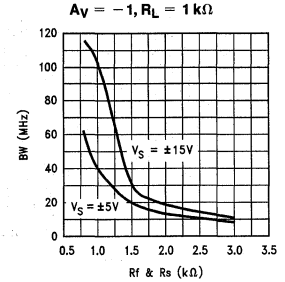
NON-INVERTING GAIN FREQUENCY RESPONSE
$V_S = \pm 5V$; $A_V = +10$;
$R_f = 820\Omega$



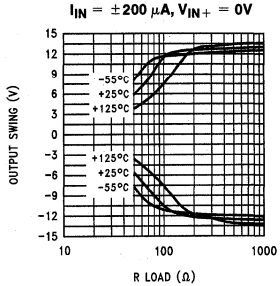
NON-INVERTING GAIN FREQUENCY COMPENSATION
$V_S = \pm 15V$; $A_V = +2$;
$R_L = 150\Omega$



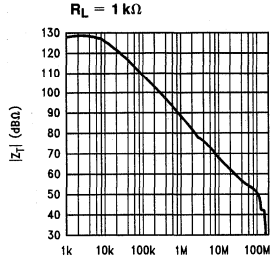
BANDWIDTH vs R_f & R_S
$A_V = -1$, $R_L = 1\ k\Omega$



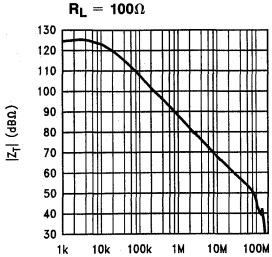
OUTPUT SWING vs R_{LOAD} PULSED, $V_S = \pm 15V$, $I_{IN} = \pm 200\ \mu A$, $V_{IN+} = 0V$



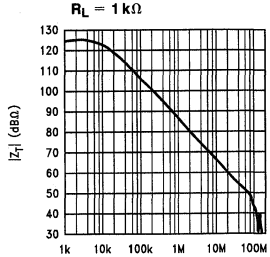
TRANSIMPEDANCE vs FREQUENCY
$V_S = \pm 15V$
$R_L = 1\ k\Omega$



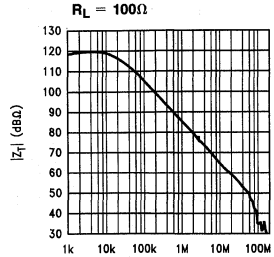
TRANSIMPEDANCE vs FREQUENCY
$V_S = \pm 15V$
$R_L = 100\Omega$



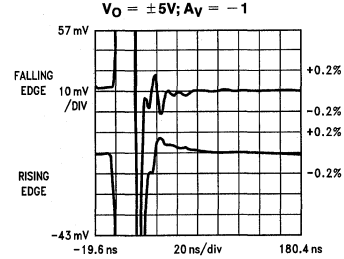
TRANSIMPEDANCE vs FREQUENCY
$V_S = \pm 5V$
$R_L = 1\ k\Omega$



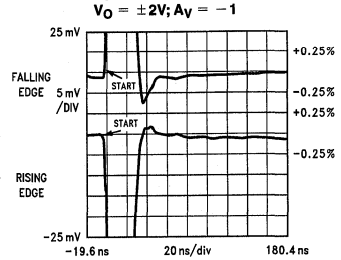
TRANSIMPEDANCE vs FREQUENCY
$V_S = \pm 5V$
$R_L = 100\Omega$



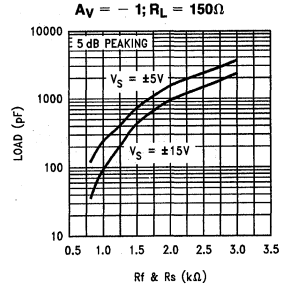
SETTLING RESPONSE
$V_S = \pm 15V$; $R_L = 150\Omega$;
$V_O = \pm 5V$; $A_V = -1$



SETTLING RESPONSE
$V_S = \pm 5V$; $R_L = 150\Omega$;
$V_O = \pm 2V$; $A_V = -1$



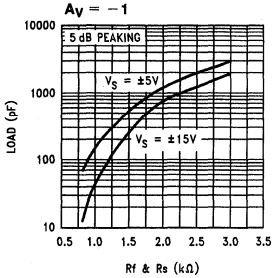
SUGGESTED R_f and R_S for C_L
$A_V = -1$; $R_L = 150\Omega$



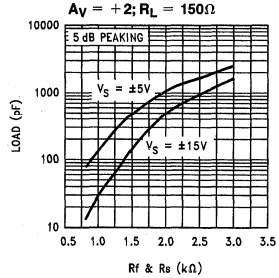
TL/H/11328–6

Typical Performance Characteristics T_A = 25°C unless otherwise noted (Continued)

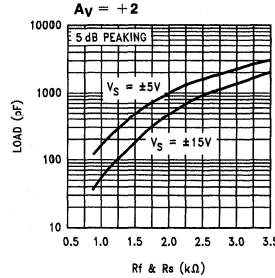
SUGGESTED R_f and R_S FOR C_L $A_V = -1$



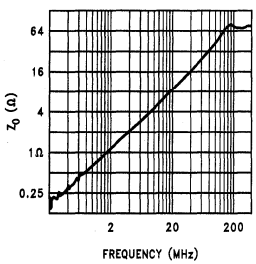
SUGGESTED R_f and R_S FOR C_L $A_V = +2$; $R_L = 150\Omega$



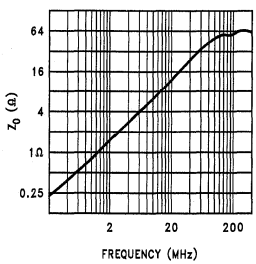
SUGGESTED R_f and R_S FOR C_L $A_V = +2$



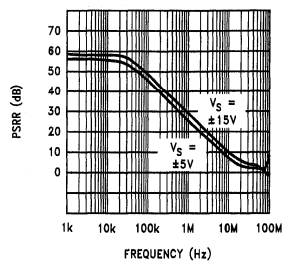
OUTPUT IMPEDANCE vs FREQ $V_S = \pm 15V$; $A_V = -1$ $R_f = 820\Omega$



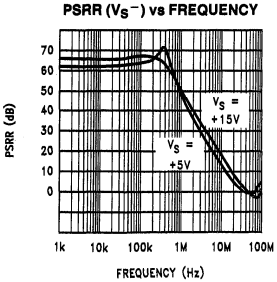
OUTPUT IMPEDANCE vs FREQ $V_S = \pm 5V$; $A_V = -1$ $R_f = 820\Omega$



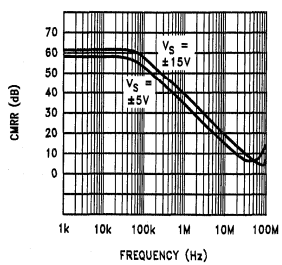
PSRR (V_S^+) vs FREQUENCY



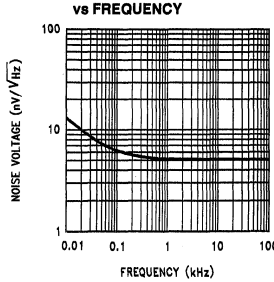
PSRR (V_S^-) vs FREQUENCY



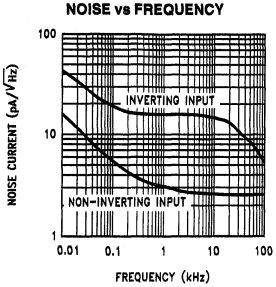
CMRR vs FREQUENCY



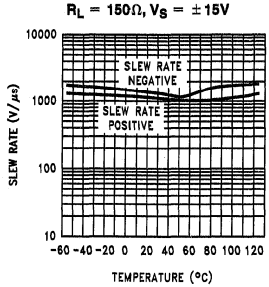
INPUT VOLTAGE NOISE vs FREQUENCY



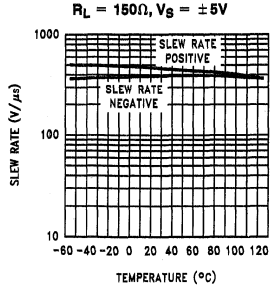
INPUT CURRENT NOISE vs FREQUENCY



SLEW RATE vs TEMPERATURE $A_V = -1$; $R_L = 150\Omega$, $V_S = \pm 15V$



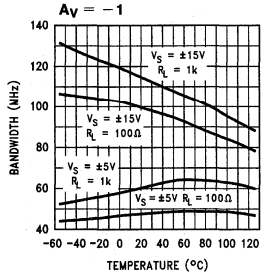
SLEW RATE vs TEMPERATURE $A_V = -1$; $R_L = 150\Omega$, $V_S = \pm 5V$



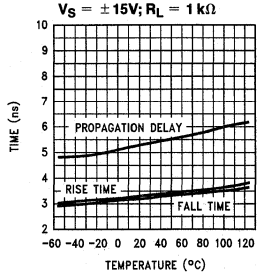
TL/H/11328-7

Typical Performance Characteristics $T_A = 25°C$ unless otherwise noted (Continued)

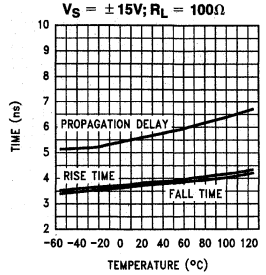
−3 dB BANDWIDTH vs TEMPERATURE $A_V = -1$



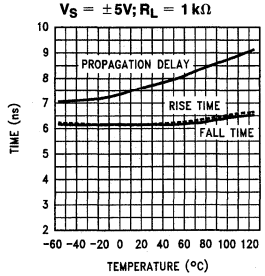
SMALL SIGNAL PULSE RESPONSE vs TEMP, $A_V = +1$ $V_S = \pm15V$; $R_L = 1\,k\Omega$



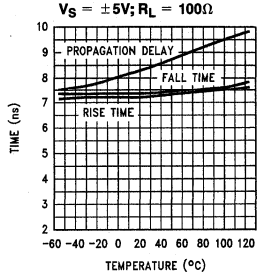
SMALL SIGNAL PULSE RESPONSE vs TEMP, $A_V = +1$ $V_S = \pm15V$; $R_L = 100\Omega$



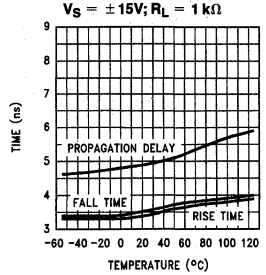
SMALL SIGNAL PULSE RESPONSE vs TEMP, $A_V = +1$ $V_S = \pm5V$; $R_L = 1\,k\Omega$



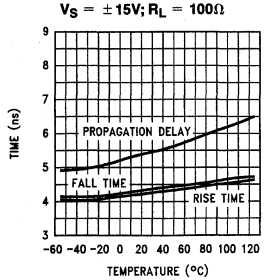
SMALL SIGNAL PULSE RESPONSE vs TEMP, $A_V = +1$ $V_S = \pm5V$; $R_L = 100\Omega$



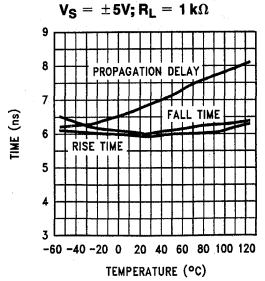
SMALL SIGNAL PULSE RESPONSE vs TEMP, $A_V = -1$ $V_S = \pm15V$; $R_L = 1\,k\Omega$



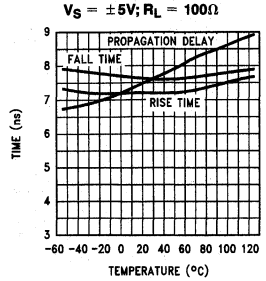
SMALL SIGNAL PULSE RESPONSE vs TEMP, $A_V = -1$ $V_S = \pm15V$; $R_L = 100\Omega$



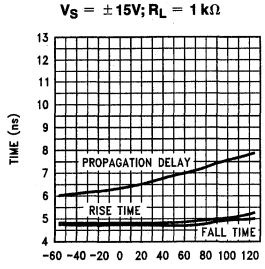
SMALL SIGNAL PULSE RESPONSE vs TEMP, $A_V = -1$ $V_S = \pm5V$; $R_L = 1\,k\Omega$



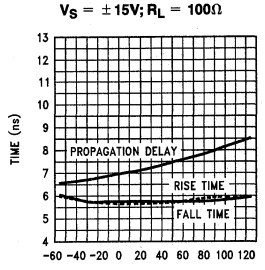
SMALL SIGNAL PULSE RESPONSE vs TEMP, $A_V = -1$ $V_S = \pm5V$; $R_L = 100\Omega$



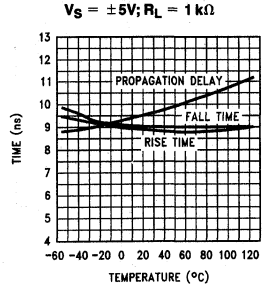
SMALL SIGNAL PULSE RESPONSE vs TEMP, $A_V = +2$ $V_S = \pm15V$; $R_L = 1\,k\Omega$



SMALL SIGNAL PULSE RESPONSE vs TEMP, $A_V = +2$ $V_S = \pm15V$; $R_L = 100\Omega$



SMALL SIGNAL PULSE RESPONSE vs TEMP, $A_V = +2$ $V_S = \pm5V$; $R_L = 1\,k\Omega$



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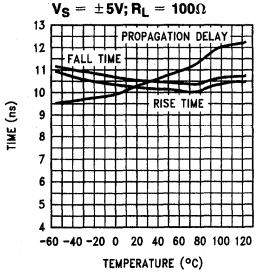
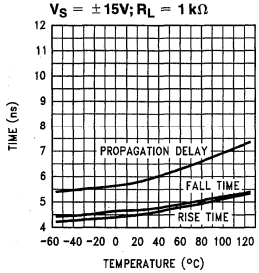
Typical Performance Characteristics $T_A = 25°C$ unless otherwise noted (Continued)

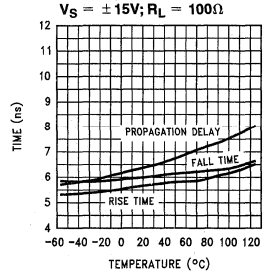
SMALL SIGNAL PULSE RESPONSE vs TEMP, $A_V = +2$ $V_S = \pm 5V$; $R_L = 100\Omega$



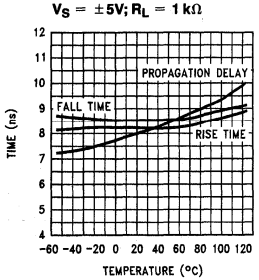
SMALL SIGNAL PULSE RESPONSE vs TEMP, $A_V = -10$ $V_S = \pm 15V$; $R_L = 1\ k\Omega$



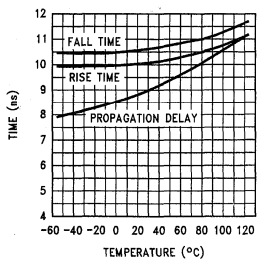
SMALL SIGNAL PULSE RESPONSE vs TEMP, $A_V = -10$ $V_S = \pm 15V$; $R_L = 100\Omega$



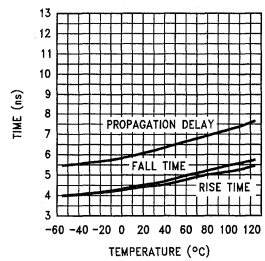
SMALL SIGNAL PULSE RESPONSE vs TEMP, $A_V = -10$ $V_S = \pm 5V$; $R_L = 1\ k\Omega$



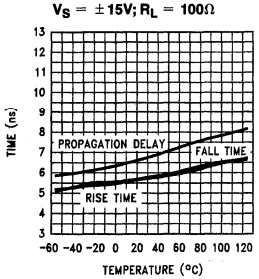
SMALL SIGNAL PULSE RESPONSE vs TEMP, $A_V = -10$ $V_S = \pm 5V$; $R_L = 100\Omega$



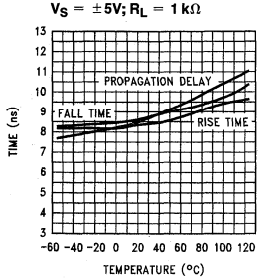
SMALL SIGNAL PULSE RESPONSE vs TEMP, $A_V = +10$ $V_S = \pm 15V$; $R_L = 1\ k\Omega$



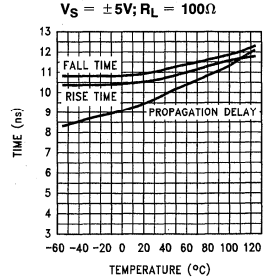
SMALL SIGNAL PULSE RESPONSE vs TEMP, $A_V = +10$ $V_S = \pm 15V$; $R_L = 100\Omega$



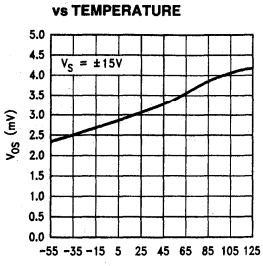
SMALL SIGNAL PULSE RESPONSE vs TEMP, $A_V = +10$ $V_S = \pm 5V$; $R_L = 1\ k\Omega$



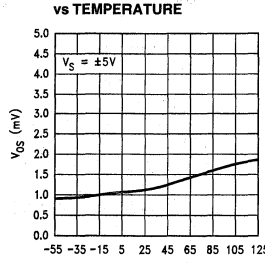
SMALL SIGNAL PULSE RESPONSE vs TEMP, $A_V = +10$ $V_S = \pm 5V$; $R_L = 100\Omega$



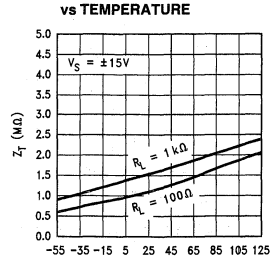
OFFSET VOLTAGE vs TEMPERATURE



OFFSET VOLTAGE vs TEMPERATURE



TRANSIMPEDANCE vs TEMPERATURE



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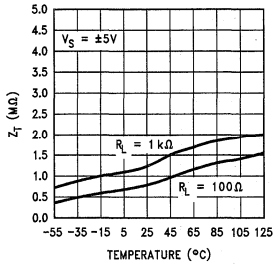
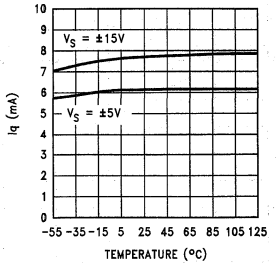
Typical Performance Characteristics T_A = 25°C unless otherwise noted (Continued)

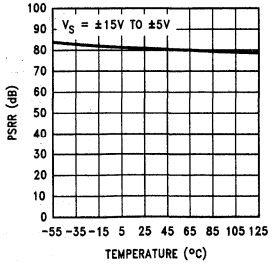
TRANSIMPEDANCE vs TEMPERATURE



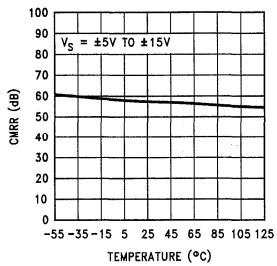
QUIESCENT CURRENT vs TEMPERATURE



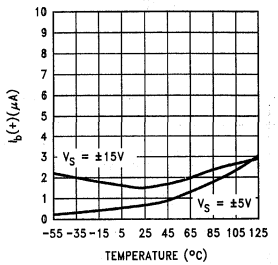
PSRR vs TEMPERATURE



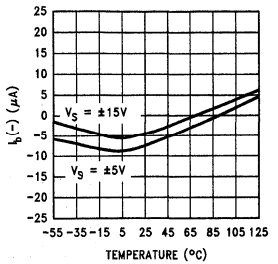
CMRR vs TEMPERATURE



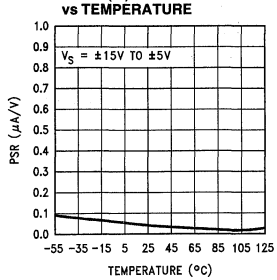
NON-INVERTING BIAS CURRENT vs TEMPERATURE



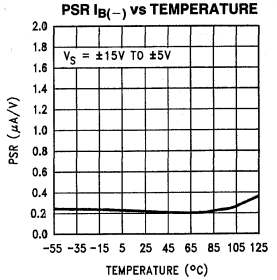
INVERTING BIAS CURRENT vs TEMPERATURE



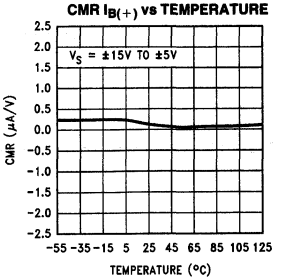
PSR $I_{B(+)}$ vs TEMPERATURE



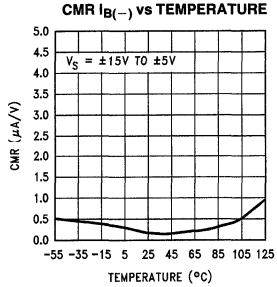
PSR $I_{B(-)}$ vs TEMPERATURE



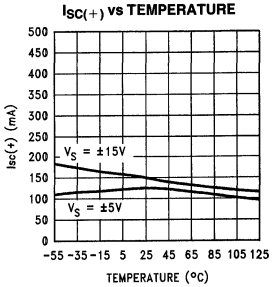
CMR $I_{B(+)}$ vs TEMPERATURE



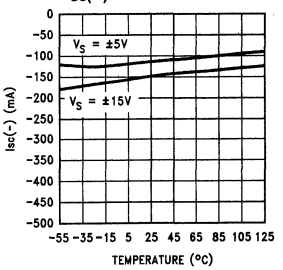
CMR $I_{B(-)}$ vs TEMPERATURE



$I_{SC(+)}$ vs TEMPERATURE



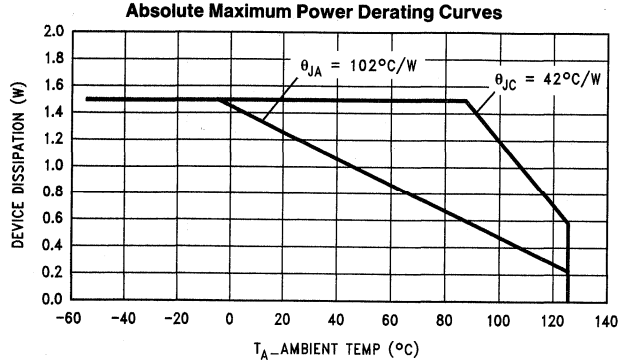
$I_{SC(-)}$ vs TEMPERATURE



TL/H/11328–9

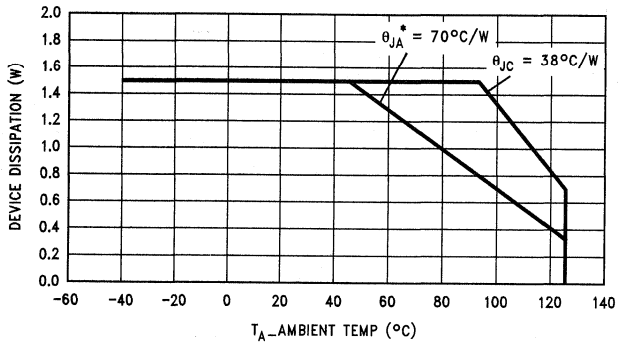
Typical Performance Characteristics

Absolute Maximum Power Derating Curves



TL/H/11328–30

N-Package



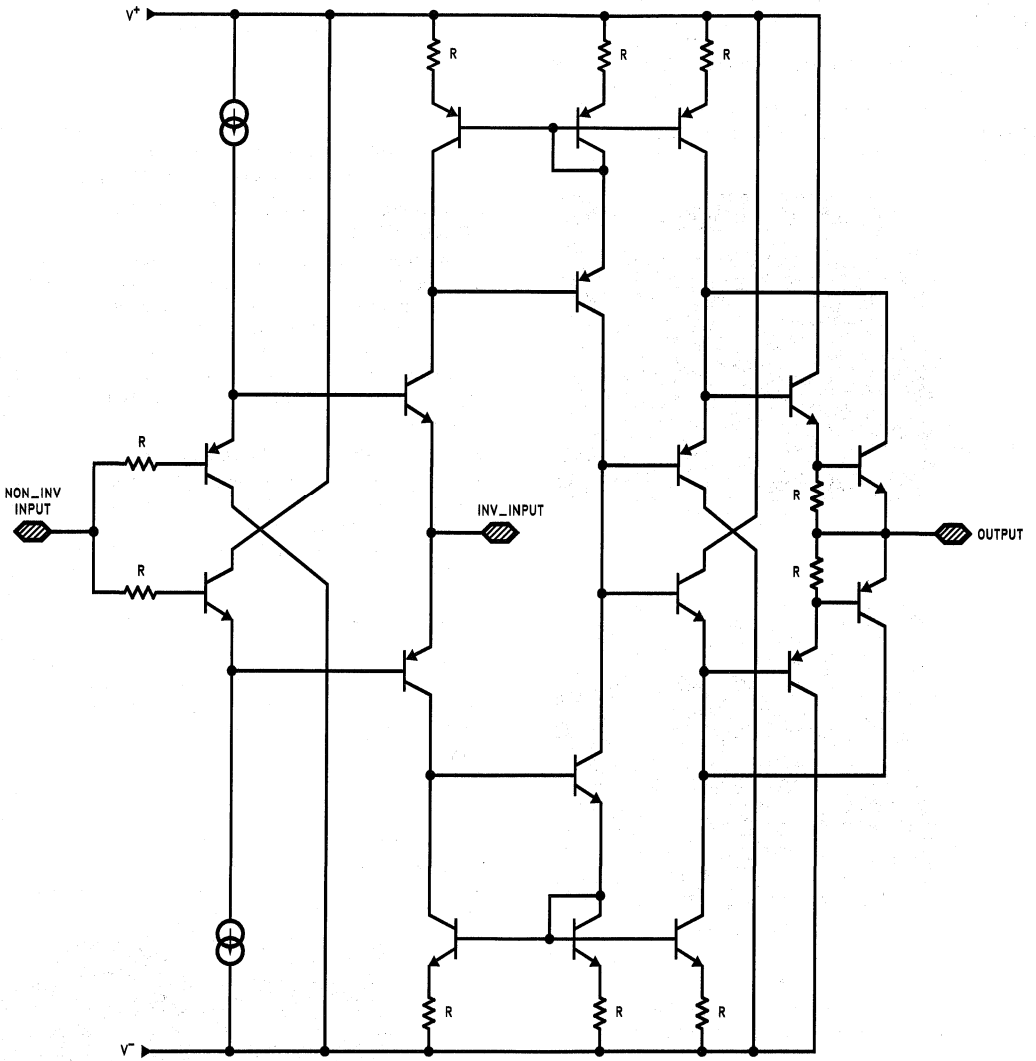
TL/H/11328–31

M-Package

*θ_{JA} = Thermal Resistance with 2 square inches of 1 ounce Copper tied to Pins 1, 8, 9 and 16.

Typical Performance Characteristics (Continued)

Simplified Schematic



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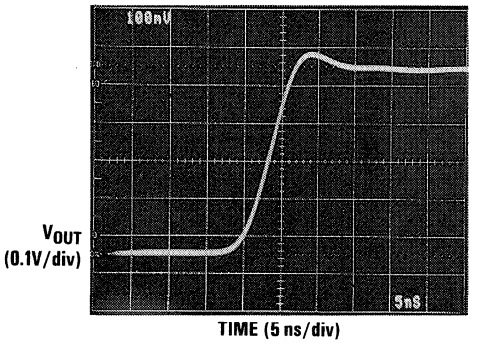
Typical Applications

CURRENT FEEDBACK TOPOLOGY

For a conventional voltage feedback amplifier the resulting small-signal bandwidth is inversely proportional to the desired gain to a first order approximation based on the gain-bandwidth concept. In contrast, the current feedback amplifier topology, such as the LM6181, transcends this limitation to offer a signal bandwidth that is relatively independent of the closed-loop gain. *Figures 1a* and *1b* illustrate that for closed loop gains of −1 and −5 the resulting pulse fidelity suggests quite similar bandwidths for both configurations.



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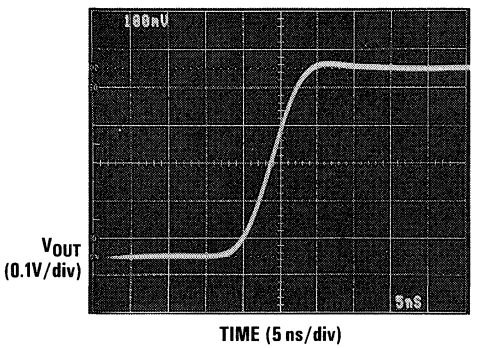
1a



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1b

FIGURES 1a, 1b: Variation of Closed Loop Gain from −1 to −5 Yields Similar Responses

The closed-loop bandwidth of the LM6181 depends on the feedback resistance, R_f. Therefore, R_S and not R_f, must be varied to adjust for the desired closed-loop gain as in *Figure 2*.

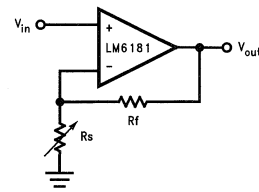

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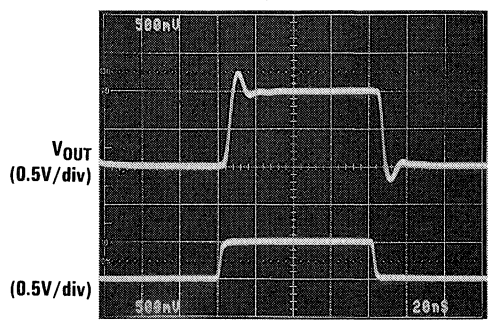
FIGURE 2. R_S Is Adjusted to Obtain the Desired Closed Loop Gain, A_{VCL}

POWER SUPPLY BYPASSING AND LAYOUT CONSIDERATIONS

A fundamental requirement for high-speed amplifier design is adequate bypassing of the power supply. It is critical to maintain a wideband low-impedance to ground at the amplifiers supply pins to insure the fidelity of high speed amplifier transient signals. 10 μF tantalum and 0.1 μF ceramic bypass capacitors are recommended for each supply pin. The bypass capacitors should be placed as close to the amplifier pins as possible (0.5″ or less).

FEEDBACK RESISTOR SELECTION: R_f

Selecting the feedback resistor, R_f, is a dominant factor in compensating the LM6181. For general applications the LM6181 will maintain specified performance with an 820Ω feedback resistor. Although this value will provide good results for most applications, it may be advantageous to adjust this value slightly. Consider, for instance, the effect on pulse responses with two different configurations where both the closed-loop gains are 2 and the feedback resistors are 820Ω, and 1640Ω, respectively. *Figures 3a* and *3b* illustrate the effect of increasing R_f while maintaining the same closed-loop gain—the amplifier bandwidth decreases. Accordingly, larger feedback resistors can be used to slow down the LM6181 (see −3 dB bandwidth vs R_f typical curves) and reduce overshoot in the time domain response. Conversely, smaller feedback resistance values than 820Ω can be used to compensate for the reduction of bandwidth at high closed loop gains, due to 2nd order effects. For example *Figure 4* illustrates reducing R_f to 500Ω to establish the desired small signal response in an amplifier configured for a closed loop gain of 25.



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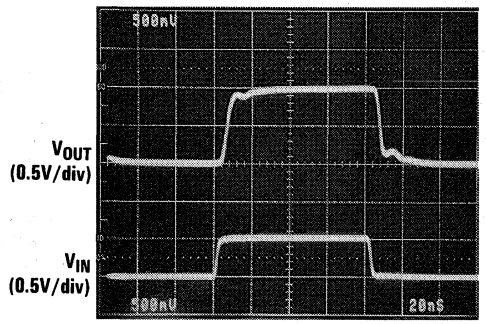
3a: R_f = 820Ω

Typical Applications (Continued)



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3b: $R_f = 1640\Omega$

FIGURES 3a, b: Increasing Compensation with Increasing R_f

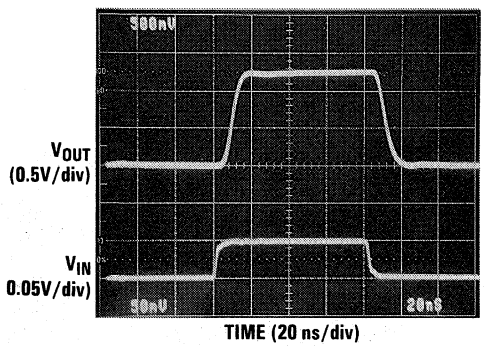

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FIGURE 4: Reducing R_f for Large Closed Loop Gains, $R_f = 500\Omega$

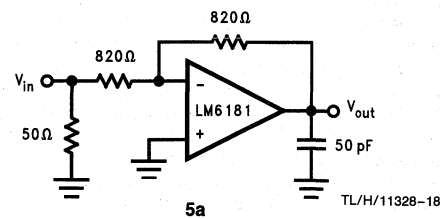
SLEW RATE CONSIDERATIONS

The slew rate characteristics of current feedback amplifiers are different than traditional voltage feedback amplifiers. In voltage feedback amplifiers slew rate limiting or non-linear amplifier behavior is dominated by the finite availability of the 1st stage tail current charging the compensation capacitor. The slew rate of current feedback amplifiers, in contrast, is not constant. Transient current at the inverting input determines slew rate for both inverting and non-inverting gains. The non-inverting configuration slew rate is also determined by input stage limitations. Accordingly, variations of slew rates occur for different circuit topologies.

DRIVING CAPACITIVE LOADS

The LM6181 can drive significantly larger capacitive loads than many current feedback amplifiers. Although the LM6181 can directly drive as much as 100 pF without oscillating, the resulting response will be a function of the feedback resistor value. *Figure 5* illustrates the small-signal pulse response of the LM6181 while driving a 50 pF load. Ringing persists for approximately 70 ns. To achieve pulse responses with less ringing either the feedback resistor can be increased (see typical curves Suggested R_f and R_s for C_L), or resistive isolation can be used (10Ω–51Ω typically works well). Either technique, however, results in lowering the system bandwidth.

Figure 6 illustrates the improvement obtained with using a 47Ω isolation resistor.



5a

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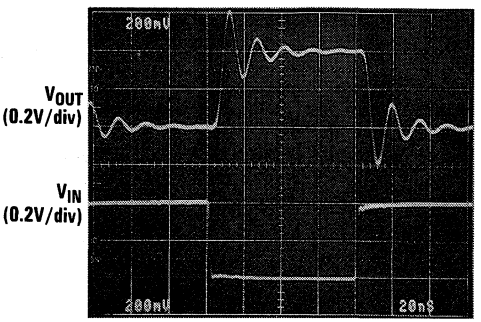

5b

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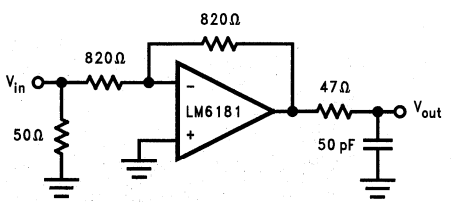
FIGURES 5a, b: $A_V = -1$, LM6181 Can Directly Drive 50 pF of Load Capacitance with 70 ns of Ringing Resulting in Pulse Response



6a

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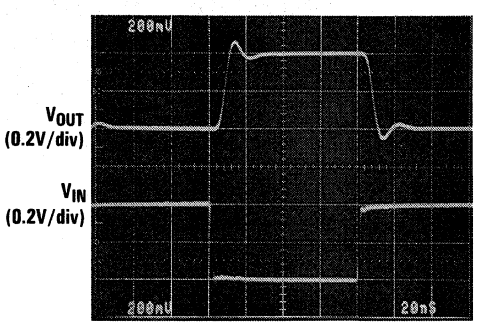


6b

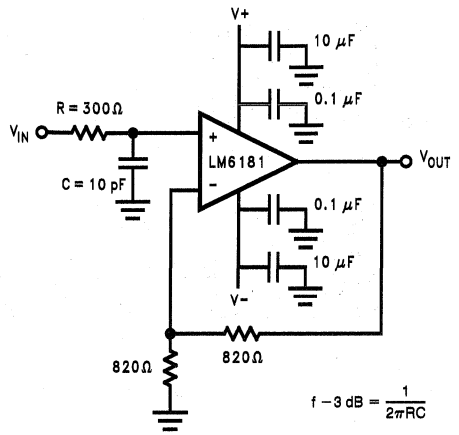
TL/H/11328-21

FIGURES 6a, b: Resistive Isolation of C_L Provides Higher Fidelity Pulse Response. R_f and R_S Could Be Increased to Maintain $A_V = -1$ and Improve Pulse Response Characteristics.

Typical Applications (Continued)

CAPACITIVE FEEDBACK

For voltage feedback amplifiers it is quite common to place a small lead compensation capacitor in parallel with feedback resistance, R_f. This compensation serves to reduce the amplifier's peaking in the frequency domain which equivalently tames the transient response. To limit the bandwidth of current feedback amplifiers, do not use a capacitor across R_f. The dynamic impedance of capacitors in the feedback loop reduces the amplifier's stability. Instead, reduced peaking in the frequency response, and bandwidth limiting can be accomplished by adding an RC circuit, as illustrated in *Figure 7b.*



7a

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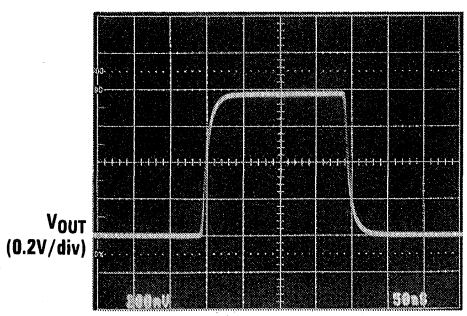

7b

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FIGURES 7a, b: RC Limits Amplifier Bandwidth to 50 MHz, Eliminating Peaking in the Resulting Pulse Response

Typical Performance Characteristics

OVERDRIVE RECOVERY

When the output or input voltage range of a high speed amplifier is exceeded, the amplifier must recover from an overdrive condition. The typical recovery times for open-loop, closed-loop, and input common-mode voltage range overdrive conditions are illustrated in *Figures 9, 11* and *12,* respectively.

The open-loop circuit of *Figure 8* generates an overdrive response by allowing the ±0.5V input to exceed the linear input range of the amplifier. Typical positive and negative overdrive recovery times shown in *Figure 9* are 5 ns and 25 ns, respectively.

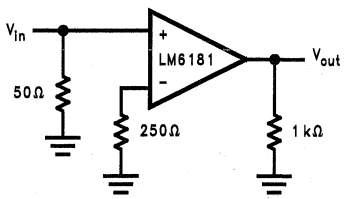

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FIGURE 8

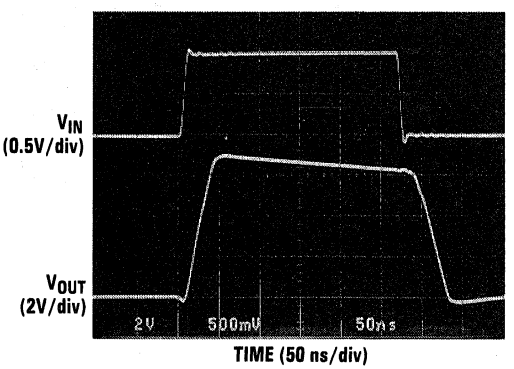

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FIGURE 9. Open-Loop Overdrive Recovery Time of 5 ns, and 25 ns from Test Circuit in *Figure 8*

Typical Performance Characteristics (Continued)

The large closed-loop gain configuration in *Figure 10* forces the amplifier output into overdrive. *Figure 11* displays the typical 30 ns recovery time to a linear output value.

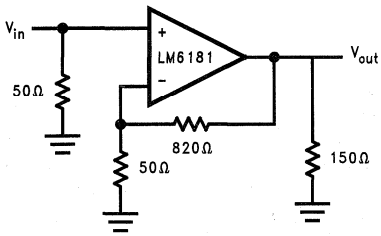

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FIGURE 10

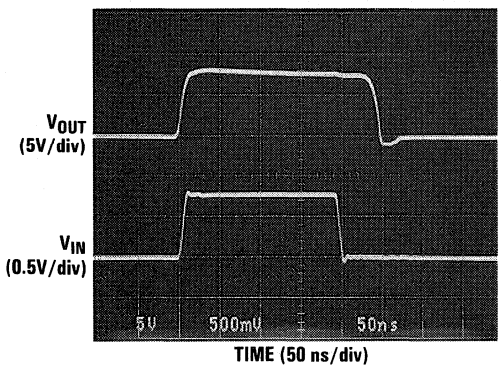

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FIGURE 11. Closed-Loop Overdrive Recovery Time of 30 ns from Exceeding Output Voltage Range from Circuit in *Figure 10*

The common-mode input of the circuit in *Figure 10* is exceeded by a 5V pulse resulting in a typical recovery time of 310 ns shown in *Figure 12*. The LM6181 supply voltage is ±5V.

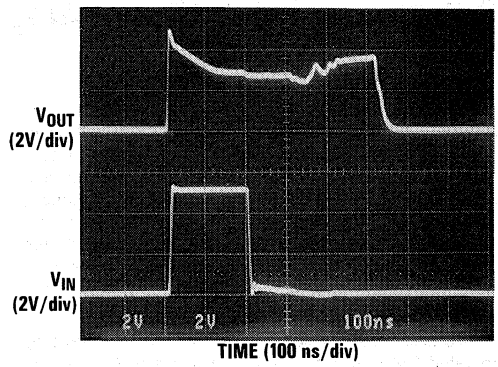

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FIGURE 12. Exceptional Output Recovery from an Input that Exceeds the Common-Mode Range

Ordering Information

Package	Temperature Range		NSC Drawing
	Military −55°C to +125°C	Industrial −40°C to +85°C	
8-Pin Molded DIP	LM6181AMN	LM6181AIN LM6181IN	N08E
16-Pin Small Outline		LM6181AIM LM6181IM	M16A

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office or Distributors for availability and specifications.

National Semiconductor

LM6313 High Speed, High Power Operational Amplifier

General Description

The LM6313 is a high-speed, high-power operational amplifier. This operational amplifier features a 35 MHz small signal bandwidth, and 250 V/μs slew rate. A compensation pin is included for adjusting the open loop bandwidth. The input stage (A1) and output stage (A2) are pinned out separately, and can be used independently. The operational amplifier is designed for low impedance loads and will deliver ±300 mA. The LM6313 has both overcurrent and thermal shutdown protection with an error flag to signal both these fault conditions.

These amplifiers are built with National's VIP™ (Vertically Integrated PNP) process which provides fast PNP transistors that are true complements to the already fast NPN devices. This advanced junction-isolated process delivers high speed performance without the need for complex and expensive dielectric isolation.

Features

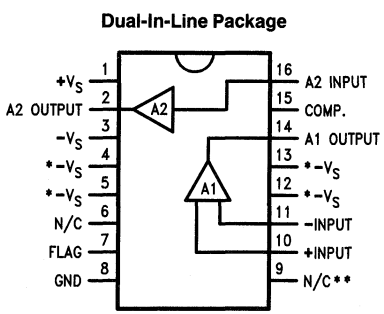
- High slew rate 250 V/μs
- Wide bandwidth 35 MHz
- Peak output current ±300 mA
- Input and output stages pinned out separately
- Single or dual supply operation
- Thermal protection
- Error flag warns of faults
- Wide supply voltage range ±5V to ±15V

Applications

- High speed ATE pin driver
- Data acquisition
- Driving capacitive loads
- Flash A-D input driver
- Precision 50Ω–75Ω video line driver
- Laser diode driver

Connection Diagram

Dual-In-Line Package



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Top View

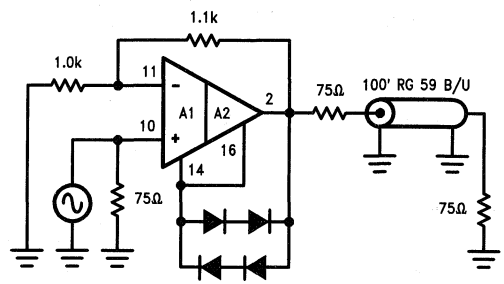
Order Number LM6313N
See NS Package Number N16A

*Heat sink pins

See Note 5 and Applications.

**Do not ground or otherwise connect to this pin.

Typical Application



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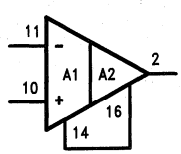
Absolute Maximum Ratings (Note 1)

Total Supply Voltage ($+V_S$ to $-V_S$)	36V (±18)
A1 Differential Input Voltage (Note 2)	±7V
A1 Input Voltage	(V+ −0.7) to (V− −7V)
A2 Input to Output Voltage	±7V
A2 Input Voltage	$\pm V_S$
Flag Output Voltage	GND to $+V_S$
Short-Circuit to Ground	(Note 3)
Storage Temperature Range	$-65°C \le T \le +150°C$
Lead Temperature (Soldering, 5 seconds)	260°C
ESD Tolerance (Note 4)	
Pins 10 and 11	±600V
All Other Pins	±1500V
Operating Temperature Range	
LM6313N	0°C to 70°C
Thermal Derating Information (Note 5)	
θ_{JA}	40°C/W
T_J (Max)	125°C

Operational Amplifier DC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for $T_A = 25°C$, and Supply Voltage $V_S = \pm 15V$. **Boldface** limits apply at temperature extremes. $V_{CM} = 0V$, $R_S = 50\Omega$, the circuit configured as in *Figure 1*.

Symbol	Parameter	Conditions	Typical	25°C Limit	0°C to 70°C Limit	Units
V_{OS}	Input Offset Voltage		5	20	**22**	mV (Max)
$\Delta V_{OS}/\Delta T$	Average Input Offset Voltage Drift		10			μV/°C
I_b	Input Bias Current		2	5	**7**	μA (Max)
I_{OS}	Input Offset Current		0.15	1.5	**1.9**	μA (Max)
$\Delta I_{OS}/\Delta T$	Average Input Offset Current Drift		0.4			nA/°C
R_{IN}	Input Resistance	Differential	325			kΩ
C_{IN}	Input Capacitance	$A_V = +1$, f = 10 MHz	2.2			pF
V_{CM}	Common-Mode Voltage Range		+14.2 −13.2	+13.8 −12.8	**+13.7** **−12.7**	V (Min)
A_{V1} A_{V2}	Voltage Gain 1 Voltage Gain 2	$R_L = 1 k\Omega$, $V_O = \pm 10V$ $R_L = 50\Omega$, $V_O = \pm 8V$	6000 5000	2500 2000	**2000** **1500**	V/V (Min)
CMRR	Common-Mode Rejection Ratio	$-10V \le V_{CM} \le +10V$	90	72	**70**	dB (Min)
PSRR	Power Supply Rejection Ratio	$\pm 5V \le V_S \le \pm 16V$	90	72	**70**	dB (Min)
V_{O1} V_{O2} V_{O3}	Output Voltage Swing 1 Output Voltage Swing 2 Output Voltage Swing 3	$R_L = 1 k\Omega$ $R_L = 100\Omega$ $R_L = 50\Omega$	13.1 12.0 11.0	11.8 10.5 9.0	**11.2** **10.0** **8.5**	±V (Min)
I_S	Supply Current	$T_J = 0°C$ $T_J = 25°C$ $T_J = 125°C$	18	23	**24** **21**	mA (Max)
I_{SC}	Peak Short-Circuit Output	(See *Figure 3*)	300			mA



TL/H/10521–3

FIGURE 1

Electrical Characteristics (Continued)

Operational Amplifier AC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for T_A = 25°C, and Supply Voltage V_S = ±15V. **Boldface** limits apply at temperature extremes. V_{CM} = 0V, R_S = 50Ω, the circuit configured as in *Figure 1*.

Symbol	Parameter	Conditions	Typical	Units
GBW	Gain-Bandwidth Product	@ f = 30 MHz	35	MHz
SR	Slew Rate	A_V = −1, R_L = 50Ω (Note 6)	250	V/μs
PBW	Power Bandwidth	V_{OUT} = 20 V_{PP}	3.0	MHz
t_S	Settling Time	10V Step to 0.1% (See *Figure 2*)	200	ns
	Phase Margin	A_V = −1, R_L = 1 kΩ, C_L = 50 pF	53	Deg
	Differential Gain		0.1	%
	Differential Phase		0.1	Deg
e_n	Input Noise Voltage	f = 10 kHz	14	nV/√Hz
i_n	Input Noise Current	f = 10 kHz	1.8	pA/√Hz

A1 DC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for T_A = 25°C, and Supply Voltage V_S = ±15V. **Boldface** limits apply at temperature extremes. V_{CM} = 0V, R_S = 50Ω.

Symbol	Parameter	Conditions	Typical	25°C Limit	0°C to 70°C Limit	Units
A_{VOL}	Large Signal Voltage Gain	V_{OUT} = ±10V, R_L = 2 kΩ V_{OUT} = ±10V, R_L = ∞	650 6000	300 2500	**250** **2000**	V/V (Min)
CMRR	Common-Mode Rejection Ratio	−10V ≤ V_{CM} ≤ +10V	90	72	**70**	dB (Min)
PSRR	Power Supply Rejection Ratio	±5V ≤ ±V_S ≤ +16V	90	72	**70**	dB (Min)
I_{SC}	Output Short Circuit Current		±60	±30	**±25**	mA (Min)

A1 AC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for T_A = 25°C, and Supply Voltage V_S = ±15V. **Boldface** limits apply at temperature extremes. R_S = 50Ω.

Symbol	Parameter	Conditions	Typical	25°C Limit	Units
GBW	Gain-Bandwidth	f = 30 MHz	37	25	MHz (Min)
SR	Slew Rate	A_V = +1, R_L = 100 kΩ, ±4 V_{IN}, ±2 V_{OUT}	250	150	V/μs (Min)

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test condition listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

Note 2: In order to achieve optimum AC performance, the input stage was designed without protective clamps. Exceeding the maximum differential input voltage results in reverse breakdown of the base-emitter junction of one of the input transistors. Degradation of the input parameters (especially V_{OS}, I_{OS}, and Noise) is proportional to the level of the externally limited breakdown current and the accumulated duration of the breakdown condition.

Note 3: Continuous short-circuit operation of A1 at elevated temperature can result in exceeding the maximum allowed junction temperature of 125°C. A2 contains current limit and thermal shutdown to protect against fault conditions. The device may be damaged by shorts to the supplies.

Note 4: Human body model, C = 100 pF, R_S = 1500Ω.

Electrical Characteristics (Continued)

A2 DC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for T_A = 25°C, and Supply Voltage V_S = ±15V. **Boldface** limits apply at temperature extremes. R_S = 50Ω.

Symbol	Parameter	Conditions	Typical	25°C Limit	0°C to 70°C Limit	Units
A_{V1}	Voltage Gain 1	R_L = 1 kΩ, V_{IN} = ±10V	0.99	0.97	**0.95**	V/mV (Min)
A_{V2}	Voltage Gain 2	R_L = 50Ω, V_{IN} = ±10V	0.9	0.85	**0.82**	V/V (Min)
V_{OS}	Offset Voltage	R_L = 1 kΩ	15	70	**100**	mV (Max)
I_b	Input Bias Current	R_L = 1 kΩ, R_S = 10 kΩ	1	6	**8**	μA (Max)
R_{IN}	Input Resistance	R_L = 50Ω	5			MΩ
C_{IN}	Input Capacitance		3.5			pF
R_O	Output Resistance	I_{OUT} = ±10 mA	3.5	5.0	**8.0**	Ω (Min)
V_O	Voltage Output Swing	R_L = 1 kΩ R_L = 100Ω R_L = 50Ω	13.7 12.5 11.0	13.0 10.5 9.0	**12.7** **10.0** **8.5**	V (Min)
PSRR	Power Supply Rejection Ratio	V_S = ±5V to ±16V	70	60	**50**	dB (Min)

A2 AC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for T_A = 25°C, and Supply Voltage V_S = ±15V. **Boldface** limits apply at temperature extremes. R_S = 50Ω.

Symbol	Parameter	Conditions	Typical	25°C Limit	Units
SR 1 SR 2	Slew Rate 1 Slew Rate 2	V_{IN} = ±11V, R_L = 1 kΩ V_{IN} = ±11V, R_L = 50Ω (Note 7)	1200 750	 550	V/μs (Min)
BW	−3 dB Bandwidth	V_{IN} = ±100 mVpp R_L = 50Ω, C_L ≤ 10 pF	65	30	MHz (Min)
t_r, t_f	Rise Time Fall Time	R_L = 1 kΩ, C_L ≤ 10 pF V_O = 100 mVpp	8		ns
P_D	Propagation Delay	R_L = 50Ω, C_L ≤ 10 pF V_O = 100 mVpp	4		ns
	Overshoot	R_L = 1 kΩ, C_L = 100 pF R_L = 50Ω, C_L = 1000 pF	13 21		%

Additional (A2) Electrical Characteristics

Unless otherwise specified, all limits guaranteed for T_A = 25°C, and Supply Voltage V_S = ±15V. **Boldface** limits apply at temperature extremes.

Symbol	Parameter	Conditions	Typical	25°C Limit	0°C to 70°C Limit	Units
V_{OL}	Flag Pin Output Low Voltage	I_{SINK} Flag Pin = 500 μA	220	340	**400**	mV (Max)
I_{OH}	Flag Pin Output High Current	V_{OH} Flag Pin = 15V (Note 8)	0.01	10	**20**	μA (Max)

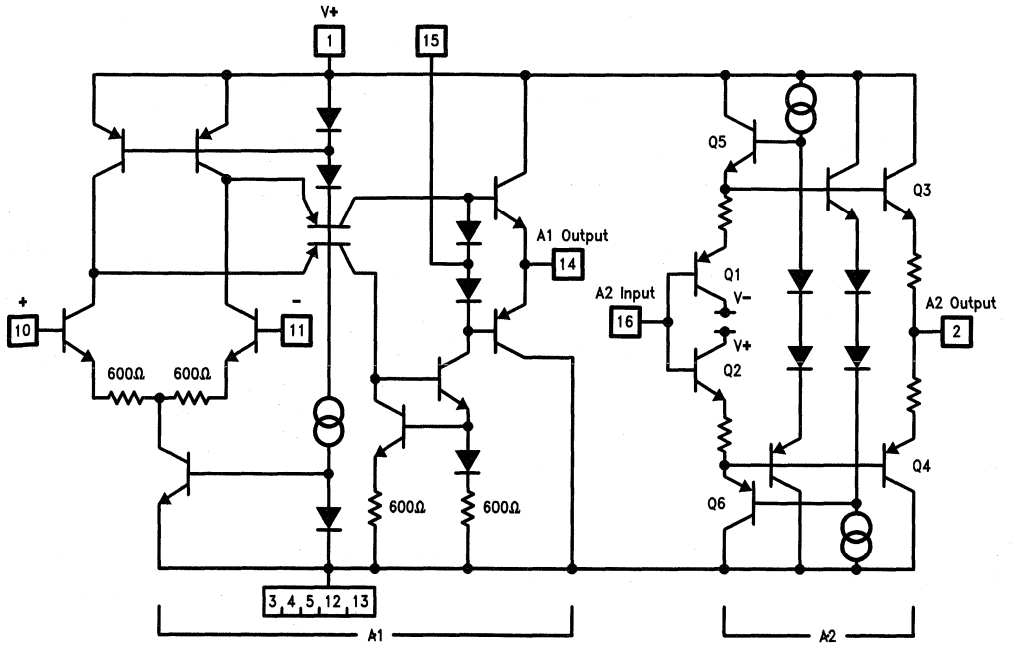
Note 5: For operation at elevated temperature, these devices must be derated to insure $T_J \leq 125°C$. $T_J = T_A + (P_D \times \theta_{JA})$. θ_{JA} for the N package mounted flush to the PCB, is 40°C/W when pins 4, 5, 12 and 13 are soldered to a total of 2 in^2 of copper trace.

Note 6: Measured between ±5V.

Note 7: V_{IN} = ±9V step input, measured between ±5V out.

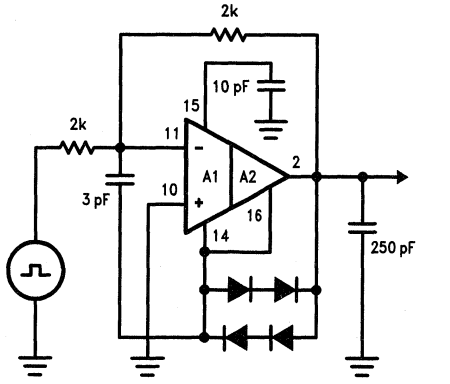
Note 8: The error flag is set during current limit or thermal shut-down. The flag is an open collector, low on fault.

Simplified Schematic



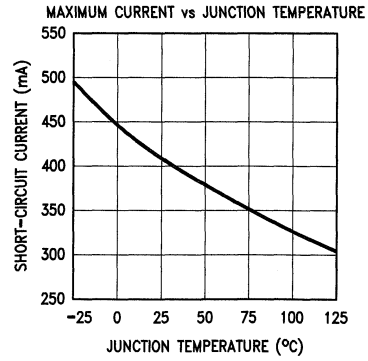
TL/H/10521–4

Settling Time Test Circuit



TL/H/10521–5

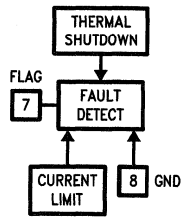
FIGURE 2



TL/H/10521–6

FIGURE 3

Protection Circuit Block Diagram

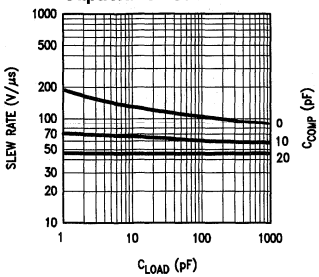


TL/H/10521–7

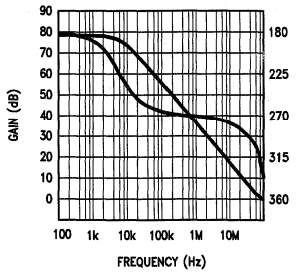
Typical Performance Characteristics Op Amp

(Unless otherwise specified, T_A = 25°C, V_S = ±15V, and R_L = 10 kΩ.)

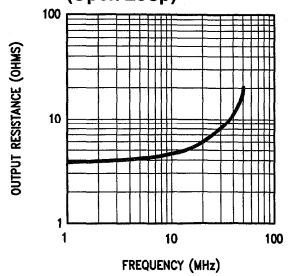
Slew Rate vs Capacitive Load



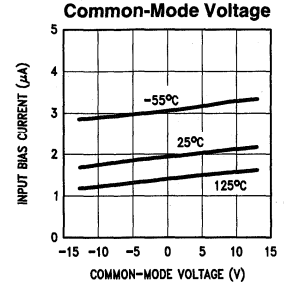
Bode Plot



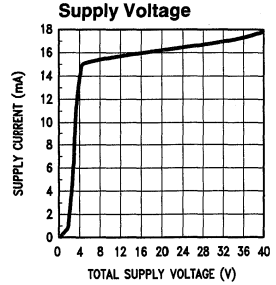
Output Resistance (Open Loop)



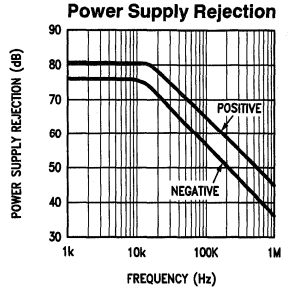
Bias Current vs Common-Mode Voltage



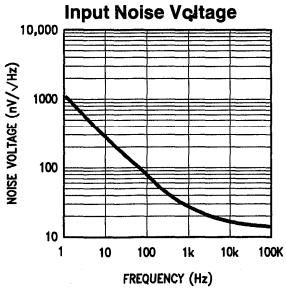
Supply Current vs Supply Voltage



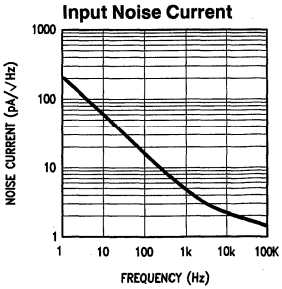
Power Supply Rejection



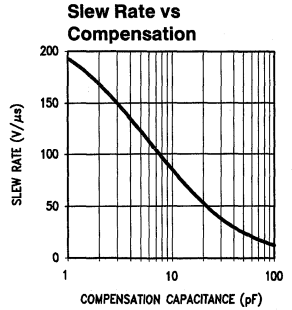
Input Noise Voltage



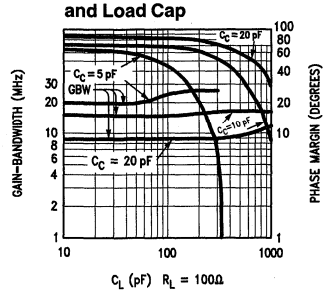
Input Noise Current



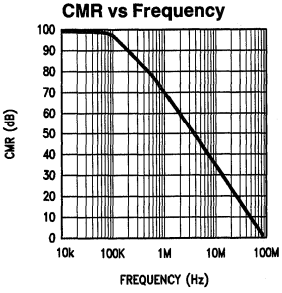
Slew Rate vs Compensation



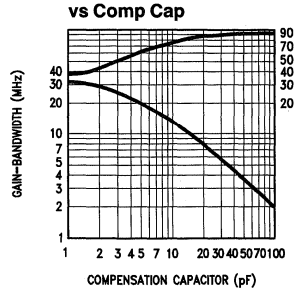
Gain-Bandwidth, Phase Margin vs Comp Cap and Load Cap



CMR vs Frequency



GBW and Phase Margin vs Comp Cap

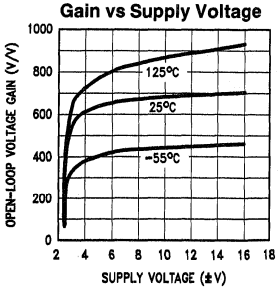


TL/H/10521–8

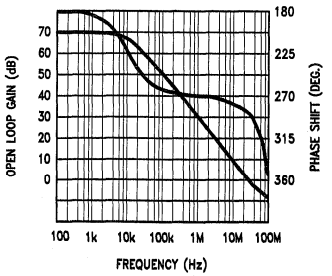
Typical Performance Characteristics A1 Only

(Unless otherwise specified, T_A = 25°C, V_S = ±15V, and R_L = 10 kΩ.)

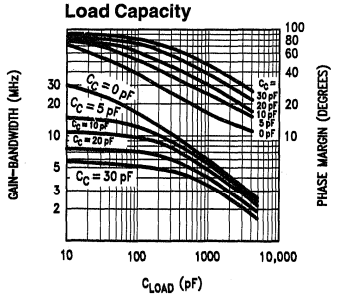
Gain vs Supply Voltage



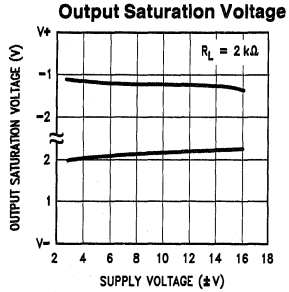
Bode Plot



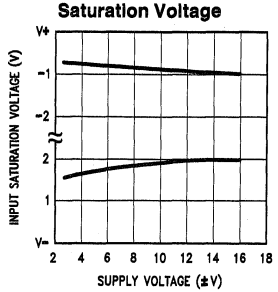
Gain-Bandwidth and Phase Margin vs Load Capacity



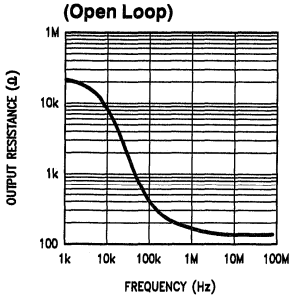
Output Saturation Voltage



Common-Mode Input Saturation Voltage



Output Resistance (Open Loop)

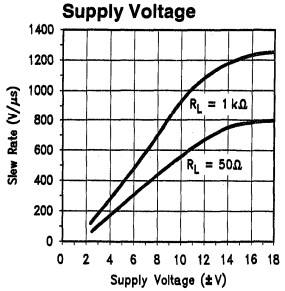


TL/H/10521–9

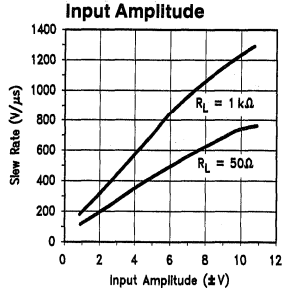
Typical Performance Characteristics A2 Only

(Unless otherwise specified, T_A = 25°C and V_S = ±15V.)

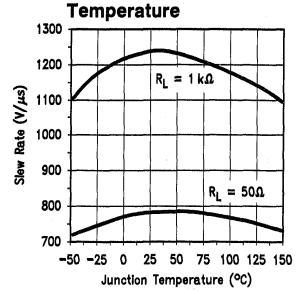
Slew Rate vs Supply Voltage



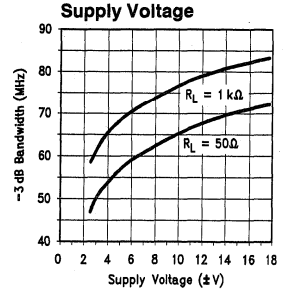
Slew Rate vs Input Amplitude



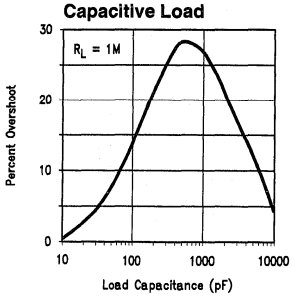
Slew Rate vs Temperature



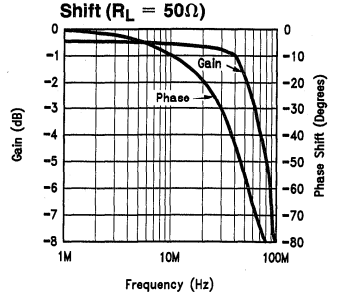
Bandwidth vs Supply Voltage



Overshoot vs Capacitive Load



Gain and Phase Shift (R_L = 50Ω)



TL/H/10521–10

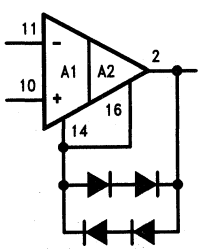
Application Hints

The LM6313 is a high-speed, high power operational amplifier that is designed for driving low-impedance loads such as 50Ω and 75Ω cables. Available in the standard, low cost, 16-pin DIP, this amplifier will drive back terminated video cables with up to 10 Vp-p. The ability to add additional compensation allows the LM6313 to drive capacitive loads of any size at bandwidths previously possible only with very expensive hybrid devices.

The LM6313 is excellent for driving high-speed flash A-to-D converters that require low-impedance drive at high frequencies. At 1 MHz, when used as a buffer, the LM6313 output impedance is below 0.1Ω. This very low output impedance also means that cables can be accurately back-terminated by just placing the characteristic impedance in series with the LM6313 output.

OVER-VOLTAGE PROTECTION

If the LM6313 is being operated on supply voltages of greater than ±5V, the possibility of damaging the output stage transistors exists. At higher supply voltages, if the output is shorted or excessive power dissipation causes the output stage to shut down, the maximum A2 input-to-output voltage, can be exceeded. This occurs when the input stage tries to drive the output while the output is at ground. To prevent this from happening, an easy solution is to place diodes around the output stage (See *Figure 4*). This will limit the maximum differential voltage to about 1.3V. Any signal diode, such as the 1N914 or the 1N4148 will work fine.



TL/H/10521–11

FIGURE 4

HEAT SINKING

When driving a low impedance load such as 50Ω, and operating from ±15V supplies, the internal power dissipation of the LM6313 can rise above 3W. To prevent overheating of the chip, which would cause the thermal protection circuitry to shut the system down, the following guidelines should be followed:

1. Reduce the supply voltage. The LM6313 will operate with little change in performance, except output voltage swing, on ±5V supplies. This will reduce the dissipation to the level where no precautions against overheating are necessary for loads of 10Ω or more.
2. Solder pins 4, 5, 12 and 13 to copper traces which are at least 0.100 inch wide and have a total area of at least 2 square inches, to obtain a θ_{JA} of 40°C/W. These four pins are connected to the back of the chip and will be at V−. They should not be used as a V− connection unless pin 3 is also connected to this same point.

SUPPLY BYPASSING

Because of the large currents required to drive low-impedance loads, supply bypassing as close as possible to the I.C. is important. At 50 MHz, a few inches of wire or circuit trace can have 20Ω or 30Ω of inductive reactance. This inductance in series with a 0.1 μF bypass capacitor can resonate at 1 MHz to 2 MHz and just appear as an inductor at higher frequencies. A 0.1 μF and a 10μF to 15 μF capacitor connected in parallel and as close as possible to the LM6313 supply pins, from each supply to ground, will give best performance.

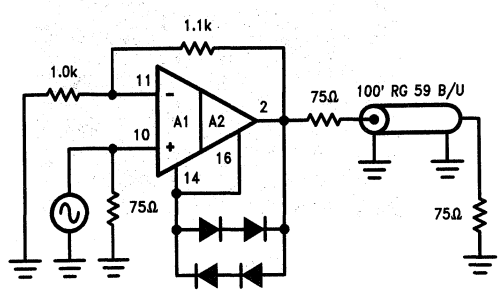
SELECTION OF COMPENSATION CAPACITOR

The compensation pin, pin 15, makes it possible to drive any load at any closed loop gain without stability problems. In most cases, where the gain is −1 or greater and the load is resistive, no compensation capacitor is required. When used at unity gain or when driving reactive loads, a small capacitor of 5 pF to 20 pF will insure optimum performance. The easiest way to determine the best value of compensation capacitor is to temporarily connect a trimmer capacitor (typical range of 2 pF to 15 pF) between pin 15, and ground, and adjust it for little or no overshoot at the output while driving the input with a square wave.

If the actual load capacitance is known, the typical graphs "Gain-Bandwidth and Phase Margin vs. Load Capacitance" can be used to select a value.

VIDEO CABLE DRIVER

The LM6313 is ideally suited for driving 50Ω or 75Ω cables. Unlike a buffer that requires a separate gain stage to make up for the losses involved in termination, the LM6313 gain can be set to 1 plus the line losses when the transmission line is end-terminated. If back-termination is needed, adding the line impedance in series with the output and raising the gain to 2 plus the expected line losses will provide a 0 dB loss system. *Figure 5* illustrates the back and end terminated video system including compensation for line losses. The excellent stability of the LM6313 with changes in supply voltages allow running the amplifier on unregulated supplies. The typical change in phase shift when the supplies are changed from ±5V to ±15V is less than 3° at 10 MHz.



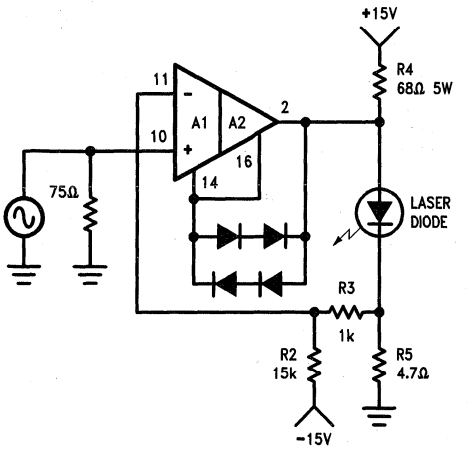
TL/H/10521–12

FIGURE 5

Application Hints (Continued)

LASER DIODE MODULATOR

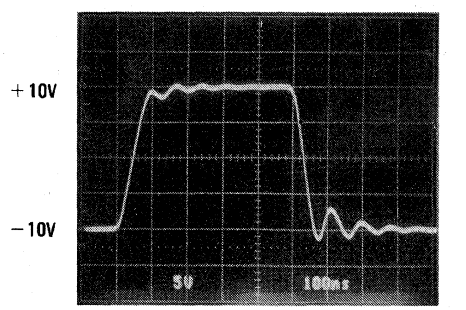
Figure 6 is a minimum component count example of a video modulator for a CW laser diode. This example biases the diode at 200 mA and modulates the current at ±200 mA per volt of signal. If it is desired to reduce power consumption and ±5V supplies are available, all that is necessary is to change R2 to 5 kΩ and R4 to 15Ω.



TL/H/10521–13

FIGURE 6

In photo 1, C_L is 1000 pF. The LM6313 is slewing at 250 V/μs, from −5V to +5V. The slew rate is 450 V/μs from +5V to −5V. This requires the op amp to deliver 450 mA into the load and remain stable.

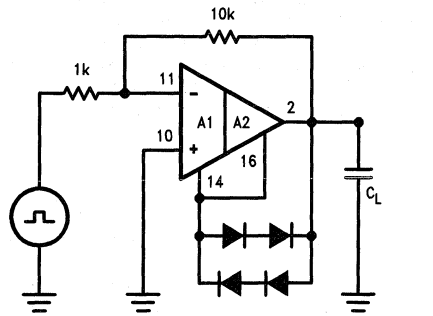


TL/H/10521–16

Photo 1

CAPACITIVE LOAD DRIVING

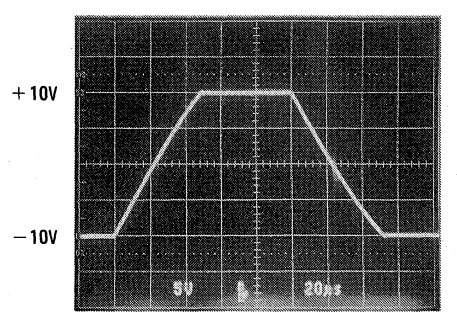
Figure 7 is the circuit used to demonstrate the ability of the LM6313 to drive capacitive loads at speeds not previously possible with monolithic op amps.



TL/H/10521–14

FIGURE 7

In photo 2, C_L is changed to 1 μF. Under these conditions, the op amp is forced into current limiting. Here the current is internally limited to about ±400 mA. Note the rapid and complete recovery to normal operation at the end of slewing.



TL/H/10521–15

Photo 2

National Semiconductor

LM13080
Programmable Power Operational Amplifier

General Description

The LM13080 is an internally compensated medium power operational amplifier designed for use in those applications requiring load currents of several hundred milliamperes. This amplifier has the added advantage of having an input stage programmed with an external resistor. The user is able to optimize the amplifier performance for each individual application with this feature. Applications include servo amplifiers and drivers, high input impedance audio amplifiers, DC-to-DC converters, precision power comparators which can either sink or source current and motor speed controls.

The LM13080 may be powered from either single or dual power supplies, and will operate from as little as 3V.

As a power operational amplifier, the LM13080 is capable of delivering 0.25A to a load. This feature allows the system designer to fulfill his medium power circuit requirements without having to add external current boost transistors to the output of a standard operational amplifier.

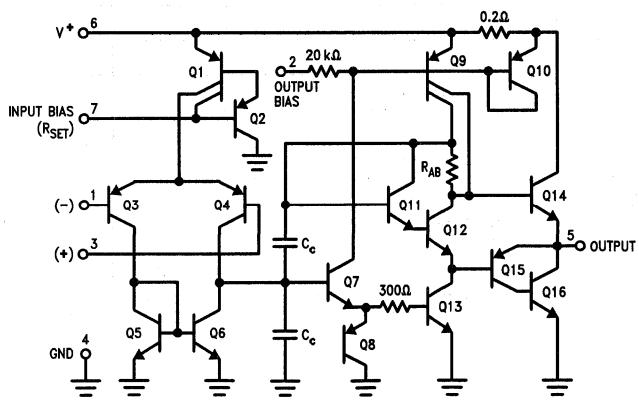
By selecting the proper input stage bias resistor it is possible to tailor the performance of the input stage to meet the needs of any particular system. Trade-offs between input offset voltage, input bias current and gain bandwidth are easily made.

An unusual feature of the LM13080 is an electronic shut-down capability.

Features

- High output current—250 mA
- Externally programmable input stage
- Low power supply operation—3V
- Electronic shut-down capability
- Internally compensated for unity gain
- Low input bias current

Schematic Diagram



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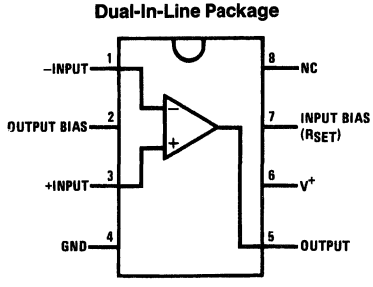
Connection Diagram

Dual-In-Line Package



TOP VIEW

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Order Number LM13080N
See NS Package Number N08E

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage Operation Range	3V to 15V ±1.5V to ±7.5V
Power Dissipation (Note 1)	1250 mW
Differential Input Voltage (Note 2)	15V
Input Voltage Range (Note 3)	−0.3V to +15V
Input Current ($V_{IN} \leq -0.3V$) (Note 4)	20 mA
Operating Temperature Range	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec.)	300°C

ESD rating to be determined.

Electrical Characteristics $V_S = 12V$, $R_{SET} = 680k$, $0°C \leq T_A \leq 70°C$, unless otherwise specified

Parameter	Conditions	Min	Typ	Max	Units
Input Offset Voltage	$T_A = 25°C$ (Note 5)		±3	±7	mV
Input Bias Current	$I_{IN(+)}$ or $I_{IN(-)}$, $T_A = 25°C$		100	400	nA
Input Offset Current	$I_{IN(+)} - I_{IN(-)}$, $T_A = 25°C$		±30	±75	nA
Supply Current	$R_L = \infty$, $T_A = 25°C$ (Note 6)		3	6	mA
Output Voltage Swing	$V_S = \pm 6V$, $T_A = 25°C$ (Note 1)				
V_{OH}	$R_L = 50\Omega$	4.5	5		V
	$R_L = 8\Omega$	2			V
V_{OL}	$R_L = 50\Omega$		−5	−4.5	V
	$R_L = 8\Omega$			−2	V
Large Signal Voltage Gain	$V_S = \pm 6V$, $R_L = 50\Omega$, $f = 100$ Hz, $T_A = 25°C$	3	10		V/mV
Input Common-Mode Voltage Range	$V_S \leq 15V$, $T_A = 25°C$ (Note 3)	1		$V_S - 1.5$	V
Input Offset Voltage	(Note 5)			±10	mV
Input Offset Voltage Drift			5		μV/°C
Input Bias Current	$I_{IN(+)}$ or $I_{IN(-)}$			600	nA
Input Offset Current	$I_{IN(+)} - I_{IN(-)}$			±150	nA
Input Offset Current Drift			50		pA/°C
Supply Current	$R_L = \infty$ (Note 6)			8	mA
Output Voltage Swing	$V_S = \pm 6V$ (Note 1)				
V_{OH}	$R_L = 50\Omega$			4	V
	$R_L = 8\Omega$			1.6	V
V_{OL}	$R_L = 50\Omega$	−4			V
	$R_L = 8\Omega$	−1.6			V

Electrical Characteristics V_S = 12V, R_{SET} = 680k, 0°C ≤ T_A ≤ 70°C, unless otherwise specified (Continued)

Parameter	Conditions	Min	Typ	Max	Units
Large Signal Voltage Gain	V_S = ±6V, R_L = 50Ω, f = 100 Hz	1			V/mV
Input Common-Mode Voltage Range	V_S ≤ 15V (Note 3)	1.25		V_S − 1.75	V
Common-Mode Rejection Ratio	T_A = 25°C	63	85		dB
Total Harmonic Distortion	R_L = 8Ω, V_O = 2 Vrms, f = 1 kHz, T_A = 25°C		0.5	5	%

Note 1: For operation at high temperatures, the LM13080 must be derated based upon a maximum junction temperature of 150°C and a thermal resistance of 100°C/W. The thermal resistance values given are for a still air ambient with the package soldered into a printed circuit board.

Note 2: Differential input voltages up to the magnitude of the power supply voltage will not damage the input circuitry. However, input voltages outside the input common-mode voltage range will not be able to properly control the output of the amplifier.

Note 3: The input voltage applied to either input should not be allowed to go more than 0.3V below the potential applied to pin 4; however, either input can be taken as high as 15V without causing damage to the circuit. Input voltages below the minimum common-mode voltage range may cause a phase reversal in the output.

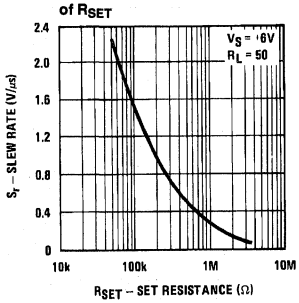
Note 4: This input current will exist only when the voltage at either input lead is driven negative. It is due to the base-isolation junction of the PNP transistor tub becoming forward biased and thereby acting as an input diode clamp. In addition to this diode action, there is also lateral NPN parasitic action on the IC chip. This transistor action can cause the output to take an undefined state for the time duration that an input is driven negative.

Note 5: V_O = 6V, R_S = 0Ω, and over the full input common-mode voltage range.

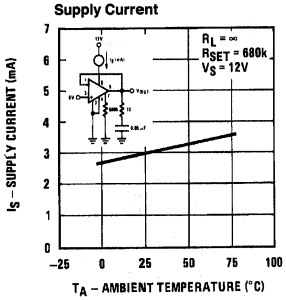
Note 6: Supply current is measured with the amplifier connected in a unity gain follower configuration and the positive input set to one-half of the supply voltage.

Typical Performance Characteristics

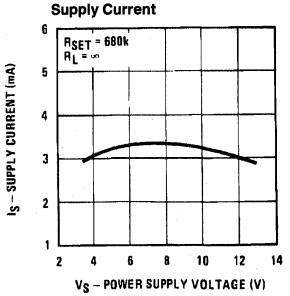
Slew Rate as Function of R_{SET}



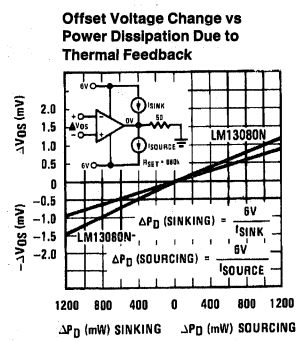
Supply Current



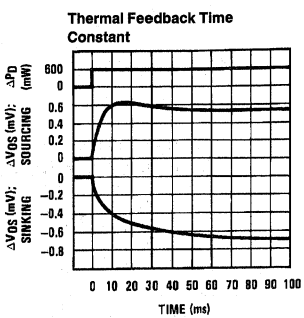
Supply Current



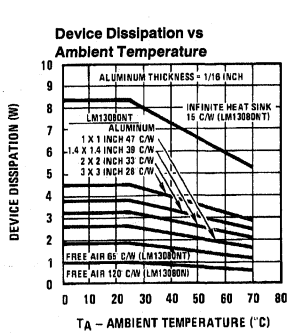
Offset Voltage Change vs Power Dissipation Due to Thermal Feedback



Thermal Feedback Time Constant



Device Dissipation vs Ambient Temperature



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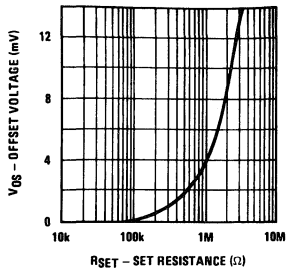
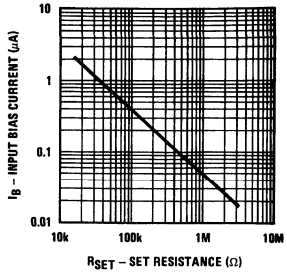
Typical Performance Characteristics (Continued)

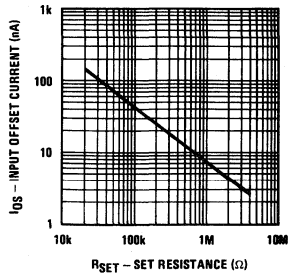
Offset Voltage



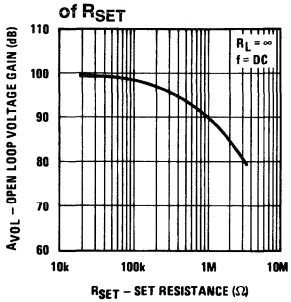
Input Bias Current



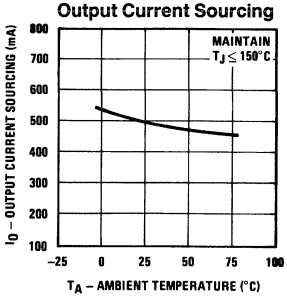
Offset Current



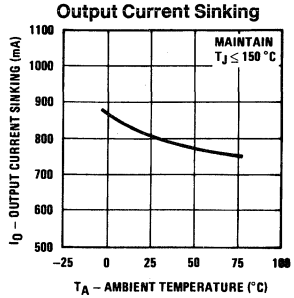
Voltage Gain as a Function of R_{SET}



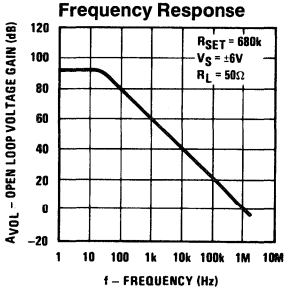
Output Current Sourcing



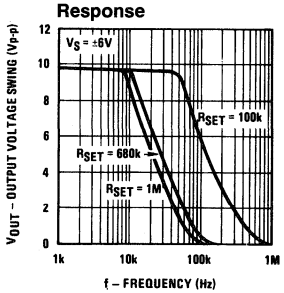
Output Current Sinking



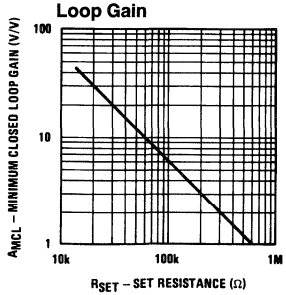
Small Signal Open Loop Frequency Response



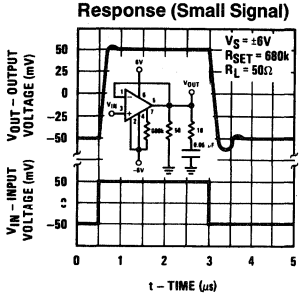
Large Signal Frequency Response



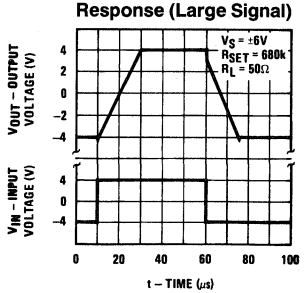
Minimum Stable Closed Loop Gain



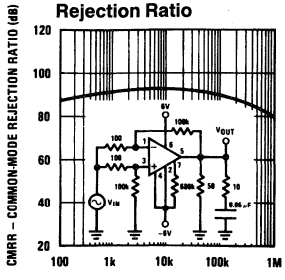
Voltage Follower Pulse Response (Small Signal)



Voltage Follower Pulse Response (Large Signal)



Common-Mode Rejection Ratio



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Application Hints

The LM13080 is a power op amp capable of sourcing or sinking more than 250 mA and does not include internal current limit or thermal shut-down. Therefore, the user must make sure that his application will not cause the power dissipation rating of the package to be exceeded. The LM13080 is rated at a maximum dissipation of 1250 mW at 25°C. For operation at temperatures above 25°C, the maximum dissipation must be derated using the equation:

$$P_D = \frac{T_J - T_A}{\Theta_{JA}}$$

where P_D is the maximum allowable power dissipation, T_J is the maximum junction temperature (150°C), T_A is the ambient temperature and Θ_{JA} is the thermal resistance of the package operated in a still air environment. Θ_{JA} for the LM13080N is 100°C/W. For example, if the LM13080N is used in free air in a 70°C ambient, the maximum power that can be dissipated is:

$$P_D = \frac{150°C - 70°C}{100°C/W} = 800\ mW$$

The LM13080 derives its ability to sink current through the use of a composite NPN/PNP output configuration. This local loop must be compensated by the series connection of a 0.05 μF capacitor and a 10Ω resistor between the output of the op amp (pin 5) and the negative power supply (pin 4). The RC does not just filter out the oscillation from the output waveform but actually stabilizes the loop.

If the inputs of the LM13080 are driven below the input common-mode voltage range, it is possible that the output will experience a phase reversal. This is particularly true for the non-inverting input ($V_{IN(+)}$). If either input is driven to a voltage level 0.3V below the substrate (pin 4) a parasitic NPN transistor will be turned ON. The emitter of this parasitic transistor is the normal input transistor epi (N-type, base) region, the base is the substrate (P-type) and the collector is every other epi region on the die. Circuit operation in this mode is unpredictable. If an input is forced below the substrate, the current flowing out of that input should be limited to 20 mA to insure that the amplifier will not be destroyed.

Programming the LM13080 is accomplished by selecting the value of R_{SET}, the input stage bias resistor, to optimize the amplifier for each particular application. An example would be an application with low source resistance which requires a low offset voltage to make a precise DC measurement. By selecting an R_{SET} of 100 kΩ, the normal offset voltage would be reduced to approximately one-fourth the value it would be if a 680k resistor was used. By studying the curves, it can be seen that the bias current will increase but an increase here has very little effect due to the small source impedance. It should also be noted that with a 100k input set resistor the gain bandwidth product will also increase, and in fact, the amplifier must be operated with a closed loop voltage gain of 6 to assure stability.

The effect of R_{SET} on the total quiescent supply current will be very small ($\Delta I_S < 5\%\ I_S$) as long as R_{SET} is 100k or greater.

To employ electronic shut-down the output bias pin, pin 2, and the negative end of the input bias resistor, R_{SET}, are connected to the negative power supply (or ground in a single power system) through a saturated NPN transistor (or other electronic switch). When the transistor is turned OFF, all of the bias currents inside the op amp are turned OFF and all input and output terminals will float. When first turned ON, the output will take about 5 μs to reach the correct level. To insure that the LM13080 is OFF, leakage in the control device must be below the level that will allow pins 2 and 7 to fall to 0.4V below V^+.

Power supply rejection is a function of the change in voltage across the input bias resistor, R_{SET}. To improve the PSRR of the LM13080, the user must be careful to bypass pin 7 to pin 6 or to establish a floating voltage referenced to the positive power supply to serve as a connection point for R_{SET}. In applications where PSRR is important, it is imperative that a supply bypass capacitor(s) be used.

Typical Applications

LINE DRIVER

The line driver circuit in *Figure 1* is able to accept an unbalanced, high impedance input and convert it to a balanced output suitable for driving a low impedance line. This is particularly useful in an environment where magnetically induced hum or noise pickup is a problem.

The outputs of the 2 LM13080s are of opposite polarity; therefore, terminating the line with a balanced load (i.e., a differential amplifier or a transformer) will cause common-mode interference pickup to be cancelled.

This circuit will drive a 20 Vp-p signal into a 50Ω load for frequencies up to 10 kHz. Above 10 kHz the output signal is slew rate limited, but the line driver will still supply a 13 Vp-p signal at 20 kHz. The voltage gain of the network is 2, and the low frequency roll-off is determined by:

$$f_L = \frac{1}{2\pi RC}$$

It can be seen that if the load is connected directly between the outputs of the amplifiers, the line driver becomes a simple bridge amplifier capable of delivering 2W into a 16Ω load.

PIEZOELECTRIC ALARM

The piezoelectric alarm shown in *Figure 2* uses a 3-terminal transducer (Gulton 101FB or equivalent) to produce an 80 dB SPL alarm.

The transducer has a feedback terminal which is connected to the non-inverting input of the LM13080, causing oscillation at the resonant frequency of the piezoelectric crystal. The alarm can be controlled through the use of the electronic shut-down feature of the amplifier. The 100k resistor and 0.1 μF capacitor are used to provide a reference voltage at the inverting input and to keep the duty cycle of the crystal oscillation close to 50%. The RC time constant of this feedback network should be much greater than the time constant of the transducer.

Typical Applications (Continued)

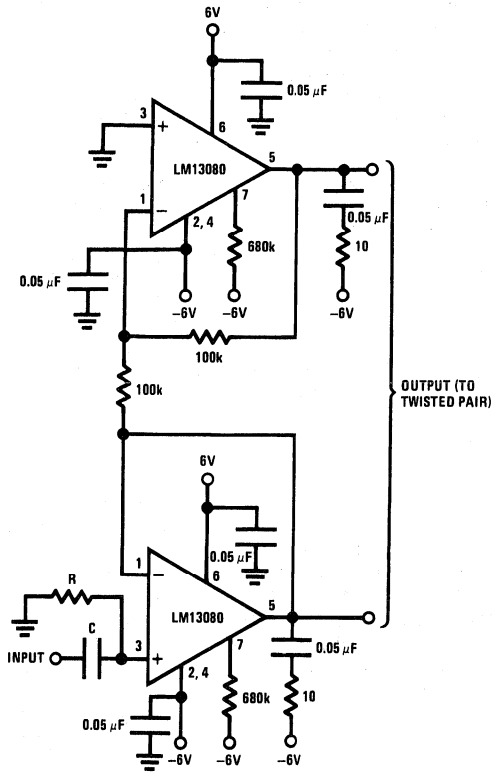

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FIGURE 1. Line Driver—Unbalanced Input to Balanced Output

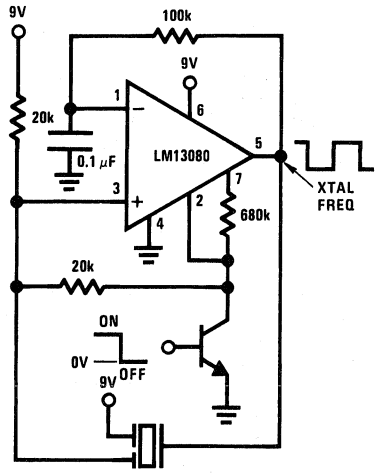

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FIGURE 2. Piezoelectric Alarm

SIRENS

Two separate circuits for sirens are shown. The first, *Figure 3*, is a 2-state or ON-OFF type siren where the LM13080 oscillates at an audio frequency and drives an 8Ω speaker and the LM339 acts as a switch which controls the audio burst rate. The second siren, *Figure 4*, provides a constant audio output but alternates between 2 separate tones. The LM13080 is set to oscillate at one basic frequency and this frequency is changed by adding a 200 kΩ charging resistor in parallel with the feedback resistor, R2.

LAMP FLASHER—RELAY DRIVER

The LM13080 is easily adaptable to such applications as low frequency warning devices. The output of the oscillator is a squarewave that is used to drive lamps or small relays. As shown in *Figure 5*, the circuit alternately flashes 2 incandescent lamps.

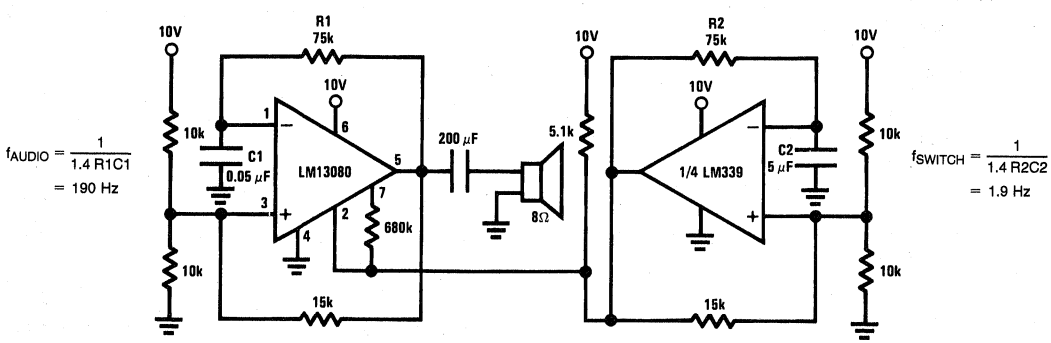

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FIGURE 3. 2-State Siren

Typical Applications (Continued)

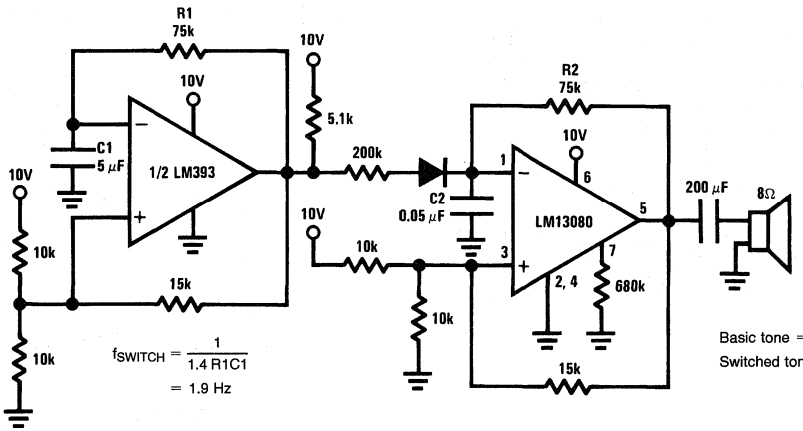

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FIGURE 4. 2-Tone Siren

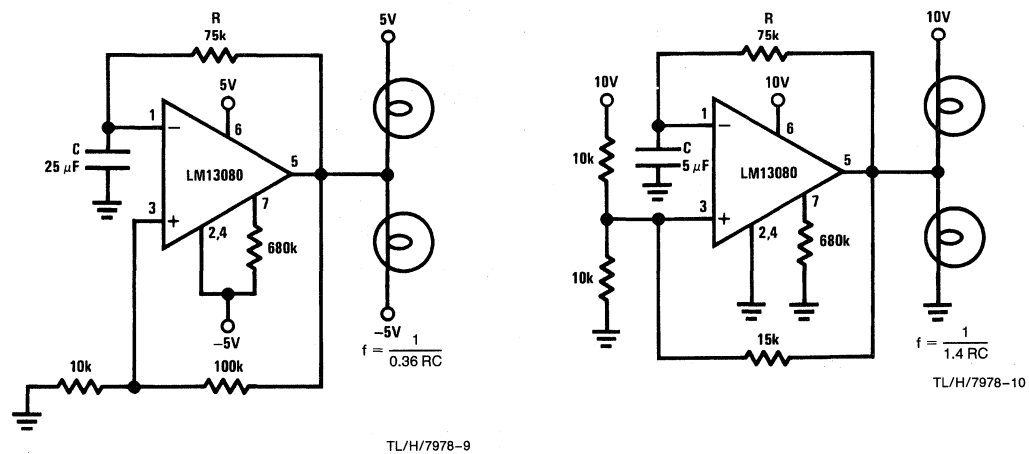


FIGURE 5. Low Frequency Lamp Flasher/Relay Driver

MOTOR SPEED CONTROL

The LM13080 can be used to construct a very simple speed control for small motors requiring less than 0.5A start current. This circuit operates by impressing the multiple of a reference voltage across the motor, and then varying the reference by means of a quasi-positive feedback to change the voltage across the motor any time the load on the motor changes.

To understand the circuit operation, it is easiest to let the voltage at the cathode of diode D1, *Figure 6*, be the input voltage, V_{IN}, to the system. Diode D1 is actually a level shift diode to bring V_{IN} into the common-mode range of the amplifier. A reference voltage is established by the combined voltage drop through the 10Ω potentiometer, R3 and the reference diode, D2 and is applied to the non-inverting input of the LM13080. Resistor R4 is a bias resistor used to keep D2 active. The 10k speed adjust potentiometer is 2 resistors in 1, where section R1 is the input resistance and section R2 is the negative feedback resistance. It can be seen that the voltage impressed across the motor is equal to:

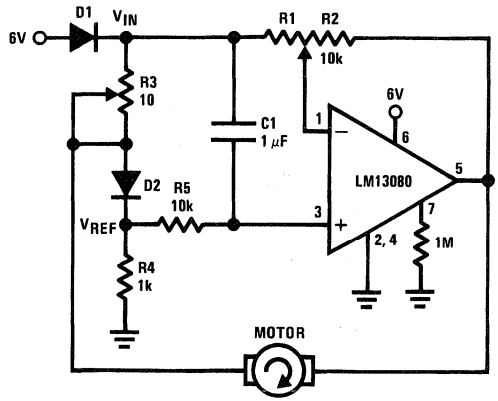
$$V_{MOTOR} = \frac{(V_{BE2} + I_3R3)\ R2}{R1} + V_{BE}$$

Typical Applications (Continued)

The positive feedback is developed as a change in the voltage across R3 due to the change in the motor current caused by a variation in the motor's load. Resistor R3 is shown as a potentiometer so that the amount of positive feedback can be adjusted for smooth operation of the motor. Capacitor C1 and resistor R5 serve as a filter for the reference voltage at the non-inverting input of the amplifier.

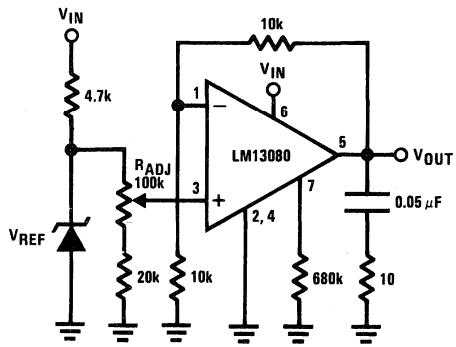
VOLTAGE REGULATORS

In normal, positive or negative regulator application such as those shown in *Figure 7* and *Figure 8*, the LM13080 has 2 major advantages over standard operational amplifiers. The LM13080 has its own on-chip pass device and in addition can either sink or source 250 mA of load current.



TL/H/7978–11

FIGURE 6. Motor Speed Control

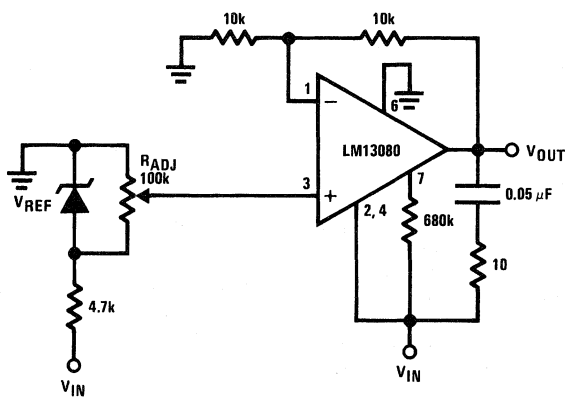


TL/H/7978–12

$2V \leq V_{OUT} \leq (V_{IN} - 2V)$

FIGURE 7. Positive Variable Voltage Regulator

Note: Pin numbers apply to miniDIP.



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$-15V \geq V_{OUT} \geq -(V_{IN} - 2V)$

FIGURE 8. Negative Variable Voltage Regulator

National Semiconductor

LM13600 Dual Operational Transconductance Amplifiers with Linearizing Diodes and Buffers

General Description

The LM13600 series consists of two current controlled transconductance amplifiers each with differential inputs and a push-pull output. The two amplifiers share common supplies but otherwise operate independently. Linearizing diodes are provided at the inputs to reduce distortion and allow higher input levels. The result is a 10 dB signal-to-noise improvement referenced to 0.5 percent THD. Controlled impedance buffers which are especially designed to complement the dynamic range of the amplifiers are provided.

Features

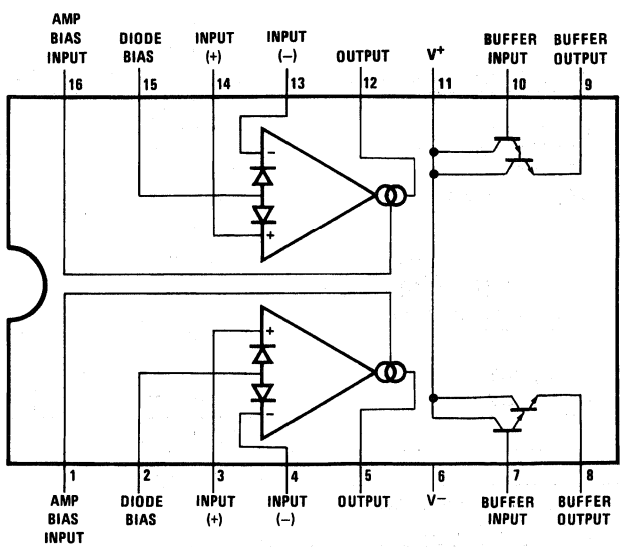
- g_m adjustable over 6 decades
- Excellent g_m linearity
- Excellent matching between amplifiers
- Linearizing diodes
- Controlled impedance buffers
- High output signal-to-noise ratio
- Wide supply range ±2V to ±22V

Applications

- Current-controlled amplifiers
- Current-controlled impedances
- Current-controlled filters
- Current-controlled oscillators
- Multiplexers
- Timers
- Sample and hold circuits

Connection Diagram

Dual-In-Line and Small Outline Packages



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Top View

Order Number LM13600M, LM13600N or LM13600AN
See NS Package Number M16A or N16A

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (Note 1)	
LM13600	36 V_{DC} or ±18V
LM13600A	44 V_{DC} or ±22V
Power Dissipation (Note 2) T_A = 25°C	570 mW
Differential Input Voltage	±5V
Diode Bias Current (I_D)	2 mA
Amplifier Bias Current (I_{ABC})	2 mA
Output Short Circuit Duration	Continuous
Buffer Output Current (Note 3)	20 mA
Operating Temperature Range	0°C to +70°C
DC Input Voltage	$+V_S$ to $-V_S$
Storage Temperature Range	−65°C to +150°C
Soldering Information	
Dual-In-Line Package	
Soldering (10 seconds)	260°C
Small Outline Package	
Vapor Phase (60 seconds)	215°C
Infrared (15 seconds)	220°C

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

Electrical Characteristics (Note 4)

Parameter	Conditions	LM13600			LM13600A			Units
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage (V_{OS})			0.4	4		0.4	1	mV
	Over Specified Temperature Range						2	mV
	I_{ABC} = 5 μA		0.3	4		0.3	1	mV
V_{OS} Including Diodes	Diode Bias Current (I_D) = 500 μA		0.5	5		0.5	2	mV
Input Offset Change	5 μA ≤ I_{ABC} ≤ 500 μA		0.1	3		0.1	1	mV
Input Offset Current			0.1	0.6		0.1	0.6	μA
Input Bias Current			0.4	5		0.4	5	μA
	Over Specified Temperature Range		1	8		1	7	μA
Forward Transconductance (g_m)		6700	9600	13000	7700	9600	12000	μmho
	Over Specified Temperature Range	5400			4000			μmho
g_m Tracking			0.3			0.3		dB
Peak Output Current	R_L = 0, I_{ABC} = 5 μA		5		3	5	7	μA
	R_L = 0, I_{ABC} = 500 μA	350	500	650	350	500	650	μA
	R_L = 0, Over Specified Temp Range	300			300			μA
Peak Output Voltage								
Positive	R_L = ∞, 5 μA ≤ I_{ABC} ≤ 500 μA	+12	+14.2		+12	+14.2		V
Negative	R_L = ∞, 5 μA ≤ I_{ABC} ≤ 500 μA	−12	−14.4		−12	−14.4		V
Supply Current	I_{ABC} = 500 μA, Both Channels		2.6			2.6		mA
V_{OS} Sensitivity								
Positive	$\Delta V_{OS}/\Delta V+$		20	150		20	150	μV/V
Negative	$\Delta V_{OS}/\Delta V-$		20	150		20	150	μV/V
CMRR		80	110		80	110		dB
Common Mode Range		±12	±13.5		±12	±13.5		V
Crosstalk	Referred to Input (Note 5) 20 Hz < f < 20 kHz		100			100		dB
Differential Input Current	I_{ABC} = 0, Input = ±4V		0.02	100		0.02	10	nA
Leakage Current	I_{ABC} = 0 (Refer to Test Circuit)		0.2	100		0.2	5	nA

Electrical Characteristics (Note 4) (Continued)

Parameter	Conditions	LM13600			LM13600A			Units
		Min	Typ	Max	Min	Typ	Max	
Input Resistance		10	26		10	26		kΩ
Open Loop Bandwidth			2			2		MHz
Slew Rate	Unity Gain Compensated		50			50		V/μs
Buffer Input Current	(Note 5), Except I_{ABC} = 0 μA		0.2	0.4		0.2	0.4	μA
Peak Buffer Output Voltage	(Note 5)	10			10			V

Note 1: For selections to a supply voltage above ±22V, contact factory.

Note 2: For operating at high temperatures, the device must be derated based on a 150°C maximum junction temperature and a thermal resistance of 175°C/W which applies for the device soldered in a printed circuit board, operating in still air.

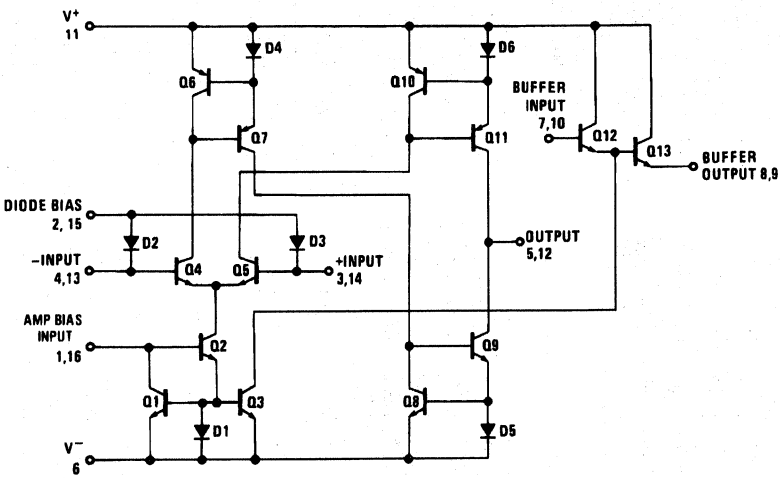
Note 3: Buffer output current should be limited so as to not exceed package dissipation.

Note 4: These specifications apply for V_S = ±15V, T_A = 25°C, amplifier bias current (I_{ABC}) = 500 μA, pins 2 and 15 open unless otherwise specified. The inputs to the buffers are grounded and outputs are open.

Note 5: These specifications apply for V_S = ±15V, I_{ABC} = 500 μA, R_{OUT} = 5 kΩ connected from the buffer output to $-V_S$ and the input of the buffer is connected to the transconductance amplifier output.

Schematic Diagram

One Operational Transconductance Amplifier



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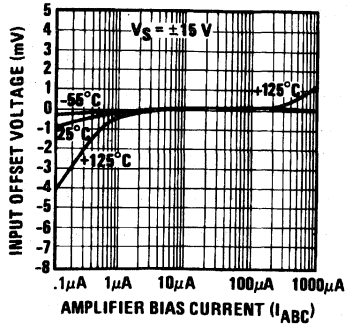
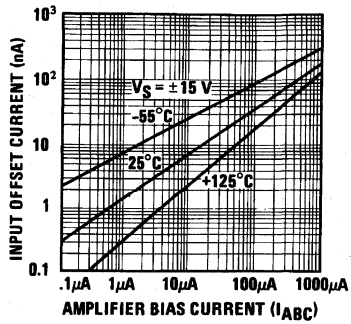
Typical Performance Characteristics

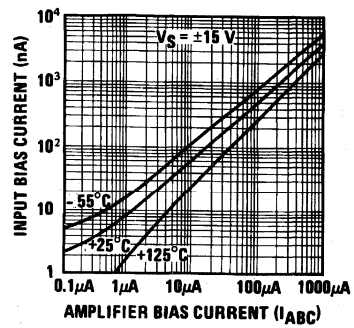
Input Offset Voltage



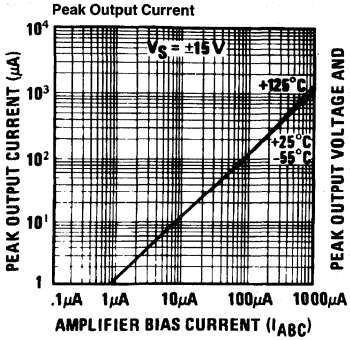
Input Offset Current



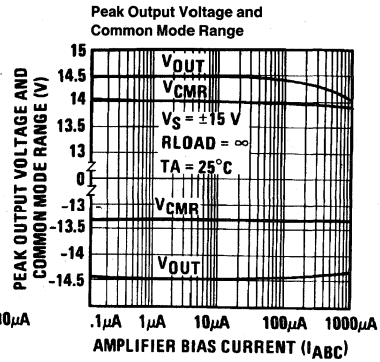
Input Bias Current



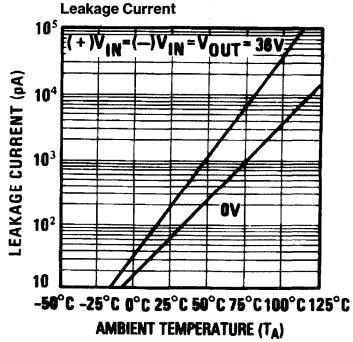
Peak Output Current



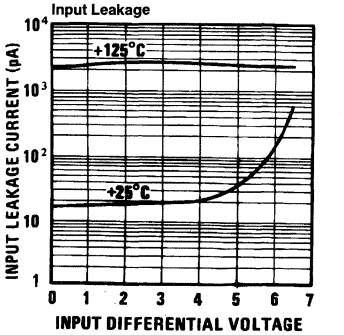
Peak Output Voltage and Common Mode Range



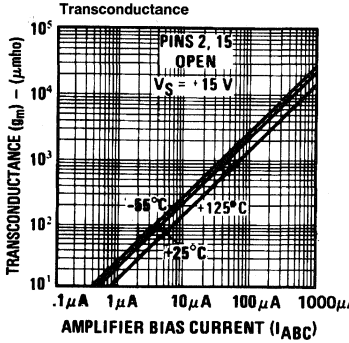
Leakage Current



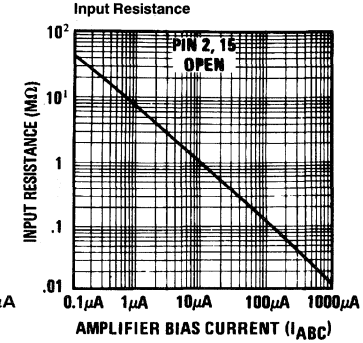
Input Leakage



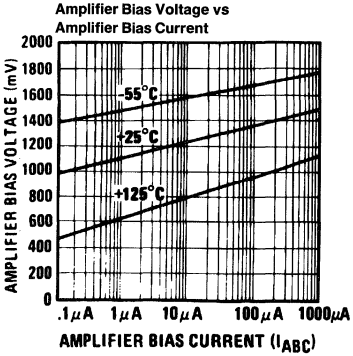
Transconductance



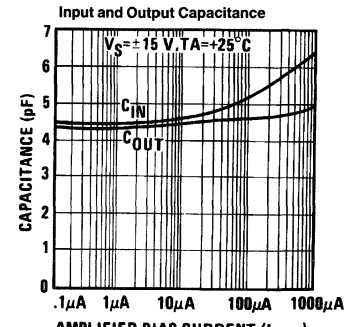
Input Resistance



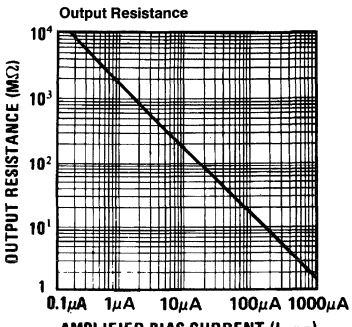
Amplifier Bias Voltage vs Amplifier Bias Current



Input and Output Capacitance



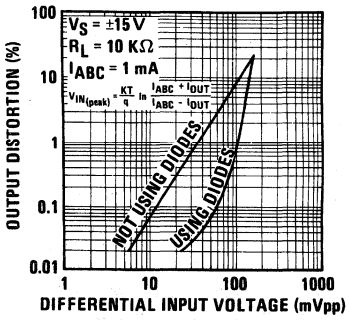
Output Resistance



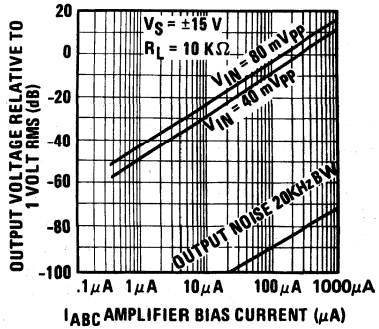
TL/H/7980–3

Typical Performance Characteristics (Continued)

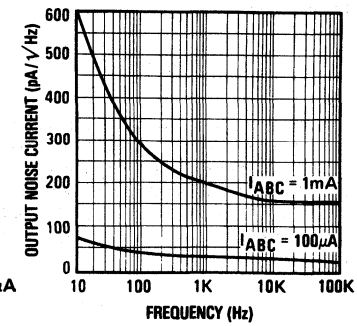
Distortion vs Differential Input Voltage



Voltage vs Amplifier Bias Current

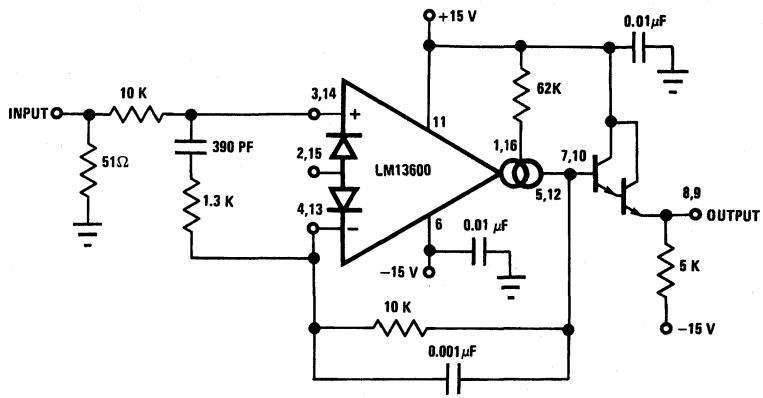


Output Noise vs Frequency



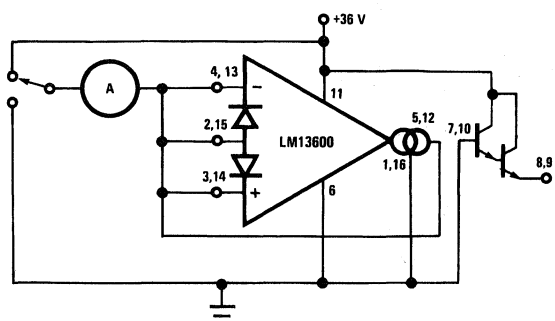
TL/H/7980–4

Unity Gain Follower

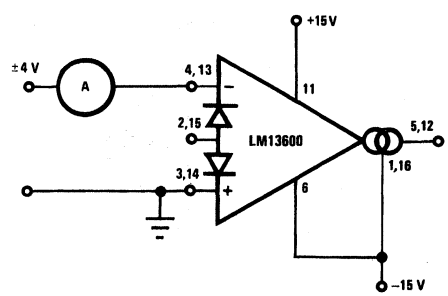


TL/H/7980–5

Leakage Current Test Circuit



Differential Input Current Test Circuit



TL/H/7980–7

TL/H/7980–6

Circuit Description

The differential transistor pair Q_4 and Q_5 form a transconductance stage in that the ratio of their collector currents is defined by the differential input voltage according to the transfer function:

$$V_{IN} = \frac{kT}{q} \ln \frac{I_5}{I_4} \quad (1)$$

where V_{IN} is the differential input voltage, kT/q is approximately 26 mV at 25°C and I_5 and I_4 are the collector currents of transistors Q_5 and Q_4 respectively. With the exception of Q_3 and Q_{13}, all transistors and diodes are identical in size. Transistors Q_1 and Q_2 with Diode D_1 form a current mirror which forces the sum of currents I_4 and I_5 to equal I_{ABC};

$$I_4 + I_5 = I_{ABC} \quad (2)$$

where I_{ABC} is the amplifier bias current applied to the gain pin.

For small differential input voltages the ratio of I_4 and I_5 approaches unity and the Taylor series of the ln function can be approximated as:

$$\frac{kT}{q} \ln \frac{I_5}{I_4} \approx \frac{kT}{q} \frac{I_5 - I_4}{I_4} \quad (3)$$

$$I_4 \approx I_5 \approx \frac{I_{ABC}}{2}$$

$$V_{IN} \left[\frac{I_{ABC}\, q}{2kT} \right] = I_5 - I_4 \quad (4)$$

Collector currents I_4 and I_5 are not very useful by themselves and it is necessary to subtract one current from the other. The remaining transistors and diodes form three current mirrors that produce an output current equal to I_5 minus I_4 thus:

$$V_{IN} \left[\frac{I_{ABC}\, q}{2kT} \right] = I_{OUT} \quad (5)$$

The term in brackets is then the transconductance of the amplifier and is proportional to I_{ABC}.

Linearizing Diodes

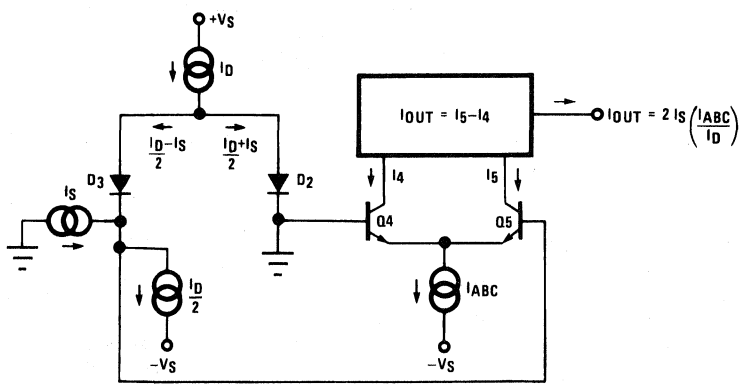
For differential voltages greater than a few millivolts, Equation 3 becomes less valid and the transconductance becomes increasingly nonlinear. *Figure 1* demonstrates how the internal diodes can linearize the transfer function of the amplifier. For convenience assume the diodes are biased with current sources and the input signal is in the form of current I_S. Since the sum of I_4 and I_5 is I_{ABC} and the difference is I_{OUT}, currents I_4 and I_5 can be written as follows:

$$I_4 = \frac{I_{ABC}}{2} - \frac{I_{OUT}}{2}, \; I_5 = \frac{I_{ABC}}{2} + \frac{I_{OUT}}{2}$$

Since the diodes and the input transistors have identical geometries and are subject to similar voltages and temperatures, the following is true:

$$\frac{kT}{q} \ln \frac{\frac{I_D}{2} + I_S}{\frac{I_D}{2} - I_S} = \frac{kT}{q} \ln \frac{\frac{I_{ABC}}{2} + \frac{I_{out}}{2}}{\frac{I_{ABC}}{2} - \frac{I_{out}}{2}}$$

$$\therefore I_{out} = I_S \left(\frac{2I_{ABC}}{I_D} \right) \quad \text{for } |I_S| < \frac{I_D}{2} \quad (6)$$



TL/H/7980–8

FIGURE 1. Linearizing Diodes

Linearizing Diodes (Continued)

Notice that in deriving Equation 6 no approximations have been made and there are no temperature-dependent terms. The limitations are that the signal current not exceed $I_D/2$ and that the diodes be biased with currents. In practice, replacing the current sources with resistors will generate insignificant errors.

Controlled Impedance Buffers

The upper limit of transconductance is defined by the maximum value of I_{ABC} (2 mA). The lowest value of I_{ABC} for which the amplifier will function therefore determines the overall dynamic range. At very low values of I_{ABC}, a buffer which has very low input bias current is desirable. An FET follower satisfies the low input current requirement, but is somewhat non-linear for large voltage swing. The controlled impedance buffer is a Darlington which modifies its input bias current to suit the need. For low values of I_{ABC}, the buffer's input current is minimal. At higher levels of I_{ABC}, transistor Q_3 biases up Q_{12} with a current proportional to I_{ABC} for fast slew rate. When I_{ABC} is changed, the DC level of the Darlington output buffer will shift. In audio applications where I_{ABC} is changed suddenly, this shift may produce an audible "pop". For these applications the LM13700 may produce superior results.

Applications—Voltage Controlled Amplifiers

Figure 2 shows how the linearizing diodes can be used in a voltage-controlled amplifier. To understand the input biasing, it is best to consider the 13 kΩ resistor as a current source and use a Thevenin equivalent circuit as shown in *Figure 3*. This circuit is similar to *Figure 1* and operates the same. The potentiometer in *Figure 2* is adjusted to minimize the effects of the control signal at the output.

For optimum signal-to-noise performance, I_{ABC} should be as large as possible as shown by the Output Voltage vs. Amplifier Bias Current graph. Larger amplitudes of input signal also improve the S/N ratio. The linearizing diodes help here by allowing larger input signals for the same output distortion as shown by the Distortion vs. Differential Input Voltage graph. S/N may be optimized by adjusting the magnitude of the input signal via R_{IN} *(Figure 2)* until the output distortion is below some desired level. The output voltage swing can then be set at any level by selecting R_L.

Although the noise contribution of the linearizing diodes is negligible relative to the contribution of the amplifier's internal transistors, I_D should be as large as possible. This minimizes the dynamic junction resistance of the diodes (r_e) and maximizes their linearizing action when balanced against R_{IN}. A value of 1 mA is recommended for I_D unless the specific application demands otherwise.

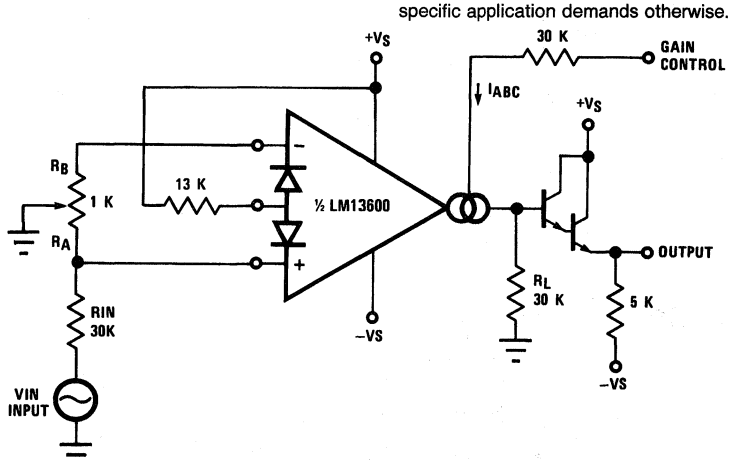


FIGURE 2. Voltage Controlled Amplifier TL/H/7980–9

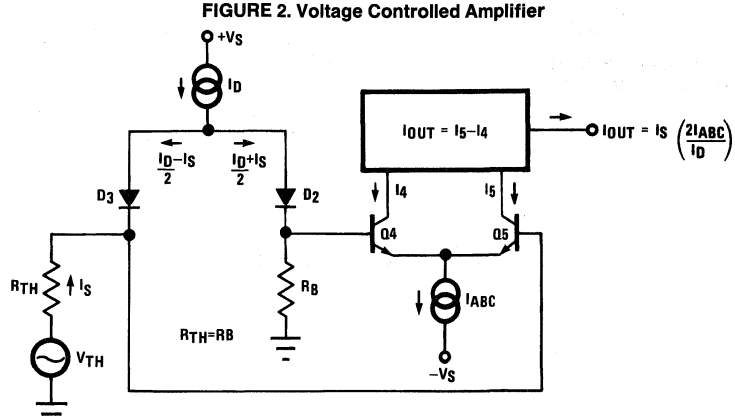


FIGURE 3. Equivalent VCA Input Circuit TL/H/7980–10

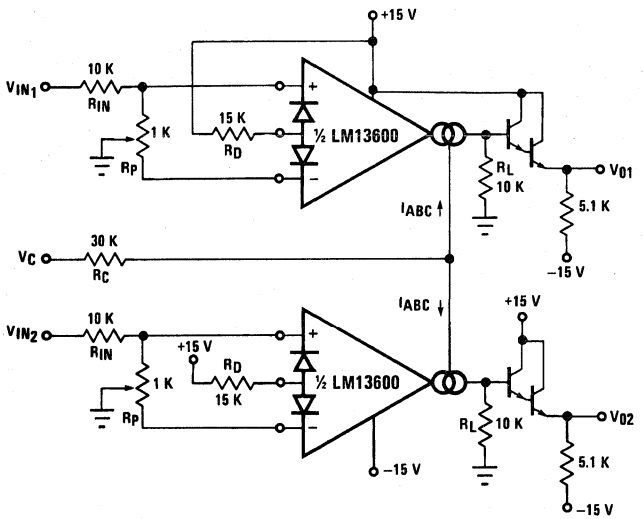
Stereo Volume Control

The circuit of Figure 4 uses the excellent matching of the two LM13600 amplifiers to provide a Stereo Volume Control with a typical channel-to-channel gain tracking of 0.3 dB. R_P is provided to minimize the output offset voltage and may be replaced with two 510Ω resistors in AC-coupled applications. For the component values given, amplifier gain is derived for *Figure 2* as being:

$$\frac{V_O}{V_{IN}} = 940 \times I_{ABC}$$

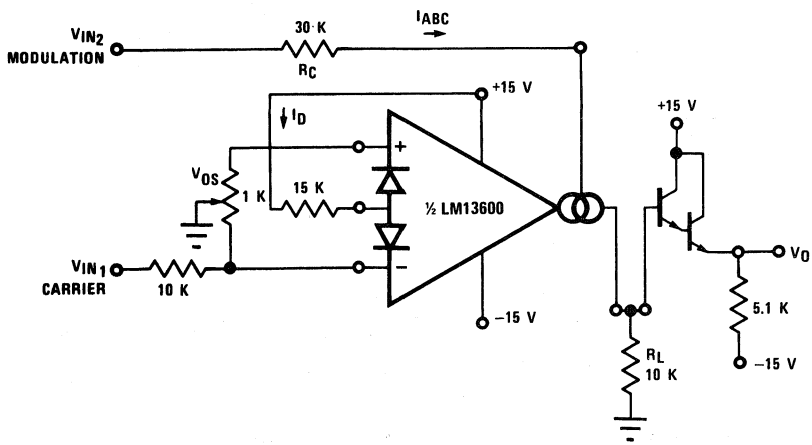
If V_C is derived from a second signal source then the circuit becomes an amplitude modulator or two-quadrant multiplier as shown in *Figure 5*, where:

$$I_O = \frac{-2I_S}{I_D}(I_{ABC}) = \frac{-2I_S}{I_D}\frac{V_{IN2}}{R_C} - \frac{2I_S}{I_D}\frac{(V^- + 1.4V)}{R_C}$$



TL/H/7980–11

FIGURE 4. Stereo Volume Control



TL/H/7980–12

FIGURE 5. Amplitude Modulator

Stereo Volume Control (Continued)

The constant term in the above equation may be cancelled by feeding $I_S \times I_D R_C/2$ ($V^- + 1.4V$) into I_O. The circuit of *Figure 6* adds R_M to provide this current, resulting in a four-quadrant multiplier where R_C is trimmed such that $V_O = 0V$ for $V_{IN2} = 0V$. R_M also serves as the load resistor for I_O.

Noting that the gain of the LM13600 amplifier of *Figure 3* may be controlled by varying the linearizing diode current I_D as well as by varying I_{ABC}, *Figure 7* shows an AGC Amplifier using this approach. As V_O reaches a high enough amplitude (3 V_{BE}) to turn on the Darlington transistors and the linearizing diodes, the increase in I_D reduces the amplifier gain so as to hold V_O at that level.

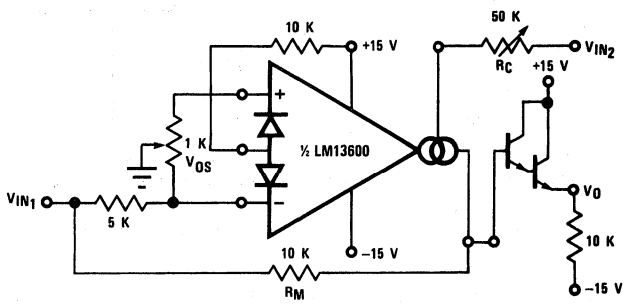
Voltage Controlled Resistors

An Operational Transconductance Amplifier (OTA) may be used to implement a Voltage Controlled Resistor as shown in *Figure 8*. A signal voltage applied at R_X generates a V_{IN} to the LM13600 which is then multiplied by the g_m of the amplifier to produce an output current, thus:

$$R_X = \frac{R + R_A}{g_m R_A}$$

where $g_m \approx 19.2\ I_{ABC}$ at 25°C. Note that the attenuation of V_O by R and R_A is necessary to maintain V_{IN} within the linear range of the LM13600 input.

Figure 9 shows a similar VCR where the linearizing diodes are added, essentially improving the noise performance of the resistor. A floating VCR is shown in *Figure 10*, where each "end" of the "resistor" may be at any voltage within the output voltage range of the LM13600.



TL/H/7980–13

FIGURE 6. Four-Quadrant Multiplier

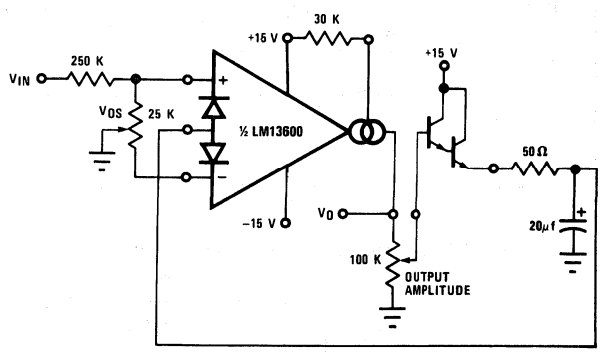


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FIGURE 7. AGC Amplifier

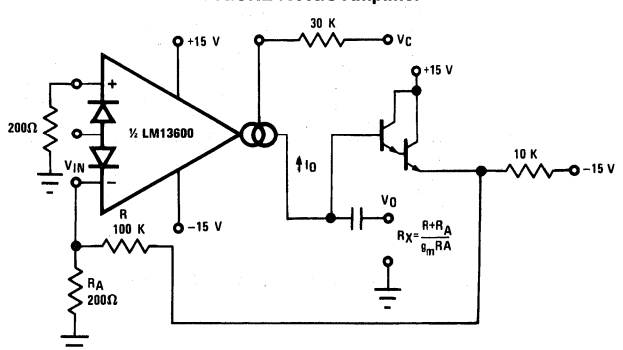

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FIGURE 8. Voltage Controlled Resistor, Single-Ended

Voltage Controlled Filters

OTA's are extremely useful for implementing voltage controlled filters, with the LM13600 having the advantage that the required buffers are included on the I.C. The VC Lo-Pass Filter of *Figure 11* performs as a unity-gain buffer amplifier at frequencies below cut-off, with the cut-off frequency being the point at which X_C/g_m equals the closed-loop gain of (R/R_A). At frequencies above cut-off the circuit provides a single RC roll-off (6 dB per octave) of the input signal amplitude with a −3 dB point defined by the given equation, where g_m is again 19.2 × I_{ABC} at room temperature. *Figure 12* shows a VC High-Pass Filter which operates in much the same manner, providing a single RC roll-off below the defined cut-off frequency.

Additional amplifiers may be used to implement higher order filters as demonstrated by the two-pole Butterworth Lo-Pass Filter of *Figure 13* and the state variable filter of *Figure 14*. Due to the excellent g_m tracking of the two amplifiers and the varied bias of the buffer Darlingtons, these filters perform well over several decades of frequency.

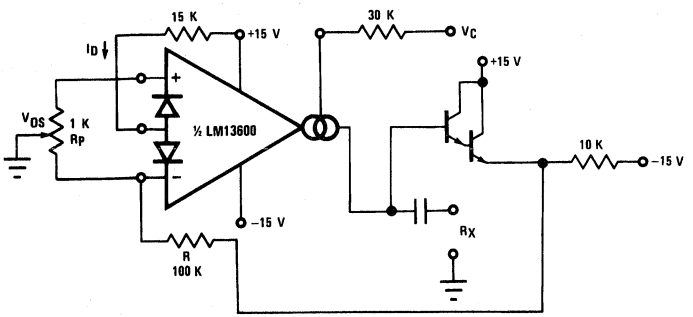

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FIGURE 9. Voltage Controlled Resistor with Linearizing Diodes

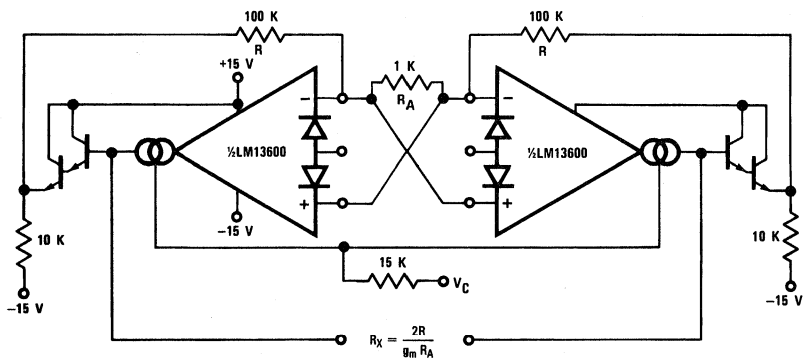

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FIGURE 10. Floating Voltage Controlled Resistor

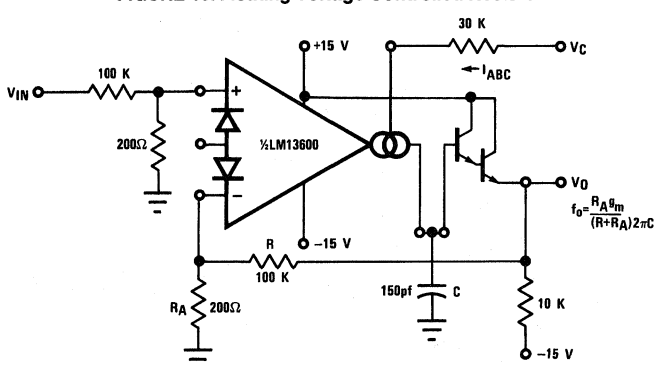

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FIGURE 11. Voltage Controlled Low-Pass Filter

Voltage Controlled Filters (Continued)

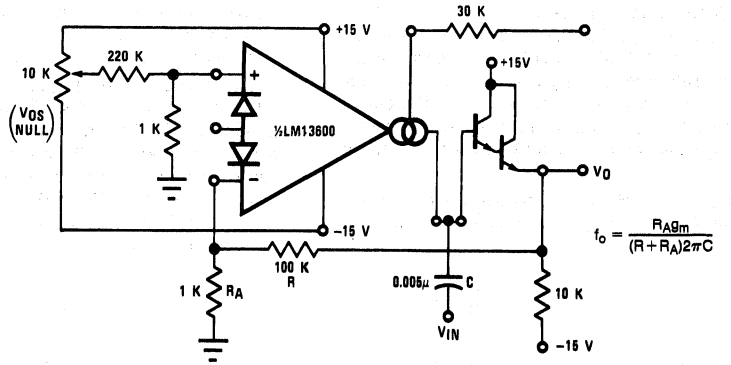

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FIGURE 12. Voltage Controlled Hi-Pass Filter

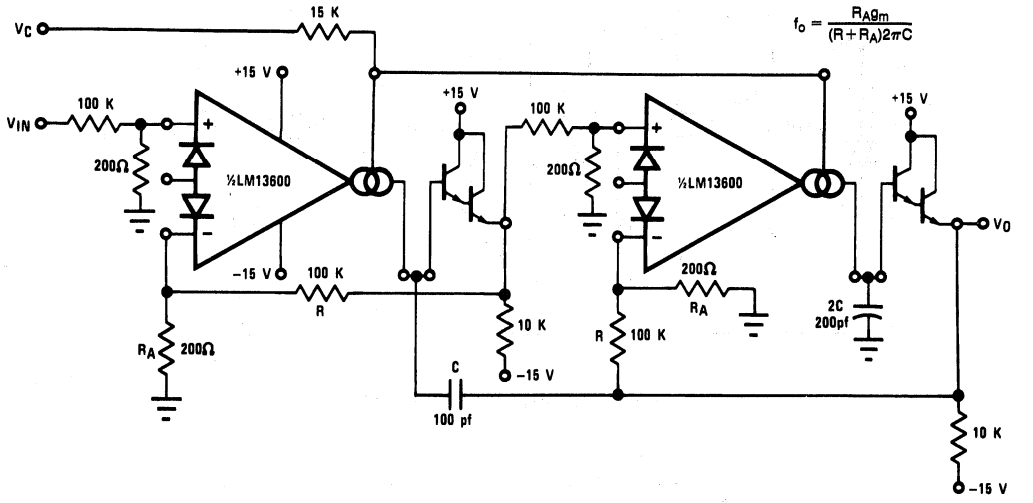

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FIGURE 13. Voltage Controlled 2-Pole Butterworth Lo-Pass Filter

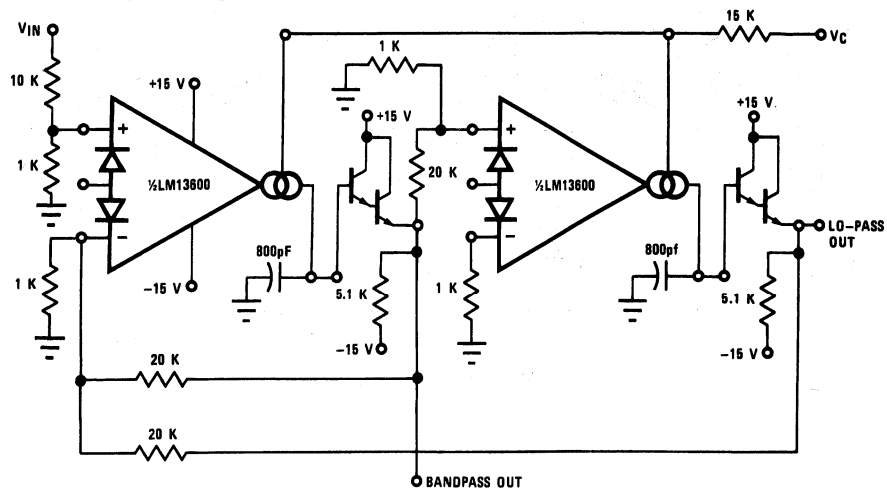

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FIGURE 14. Voltage Controlled State Variable Filter

Voltage Controlled Oscillators

The classic Triangular/Square Wave VCO of *Figure 15* is one of a variety of Voltage Controlled Oscillators which may be built utilizing the LM13600. With the component values shown, this oscillator provides signals from 200 kHz to below 2 Hz as I_C is varied from 1 mA to 10 nA. The output amplitudes are set by $I_A \times R_A$. Note that the peak differential input voltage must be less than 5V to prevent zenering the inputs.

A few modifications to this circuit produce the ramp/pulse VCO of *Figure 16*. When V_{O2} is high, I_F is added to I_C to increase amplifier A1's bias current and thus to increase the charging rate of capacitor C. When V_{O2} is low, I_F goes to zero and the capacitor discharge current is set by I_C.

The VC Lo-Pass Filter of *Figure 11* may be used to produce a high-quality sinusoidal VCO. The circuit of *Figure 16* employs two LM13600 packages, with three of the amplifiers configured as lo-pass filters and the fourth as a limiter/inverter. The circuit oscillates at the frequency at which the loop phase-shift is 360° or 180° for the inverter and 60° per filter stage. This VCO operates from 5 Hz to 50 kHz with less than 1% THD.

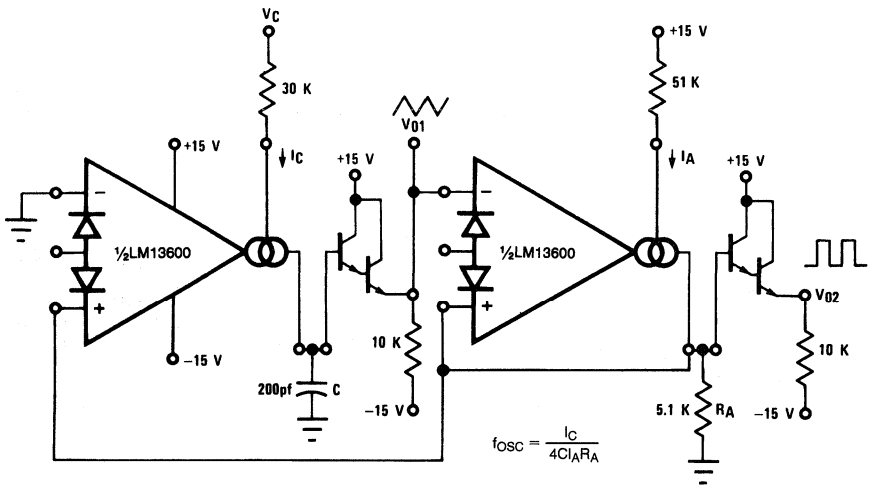

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FIGURE 15. Triangular/Square-Wave VCO

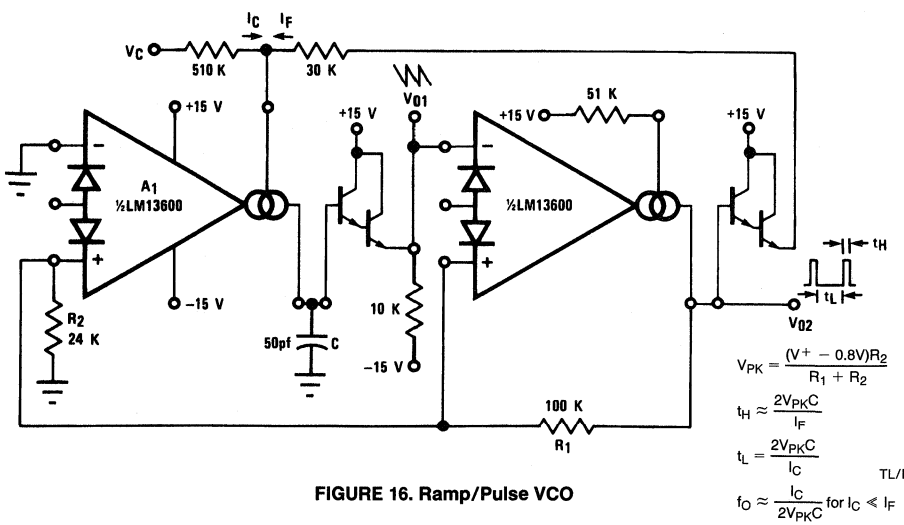

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FIGURE 16. Ramp/Pulse VCO

Voltage Controlled Oscillators (Continued)

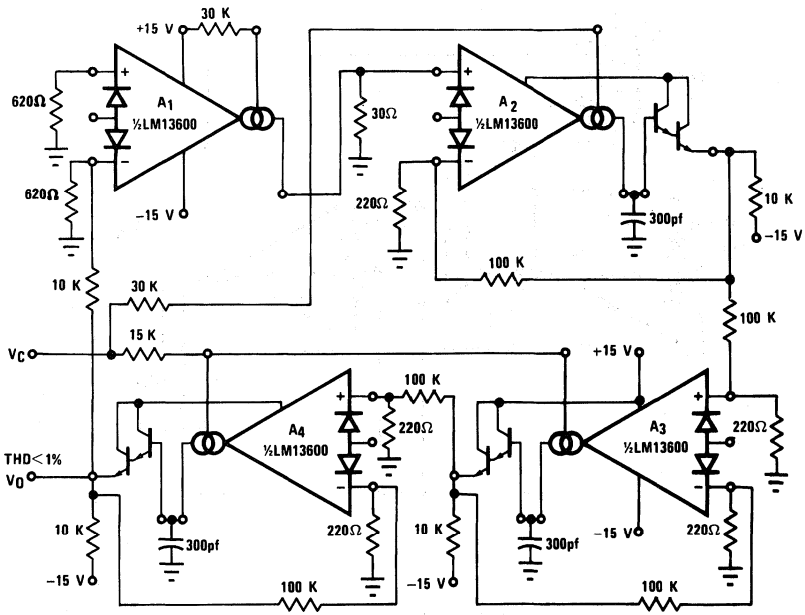

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FIGURE 17. Sinusoidal VCO

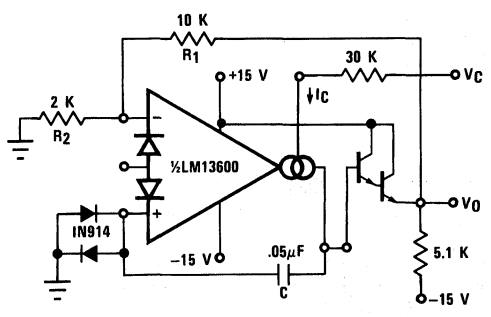

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FIGURE 18. Single Amplifier VCO

Figure 18 shows how to build a VCO using one amplifier when the other amplifier is needed for another function.

Additional Applications

Figure 19 presents an interesting one-shot which draws no power supply current until it is triggered. A positive-going trigger pulse of at least 2V amplitude turns on the amplifier through R_B and pulls the non-inverting input high. The amplifier regenerates and latches its output high until capacitor C charges to the voltage level on the non-inverting input. The output then switches low, turning off the amplifier and discharging the capacitor. The capacitor discharge rate is increased by shorting the diode bias pin to the inverting input so than an additional discharge current flows through D_I when the amplifier output switches low. A special feature of this timer is that the other amplifier, when biased from V_O, can perform another function and draw zero stand-by power as well.

The operation of the multiplexer of *Figure 20* is very straightforward. When A1 is turned on it holds V_O equal to V_{IN1} and when A2 is supplied with bias current then it controls V_O. C_C and R_C serve to stabilize the unity-gain configuration of amplifiers A1 and A2. The maximum clock rate is limited to about 200 kHz by the LM13600 slew rate into 150 pF when the (V_{IN1}-V_{IN2}) differential is at its maximum allowable value of 5V.

The Phase-Locked Loop of *Figure 21* uses the four-quadrant multiplier of *Figure 6* and the VCO of *Figure 18* to produce a PLL with a ±5% hold-in range and an input sensitivity of about 300 mV.

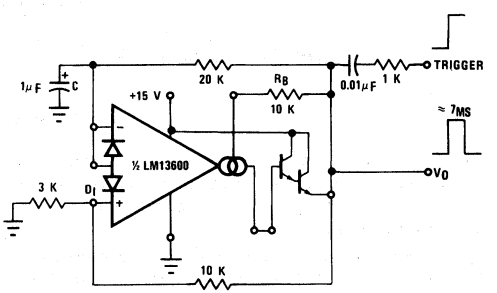

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FIGURE 19. Zero Stand-By Power Timer

Additional Applications (Continued)

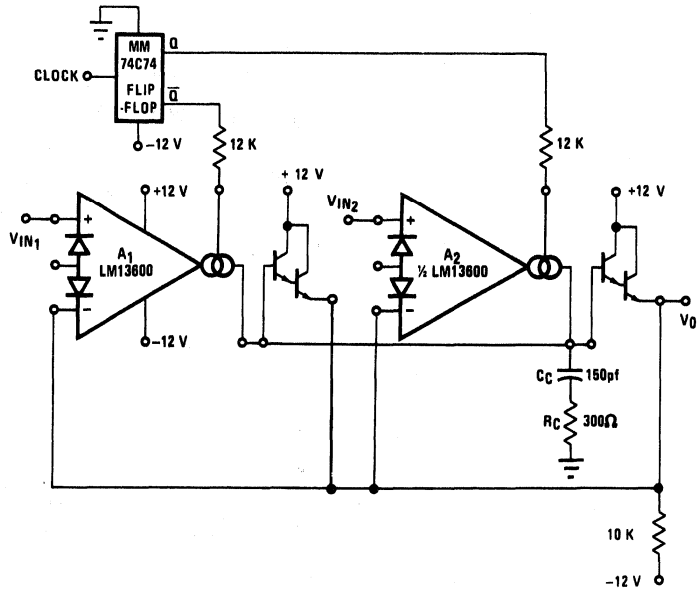

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FIGURE 20. Multiplexer

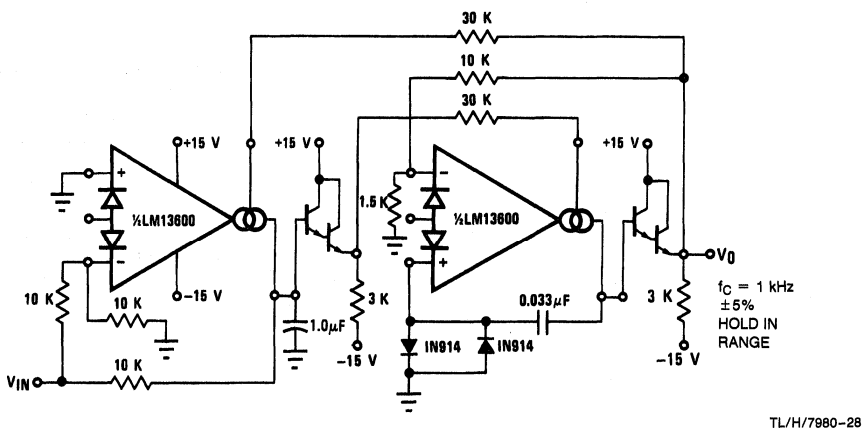

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FIGURE 21. Phase Lock Loop

The Schmitt Trigger of *Figure 22* uses the amplifier output current into R to set the hysteresis of the comparator; thus $V_H = 2 \times R \times I_B$. Varying I_B will produce a Schmitt Trigger with variable hysteresis.

Figure 23 shows a Tachometer or Frequency-to-Voltage converter. Whenever A1 is toggled by a positive-going input, an amount of charge equal to $(V_H - V_L)\, C_t$ is sourced into C_f and R_t. This once-per-cycle charge is then balanced by the current of V_O/R_t. The maximum f_{IN} is limited by the amount of time required to charge C_t from V_L to V_H with a current of I_B, where V_L and V_H represent the maximum low and maximum high output voltage swing of the LM13600. D1 is added to provide a discharge path for C_t when A1 switches low.

The Peak Detector of *Figure 24* uses A2 to turn on A1 whenever V_{IN} becomes more positive than V_O. A1 then charges storage capacitor C to hold V_O equal to $V_{IN}PK$. One precaution to observe when using this circuit: the Darlington transistor used must be on the same side of the package as A2 since the A1 Darlington will be turned on and off with A1. Pulling the output of A2 low through D1 serves to turn off A1 so that V_O remains constant.

Additional Applications (Continued)

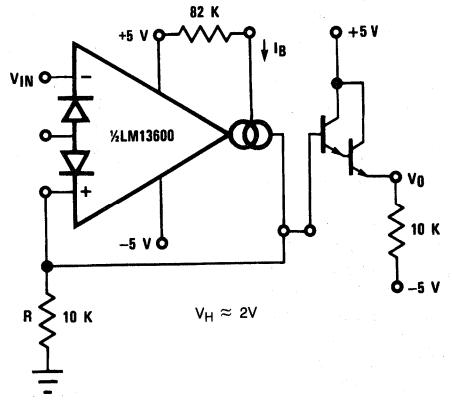

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FIGURE 22. Schmitt Trigger

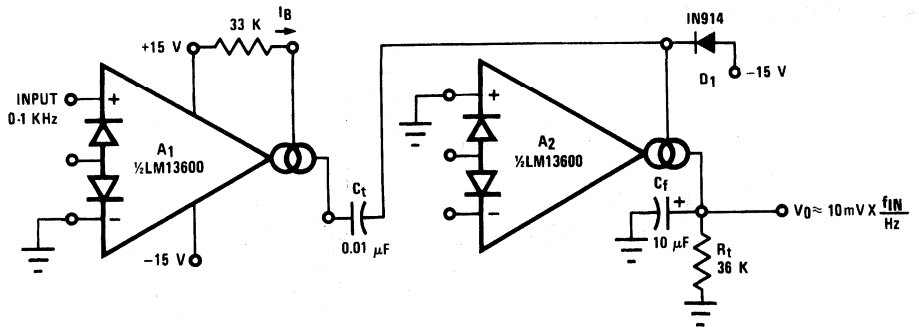

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FIGURE 23. Tachometer

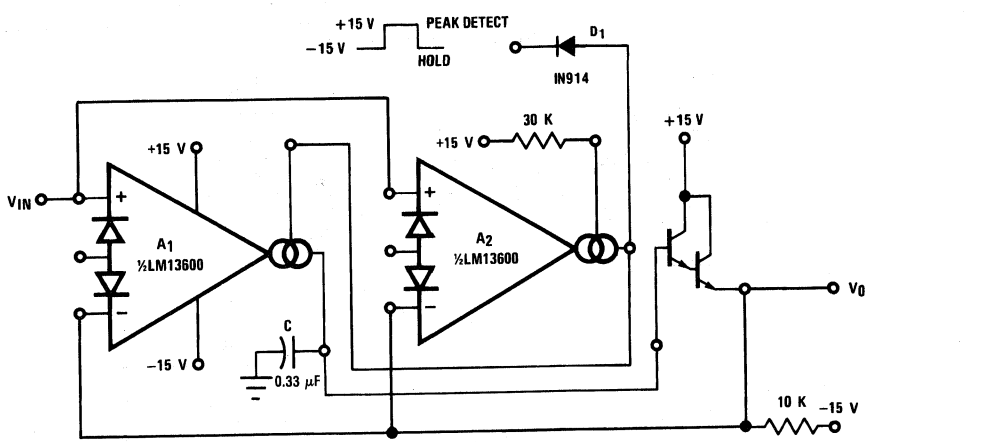

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FIGURE 24. Peak Detector and Hold Circuit

Additional Applications (Continued)

The Sample-Hold circuit of *Figure 25* also requires that the Darlington buffer used be from the other (A2) half of the package and that the corresponding amplifier be biased on continuously. The Ramp-and-Hold of *Figure 26* sources I_B into capacitor C whenever the input to A1 is brought high, giving a ramp-rate of about 1 V/ms for the component values shown.

The true-RMS converter of *Figure 27* is essentially an automatic gain control amplifier which adjusts its gain such that the AC power at the output of amplifier A1 is constant. The output power of amplifier A1 is monitored by squaring amplifier A2 and the average compared to a reference voltage with amplifier A3. The output of A3 provides bias current to the diodes of A1 to attenuate the input signal. Because the output power of A1 is held constant, the RMS value is constant and the attentuation is directly proportional to the RMS value of the input voltage. The attenuation is also proportional to the diode bias current. Amplifier A4 adjusts the ratio of currents through the diodes to be equal and therefore the voltage at the output of A4 is proportional to the RMS value of the input voltage. The calibration potentiometer is set such that V_O reads directly in RMS volts.

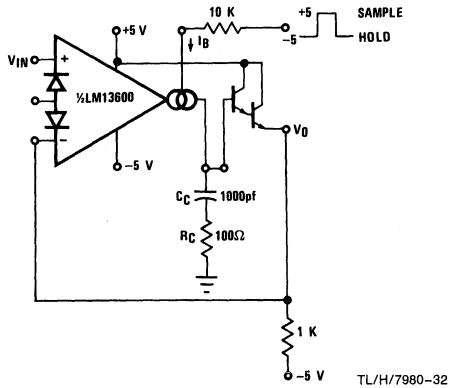

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FIGURE 25. Sample-Hold Circuit

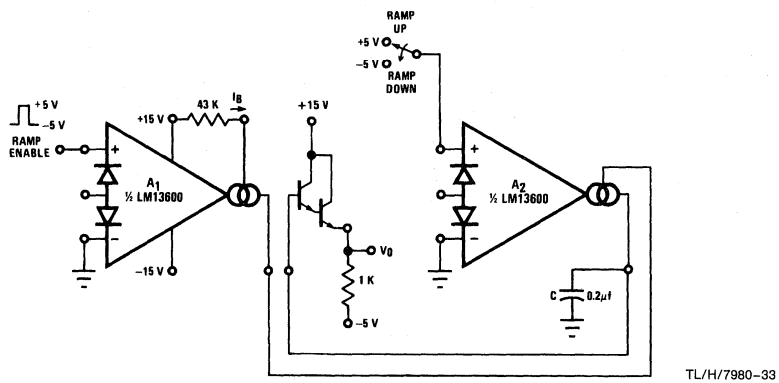

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FIGURE 26. Ramp and Hold

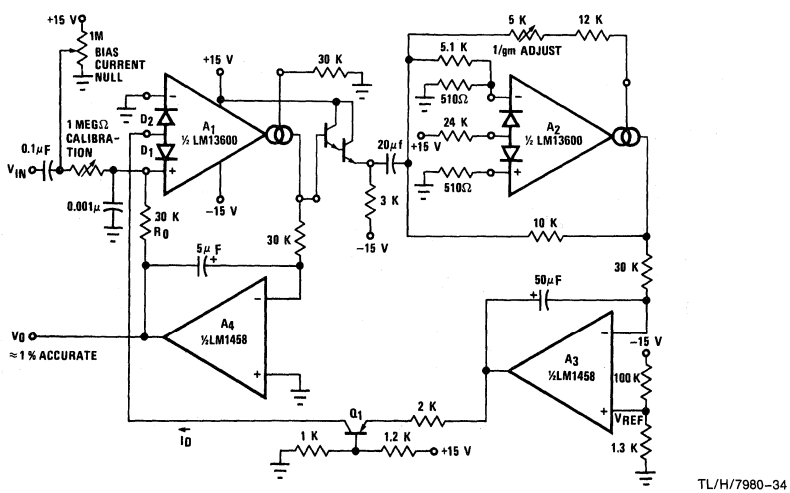

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FIGURE 27. True RMS Converter

Additional Applications (Continued)

The circuit of *Figure 28* is a voltage reference of variable temperature coefficient. The 100 kΩ potentiometer adjusts the output voltage which has a positive TC above 1.2V, zero TC at about 1.2V and negative TC below 1.2V. This is accomplished by balancing the TC of the A2 transfer function against the complementary TC of D1.

The log amplifier of *Figure 29* responds to the ratio of currents through buffer transistors Q3 and Q4. Zero temperature dependence for V_{OUT} is ensured because the TC of the A2 transfer function is equal and opposite to the TC of the logging transistors Q3 and Q4.

The wide dynamic range of the LM13600 allows easy control of the output pulse width in the Pulse Width Modulator of *Figure 30*.

For generating I_{ABC} over a range of 4 to 6 decades of current, the system of *Figure 31* provides a logarithmic current out for a linear voltage in.

Since the closed-loop configuration ensures that the input to A2 is held equal to 0V, the output current of A1 is equal to $I_3 = -V_C/R_C$.

The differential voltage between Q1 and Q2 is attenuated by the R1, R2 network so that A1 may be assumed to be operating within its linear range. From equation (5), the input voltage to A1 is:

$$V_{IN}1 = \frac{-2kTI_3}{qI_2} = \frac{2kTV_C}{qI_2R_C}$$

The voltage on the base of Q1 is then

$$V_B1 = \frac{(R_1+R_2)\,V_{IN}1}{R_1}$$

The ratio of the Q1 and Q2 collector currents is defined by:

$$V_B1 = \frac{kT}{q}\ln\frac{I_{C2}}{I_{C1}} \approx \frac{kT}{q}\ln\frac{I_{ABC}}{I_1}$$

Combining and solving for I_{ABC} yields:

$$I_{ABC} = I_1 \exp\left[\frac{2(R_1+R_2)\,V_C}{R_1I_2R_C}\right]$$

This logarithmic current can be used to bias the circuit of *Figure 4* provide a temperature independent stereo attenuation characteristic.

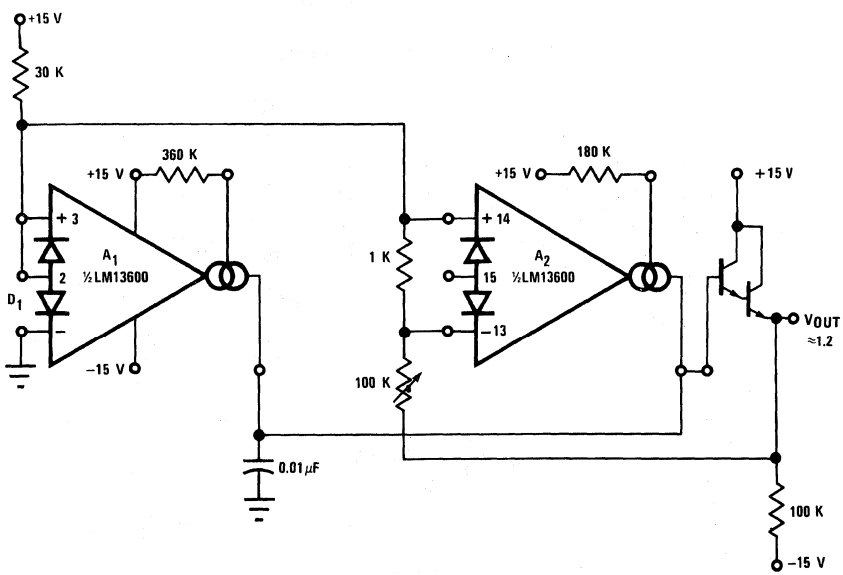

FIGURE 28. Delta VBE Reference

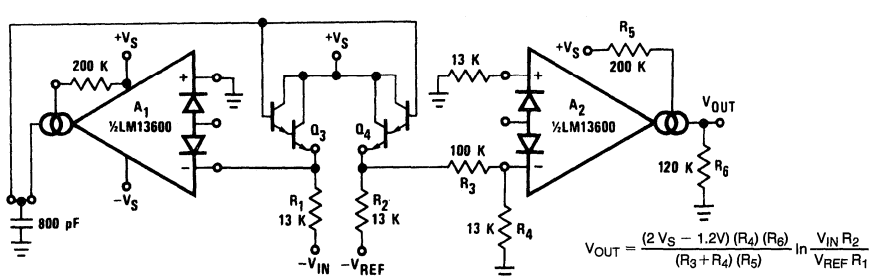

FIGURE 29. Log Amplifier

Additional Applications (Continued)

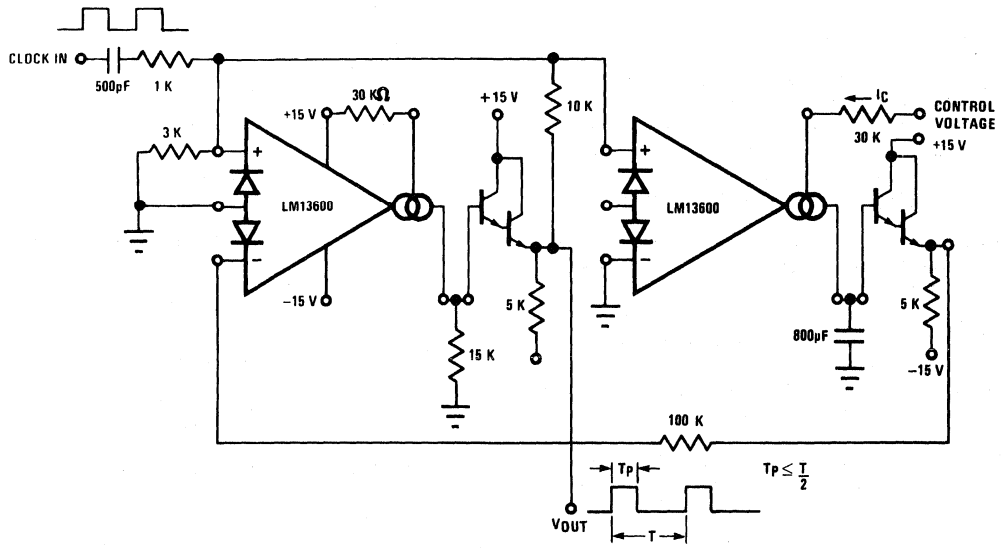

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FIGURE 30. Pulse Width Modulator

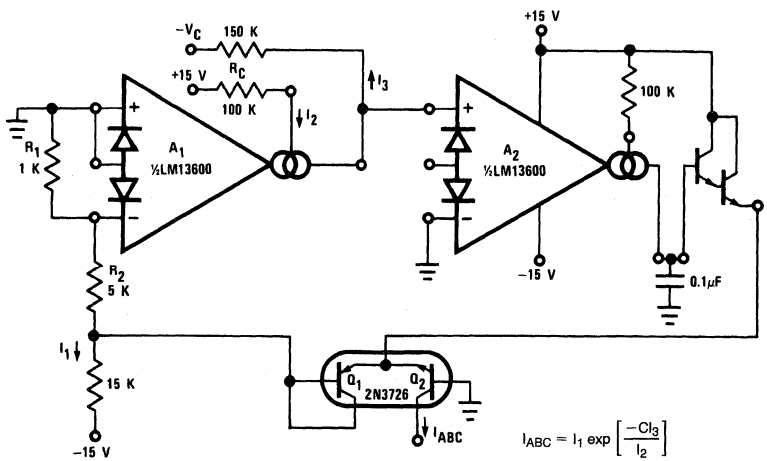

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FIGURE 31. Logarithmic Current Source

National Semiconductor

LMC660
CMOS Quad Operational Amplifier

General Description

The LMC660 CMOS Quad operational amplifier is ideal for operation from a single supply. It operates from +5V to +15V and features rail-to-rail output swing in addition to an input common-mode range that includes ground. Performance limitations that have plagued CMOS amplifiers in the past are not a problem with this design. Input V_{OS}, drift, and broadband noise as well as voltage gain into realistic loads (2 kΩ and 600Ω) are all equal to or better than widely accepted bipolar equivalents.

This chip is built with National's advanced Double-Poly Silicon-Gate CMOS process.

See the LMC662 datasheet for a dual CMOS operational amplifier with these same features.

Features

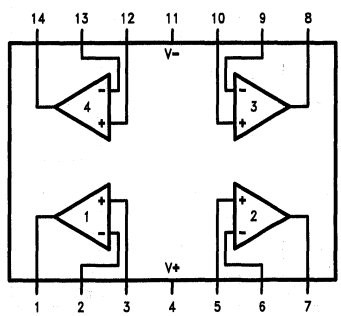
- Rail-to-rail output swing
- Specified for 2 kΩ and 600Ω loads
- High voltage gain 126 dB
- Low input offset voltage 3 mV
- Low offset voltage drift 1.3 μV/°C
- Ultra low input bias current 2 fA
- Input common-mode range includes V−
- Operating range from +5V to +15V supply
- I_{SS} = 375 μA/amplifier; independent of V^+
- Low distortion 0.01% at 10 kHz
- Slew rate 1.1 V/μs
- Available in extended temperature range (−40°C to +125°C); ideal for automotive applications
- Available to Standard Military Drawing specification

Applications

- High-impedance buffer or preamplifier
- Precision current-to-voltage converter
- Long-term integrator
- Sample-and-Hold circuit
- Peak detector
- Medical instrumentation
- Industrial controls
- Automotive sensors

Connection Diagram

14-Pin DIP/SO



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Ordering Information

Package	Temperature Range				NSC Drawing
	Military −55°C to +125°C	Extended −40°C +125°C	Industrial −40°C to +85°C	Commercial 0°C to +70°C	
14-Pin Ceramic DIP	LMC660AMJ/883				J14A
14-Pin Small Outline		LMC660EM	LMC660AIM	LMC660CM	M14A
14-Pin Molded DIP		LMC660EN	LMC660AIN	LMC660CN	N14A
14-Pin Side Brazed Ceramic DIP	LMC660AMD				D14E

Absolute Maximum Ratings (Note 3)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Differential Input Voltage	±Supply Voltage
Supply Voltage	16V
Output Short Circuit to V^+	(Note 12)
Output Short Circuit to V^-	(Note 1)
Lead Temperature (Soldering, 10 sec.)	260°C
Storage Temp. Range	−65°C to +150°C
Voltage at Input/Output Pins	$(V^+) + 0.3V, (V^-) - 0.3V$
Current at Output Pin	±18 mA
Current at Input Pin	±5 mA
Current at Power Supply Pin	35 mA
Power Dissipation	(Note 2)
Junction Temperature	150°C
ESD tolerance (Note 8)	500V

Operating Ratings

Temperature Range	
LMC660AMJ/883, LMC660AMD	$-55°C \le T_J \le +125°C$
LMC660AI	$-40°C \le T_J \le +85°C$
LMC660C	$0°C \le T_J \le +70°C$
LMC660E	$-40°C \le T_J \le +125°C$
Supply Voltage Range	4.75V to 15.5V
Power Dissipation	(Note 10)
Thermal Resistance (θ_{JA}) (Note 11)	
14-Pin Ceramic DIP	90°C/W
14-Pin Molded DIP	85°C/W
14-Pin SO	115°C/W
14-Pin Side Brazed Ceramic DIP	90°C/W

DC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for T_J = 25°C. **Boldface** limits apply at the temperature extremes. V^+ = 5V, V^- = 0V, V_{CM} = 1.5V, V_O = 2.5V and R_L > 1M unless otherwise specified.

Parameter	Conditions	Typ (Note 4)	LMC660AMD LMC660AMJ/883 Limit (Notes 4, 9)	LMC660AI Limit (Note 4)	LMC660C Limit (Note 4)	LMC660E Limit (Note 4)	Units
Input Offset Voltage		1	3 **3.5**	3 **3.3**	6 **6.3**	6 **6.5**	mV max
Input Offset Voltage Average Drift		1.3					µV/°C
Input Bias Current		0.002	20 **100**	**4**	**2**	**60**	pA max
Input Offset Current		0.001	20 **100**	**2**	**1**	**60**	pA max
Input Resistance		>1					TeraΩ
Common Mode Rejection Ratio	$0V \le V_{CM} \le 12.0V$ $V^+ = 15V$	83	70 **68**	70 **68**	63 **62**	63 **60**	dB min
Positive Power Supply Rejection Ratio	$5V \le V^+ \le 15V$ $V_O = 2.5V$	83	70 **68**	70 **68**	63 **62**	63 **60**	dB min
Negative Power Supply Rejection Ratio	$0V \le V^- \le -10V$	94	84 **82**	84 **83**	74 **73**	74 **70**	dB min
Input Common-Mode Voltage Range	V^+ = 5V & 15V For CMRR ≥ 50 dB	−0.4	−0.1 **0**	−0.1 **0**	−0.1 **0**	−0.1 **0**	V max
		$V^+ - 1.9$	$V^+ - 2.3$ $\mathbf{V^+ - 2.6}$	$V^+ - 2.3$ $\mathbf{V^+ - 2.5}$	$V^+ - 2.3$ $\mathbf{V^+ - 2.4}$	$V^+ - 2.3$ $\mathbf{V^+ - 2.6}$	V min
Large Signal Voltage Gain	R_L = 2 kΩ (Note 5) Sourcing	2000	400 **300**	400 **440**	200 **300**	200 **100**	V/mV min
	Sinking	500	180 **70**	180 **120**	90 **80**	90 **40**	V/mV min
	R_L = 600Ω (Note 5) Sourcing	1000	200 **150**	200 **220**	100 **150**	100 **75**	V/mV min
	Sinking	250	100 **35**	100 **60**	50 **40**	50 **20**	V/mV min

DC Electrical Characteristics (Continued)

Unless otherwise specified, all limits guaranteed for T_J = 25°C. **Boldface** limits apply at the temperature extremes. V^+ = 5V, V^- = 0V, V_{CM} = 1.5V, V_O = 2.5V and R_L > 1M unless otherwise specified.

Parameter	Conditions	Typ (Note 4)	LMC660AMD LMC660AMJ/883 Limit (Notes 4, 9)	LMC660AI Limit (Note 4)	LMC660C Limit (Note 4)	LMC660E Limit (Note 4)	Units
Output Swing	V^+ = 5V R_L = 2 kΩ to $V^+/2$	4.87	4.82 **4.77**	4.82 **4.79**	4.78 **4.76**	4.78 **4.70**	V min
		0.10	0.15 **0.19**	0.15 **0.17**	0.19 **0.21**	0.19 **0.25**	V max
	V^+ = 5V R_L = 600Ω to $V^+/2$	4.61	4.41 **4.24**	4.41 **4.31**	4.27 **4.21**	4.27 **4.10**	V min
		0.30	0.50 **0.63**	0.50 **0.56**	0.63 **0.69**	0.63 **0.75**	V max
	V^+ = 15V R_L = 2 kΩ to $V^+/2$	14.63	14.50 **14.40**	14.50 **14.44**	14.37 **14.32**	14.37 **14.25**	V min
		0.26	0.35 **0.43**	0.35 **0.40**	0.44 **0.48**	0.44 **0.55**	V max
	V^+ = 15V R_L = 600Ω to $V^+/2$	13.90	13.35 **13.02**	13.35 **13.15**	12.92 **12.76**	12.92 **12.60**	V min
		0.79	1.16 **1.42**	1.16 **1.32**	1.45 **1.58**	1.45 **1.75**	V max
Output Current V^+ = 5V	Sourcing, V_O = 0V	22	16 **12**	16 **14**	13 **11**	13 **9**	mA min
	Sinking, V_O = 5V	21	16 **12**	16 **14**	13 **11**	13 **9**	mA min
Output Current V^+ = 15V	Sourcing, V_O = 0V	40	19 **19**	28 **25**	23 **21**	23 **15**	mA min
	Sinking, V_O = 13V (Note 12)	39	19 **19**	28 **24**	23 **20**	23 **15**	mA min
Supply Current	All Four Amplifiers V_O = 1.5V	1.5	2.2 **2.9**	2.2 **2.6**	2.7 **2.9**	2.7 **3.0**	mA max

AC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for $T_J = 25°C$. **Boldface** limits apply at the temperature extremes. $V^+ = 5V$, $V^- = 0V$, $V_{CM} = 1.5V$, $V_O = 2.5V$ and $R_L > 1M$ unless otherwise specified.

Parameter	Conditions	Typ (Note 4)	LMC660AMD LMC660AMJ/883	LMC660AI	LMC660C	LMC660E	Units
			Limit (Notes 4, 9)	Limit (Note 4)	Limit (Note 4)	Limit (Note 4)	
Slew Rate	(Note 6)	1.1	0.8 **0.5**	0.8 **0.6**	0.8 **0.7**	0.8 **0.4**	V/μs min
Gain-Bandwidth Product		1.4	**0.5**				MHz
Phase Margin		50					Deg
Gain Margin		17					dB
Amp-to-Amp Isolation	(Note 7)	130					dB
Input Referred Voltage Noise	F = 1 kHz	22					nV/√Hz
Input Referred Current Noise	F = 1 kHz	0.0002					pA/√Hz
Total Harmonic Distortion	F = 10 kHz, $A_V = -10$ $R_L = 2\,k\Omega$, $V_O = 8\,V_{PP}$ $V^+ = 15V$	0.01					%

Note 1: Applies to both single supply and split supply operation. Continuous short circuit operation at elevated ambient temperature and/or multiple Op Amp shorts can result in exceeding the maximum allowed junction temperature of 150°C. Output currents in excess of ±30 mA over long term may adversely affect reliability.

Note 2: The maximum power dissipation is a function of $T_{J(max)}$, θ_{JA}, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(max)} - T_A)/\theta_{JA}$.

Note 3: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed.

Note 4: Typical values represent the most likely parametric norm. Limits are guaranteed by testing or correlation.

Note 5: $V^+ = 15V$, $V_{CM} = 7.5V$ and R_L connected to 7.5V. For Sourcing tests, $7.5V \le V_O \le 11.5V$. For Sinking tests, $2.5V \le V_O \le 7.5V$.

Note 6: $V^+ = 15V$. Connected as Voltage Follower with 10V step input. Number specified is the slower of the positive and negative slew rates.

Note 7: Input referred. $V^+ = 15V$ and $R_L = 10\,k\Omega$ connected to $V^+/2$. Each amp excited in turn with 1 kHz to produce $V_O = 13\,V_{PP}$.

Note 8: Human body model, 1.5 kΩ in series with 100 pF.

Note 9: A military RETS electrical test specification is available on request. At the time of printing, the LMC660AMJ/883 RETS spec complied fully with the boldface limits in this column. The LMC660AMJ/883 may also be procured to a Standard Military Drawing specification.

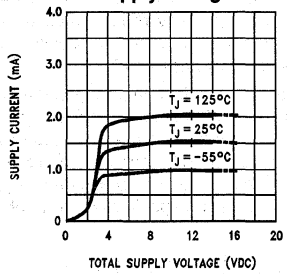
Note 10: For operating at elevated temperatures the device must be derated based on the thermal resistance θ_{JA} with $P_D = (T_J - T_A)/\theta_{JA}$.

Note 11: All numbers apply for packages soldered directly into a PC board.

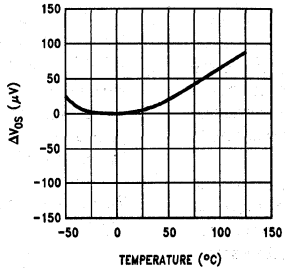
Note 12: Do not connect output to V^+ when V^+ is greater than 13V or reliability may be adversely affected.

Typical Performance Characteristics $V_S = \pm 7.5V$, $T_A = 25°C$ unless otherwise specified

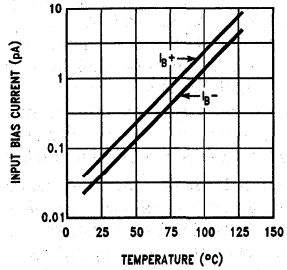
Supply Current vs Supply Voltage



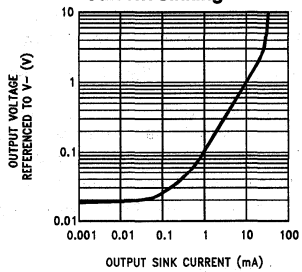
Offset Voltage



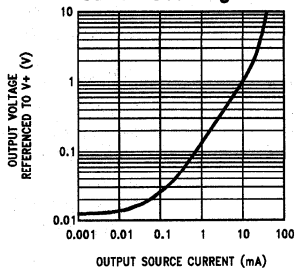
Input Bias Current



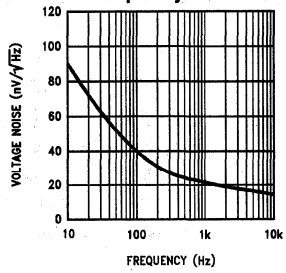
Output Characteristics Current Sinking



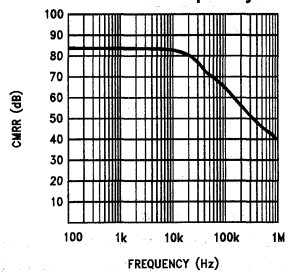
Output Characteristics Current Sourcing



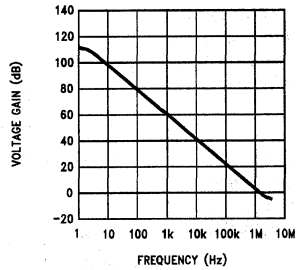
Input Voltage Noise vs Frequency



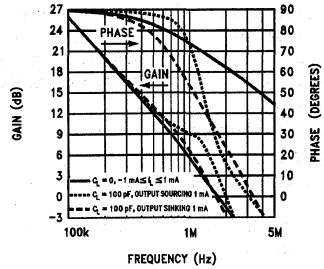
CMRR vs Frequency



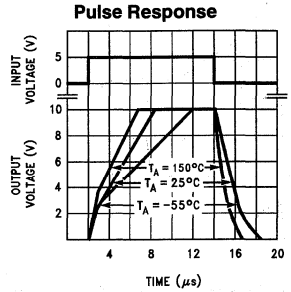
Open-Loop Frequency Response



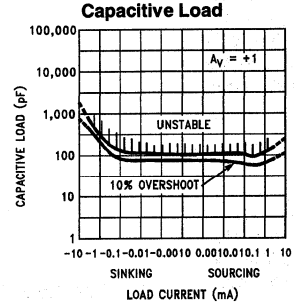
Frequency Response vs Capacitive Load



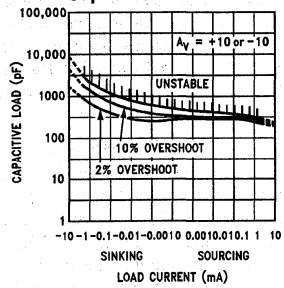
Non-Inverting Large Signal Pulse Response



Stability vs Capacitive Load



Stability vs Capacitive Load



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Note: Avoid resistive loads of less than 500Ω, as they may cause instability.

Application Hints

Amplifier Topology

The topology chosen for the LMC660, shown in *Figure 1*, is unconventional (compared to general-purpose op amps) in that the traditional unity-gain buffer output stage is not used; instead, the output is taken directly from the output of the integrator, to allow rail-to-rail output swing. Since the buffer traditionally delivers the power to the load, while maintaining high op amp gain and stability, and must withstand shorts to either rail, these tasks now fall to the integrator.

As a result of these demands, the integrator is a compound affair with an embedded gain stage that is doubly fed forward (via C_f and Cff) by a dedicated unity-gain compensation driver. In addition, the output portion of the integrator is a push-pull configuration for delivering heavy loads. While sinking current the whole amplifier path consists of three gain stages with one stage fed forward, whereas while sourcing the path contains four gain stages with two fed forward.

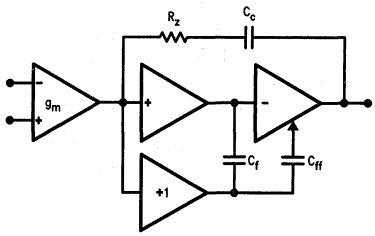

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FIGURE 1. LMC660 Circuit Topology (Each Amplifier)

The large signal voltage gain while sourcing is comparable to traditional bipolar op amps, even with a 600Ω load. The gain while sinking is higher than most CMOS op amps, due to the additional gain stage; however, under heavy load (600Ω) the gain will be reduced as indicated in the Electrical Characteristics.

Compensating Input Capacitance

The high input resistance of the LMC660 op amps allows the use of large feedback and source resistor values without losing gain accuracy due to loading. However, the circuit will be especially sensitive to its layout when these large-value resistors are used.

Every amplifier has some capacitance between each input and AC ground, and also some differential capacitance between the inputs. When the feedback network around an amplifier is resistive, this input capacitance (along with any additional capacitance due to circuit board traces, the socket, etc.) and the feedback resistors create a pole in the feedback path. In the following General Operational Amplifier circuit, *Figure 2* the frequency of this pole is

$$fp = \frac{1}{2\pi C_S R_P}$$

where C_S is the total capacitance at the inverting input, including amplifier input capcitance and any stray capacitance from the IC socket (if one is used), circuit board traces, etc., and R_P is the parallel combination of R_F and R_{IN}. This formula, as well as all formulae derived below, apply to inverting and non-inverting op-amp configurations.

When the feedback resistors are smaller than a few kΩ, the frequency of the feedback pole will be quite high, since C_S is generally less than 10 pF. If the frequency of the feedback pole is much higher than the "ideal" closed-loop bandwidth (the nominal closed-loop bandwidth in the absence of C_S), the pole will have a negligible effect on stability, as it will add only a small amount of phase shift.

However, if the feedback pole is less than approximately 6 to 10 times the "ideal" −3 dB frequency, a feedback capacitor, C_F, should be connected between the output and the inverting input of the op amp. This condition can also be stated in terms of the amplifier's low-frequency noise gain: To maintain stability a feedback capacitor will probably be needed if

$$\left(\frac{R_F}{R_{IN}} + 1\right) \leq \sqrt{6 \times 2\pi \times GBW \times R_F \times C_S}$$

where $\left(\frac{R_F}{R_{IN}} + 1\right)$ is the amplifier's low-frequency noise gain and GBW is the amplifier's gain bandwidth product. An amplifier's low-frequency noise gain is represented by the formula $\left(\frac{R_F}{R_{IN}} + 1\right)$ regardless of whether the amplifier is being used in inverting or non-inverting mode. Note that a feedback capacitor is more likely to be needed when the noise gain is low and/or the feedback resistor is large.

If the above condition is met (indicating a feedback capacitor will probably be needed), and the noise gain is large enough that:

$$\left(\frac{R_F}{R_{IN}} + 1\right) \geq 2\sqrt{GBW \times R_F \times C_S},$$

the following value of feedback capacitor is recommended:

$$C_F = \frac{C_S}{2\left(\frac{R_F}{R_{IN}} + 1\right)}$$

If

$$\left(\frac{R_F}{R_{IN}} + 1\right) < 2\sqrt{GBW \times R_F \times C_S}$$

the feedback capacitor should be:

$$C_F = \sqrt{\frac{C_S}{GBW \times R_F}}$$

Note that these capacitor values are usually significant smaller than those given by the older, more conservative formula:

$$C_F = \frac{C_S R_{IN}}{R_F}$$

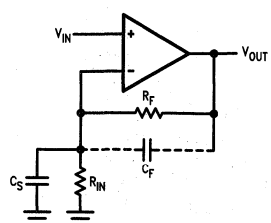

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FIGURE 2. General Operational Amplifier Circuit

C_S consists of the amplifier's input capacitance plus any stray capacitance from the circuit board and socket. C_F compensates for the pole caused by C_S and the feedback resistors.

Application Hints (Continued)

Using the smaller capacitors will give much higher bandwidth with little degradation of transient response. It may be necessary in any of the above cases to use a somewhat larger feedback capacitor to allow for unexpected stray capacitance, or to tolerate additional phase shifts in the loop, or excessive capacitive load, or to decrease the noise or bandwidth, or simply because the particular circuit implementation needs more feedback capacitance to be sufficiently stable. For example, a printed circuit board's stray capacitance may be larger or smaller than the breadboard's, so the actual optimum value for C_F may be different from the one estimated using the breadboard. In most cases, the values of C_F should be checked on the actual circuit, starting with the computed value.

Capacitive Load Tolerance

Like many other op amps, the LMC660 may oscillate when its applied load appears capacitive. The threshold of oscillation varies both with load and circuit gain. The configuration most sensitive to oscillation is a unity-gain follower. See Typical Performance Characteristics.

The load capacitance interacts with the op amp's output resistance to create an additional pole. If this pole frequency is sufficiently low, it will degrade the op amp's phase margin so that the amplifier is no longer stable at low gains. As shown in *Figure 3a,* the addition of a small resistor (50Ω to 100Ω) in series with the op amp's output, and a capacitor (5 pF to 10 pF) from inverting input to output pins, returns the phase margin to a safe value without interfering with lower-frequency circuit operation. Thus larger values of capacitance can be tolerated without oscillation. Note that in all cases, the output will ring heavily when the load capacitance is near the threshold for oscillation.

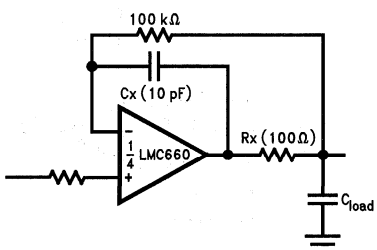

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FIGURE 3a. Rx, Cx Improve Capacitive Load Tolerance

Capacitive load driving capability is enhanced by using a pull up resistor to V^+ *(Figure 3b).* Typically a pull up resistor conducting 500 μA or more will significantly improve capacitive load responses. The value of the pull up resistor must be determined based on the current sinking capability of the amplifier with respect to the desired output swing. Open loop gain of the amplifier can also be affected by the pull up resistor (see Electrical Characteristics).

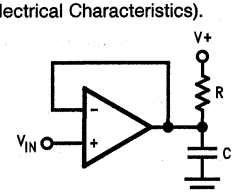

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FIGURE 3b. Compensating for Large Capacitive Loads with a Pull Up Resistor

PRINTED-CIRCUIT-BOARD LAYOUT FOR HIGH-IMPEDANCE WORK

It is generally recognized that any circuit which must operate with less than 1000 pA of leakage current requires special layout of the PC board. When one wishes to take advantage of the ultra-low bias current of the LMC662, typically less than 0.04 pA, it is essential to have an excellent layout. Fortunately, the techniques for obtaining low leakages are quite simple. First, the user must not ignore the surface leakage of the PC board, even though it may sometimes appear acceptably low, because under conditions of high humidity or dust or contamination, the surface leakage will be appreciable.

To minimize the effect of any surface leakage, lay out a ring of foil completely surrounding the LMC660's inputs and the terminals of capacitors, diodes, conductors, resistors, relay terminals, etc. connected to the op-amp's inputs. See *Figure 4.* To have a significant effect, guard rings should be placed on both the top and bottom of the PC board. This PC foil must then be connected to a voltage which is at the same voltage as the amplifier inputs, since no leakage current can flow between two points at the same potential. For example, a PC board trace-to-pad resistance of $10^{12}\Omega$, which is normally considered a very large resistance, could leak 5 pA if the trace were a 5V bus adjacent to the pad of an input. This would cause a 100 times degradation from the LMC660's actual performance. However, if a guard ring is held within 5 mV of the inputs, then even a resistance of $10^{11}\Omega$ would cause only 0.05 pA of leakage current, or perhaps a minor (2:1) degradation of the amplifier's performance. See *Figures 5a, 5b, 5c* for typical connections of guard rings for standard op-amp configurations. If both inputs are active and at high impedance, the guard can be tied to ground and still provide some protection; see *Figure 5d.*

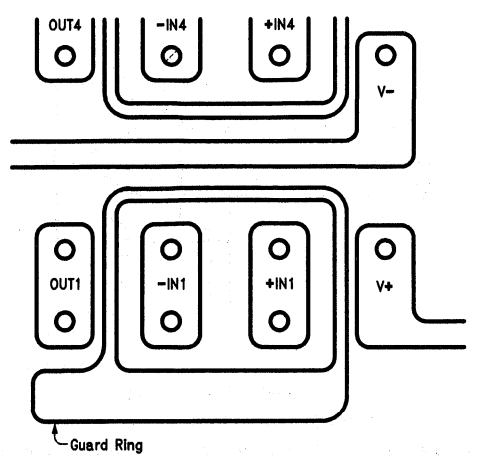

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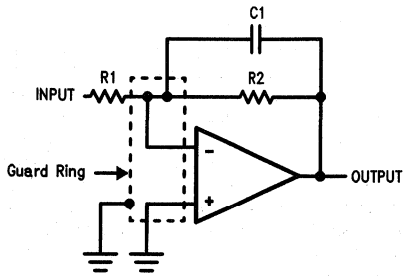
FIGURE 4. Example, using the LMC660, of Guard Ring in P.C. Board Layout

Application Hints (Continued)



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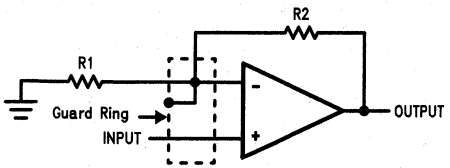
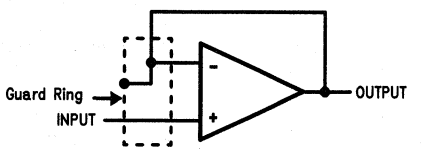
(a) Inverting Amplifier



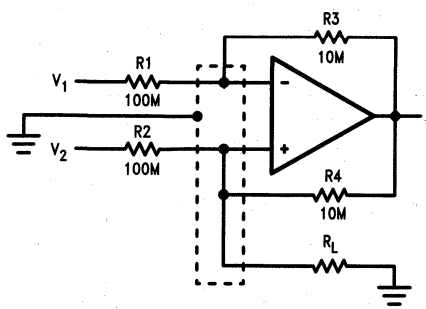
TL/H/8767–18

(b) Non-Inverting Amplifier



TL/H/8767–19

(c) Follower

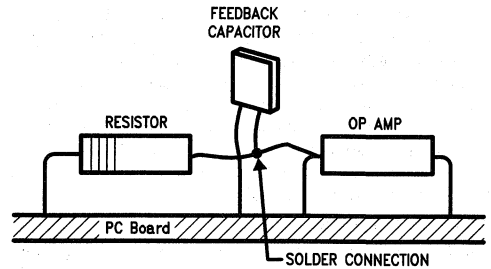


TL/H/8767–20

(d) Howland Current Pump

FIGURE 5. Guard Ring Connections

The designer should be aware that when it is inappropriate to lay out a PC board for the sake of just a few circuits, there is another technique which is even better than a guard ring on a PC board: Don't insert the amplifier's input pin into the board at all, but bend it up in the air and use only air as an insulator. Air is an excellent insulator. In this case you may have to forego some of the advantages of PC board construction, but the advantages are sometimes well worth the effort of using point-to-point up-in-the-air wiring. See *Figure 6*.



TL/H/8767–21

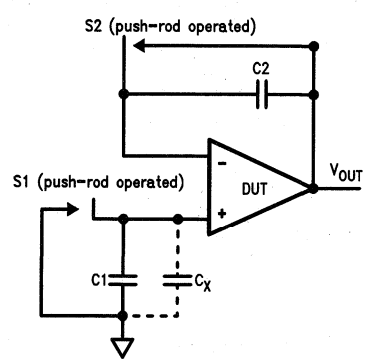
(Input pins are lifted out of PC board and soldered directly to components. All other pins connected to PC board.)

FIGURE 6. Air Wiring

BIAS CURRENT TESTING

The test method of *Figure 7* is appropriate for bench-testing bias current with reasonable accuracy. To understand its operation, first close switch S2 momentarily. When S2 is opened, then

$$I_b^- = \frac{dV_{OUT}}{dt} \times C2.$$



TL/H/8767–22

FIGURE 7. Simple Input Bias Current Test Circuit

A suitable capacitor for C2 would be a 5 pF or 10 pF silver mica, NPO ceramic, or air-dielectric. When determining the magnitude of I_b^-, the leakage of the capacitor and socket must be taken into account. Switch S2 should be left shorted most of the time, or else the dielectric absorption of the capacitor C2 could cause errors.

Similarly, if S1 is shorted momentarily (while leaving S2 shorted)

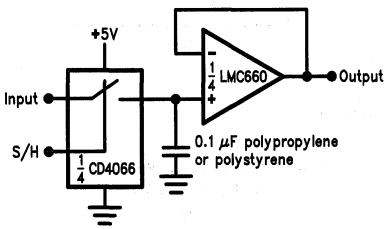
$$I_b^+ = \frac{dV_{OUT}}{dt} \times (C1 + C_X)$$

where C_X is the stray capacitance at the + input.

Typical Single-Supply Applications (V^+ = 5.0 VDC)

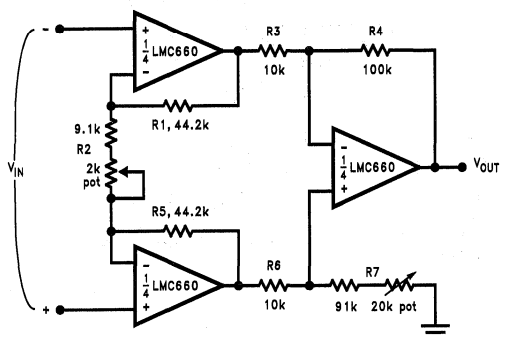
Additional single-supply applications ideas can be found in the LM324 datasheet. The LMC660 is pin-for-pin compatible with the LM324 and offers greater bandwidth and input resistance over the LM324. These features will improve the performance of many existing single-supply applications. Note, however, that the supply voltage range of the LMC660 is smaller than that of the LM324.

Low-Leakage Sample-and-Hold



TL/H/8767–7

Instrumentation Amplifier



TL/H/8767–8

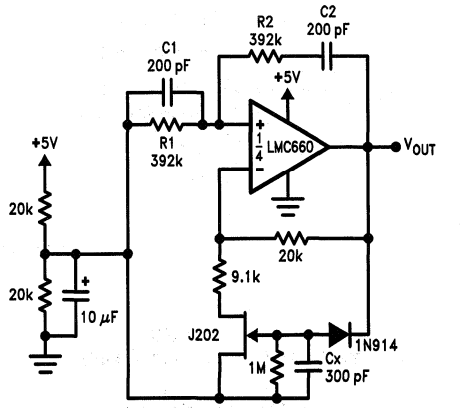
If R1 = R5, R3 = R6, and R4 = R7; then

$$\frac{V_{OUT}}{V_{IN}} = \frac{R2 + 2R1}{R2} \times \frac{R4}{R3}$$

$\therefore A_V \approx 100$ for circuit shown.

For good CMRR over temperature, low drift resistors should be used. Matching of R3 to R6 and R4 to R7 affect CMRR. Gain may be adjusted through R2. CMRR may be adjusted through R7.

Sine-Wave Oscillator



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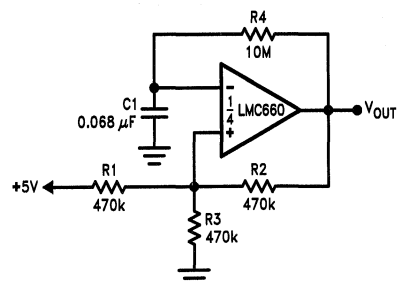
Oscillator frequency is determined by R1, R2, C1, and C2:

fosc = $1/2\pi RC$, where R = R1 = R2 and C = C1 = C2.

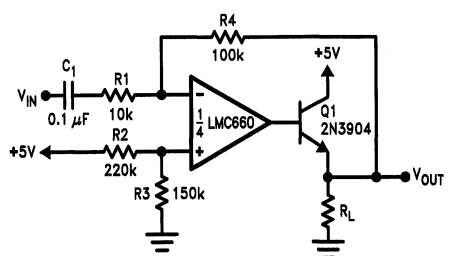
This circuit, as shown, oscillates at 2.0 kHz with a peak-to-peak output swing of 4.5V.

1 Hz Square-Wave Oscillator



TL/H/8767–10

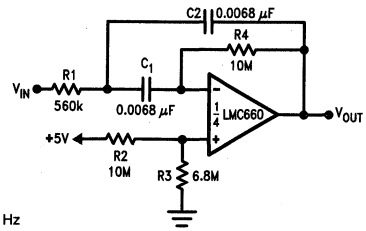
Power Amplifier



TL/H/8767–11

Typical Single-Supply Applications (V^+ = 5.0 VDC) (Continued)

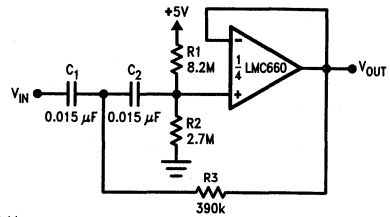
10 Hz Bandpass Filter



f_O = 10 Hz
Q = 2.1
Gain = −8.8

TL/H/8767–12

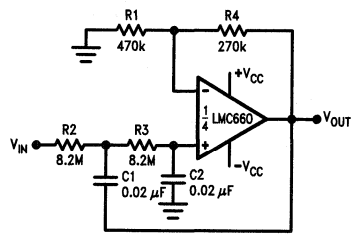
10 Hz High-Pass Filter



f_c = 10 Hz
d = 0.895
Gain = 1
2 dB passband ripple

TL/H/8767–13

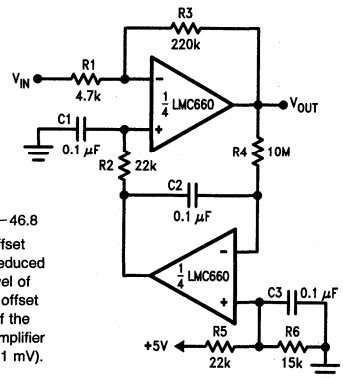
1 Hz Low-Pass Filter (Maximally Flat, Dual Supply Only)



f_c = 1 Hz
d = 1.414
Gain = 1.57

TL/H/8767–14

High Gain Amplifier with Offset Voltage Reduction



Gain = −46.8

Output offset voltage reduced to the level of the input offset voltage of the bottom amplifier (typically 1 mV).

TL/H/8767–15

National Semiconductor

LMC662
CMOS Dual Operational Amplifier

General Description

The LMC662 CMOS Dual operational amplifier is ideal for operation from a single supply. It operates from +5V to +15V and features rail-to-rail output swing in addition to an input common-mode range that includes ground. Performance limitations that have plagued CMOS amplifiers in the past are not a problem with this design. Input V_{OS}, drift, and broadband noise as well as voltage gain into realistic loads (2 kΩ and 600Ω) are all equal to or better than widely accepted bipolar equivalents.

This chip is built with National's advanced Double-Poly Silicon-Gate CMOS process.

See the LMC660 datasheet for a Quad CMOS operational amplifier with these same features.

Features

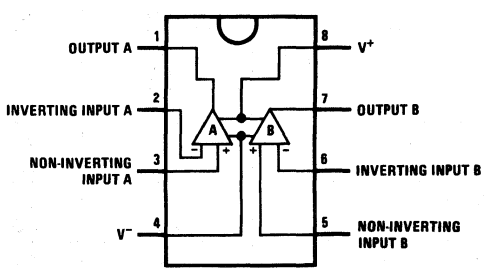
- Rail-to-rail output swing
- Specified for 2 kΩ and 600Ω loads
- High voltage gain 126 dB
- Low input offset voltage 3 mV
- Low offset voltage drift 1.3 μV/°C
- Ultra low input bias current 2 fA
- Input common-mode range includes V^-
- Operating range from +5V to +15V supply
- I_{SS} = 400 μA/amplifier; independent of V^+
- Low distortion 0.01% at 10 kHz
- Slew rate 1.1 V/μs
- Available in extended temperature range (−40°C to +125°C); ideal for automotive applications
- Available to a Standard Military Drawing specification

Applications

- High-impedance buffer or preamplifier
- Precision current-to-voltage converter
- Long-term integrator
- Sample-and-hold circuit
- Peak detector
- Medical instrumentation
- Industrial controls
- Automotive sensors

Connection Diagram

8-Pin DIP/SO



TL/H/9763–1

Ordering Information

Package	Temperature Range				NSC Drawing
	Military	Extended	Industrial	Commercial	
8-Pin Ceramic DIP	LMC662AMJ/883				J08A
8-Pin Small Outline		LMC662EM	LMC662AIM	LMC662CM	M08A
8-Pin Molded DIP		LMC662EN	LMC662AIN	LMC662CN	N08E
8-Pin Side Brazed Ceramic DIP	LMC662AMD				D08C

Absolute Maximum Ratings (Note 3)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Differential Input Voltage	±Supply Voltage
Supply Voltage ($V^+ - V^-$)	16V
Output Short Circuit to V^+	(Note 12)
Output Short Circuit to V^-	(Note 1)
Lead Temperature (Soldering, 10 sec.)	260°C
Storage Temp. Range	−65°C to +150°C
Voltage at Input/Output Pins	(V^+) +0.3V, (V^-) −0.3V
Current at Output Pin	±18 mA
Current at Input Pin	±5 mA
Current at Power Supply Pin	35 mA
Power Dissipation	(Note 2)
Junction Temperature	150°C
ESD Tolerance (Note 8)	500V

Operating Ratings (Note 3)

Temperature Range	
LMC662AMJ/883, LMC662AMD	$-55°C \le T_J \le +125°C$
LMC662AI	$-40°C \le T_J \le +85°C$
LMC662C	$0°C \le T_J \le +70°C$
LMC662E	$-40°C \le T_J \le +125°C$
Supply Voltage Range	4.75V to 15.5V
Power Dissipation	(Note 10)
Thermal Resistance (θ_{JA}) (Note 11)	
8-Pin Ceramic DIP	100°C/W
8-Pin Molded DIP	101°C/W
8-Pin SO	165°C/W
8-Pin Side Brazed Ceramic DIP	100°C/W

DC Electrical Characteristics

unless otherwise specified, all limits guaranteed for T_J = 25°C. **Boldface** limits apply at the temperature extremes. V^+ = 5V, V^- = 0V, V_{CM} = 1.5V, V_O = 2.5V and R_L > 1M unless otherwise specified.

Parameter	Conditions	Typ (Note 4)	LMC662AMJ/883 LMC662AMD	LMC662AI	LMC662C	LMC662E	Units
			Limit (Note 4, 9)	Limit (Note 4)	Limit (Note 4)	Limit (Note 4)	
Input Offset Voltage		1	3 **3.5**	3 **3.3**	6 **6.3**	6 **6.5**	mV max
Input Offset Voltage Average Drift		1.3					µV/°C
Input Bias Current		0.002	20 **100**	**4**	**2**	**60**	pA max
Input Offset Current		0.001	20 **100**	**2**	**1**	**60**	pA max
Input Resistance		>1					Teraohm
Common Mode Rejection Ratio	0V ≤ V_{CM} ≤ 12.0V V^+ = 15V	83	70 **68**	70 **68**	63 **62**	63 **60**	dB min
Positive Power Supply Rejection Ratio	5V ≤ V^+ ≤ 15V V_O = 2.5V	83	70 **68**	70 **68**	63 **62**	63 **60**	dB min
Negative Power Supply Rejection Ratio	0V ≤ V^- ≤ −10V	94	84 **82**	84 **83**	74 **73**	74 **70**	dB min
Input Common-Mode Voltage Range	V^+ = 5V & 15V For CMRR ≥ 50 dB	−0.4	−0.1 **0**	−0.1 **0**	−0.1 **0**	−0.1 **0**	V max
		$V^+ - 1.9$	$V^+ - 2.3$ $\mathbf{V^+ - 2.6}$	$V^+ - 2.3$ $\mathbf{V^+ - 2.5}$	$V^+ - 2.3$ $\mathbf{V^+ - 2.4}$	$V^+ - 2.3$ $\mathbf{V^+ - 2.6}$	V min
Large Signal Voltage Gain	R_L = 2 kohm (Note 5) Sourcing	2000	400 **300**	400 **440**	200 **300**	200 **100**	V/mV min
	Sinking	500	180 **70**	180 **120**	90 **80**	90 **40**	V/mV min
	R_L = 600ohm (Note 5) Sourcing	1000	200 **150**	200 **220**	100 **150**	100 **75**	V/mV min
	Sinking	250	100 **35**	100 **60**	50 **40**	50 **20**	V/mV min

DC Electrical Characteristics (Continued)

unless otherwise specified, all limits guaranteed for T_J = 25°C. **Boldface** limits apply at the temperature extremes. V^+ = 5V, V^- = 0V, V_{CM} = 1.5V, V_O = 2.5V and R_L > 1M unless otherwise specified.

Parameter	Conditions	Typ (Note 4)	LMC662AMJ/883 LMC662AMD	LMC662AI	LMC662C	LMC662E	Units
			Limit (Note 4, 9)	Limit (Note 4)	Limit (Note 4)	Limit (Note 4)	
Output Swing	V^+ = 5V R_L = 2 kΩ to $V^+/2$	4.87	4.82 **4.77**	4.82 **4.79**	4.78 **4.76**	4.78 **4.70**	V min
		0.10	0.15 **0.19**	0.15 **0.17**	0.19 **0.21**	0.19 **0.25**	V max
	V^+ = 5V R_L = 600Ω to $V^+/2$	4.61	4.41 **4.24**	4.41 **4.31**	4.27 **4.21**	4.27 **4.10**	V min
		0.30	0.50 **0.63**	0.50 **0.56**	0.63 **0.69**	0.63 **0.75**	V max
	V^+ = 15V R_L = 2 kΩ to $V^+/2$	14.63	14.50 **14.40**	14.50 **14.44**	14.37 **14.32**	14.37 **14.25**	V min
		0.26	0.35 **0.43**	0.35 **0.40**	0.44 **0.48**	0.44 **0.55**	V max
	V^+ = 15V R_L = 600Ω to $V^+/2$	13.90	13.35 **13.02**	13.35 **13.15**	12.92 **12.76**	12.92 **12.60**	V min
		0.79	1.16 **1.42**	1.16 **1.32**	1.45 **1.58**	1.45 **1.75**	V max
Output Current V^+ = 5V	Sourcing, V_O = 0V	22	16 **12**	16 **14**	13 **11**	13 **9**	mA min
	Sinking, V_O = 5V	21	16 **12**	16 **14**	13 **11**	13 **9**	mA min
Output Current V^+ = 15V	Sourcing, V_O = 0V	40	19 **19**	28 **25**	23 **21**	23 **15**	mA min
	Sinking, V_O = 13V (Note 12)	39	19 **19**	28 **24**	23 **20**	23 **15**	mA min
Supply Current	Both Amplifiers V_O = 1.5V	0.75	1.3 **1.8**	1.3 **1.5**	1.6 **1.8**	1.6 **1.9**	mA max

AC Electrical Characteristics

unless otherwise specified, all limits guaranteed for T_J = 25°C. **Boldface** limits apply at the temperature extremes. V^+ = 5V, V^- = 0V, V_{CM} = 1.5V, V_O = 2.5V and R_L > 1M unless otherwise specified.

Parameter	Conditions	Typ (Note 4)	LMC662AMJ/883 LMC662AMD	LMC662AI	LMC662C	LMC662E	Units
			Limit (Note 4, 9)	Limit (Note 4)	Limit (Note 4)	Limit (Note 4)	
Slew Rate	(Note 6)	1.1	0.8 **0.5**	0.8 **0.6**	0.8 **0.7**	0.8 **0.4**	V/μs min
Gain-Bandwidth Product		1.4	**0.5**				MHz
Phase Margin		50					Deg
Gain Margin		17					dB
Amp-to-Amp Isolation	(Note 7)	130					dB
Input-Referred Voltage Noise	F = 1 kHz	22					nV/$\sqrt{\text{Hz}}$
Input-Referred Current Noise	F = 1 kHz	0.0002					pA/$\sqrt{\text{Hz}}$
Total Harmonic Distortion	F = 10 kHz, A_V = −10 R_L = 2 kΩ, V_O = 8 V_{PP} V^+ = 15V	0.01					%

Note 1: Applies to both single-supply and split-supply operation. Continuous short circuit operation at elevated ambient temperature and/or multiple Op Amp shorts can result in exceeding the maximum allowed junction temperature of 150°C. Output currents in excess of ±30 mA over long term may adversely affect reliability.

Note 2: The maximum power dissipation is a function of $T_{J(max)}$, θ_{JA}, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(max)}-T_A)/\theta_{JA}$.

Note 3: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed.

Note 4: Typical values represent the most likely parametric norm. Limits are guaranteed by testing or correlation.

Note 5: V^+ = 15V, V_{CM} = 7.5V and R_L connected to 7.5V. For Sourcing tests, 7.5V ≤ V_O ≤ 11.5V. For Sinking tests, 2.5V ≤ V_O ≤ 7.5V.

Note 6: V^+ = 15V. Connected as Voltage Follower with 10V step input. Number specified is the slower of the positive and negative slew rates.

Note 7: Input referred. V^+ = 15V and R_L = 10 kΩ connected to $V^+/2$. Each amp excited in turn with 1 kHz to produce V_O = 13 V_{PP}.

Note 8: Human body model, 1.5 kΩ in series with 100 pF.

Note 9: A military RETS electrical test specification is available on request. At the time of printing, the LMC662AMJ/883 RETS spec complied fully with the boldface limits in this column. The LMC662AMJ/883 may also be procured to a Standard Military Drawing specification.

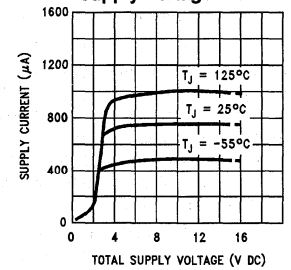
Note 10: For operating at elevated temperatures the device must be derated based on the thermal resistance θ_{JA} with $P_D = (T_J-T_A)/\theta_{JA}$.

Note 11: All numbers apply for packages soldered directly into a PC board.

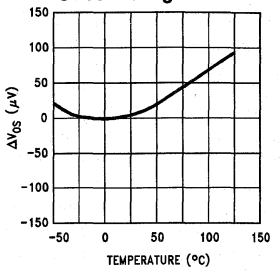
Note 12: Do not connect output to V^+ when V^+ is greater than 13V or reliability may be adversely affected.

Typical Performance Characteristics $V_S = \pm 7.5V$, $T_A = 25°C$ unless otherwise specified

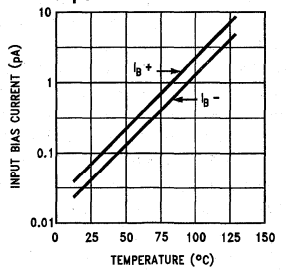
Supply Current vs Supply Voltage



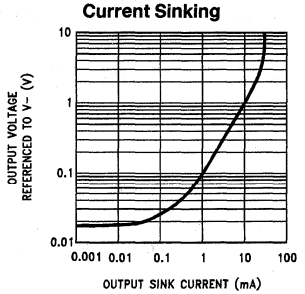
Offset Voltage



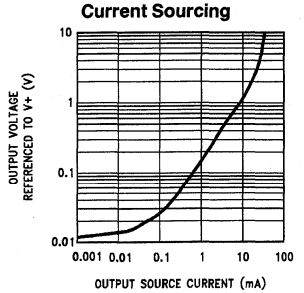
Input Bias Current



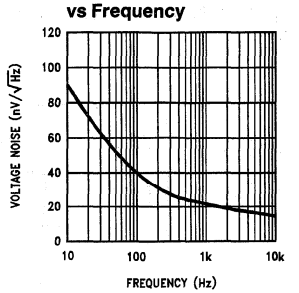
Output Characteristics Current Sinking



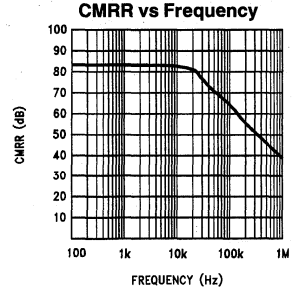
Output Characteristics Current Sourcing



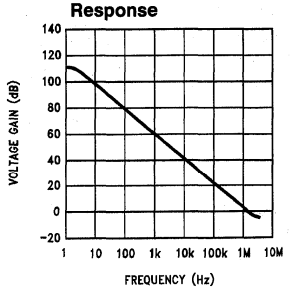
Input Voltage Noise vs Frequency



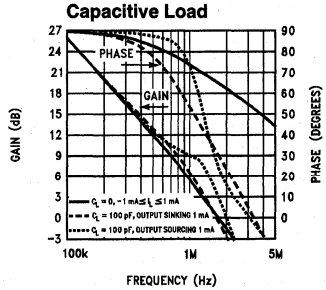
CMRR vs Frequency



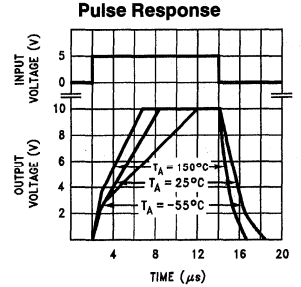
Open-Loop Frequency Response



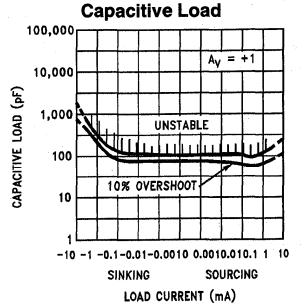
Frequency Response vs Capacitive Load



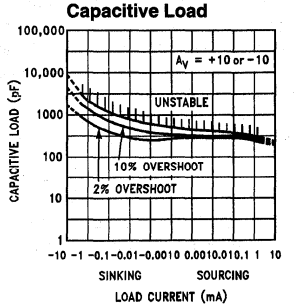
Non-Inverting Large Signal Pulse Response



Stability vs Capacitive Load



Stability vs Capacitive Load



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Note: Avoid resistive loads of less than 500Ω, as they may cause instability.

Note: Avoid resistive loads of less than 500Ω, as they may cause instability.

Application Hints

AMPLIFIER TOPOLOGY

The topology chosen for the LMC662, shown in *Figure 1*, is unconventional (compared to general-purpose op amps) in that the traditional unity-gain buffer output stage is not used; instead, the output is taken directly from the output of the integrator, to allow rail-to-rail output swing. Since the buffer traditionally delivers the power to the load, while maintaining high op amp gain and stability, and must withstand shorts to either rail, these tasks now fall to the integrator.

As a result of these demands, the integrator is a compound affair with an embedded gain stage that is doubly fed forward (via C_f and C_{ff}) by a dedicated unity-gain compensation driver. In addition, the output portion of the integrator is a push-pull configuration for delivering heavy loads. While sinking current the whole amplifier path consists of three gain stages with one stage fed forward, whereas while sourcing the path contains four gain stages with two fed forward.

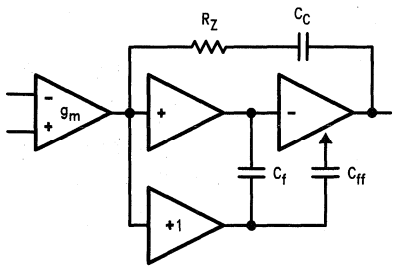

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FIGURE 1. LMC662 Circuit Topology (Each Amplifier)

The large signal voltage gain while sourcing is comparable to traditional bipolar op amps, even with a 600Ω load. The gain while sinking is higher than most CMOS op amps, due to the additional gain stage; however, under heavy load (600Ω) the gain will be reduced as indicated in the Electrical Characteristics.

COMPENSATING INPUT CAPACITANCE

The high input resistance of the LMC662 op amps allows the use of large feedback and source resistor values without losing gain accuracy due to loading. However, the circuit will be especially sensitive to its layout when these large-value resistors are used.

Every amplifier has some capacitance between each input and AC ground, and also some differential capacitance between the inputs. When the feedback network around an amplifier is resistive, this input capacitance (along with any additional capacitance due to circuit board traces, the socket, etc.) and the feedback resistors create a pole in the feedback path. In the following General Operational Amplifier Circuit, *Figure 2*, the frequency of this pole is

$$f_p = \frac{1}{2\pi C_S R_P}$$

where C_S is the total capacitance at the inverting input, including amplifier input capacitance and any stray capacitance from the IC socket (if one is used), circuit board traces, etc., and R_P is the parallel combination of R_F and R_{IN}. This formula, as well as all formulae derived below, apply to inverting and non-inverting op-amp configurations.

When the feedback resistors are smaller than a few kΩ, the frequency of the feedback pole will be quite high, since C_S is generally less than 10 pF. If the frequency of the feedback pole is much higher than the "ideal" closed-loop bandwidth (the nominal closed-loop bandwidth in the absence of C_S), the pole will have a negligible effect on stability, as it will add only a small amount of phase shift.

However, if the feedback pole is less than approximately 6 to 10 times the "ideal" −3 dB frequency, a feedback capacitor, C_F, should be connected between the output and the inverting input of the op amp. This condition can also be stated in terms of the amplifier's low-frequency noise gain: To maintain stability, a feedback capacitor will probably be needed if

$$\left(\frac{R_F}{R_{IN}} + 1\right) \leq \sqrt{6 \times 2\pi \times GBW \times R_F \times C_S}$$

where

$$\left(\frac{R_F}{R_{IN}} + 1\right)$$

is the amplifier's low-frequency noise gain and GBW is the amplifier's gain bandwidth product. An amplifier's low-frequency noise gain is represented by the formula

$$\left(\frac{R_F}{R_{IN}} + 1\right)$$

regardless of whether the amplifier is being used in an inverting or non-inverting mode. Note that a feedback capacitor is more likely to be needed when the noise gain is low and/or the feedback resistor is large.

If the above condition is met (indicating a feedback capacitor will probably be needed), and the noise gain is large enough that:

$$\left(\frac{R_F}{R_{IN}} + 1\right) \geq 2\sqrt{GBW \times R_F \times C_S}\,,$$

the following value of feedback capacitor is recommended:

$$C_F = \frac{C_S}{2\left(\frac{R_F}{R_{IN}} + 1\right)}$$

If

$$\left(\frac{R_F}{R_{IN}} + 1\right) < 2\sqrt{GBW \times R_F \times C_S}\,,$$

the feedback capacitor should be:

$$C_F = \sqrt{\frac{C_S}{GBW \times R_F}}$$

Note that these capacitor values are usually significantly smaller than those given by the older, more conservative formula:

$$C_F = \frac{C_S R_{IN}}{R_F}.$$

Application Hints (Continued)

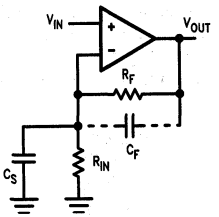

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FIGURE 2. General Operational Amplifier Circuit

C_S consists of the amplifier's input capacitance plus any stray capacitance from the circuit board and socket. C_F compensates for the pole caused by C_S and the feedback resistor.

Using the smaller capacitors will give much higher bandwidth with little degradation of transient response. It may be necessary in any of the above cases to use a somewhat larger feedback capacitor to allow for unexpected stray capacitance, or to tolerate additional phase shifts in the loop, or excessive capacitive load, or to decrease the noise or bandwidth, or simply because the particular circuit implementation needs more feedback capacitance to be sufficiently stable. For example, a printed circuit board's stray capacitance may be larger or smaller than the breadboard's, so the actual optimum value for C_F may be different from the one estimated using the breadboard. In most cases, the value of C_F should be checked on the actual circuit, starting with the computed value.

CAPACITIVE LOAD TOLERANCE

Like many other op amps, the LMC662 may oscillate when its applied load appears capacitive. The threshold of oscillation varies both with load and circuit gain. The configuration most sensitive to oscillation is a unity-gain follower. See the Typical Performance Characteristics.

The load capacitance interacts with the op amp's output resistance to create an additional pole. If this pole frequency is sufficiently low, it will degrade the op amp's phase margin so that the amplifier is no longer stable at low gains. As shown in *Figure 3a*, the addition of a small resistor (50Ω to 100Ω) in series with the op amp's output, and a capacitor (5 pF to 10 pF) from inverting input to output pins, returns the phase margin to a safe value without interfering with lower-frequency circuit operation. Thus, larger values of capacitance can be tolerated without oscillation. Note that in all cases, the output will ring heavily when the load capacitance is near the threshold for oscillation.

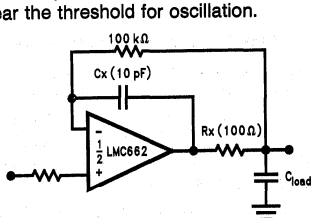

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FIGURE 3a. Rx, Cx Improve Capacitive Load Tolerance

Capacitive load driving capability is enhanced by using a pull up resistor to V^+ *(Figure 3b)*. Typically a pull up resistor conducting 500 μA or more will significantly improve capacitive load responses. The value of the pull up resistor must be determined based on the current sinking capability of the amplifier with respect to the desired output swing. Open loop gain of the amplifier can also be affected by the pull up resistor (see Electrical Characteristics).

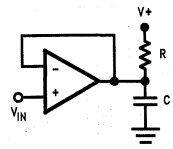

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FIGURE 3b. Compensating for Large Capacitive Loads with a Pull Up Resistor

PRINTED-CIRCUIT-BOARD LAYOUT FOR HIGH-IMPEDANCE WORK

It is generally recognized that any circuit which must operate with less than 1000 pA of leakage current requires special layout of the PC board. When one wishes to take advantage of the ultra-low bias current of the LMC662, typically less than 0.04 pA, it is essential to have an excellent layout. Fortunately, the techniques for obtaining low leakages are quite simple. First, the user must not ignore the surface leakage of the PC board, even though it may sometimes appear acceptably low, because under conditions of high humidity or dust or contamination, the surface leakage will be appreciable.

To minimize the effect of any surface leakage, lay out a ring of foil completely surrounding the LMC662's inputs and the terminals of capacitors, diodes, conductors, resistors, relay terminals, etc. connected to the op-amp's inputs. See *Figure 4*. To have a significant effect, guard rings should be placed on both the top and bottom of the PC board. This PC foil must then be connected to a voltage which is at the same voltage as the amplifier inputs, since no leakage current can flow between two points at the same potential. For example, a PC board trace-to-pad resistance of $10^{12}\Omega$, which is normally considered a very large resistance, could leak 5 pA if the trace were a 5V bus adjacent to the pad of an input. This would cause a 100 times degradation from the LMC662's actual performance. However, if a guard ring is held within 5 mV of the inputs, then even a resistance of $10^{11}\Omega$ would cause only 0.05 pA of leakage current, or perhaps a minor (2:1) degradation of the amplifier's performance. See *Figures 5a, 5b, 5c* for typical connections of guard rings for standard op-amp configurations. If both inputs are active and at high impedance, the guard can be tied to ground and still provide some protection; see *Figure 5d*.

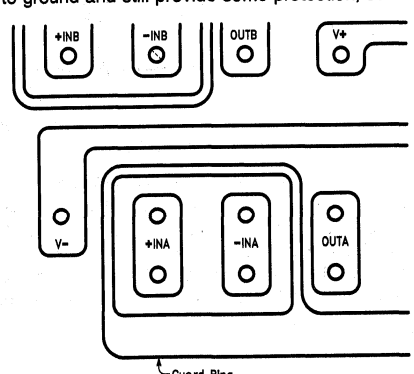

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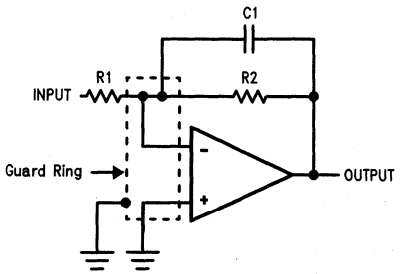
FIGURE 4. Example, using the LMC660, of Guard Ring in P.C. Board Layout

Application Hints (Continued)



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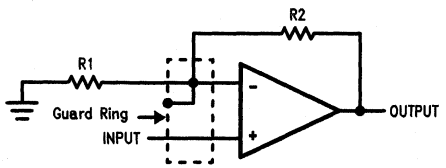
(a) Inverting Amplifier



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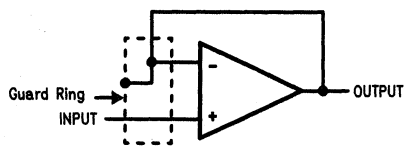
(b) Non-Inverting Amplifier



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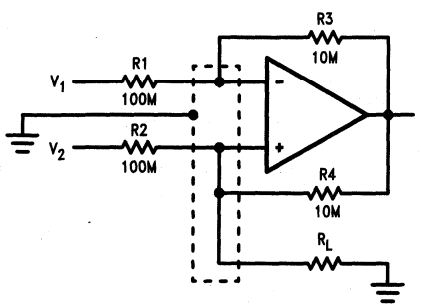
(c) Follower



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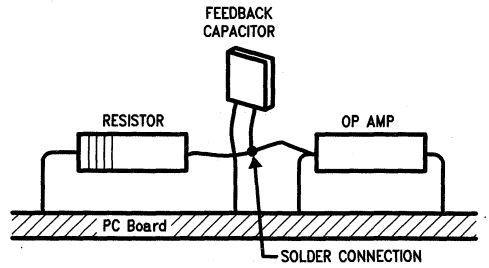
(d) Howland Current Pump

FIGURE 5. Guard Ring Connections

The designer should be aware that when it is inappropriate to lay out a PC board for the sake of just a few circuits, there is another technique which is even better than a guard ring on a PC board: Don't insert the amplifier's input pin into the board at all, but bend it up in the air and use only air as an insulator. Air is an excellent insulator. In this case you may have to forego some of the advantages of PC board construction, but the advantages are sometimes well worth the effort of using point-to-point up-in-the-air wiring. See *Figure 6*.



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(Input pins are lifted out of PC board and soldered directly to components. All other pins connected to PC board.)

FIGURE 6. Air Wiring

BIAS CURRENT TESTING

The test method of *Figure 7* is appropriate for bench-testing bias current with reasonable accuracy. To understand its operation, first close switch S2 momentarily. When S2 is opened, then

$$I_b^- = \frac{dV_{OUT}}{dt} \times C2.$$

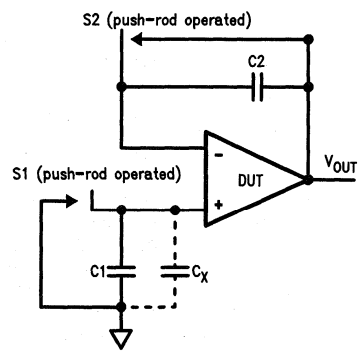

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FIGURE 7. Simple Input Bias Current Test Circuit

A suitable capacitor for C2 would be a 5 pF or 10 pF silver mica, NPO ceramic, or air-dielectric. When determining the magnitude of I_b^-, the leakage of the capacitor and socket must be taken into account. Switch S2 should be left shorted most of the time, or else the dielectric absorption of the capacitor C2 could cause errors.

Similarly, if S1 is shorted momentarily (while leaving S2 shorted)

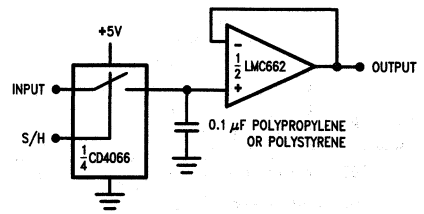
$$I_b^+ = \frac{dV_{OUT}}{dt} \times (C1 + C_X)$$

where C_X is the stray capacitance at the + input.

Typical Single-Supply Applications ($V^+ = 5.0\ V_{DC}$)

Additional single-supply applications ideas can be found in the LM358 datasheet. The LMC662 is pin-for-pin compatible with the LM358 and offers greater bandwidth and input resistance over the LM358. These features will improve the performance of many existing single-supply applications. Note, however, that the supply voltage range of the LM662 is smaller than that of the LM358.

Low-Leakage Sample-and-Hold



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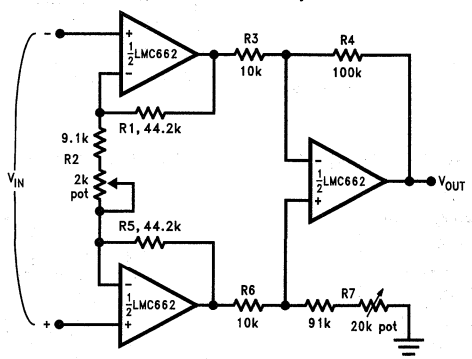
Instrumentation Amplifier



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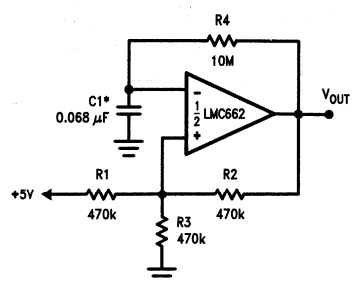
If $R_1 = R_5$, $R_3 = R_6$, and $R_4 = R_7$; then

$$\frac{V_{OUT}}{V_{IN}} = \frac{R2 + 2R1}{R2} \times \frac{R4}{R3}$$

$\therefore A_V \approx 100$ for circuit shown.

For good CMRR over temperature, low drift resistors should be used. Matching of R3 to R6 and R4 to R7 affects CMRR. Gain may be adjusted through R2. CMRR may be adjusted through R7.

1 Hz Square-Wave Oscillator



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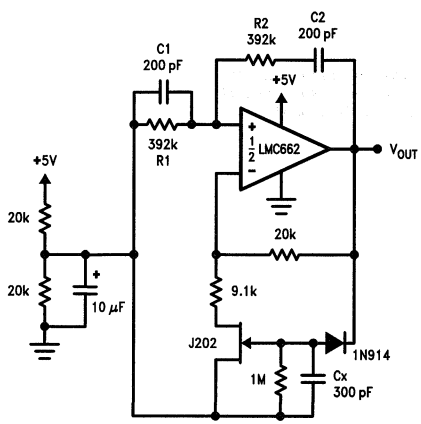
Sine-Wave Oscillator



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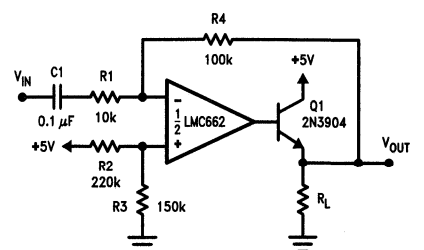
Oscillator frequency is determined by R1, R2, C1, and C2:

$$f_{OSC} = 1/2\pi RC$$

where R = R1 = R2 and C = C1 = C2.

This circuit, as shown, oscillates at 2.0 kHz with a peak-to-peak output swing of 4.5V

Power Amplifier



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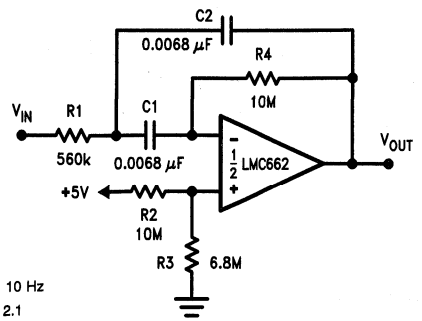
Typical Single-Supply Applications (V^+ = 5.0 V_{DC}) (Continued)

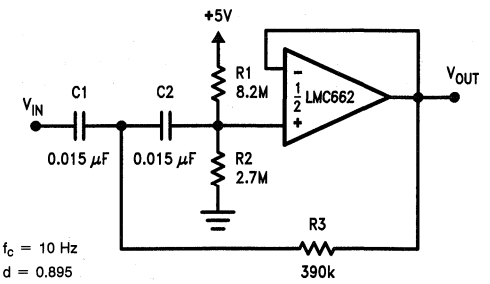
10 Hz Bandpass Filter



f_O = 10 Hz
Q = 2.1
Gain = −8.8

TL/H/9763–11

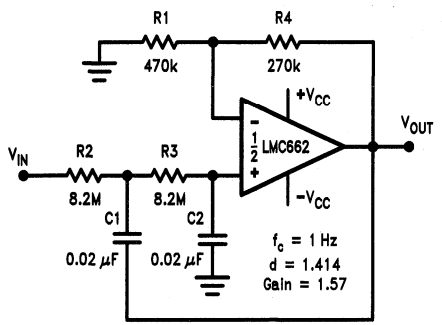
10 Hz High-Pass Filter



f_c = 10 Hz
d = 0.895
Gain = 1
2 dB passband ripple

TL/H/9763–12

1 Hz Low-Pass Filter (Maximally Flat, Dual Supply Only)



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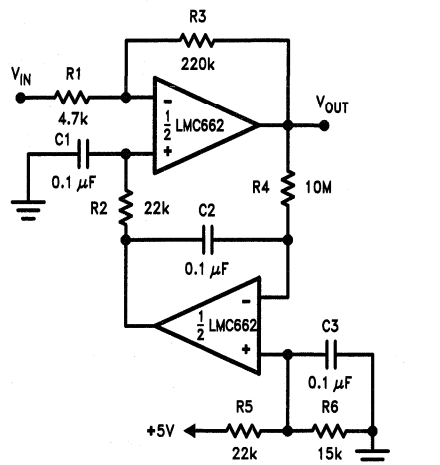
High Gain Amplifier with Offset Voltage Reduction



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Gain = −46.8

Output offset voltage reduced to the level of the input offset voltage of the bottom amplifier (typically 1 mV).

National Semiconductor

LMC6022
Low Power CMOS Dual Operational Amplifier

General Description

The LMC6022 is a CMOS dual operational amplifier which can operate from either a single supply or dual supplies. Its performance features include an input common-mode range that reaches V⁻, low input bias current, and voltage gain (into 100k and 5 kΩ loads) that is equal to or better than widely accepted bipolar equivalents, while the power supply requirement is less than 0.5 mW.

This chip is built with National's advanced Double-Poly Silicon-Gate CMOS process.

See the LMC6024 datasheet for a CMOS quad operational amplifier with these same features.

Features

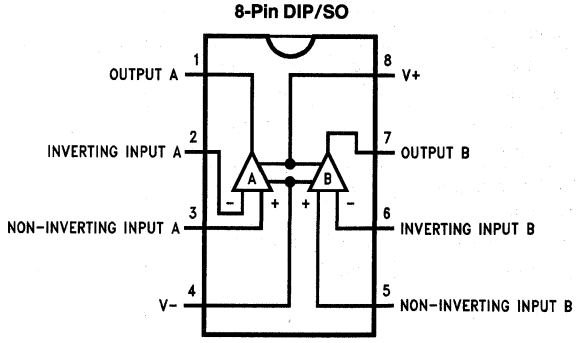
- Specified for 100 kΩ and 5 kΩ loads
- High voltage gain 120 dB
- Low offset voltage drift 2.5 μV/°C
- Ultra low input bias current 40 fA
- Input common-mode range includes V⁻
- Operating range from +5V to +15V supply
- Low distortion 0.01% at 1 kHz
- Slew rate 0.11 V/μs
- Micropower operation 0.5 mW

Applications

- High-impedance buffer or preamplifier
- Current-to-voltage converter
- Long-term integrator
- Sample-and-hold circuit
- Peak detector
- Medical instrumentation
- Industrial controls

Connection Diagram

8-Pin DIP/SO



TL/H/11236-1

Top View

Ordering Information

Temperature Range Industrial $-40°C \leq T_J \leq +85°C$	Package	NSC Drawing
LMC6022IN	8-Pin Molded DIP	N08E
LMC6022IM	8-Pin Small Outline	M08A

Absolute Maximum Ratings (Note 1)

Differential Input Voltage	±Supply Voltage
Supply Voltage ($V^+ - V^-$)	16V
Lead Temperature (Soldering, 10 sec.)	260°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature	150°C
ESD Tolerance (Note 4)	500V
Voltage at Output/Input Pin	(V^+) +0.3V, (V^-) −0.3V
Current at Output Pin	±18 mA
Current at Power Supply Pin	35 mA
Power Dissipation	(Note 3)
Current at Input Pin	±5 mA
Output Short Circuit to V^-	(Note 2)
Output Short Circuit to V^+	(Note 12)

Operating Ratings

Temperature Range	$-40°C \le T_J \le +85°C$
Supply Voltage Range	4.75V to 15.5V
Power Dissipation	(Note 10)
Thermal Resistance (θ_{JA}), (Note 11)	
8-Pin DIP	101°C/W
8-Pin SO	165°C/W

DC Electrical Characteristics

The following specifications apply for $V^+ = 5V$, $V^- = 0V$, $V_{CM} = 1.5V$, $V_O = 2.5V$, and $R_L = 1M$ unless otherwise noted. **Boldface** limits apply at the temperature extremes; all other limits $T_J = 25°C$.

Symbol	Parameter	Conditions	Typical (Note 5)	LMC6022I Limit (Note 6)	Units
V_{OS}	Input Offset Voltage		1	9 **11**	mV max
$\Delta V_{OS}/\Delta T$	Input Offset Voltage Average Drift		2.5		μV/°C
I_B	Input Bias Current		0.04	 **200**	pA max
I_{OS}	Input Offset Current		0.01	 **100**	pA max
R_{IN}	Input Resistance		>1		TeraΩ
CMRR	Common Mode Rejection Ratio	$0V \le V_{CM} \le 12V$ $V^+ = 15V$	83	63 **61**	dB min
+PSRR	Positive Power Supply Rejection Ratio	$5V \le V^+ \le 15V$	83	63 **61**	dB min
−PSRR	Negative Power Supply Rejection Ratio	$0V \le V^- \le -10V$	94	74 **73**	dB min
V_{CM}	Input Common-Mode Voltage Range	$V^+ = 5V$ & 15V For CMRR ≥ 50 dB	−0.4	−0.1 **0**	V max
			$V^+ - 1.9$	$V^+ - 2.3$ $\mathbf{V^+ - 2.5}$	V min
A_V	Large Signal Voltage Gain	$R_L = 100 k\Omega$ (Note 7) Sourcing	1000	200 **100**	V/mV min
		Sinking	500	90 **40**	V/mV min
		$R_L = 5 k\Omega$ (Note 7) Sourcing	1000	100 **75**	V/mV min
		Sinking	250	50 **20**	V/mV min

DC Electrical Characteristics (Continued)

The following specifications apply for $V^+ = 5V$, $V^- = 0V$, $V_{CM} = 1.5V$, $V_O = 2.5V$, and $R_L = 1M$ unless otherwise noted. **Boldface** limits apply at the temperature extremes; all other limits $T_J = 25°C$.

Symbol	Parameter	Conditions	Typical (Note 5)	LMC6022I Limit (Note 6)	Units
V_O	Output Voltage Swing	$V^+ = 5V$ $R_L = 100\ k\Omega$ to 2.5V	4.987	4.40 **4.43**	V min
			0.004	0.06 **0.09**	V max
		$V^+ = 5V$ $R_L = 5\ k\Omega$ to 2.5V	4.940	4.20 **4.00**	V min
			0.040	0.25 **0.35**	V max
		$V^+ = 15V$ $R_L = 100\ k\Omega$ to 7.5V	14.970	14.00 **13.90**	V min
			0.007	0.06 **0.09**	V max
		$V^+ = 15V$ $R_L = 5\ k\Omega$ to 7.5V	14.840	13.70 **13.50**	V min
			0.110	0.32 **0.40**	V max
I_O	Output Current	$V^+ = 5V$ Sourcing, $V_O = 0V$	22	13 **9**	mA min
		Sinking, $V_O = 5V$ (Note 2)	21	13 **9**	mA min
		$V^+ = 15V$ Sourcing, $V_O = 0V$	40	23 **15**	mA min
		Sinking, $V_O = 13V$ (Note 12)	39	23 **15**	mA min
I_S	Supply Current	Both Amplifiers $V_O = 1.5V$	86	140 **165**	μA max

AC Electrical Characteristics

The following specifications apply for $V^+ = 5V$, $V^- = 0V$, $V_{CM} = 1.5V$, $V_O = 2.5V$, and $R_L = 1M$ unless other otherwise noted. **Boldface** limits apply at the temperature extremes; all other limits $T_J = 25°C$.

Symbol	Parameter	Conditions	Typical (Note 5)	LMC6022I Limit (Note 6)	Units
SR	Slew Rate	(Note 8)	0.11	0.05 **0.03**	V/μs min
GBW	Gain-Bandwidth Product		0.35		MHz
ϕ_M	Phase Margin		50		Deg
G_M	Gain Margin		17		dB
	Amp-to-Amp Isolation	(Note 9)	130		dB
e_n	Input-Referred Voltage Noise	F = 1 kHz	42		nV/$\sqrt{Hz}$
i_n	Input-Referred Current Noise	F = 1 kHz	0.0002		pA/$\sqrt{Hz}$

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to component may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed.

Note 2: Applies to both single-supply and split-supply operation. Continuous short circuit operation at elevated ambient temperature and/or multiple Op Amp shorts can result in exceeding the maximum allowed junction temperature of 150°C. Output currents in excess of ±30 mA over long term may adversely affect reliability.

Note 3: The maximum power dissipation is a function of $T_{J(max)}$, θ_{JA} and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(max)} - T_A)/\theta_{JA}$.

Note 4: Human body model, 100 pF discharged through a 1.5 kΩ resistor.

Note 5: Typical values represent the most likely parametric norm.

Note 6: All limits are guaranteed by testing or correlation.

Note 7: $V^+ = 15V$, $V_{CM} = 7.5V$, and R_L connected to 7.5V. For Sourcing tests, $7.5V \le V_O \le 11.5V$. For Sinking tests, $2.5V \le V_O \le 7.5V$.

Note 8: $V^+ = 15V$. Connected as Voltage Follower with 10V step input. Number specified is the slower of the positive and negative slew rates.

Note 9: Input referred. $V^+ = 15V$ and $R_L = 100$ kΩ connected to 7.5V. Each amp excited in turn with 1 kHz to produce $V_O = 13\ V_{PP}$.

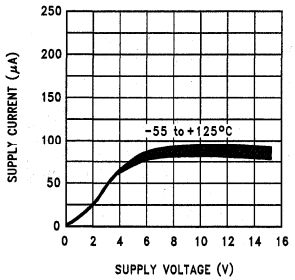
Note 10: For operating at elevated temperatures the device must be derated based on the thermal resistance θ_{JA} with $P_D = (T_J - T_A)/\theta_{JA}$.

Note 11: All numbers apply for packages soldered directly into a PC board.

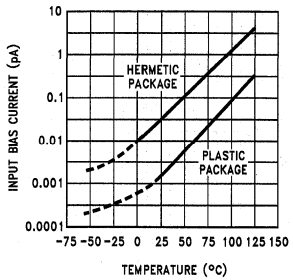
Note 12: Do not connect output to V^+ when V^+ is greater than 13V or reliability may be adversely affected.

Typical Performance Characteristics $V_S = \pm 7.5V$, $T_A = 25°C$ unless otherwise specified

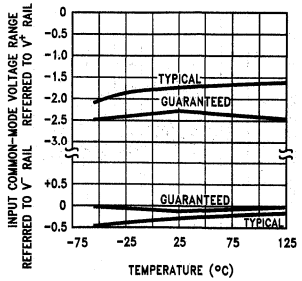
Supply Current vs Supply Voltage



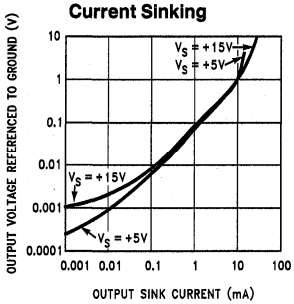
Input Bias Current vs Temperature



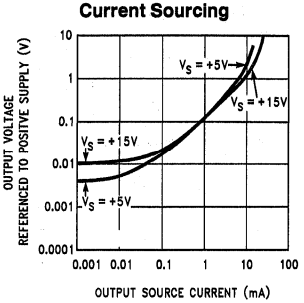
Input Common-Mode Voltage Range vs Temperature



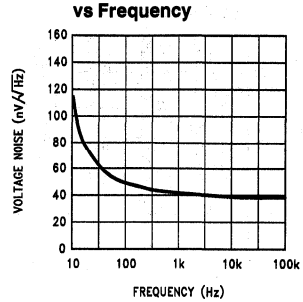
Output Characteristics Current Sinking



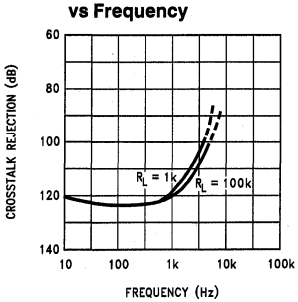
Output Characteristics Current Sourcing



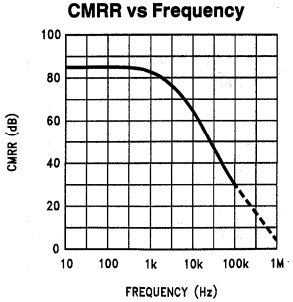
Input Voltage Noise vs Frequency



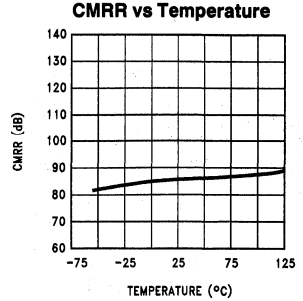
Crosstalk Rejection vs Frequency



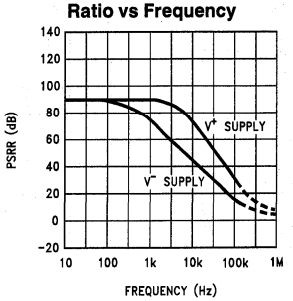
CMRR vs Frequency



CMRR vs Temperature



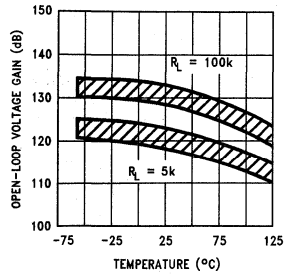
Power Supply Rejection Ratio vs Frequency



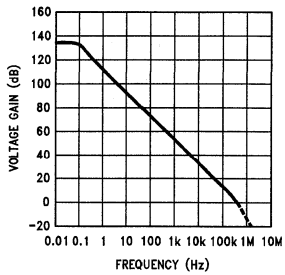
TL/H/11236–2

Typical Performance Characteristics $V_S = \pm 7.5V$, $T_A = 25°C$ unless otherwise specified (Continued)

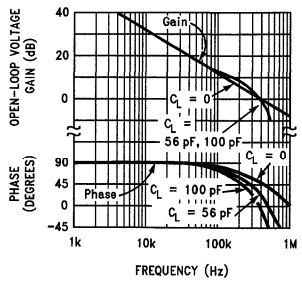
Open-Loop Voltage Gain vs Temperature



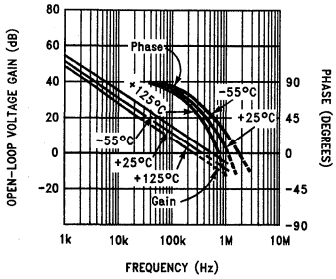
Open-Loop Frequency Response



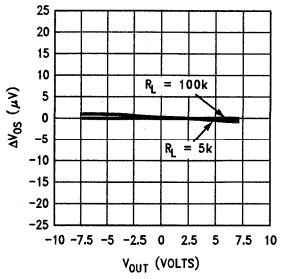
Gain and Phase Responses vs Load Capacitance



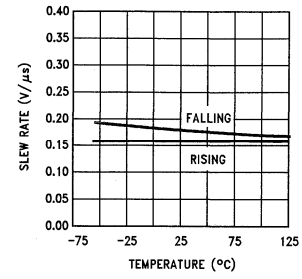
Gain and Phase Responses vs Temperature



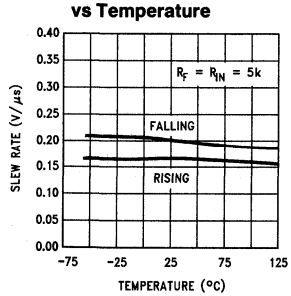
Gain Error (V_{OS} vs V_{OUT})



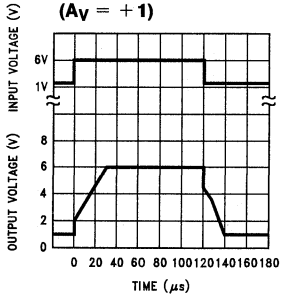
Non-Inverting Slew Rate vs Temperature



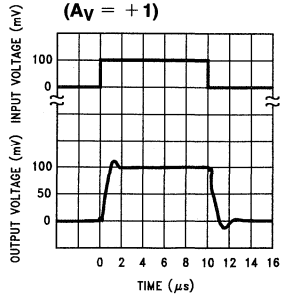
Inverting Slew Rate vs Temperature



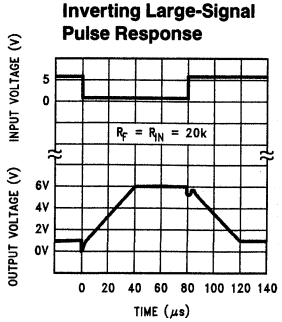
Large-Signal Pulse Non-Inverting Response ($A_V = +1$)



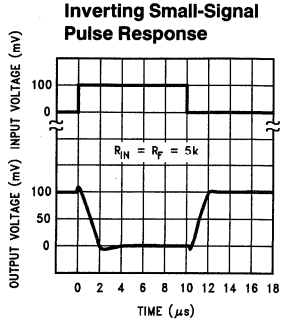
Non-Inverting Small Signal Pulse Response ($A_V = +1$)



Inverting Large-Signal Pulse Response



Inverting Small-Signal Pulse Response



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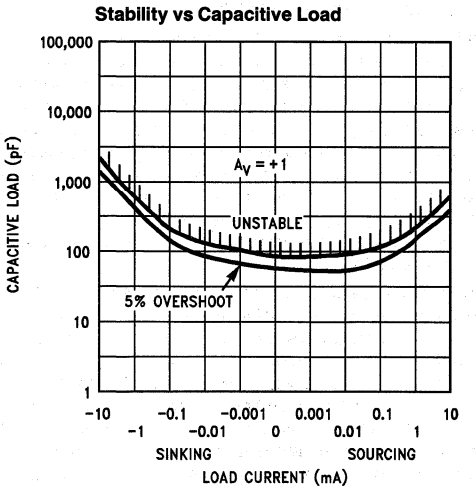
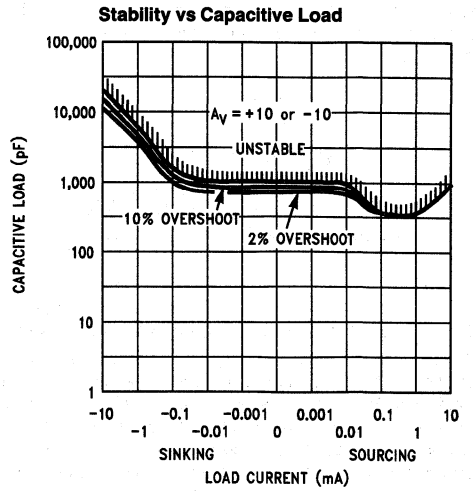
Typical Performance Characteristics $V_S = \pm 7.5V$, $T_A = 25°C$ (Continued)



TL/H/11236–4



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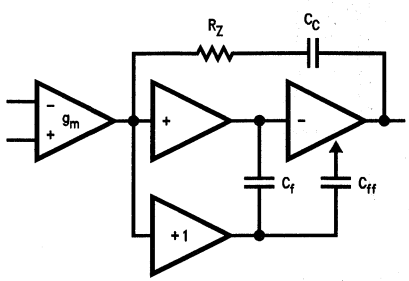
Note: Avoid resistive loads of less than 500Ω, as they may cause instability.

Application Hints

AMPLIFIER TOPOLOGY

The topology chosen for the LMC6022 is unconventional (compared to general-purpose op amps) in that the traditional unity-gain buffer output stage is not used; instead, the output is taken directly from the output of the integrator, to allow rail-to-rail output swing. Since the buffer traditionally delivers the power to the load, while maintaining high op amp gain and stability, and must withstand shorts to either rail, these tasks now fall to the integrator.

As a result of these demands, the integrator is a compound affair with an embedded gain stage that is doubly fed forward (via C_f and C_{ff}) by a dedicated unity-gain compensation driver. In addition, the output portion of the integrator is a push-pull configuration for delivering heavy loads. While sinking current the whole amplifier path consists of three gain stages with one stage fed forward, whereas while sourcing the path contains four gain stages with two fed forward.



TL/H/11236–6

FIGURE 1. LMC6022 Circuit Topology (Each Amplifier)

The large signal voltage gain while sourcing is comparable to traditional bipolar op amps for load resistance of at least 5 kΩ. The gain while sinking is higher than most CMOS op amps, due to the additional gain stage; however, when driving load resistance of 5 kΩ or less, the gain will be reduced as indicated in the Electrical Characteristics. The op amp can drive load resistance as low as 500Ω without instability.

COMPENSATING INPUT CAPACITANCE

Refer to the LMC660 or LMC662 datasheets to determine whether or not a feedback capacitor will be necessary for compensation and what the value of that capacitor would be.

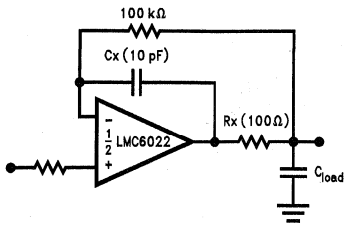
CAPACITIVE LOAD TOLERANCE

Like many other op amps, the LMC6022 may oscillate when its applied load appears capacitive. The threshold of oscillation varies both with load and circuit gain. The configuration most sensitive to oscillation is a unity-gain follower. See the Typical Performance Characteristics.

The load capacitance interacts with the op amp's output resistance to create an additional pole. If this pole frequency is sufficiently low, it will degrade the op amp's phase margin so that the amplifier is no longer stable at low gains. The addition of a small resistor (50Ω to 100Ω) in series with the op amp's output, and a capacitor (5 pF to 10 pF) from inverting input to output pins, returns the phase margin to a safe value without interfering with lower-frequency circuit

Application Hints (Continued)

operation. Thus, larger values of capacitance can be tolerated without oscillation. Note that in all cases, the output will ring heavily when the load capacitance is near the threshold for oscillation.



TL/H/11236–7

FIGURE 2a. Rx, Cx Improve Capacitive Load Tolerance

Capacitive load driving capability is enhanced by using a pull up resistor to V^+ (*Figure 2b*). Typically a pull up resistor conducting 50 μA or more will significantly improve capacitive load responses. The value of the pull up resistor must be determined based on the current sinking capability of the amplifier with respect to the desired output swing. Open loop gain of the amplifier can also be affected by the pull up resistor (see Electrical Characteristics).

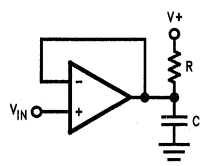


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FIGURE 2b. Compensating for Large Capacitive Loads with a Pull Up Resistor

PRINTED-CIRCUIT-BOARD LAYOUT FOR HIGH-IMPEDANCE WORK

It is generally recognized that any circuit which must operate with less than 1000 pA of leakage current requires special layout of the PC board. When one wishes to take advantage of the ultra-low bias current of the LMC6022, typically less than 0.04 pA, it is essential to have an excellent layout. Fortunately, the techniques for obtaining low leakages are quite simple. First, the user must not ignore the surface leakage of the PC board, even though it may sometimes appear acceptably low, because under conditions of high humidity or dust or contamination, the surface leakage will be appreciable.

To minimize the effect of any surface leakage, lay out a ring of foil completely surrounding the LMC6022's inputs and the terminals of capacitors, diodes, conductors, resistors, relay terminals, etc. connected to the op-amp's inputs. See *Figure 3*. To have a significant effect, guard rings should be placed on both the top and bottom of the PC board. This PC foil must then be connected to a voltage which is at the same voltage as the amplifier inputs, since no leakage current can flow between two points at the same potential. For example, a PC board trace-to-pad resistance of $10^{12}\Omega$, which is normally considered a very large resistance, could leak 5 pA if the trace were a 5V bus adjacent to the pad of an input. This would cause a 100 times degradation from the LMC6022's actual performance. However, if a guard ring is held within 5 mV of the inputs, then even a resistance of $10^{11}\Omega$ would cause only 0.05 pA of leakage current, or perhaps a minor (2:1) degradation of the amplifier's performance. See *Figures 4a*, *4b*, *4c* for typical connections of guard rings for standard op-amp configurations. If both inputs are active and at high impedance, the guard can be tied to ground and still provide some protection; see *Figure 4d*.

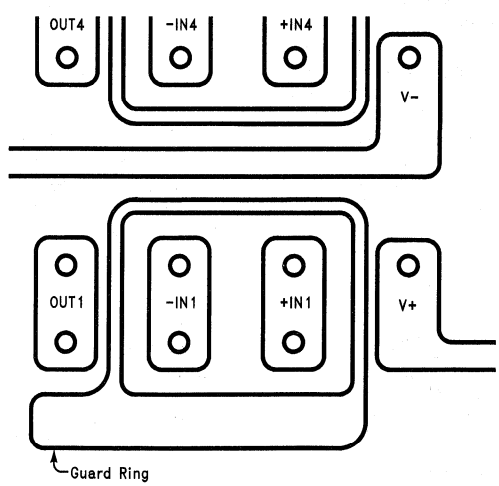

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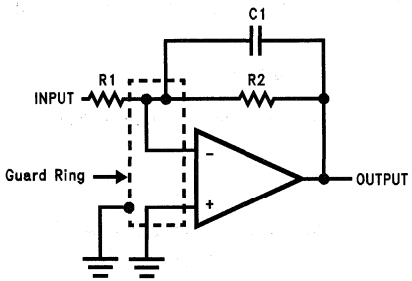
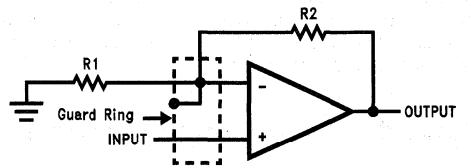
FIGURE 3. Example of Guard Ring in P.C. Board Layout (Using the LMC6024)

Application Hints (Continued)



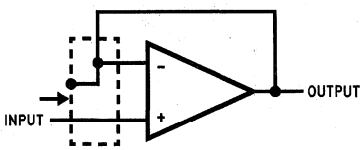
TL/H/11236–9

(a) Inverting Amplifier



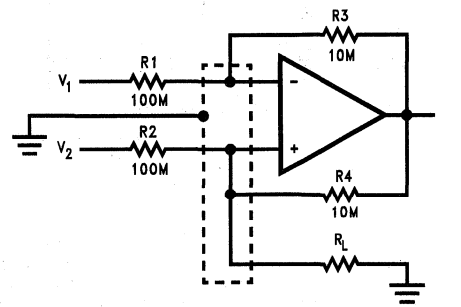
TL/H/11236–10

(b) Non-Inverting Amplifier



TL/H/11236–11

(c) Follower

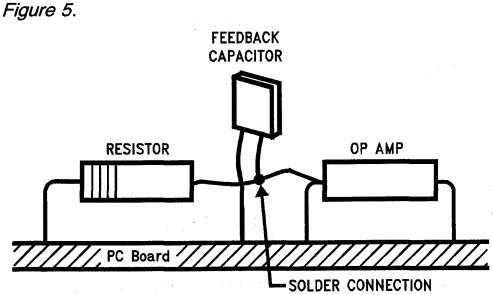


TL/H/11236–12

(d) Howland Current Pump

FIGURE 4. Guard Ring Connections

The designer should be aware that when it is inappropriate to lay out a PC board for the sake of just a few circuits, there is another technique which is even better than a guard ring on a PC board: Don't insert the amplifier's input pin into the board at all, but bend it up in the air and use only air as an insulator. Air is an excellent insulator. In this case you may have to forego some of the advantages of PC board construction, but the advantages are sometimes well worth the effort of using point-to-point up-in-the-air wiring. See *Figure 5*.



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(Input pins are lifted out of PC board and soldered directly to components. All other pins connected to PC board.)

FIGURE 5. Air Wiring

BIAS CURRENT TESTING

The test method of *Figure 6* is appropriate for bench-testing bias current with reasonable accuracy. To understand its operation, first close switch S2 momentarily. When S2 is opened, then

$$I^- = \frac{dV_{OUT}}{dt} \times C2.$$

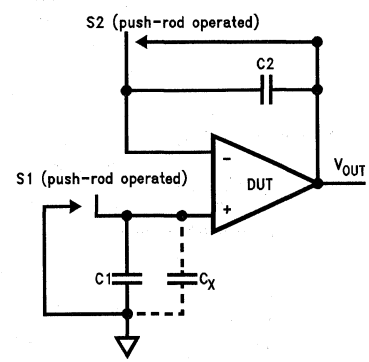

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FIGURE 6. Simple Input Bias Current Test Circuit

Application Hints (Continued)

A suitable capacitor for C2 would be a 5 pF or 10 pF silver mica, NPO ceramic, or air-dielectric. When determining the magnitude of I^-, the leakage of the capacitor and socket must be taken into account. Switch S2 should be left shorted most of the time, or else the dielectric absorption of the capacitor C2 could cause errors.

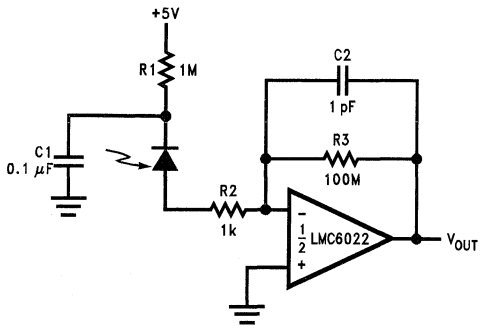
Similarly, if S1 is shorted momentarily (while leaving S2 shorted)

$$I^+ = \frac{dV_{OUT}}{dt} \times (C1 + C_x)$$

where C_x is the stray capacitance at the + input.

Typical Single-Supply Applications ($V^+ = 5.0\ V_{DC}$)

Photodiode Current-to-Voltage Converter



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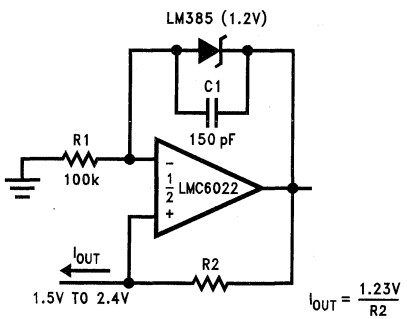
Note: A 5V bias on the photodiode can cut its capacitance by a factor of 2 or 3, leading to improved response and lower noise. However, this bias on the photodiode will cause photodiode leakage (also known as its dark current).

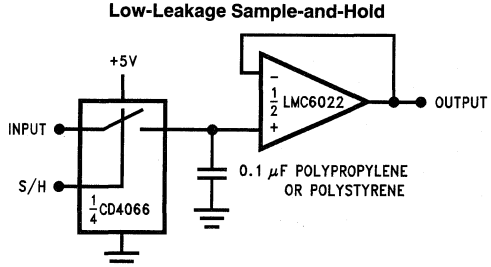
Micropower Current Source



TL/H/11236–16

(Upper limit of output range dictated by input common-mode range; lower limit dictated by minimum current requirement of LM385.)

Low-Leakage Sample-and-Hold



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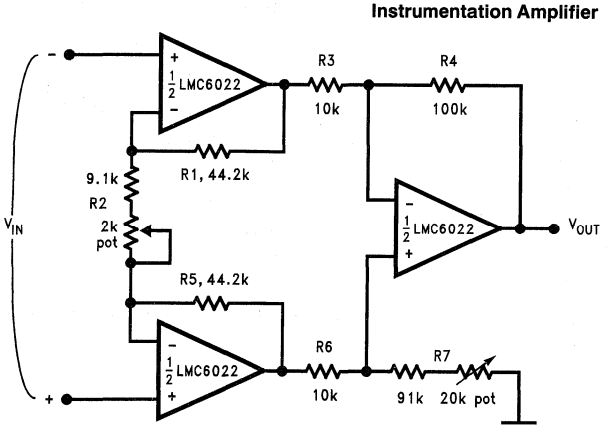
Instrumentation Amplifier



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If R1 = R5, R3 = R6, and R4 = R7;

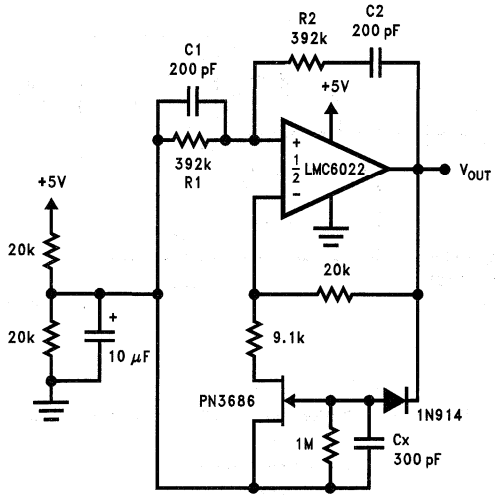
Then $\frac{V_{OUT}}{V_{IN}} = \frac{R2 + 2R1}{R2} \times \frac{R4}{R3}$

$\therefore A_V \approx 100$ for circuit shown

For good CMRR over temperature, low drift resistors should be used. Matching of R3 to R6 and R4 to R7 affects CMRR. Gain may be adjusted through R2. CMRR may be adjusted through R7.

Typical Single-Supply Applications (V^+ = 5.0 V_{DC}) (Continued)

Sine-Wave Oscillator



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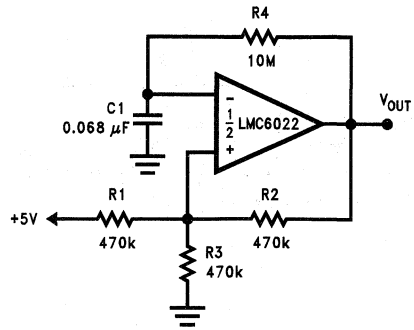
Oscillator frequency is determined by R1, R2, C1, and C2:

$$f_{OSC} = 1/2\pi RC$$

where R = R1 = R2 and C = C1 = C2.

This circuit, as shown, oscillates at 2.0 kHz with a peak-to-peak output swing of 4.5V.

1 Hz Square-Wave Oscillator



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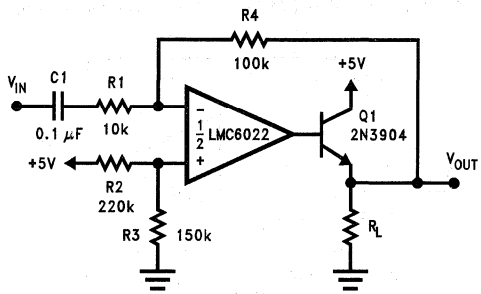
Power Amplifier



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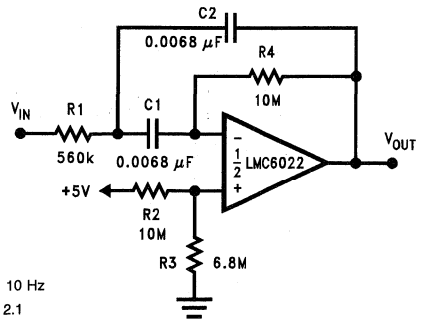
Typical Single-Supply Applications ($V^+ = 5.0\ V_{DC}$) (Continued)

10 Hz Bandpass Filter



$f_O = 10$ Hz
$Q = 2.1$
Gain = −8.8

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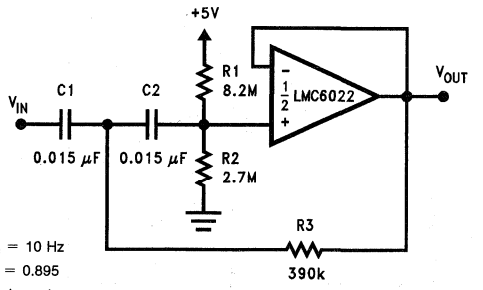
10 Hz High-Pass Filter (2 dB Dip)



$f_c = 10$ Hz
$d = 0.895$
Gain = 1

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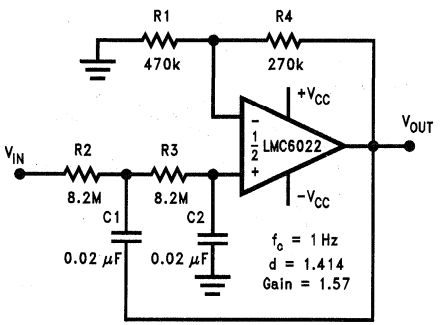
1 Hz Low-Pass Filter (Maximally Flat, Dual Supply Only)



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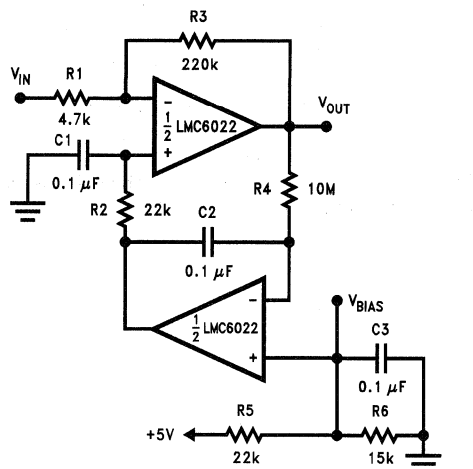
High Gain Amplifier with Offset Voltage Reduction



Gain = −46.8

Output offset voltage reduced to the level of the input offset voltage of the bottom amplifier (typically 1 mV), referred to V_{BIAS}.

TL/H/11236-25

National Semiconductor

LMC6024
Low Power CMOS Quad Operational Amplifier

General Description

The LMC6024 is a CMOS quad operational amplifier which can operate from either a single supply or dual supplies. Its performance features include an input common-mode range that reaches V^-, low input bias current and voltage gain (into 100 kΩ and 5 kΩ loads) that is equal to or better than widely accepted bipolar equivalents, while the power supply requirement is less than 1 mW.

This chip is built with National's advanced Double-Poly Silicon-Gate CMOS process.

See the LMC6022 datasheet for a CMOS dual operational amplifier with these same features.

Features

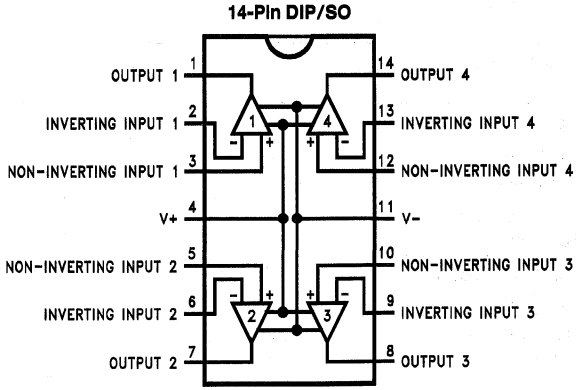
- Specified for 100 kΩ and 5 kΩ loads
- High voltage gain 120 dB
- Low offset voltage drift 2.5 μV/°C
- Ultra low input bias current 40 fA
- Input common-mode range includes V^-
- Operating range from +5V to +15V supply
- Low distortion 0.01% at 1 kHz
- Slew rate 0.11 V/μs
- Micropower operation 1 mW

Applications

- High-impedance buffer or preamplifier
- Current-to-voltage converter
- Long-term integrator
- Sample-and-hold circuit
- Peak detector
- Medical instrumentation
- Industrial controls

Connection Diagram

14-Pin DIP/SO



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Top View

Ordering Information

Temperature Range Industrial $-40°C \leq T_J \leq +85°C$	Package	NSC Drawing
LMC6024IN	14-Pin Molded DIP	N14A
LMC6024IM	14-Pin Small Outline	M14A

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Differential Input Voltage	±Supply Voltage
Supply Voltage ($V^+ - V^-$)	16V
Lead Temperature (Soldering, 10 sec.)	260°C
Storage Temperature Range	−65°C to +150°C
Voltage at Output/Input Pin	$(V^+) + 0.3V, (V^-) - 0.3V$
Current at Input Pin	±5 mA
Current at Output Pin	±18 mA
Current at Power Supply Pin	35 mA
Output Short Circuit to V^+	(Note 12)
Output Short Circuit to V^-	(Note 2)
Junction Temperature	150°C
ESD Tolerance (Note 4)	500V
Power Dissipation	(Note 3)

Operating Ratings

Temperature Range	$-40°C \le T_J \le +85°C$
Supply Voltage Range	4.75V to 15.5V
Power Dissipation	(Note 10)
Thermal Resistance (θ_{JA}), (Note 11)	
14-Pin DIP	85°C/W
14-Pin SO	115°C/W

DC Electrical Characteristics

The following specifications apply for $V^+ = 5V$, $V^- = 0V$, $V_{CM} = 1.5V$, $V_O = 2.5V$, and $R_L = 1M$ unless otherwise noted. **Boldface** limits apply at the temperature extremes; all other limits $T_J = 25°C$.

Symbol	Parameter	Conditions	Typical (Note 5)	LMC6024I Limit (Note 6)	Units
V_{OS}	Input Offset Voltage		1	9 **11**	mV Max
$\Delta V_{OS}/\Delta T$	Input Offset Voltage Average Drift		2.5		μV/°C
I_B	Input Bias Current		0.04	 **200**	pA Max
I_{OS}	Input Offset Current		0.01	 **100**	pA Max
R_{IN}	Input Resistance		>1		TeraΩ
CMRR	Common Mode Rejection Ratio	$0V \le V_{CM} \le 12V$ $V^+ = 15V$	83	63 **61**	dB Min
+PSRR	Positive Power Supply Rejection Ratio	$5V \le V^+ \le 15V$	83	63 **61**	dB Min
−PSRR	Negative Power Supply Rejection Ratio	$0V \le V^- \le -10V$	94	74 **73**	dB Min
V_{CM}	Input Common-Mode Voltage Range	$V^+ = 5V$ and 15V For CMRR ≥ 50 DB	−0.4	−0.1 **0**	V Max
			$V^+ - 1.9$	$V^+ - 2.3$ $\mathbf{V^+ - 2.5}$	V Min
A_V	Large Signal Voltage Gain	$R_L = 100 k\Omega$ (Note 7) Sourcing	1000	200 **100**	V/mV Min
		Sinking	500	90 **40**	V/mV Min
		$R_L = 5 k\Omega$ (Note 7) Sourcing	1000	100 **75**	V/mV Min
		Sinking	250	50 **20**	V/mV Min

DC Electrical Characteristics (Continued)

The following specifications apply for $V^+ = 5V$, $V^- = 0V$, $V_{CM} = 1.5V$, $V_O = 2.5V$, and $R_L = 1M$ unless otherwise noted. **Boldface** limits apply at the temperature extremes; all other limits $T_J = 25°C$.

Symbol	Parameter	Conditions	Typical (Note 5)	LMC6024I Limit (Note 6)	Units
V_O	Output Voltage Swing	$V^+ = 5V$ $R_L = 100\ k\Omega$ to 2.5V	4.987	4.40 **4.43**	V Min
			0.004	0.06 **0.09**	V Max
		$V^+ = 5V$ $R_L = 5\ k\Omega$ to 2.5V	4.940	4.20 **4.00**	V Min
			0.040	0.25 **0.35**	V Max
		$V^+ = 15V$ $R_L = 100\ k\Omega$ to 7.5V	14.970	14.00 **13.90**	V Min
			0.007	0.06 **0.09**	V Max
		$V^+ = 15V$ $R_L = 5\ k\Omega$ to 7.5V	14.840	13.70 **13.50**	V Min
			0.110	0.32 **0.40**	V Max
I_O	Output Current	$V^+ = 5V$ Sourcing, $V_O = 0V$	22	13 **9**	mA Min
		Sinking $V_O = 5V$ (Note 2)	21	13 **9**	mA Min
		$V^+ = 15V$ Sourcing, $V_O = 0V$	40	23 **15**	mA Min
		Sinking, $V_O = 13V$ (Note 12)	39	23 **15**	mA Min
I_S	Supply Current	All Four Amplifiers $V_O = 1.5V$	160	240 **280**	μA Max

AC Electrical Characteristics

The following specifications apply for $V^+ = 5V$, $V^- = 0V$, $V_{CM} = 1.5V$, $V_O = 2.5V$, and $R_L = 1M$ unless otherwise noted. **Boldface** limits apply at the temperature extremes; all other limits $T_J = 25°C$.

Symbol	Parameter	Conditions	Typical (Note 5)	LMC6024I Limit (Note 6)	Units
SR	Slew Rate	(Note 8)	0.11	0.05 **0.03**	V/μs Min
GBW	Gain-Bandwidth Product		0.35		MHz
θ_M	Phase Margin		50		Deg
G_M	Gain Margin		17		dB
	Amp-to-Amp Isolation	(Note 9)	130		dB
e_n	Input-Referred Voltage Noise	F = 1 kHz	42		nV/$\sqrt{Hz}$
i_n	Input-Referred Current Noise	F = 1 kHz	0.0002		pA/$\sqrt{Hz}$

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the component may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed.

Note 2: Applies to both single-supply and split-supply operation. Continuous short circuit operation at elevated ambient temperature and/or multiple Op Amp shorts can result in exceeding the maximum allowed junction temperature of 150°C. Output currents in excess of ±30 mA over long term may adversly affect reliability.

Note 3: The maximum power dissipation is a function of $T_{J(max)}$, θ_{JA}, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(max)} - T_A)/\theta_{JA}$.

Note 4: Human body model, 100 pF discharge through a 1.5 kΩ resistor.

Note 5: Typical values represent the most likely parametric norm.

Note 6: All limits are guaranteed by testing or correlation.

Note 7: $V^+ = 15V$, $V_{CM} = 7.5V$, and R_L connected to 7.5V. For Sourcing tests, $7.5V \le V_O \le 11.5V$. For Sinking tests, $2.5V \le V_O \le 7.5V$.

Note 8: $V^+ = 15V$. Connected as Voltage Follower with 10V step input. Number specified is the slower of the positive and negative slew rates.

Note 9: Input referred, $V^+ = 15V$ and $R_L = 100$ kΩ connected to 7.5V. Each amp excited in turn with 1 kHz to produce $V_O = 13\ V_{PP}$.

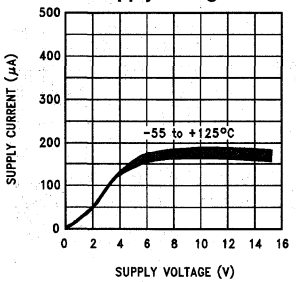
Note 10: For operating at elevated temperatures the device must be derated based on the thermal resistance θ_{JA} with $P_D = (T_J - T_A)/\theta_{JA}$.

Note 11: All numbers apply for packages soldered directly into a PC board.

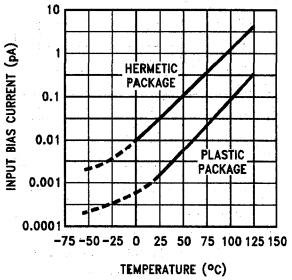
Note 12: Do not connect output to V^+ when V^+ is greater than 13V or reliability may be adversely affected.

Typical Performance Characteristics $V_S = \pm 7.5V$, $T_A = 25°C$ unless otherwise specified

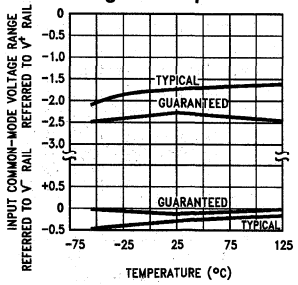
Supply Current vs Supply Voltage



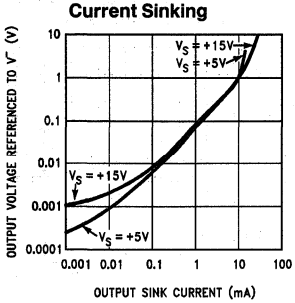
Input Bias Current vs Temperature



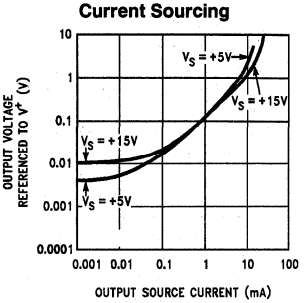
Common-Mode Voltage Range vs Temperature



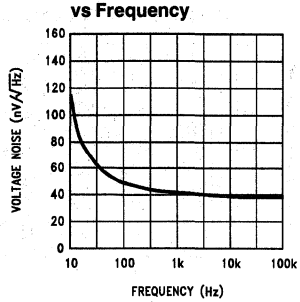
Output Characteristics Current Sinking



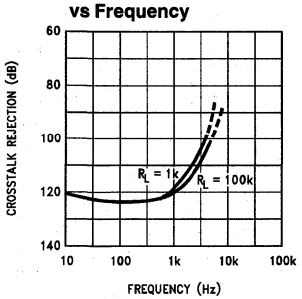
Output Characteristics Current Sourcing



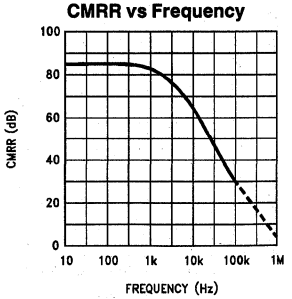
Input Voltage Noise vs Frequency



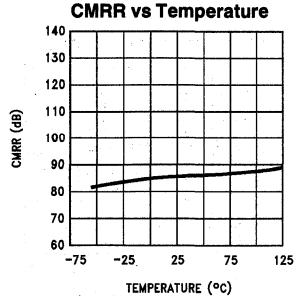
Crosstalk Rejection vs Frequency



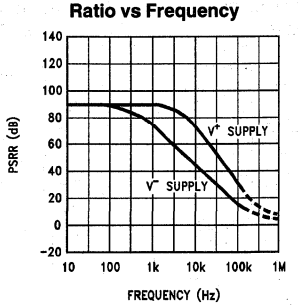
CMRR vs Frequency



CMRR vs Temperature



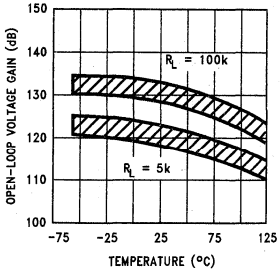
Power Supply Rejection Ratio vs Frequency



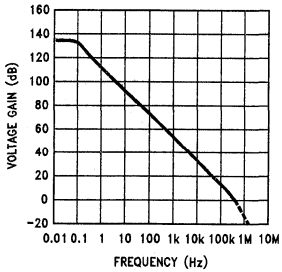
TL/H/11235–2

Typical Performance Characteristics $V_S = \pm 7.5V$, $T_A = 25°C$ unless otherwise specified (Continued)

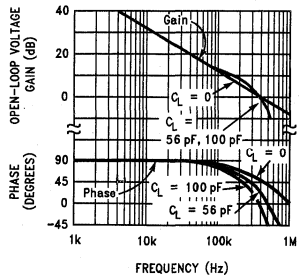
Open-Loop Voltage Gain vs Temperature



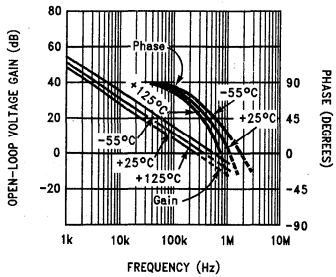
Open-Loop Frequency Response



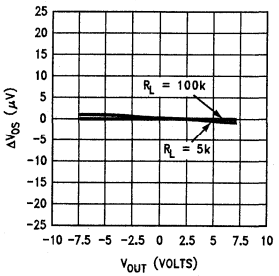
Gain and Phase Responses vs Load Capacitance



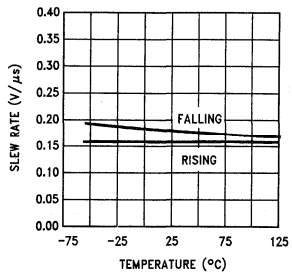
Gain and Phase Responses vs Temperature



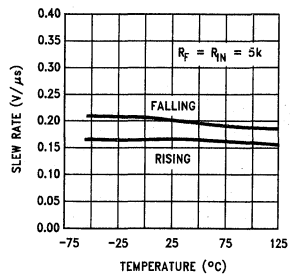
Gain Error (V_{OS} vs V_{OUT})



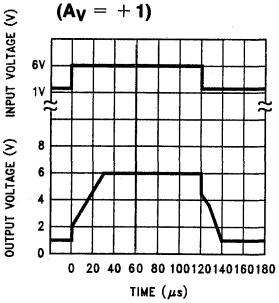
Non-Inverting Slew Rate vs Temperature



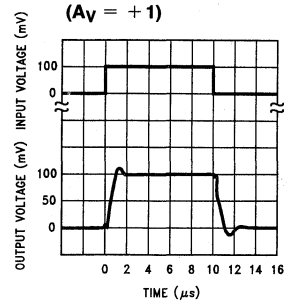
Inverting Slew Rate vs Temperature



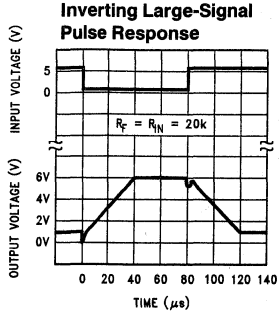
Large-Signal Pulse Non-Inverting Response ($A_V = +1$)



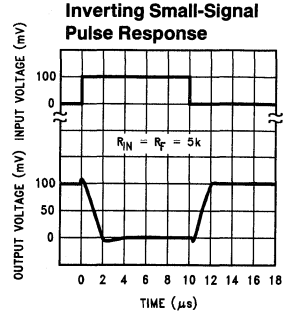
Non-Inverting Small Signal Pulse Response ($A_V = +1$)



Inverting Large-Signal Pulse Response



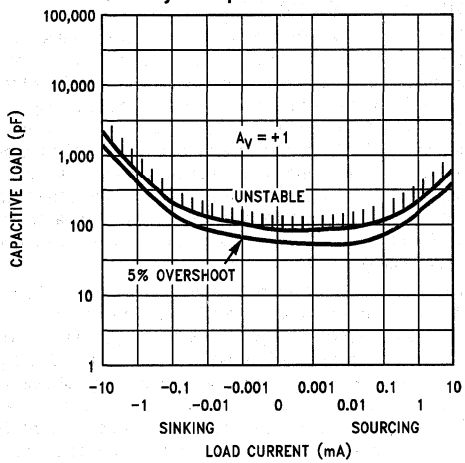
Inverting Small-Signal Pulse Response



TL/H/11235-3

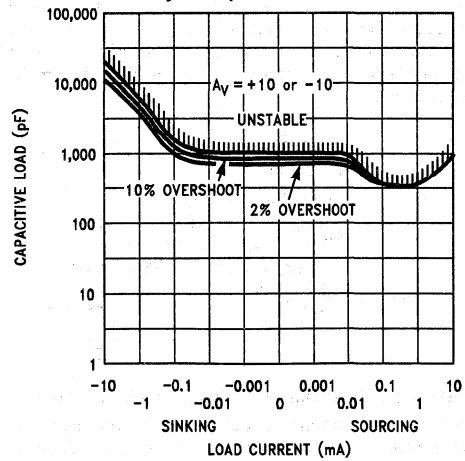
Typical Performance Characteristics $V_S = \pm 7.5V$, $T_A = 25°C$ unless otherwise specified (Continued)

Stability vs Capacitive Load



TL/H/11235–4

Stability vs Capacitive Load



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Note: Avoid resistive loads of less than 500Ω, as they may cause instability.

Application Hints

AMPLIFIER TOPOLOGY

The topology chosen for the LMC6024 is unconventional (compared to general-purpose op amps) in that the traditional unity-gain buffer output stage is not used; instead, the output is taken directly from the output of the integrator, to allow rail-to-rail output swing. Since the buffer traditionally delivers the power to the load, while maintaining high op amp gain and stability, and must withstand shorts to either rail, these tasks now fall to the integrator.

As a result of these demands, the integrator is a compound affair with an embedded gain stage that is doubly fed forward (via C_f and C_{ff}) by a dedicated unity-gain compensation driver. In addition, the output portion of the integrator is a push-pull configuration for delivering heavy loads. While sinking current the whole amplifier path consists of three gain stages with one stage fed forward, whereas while sourcing the path contains four gain stages with two fed forward.

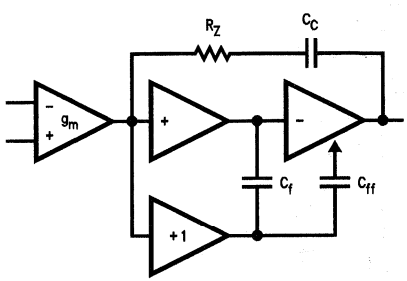

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FIGURE 1. LMC6024 Circuit Topology (Each Amplifier)

The large signal voltage gain while sourcing is comparable to traditional bipolar op amps, for load resistance of at least 5 kΩ. The gain while sinking is higher than most CMOS op amps, due to the additional gain stage; however, when driving load resistance of 5 kΩ or less, the gain will be reduced as indicated in the Electrical Characterisitics. The op amp can drive load resistance as low as 500Ω without instability.

COMPENSATING INPUT CAPACITANCE

Refer to the LMC660 or LMC662 datasheets to determine whether or not a feedback capacitor will be necessary for compensation and what the value of that capacitor would be.

CAPACITIVE LOAD TOLERANCE

Like many other op amps, the LMC6024 may oscillate when its applied load appears capacitive. The threshold of oscillation varies both with load and circuit gain. The configuration most sensitive to oscillation is a unity-gain follower. See the Typical Performance Characteristics.

The load capacitance interacts with the op amp's output resistance to create an additional pole. If this pole frequency is sufficiently low, it will degrade the op amp's phase margin so that the amplifier is no longer stable at low gains. The addition of a small resistor (50Ω to 100Ω) in series with the op amp's output, and a capacitor (5 pF to 10 pF) from

Application Hints (Continued)

inverting input to output pins, returns the phase margin to a safe value without interfering with lower-frequency circuit operation. Thus, larger values of capacitance can be tolerated without oscillation. Note that in all cases, the output will ring heavily when the load capcitance is near the threshold for oscillation.

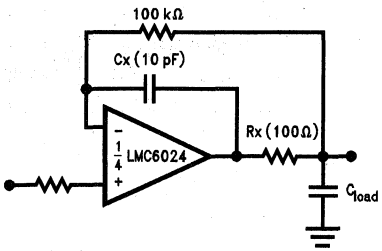

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FIGURE 2a. Rx, Cx Improve Capacitive Load Tolerance

Capacitive load driving capability is enhanced by using a pull up resistor to V^+ *(Figure 2b)*. Typically a pull up resistor conducting 50 μA or more will significantly improve capacitive load responses. The value of the pull up resistor must be determined based on the current sinking capability of the amplifier with respect to the desired output swing. Open loop gain of the amplifier can also be affected by the pull up resistor (see Electrical Characteristics).

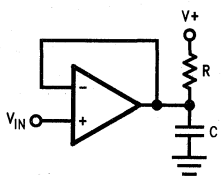

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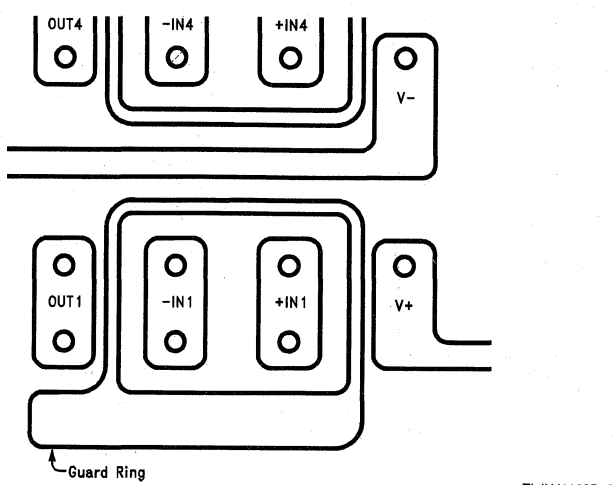
FIGURE 2b. Compensating for Large Capacitive Loads with a Pull Up Resistor

PRINTED-CIRCUIT-BOARD LAYOUT FOR HIGH-IMPEDANCE WORK

It is generally recognized that any circuit which must operate with less than 1000 pA of leakage current requires special layout of the PC board. When one wishes to take advantage of the ultra-low bias current of the LMC6024, typically less than 0.04 pA, it is essential to have an excellent layout. Fortunately, the techniques for obtaining low leakages are quite simple. First, the user must not ignore the surface leakage of the PC board, even though it may sometimes appear acceptably low, because under conditions of high humidity or dust or contamination, the surface leakage will be appreciable.

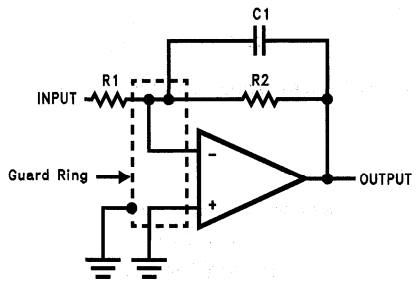
To minimize the effect of any surface leakage, lay out a ring of foil completely surrounding the LMC6024's inputs and the terminals of capacitors, diodes, conductors, resistors, relay terminals, etc. connected to the op-amp's inputs. See *Figure 3*. To have a significant effect, guard rings should be placed on both the top and bottom of the PC board. This PC foil must then be connected to a voltage which is at the same voltage as the amplifier inputs, since no leakage current can flow between two points at the same potential. For example, a PC board trace-to-pad resistance of 10^{12} ohms, which is normally considered a very large resistance, could leak 5 pA if the trace were a 5V bus adjacent to the pad of an input. This would cause a 100 times degradation from the LMC6024's actual performance. However, if a guard ring is held within 5 mV of the inputs, then even a resistance of 10^{11} ohms would cause only 0.05 pA of leakage current, or perhaps a minor (2:1) degradation of the amplifier's performance. See *Figures 4a, 4b, 4c* for typical connections of guard rings for standard op-amp configurations. If both inputs are active and at high impedance, the guard can be tied to ground and still provide some protection; see *Figure 4d*.



TL/H/11235–8

FIGURE 3. Example of Guard Ring in P.C. Board Layout (Using the LMC6024)

Application Hints (Continued)



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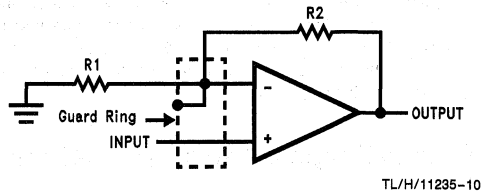
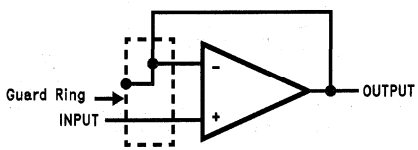
(a) Inverting Amplifier



TL/H/11235-10

(b) Non-Inverting Amplifier



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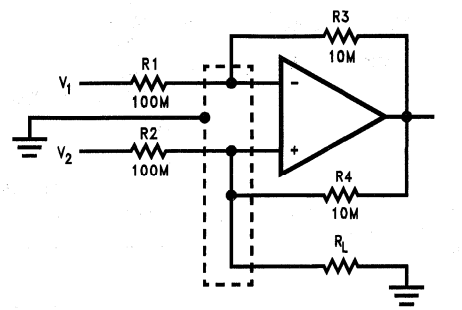
(c) Follower

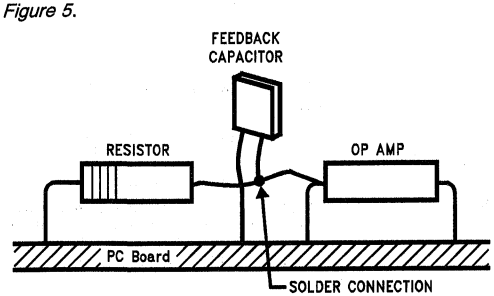


TL/H/11235-12

(d) Howland Current Pump

FIGURE 4. Guard Ring Connections

The designer should be aware that when it is inappropriate to lay out a PC board for the sake of just a few circuits, there is another technique which is even better than a guard ring on a PC board: Don't insert the amplifier's input pin into the board at all, but bend it up in the air and use only air as an insulator. Air is an excellent insulator. In this case you may have to forego some of the advantages of PC board construction, but the advantages are sometimes well worth the effort of using point-to-point up-in-the-air wiring. See *Figure 5*.



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(Input pins are lifted out of PC board and soldered directly to components. All other pins connected to PC board.)

FIGURE 5. Air Wiring

BIAS CURRENT TESTING

The test method of *Figure 6* is appropriate for bench-testing bias current with reasonable accuracy. To understand its operation, first close switch S2 momentarily. When S2 is opened, then

$$I^- = \frac{dV_{OUT}}{dt} \times C2.$$

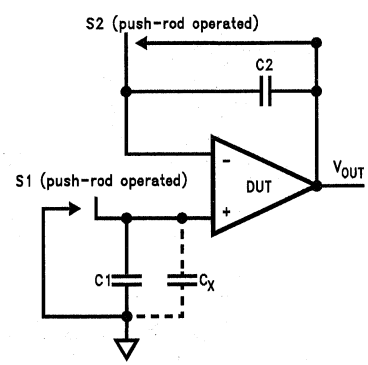

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FIGURE 6. Simple Input Bias Current Test Circuit

Application Hints (Continued)

A suitable capacitor for C2 would be a 5 pF or 10 pF silver mica, NPO ceramic, or air-dielectric. When determining the magnitude of I^-, the leakage of the capacitor and socket must be taken into account. Switch S2 should be left shorted most of the time, or else the dielectric absorption of the capacitor C2 could cause errors.

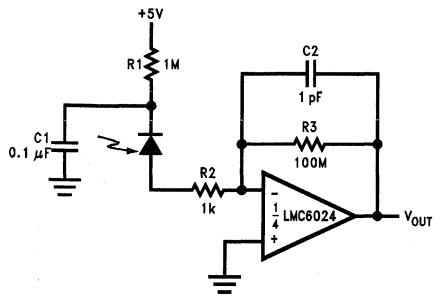
Similarly, if S1 is shorted momentarily (while leaving S2 shorted)

$$I^+ = \frac{dV_{OUT}}{dt} \times (C1 + C_X)$$

where C_X is the stray capacitance at the + input.

Typical Single-Supply Applications ($V^+ = 5.0\ V_{DC}$)

Photodiode Current-to-Voltage Converter



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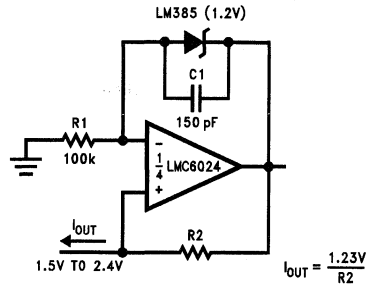
Note: A 5V bias on the photodiode can cut its capacitance by a factor of 2 or 3, leading to improved response and lower noise. However, this bias on the photodiode will cause photodiode leakage (also known as its dark current).

Micropower Current Source



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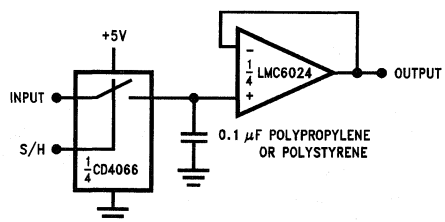
(Upper limit of output range dictated by input common-mode range; lower limit dictated by minimum current requirement of LM385.)

Low-Leakage Sample-and-Hold



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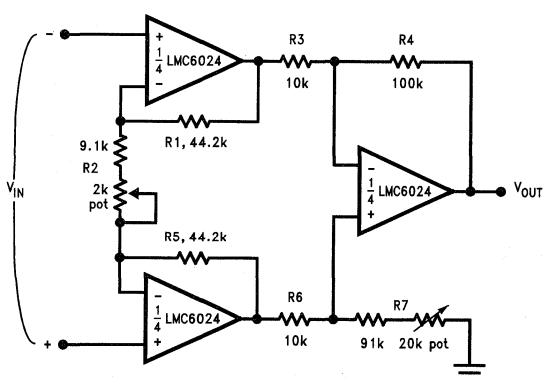
Instrumentation Amplifier



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If R1 = R5, R3 = R6, and R4 = R7;

Then

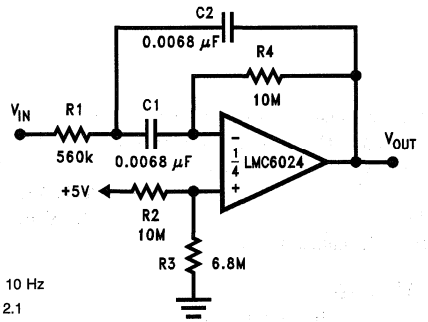
$$\frac{V_{OUT}}{V_{IN}} = \frac{R2 + 2R1}{R2} \times \frac{R4}{R3}$$

$\therefore A_V \approx 100$ for circuit shown.

For good CMRR over temperature, low drift resistors should be used. Matching of R3 to R6 and R4 to R7 affects CMRR. Gain may be adjusted through R2. CMRR may be adjusted through R7.

Typical Single-Supply Applications ($V^+ = 5.0\ V_{DC}$) (Continued)

10 Hz Bandpass Filter



f_O = 10 Hz
Q = 2.1
Gain = −8.8

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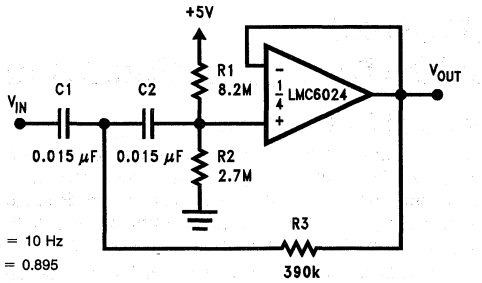
10 Hz High-Pass Filter (2 dB Dip)



f_c = 10 Hz
d = 0.895
Gain = 1

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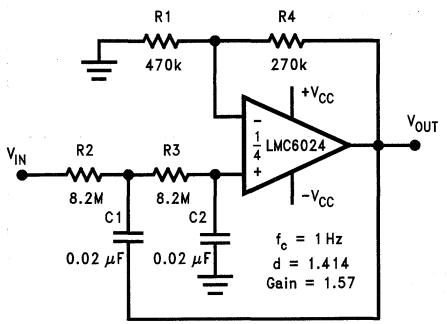
1 Hz Low-Pass Filter (Maximally Flat, Dual Supply Only)



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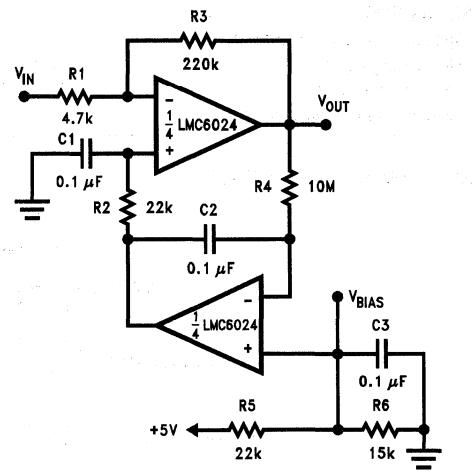
High Gain Amplifier with Offset Voltage Reduction



Gain = −46.8

Output offset voltage reduced to the level of the input offset voltage of the bottom amplifier (typically 1 mV), referred to V_{BIAS}.

TL/H/11235–22

National Semiconductor

LMC6032
CMOS Dual Operational Amplifier

General Description

The LMC6032 is a CMOS dual operational amplifier which can operate from either a single supply or dual supplies. Its performance features include an input common-mode range that reaches ground, low input bias current, and high voltage gain into realistic loads, such as 2 kΩ and 600Ω.

This chip is built with National's advanced Double-Poly Silicon-Gate CMOS process.

See the LMC6034 datasheet for a CMOS quad operational amplifier with these same features. For higher performance characteristics refer to the LMC662.

Features

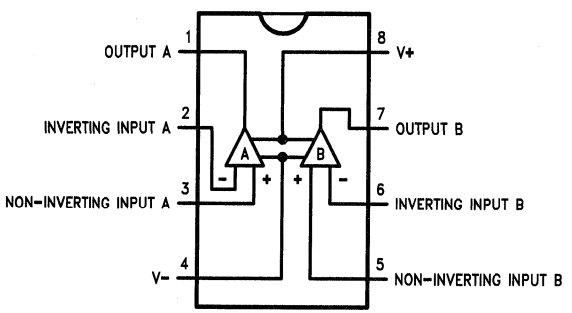
- Specified for 2 kΩ and 600Ω loads
- High voltage gain 126 dB
- Low offset voltage drift 2.3 μV/°C
- Ultra low input bias current 40 fA
- Input common-mode range includes V−
- Operating range from +5V to +15V supply
- I_{SS} = 400 μA/amplifier; independent of V+
- Low distortion 0.01% at 10 kHz
- Slew rate 1.1 V/μs
- Improved performance over TLC272

Applications

- High-impedance buffer or preamplifier
- Current-to-voltage converter
- Long-term integrator
- Sample-and-hold circuit
- Medical instrumentation

Connection Diagram

8-Pin DIP/SO



TL/H/11135–1

Top View

Ordering Information

Temperature Range Industrial −40°C ≤ T_J ≤ +85°C	Package	NSC Drawing
LMC6032IN	8-Pin Molded DIP	N08E
LMC6032IM	8-Pin Small Outline	M08A

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Differential Input Voltage	±Supply Voltage
Supply Voltage ($V^+ - V^-$)	16V
Output Short Circuit to V^+	(Note 10)
Output Short Circuit to V^-	(Note 2)
Lead Temperature (Soldering, 10 sec.)	260°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature	150°C
ESD Tolerance (Note 4)	500V
Power Dissipation	(Note 3)
Voltage at Output/Input Pin	$(V^+) + 0.3V$, $(V^-) - 0.3V$
Current at Output Pin	±18 mA
Current at Input Pin	±5 mA
Current at Power Supply Pin	35 mA

Operating Ratings (Note 1)

Temperature Range	$-40°C \le T_J \le +85°C$
Supply Voltage Range	4.75V to 15.5V
Power Dissipation	(Note 11)
Thermal Resistance (θ_{JA}), (Note 12)	
8-Pin DIP	101°C/W
8-Pin SO	165°C/W

DC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for $T_J = 25°C$. **Boldface** limits apply at the temperature extremes. $V^+ = 5V$, $V^- = GND = 0V$, $V_{CM} = 1.5V$, $V_{OUT} = 2.5V$ and $R_L > 1M$ unless otherwise specified.

Symbol	Parameter	Conditions	Typical (Note 5)	LMC6032I Limit (Note 6)	Units
V_{OS}	Input Offset Voltage		1	9 **11**	mV max
$\Delta V_{OS}/\Delta T$	Input Offset Voltage Average Drift		2.3		μV/°C
I_B	Input Bias Current		0.04	**200**	pA max
I_{OS}	Input Offset Current		0.01	**100**	pA max
R_{IN}	Input Resistance		>1		TeraΩ
CMRR	Common Mode Rejection Ratio	$0V \le V_{CM} \le 12V$ $V^+ = 15V$	83	63 **60**	dB min
+PSRR	Positive Power Supply Rejection Ratio	$5V \le V^+ \le 15V$ $V_O = 2.5V$	83	63 **60**	dB min
−PSRR	Negative Power Supply Rejection Ratio	$0V \le V^- \le -10V$	94	74 **70**	dB min
V_{CM}	Input Common-Mode Voltage Range	$V^+ = 5V$ & 15V For CMRR ≥ 50 dB	−0.4	−0.1 **0**	V max
			$V^+ - 1.9$	$V^+ - 2.3$ $\mathbf{V^+ - 2.6}$	V min
A_V	Large Signal Voltage Gain	$R_L = 2k\Omega$ (Note 7) Sourcing	2000	200 **100**	V/mV min
		Sinking	500	90 **40**	V/mV min
		$R_L = 600\Omega$ (Note 7) Sourcing	1000	100 **75**	V/mV min
		Sinking	250	50 **20**	V/mV min

DC Electrical Characteristics (Continued)

Unless otherwise specified, all limits guaranteed for T_J = 25°C. **Boldface** limits apply at the temperature extremes. V^+ = 5V, V^- = GND = 0V, V_{CM} = 1.5V, V_{OUT} = 2.5V and R_L > 1M unless otherwise specified.

Symbol	Parameter	Conditions	Typical (Note 5)	LMC6032I Limit (Note 6)	Units
V_O	Output Voltage Swing	V^+ = 5V R_L = 2 kΩ to 2.5V	4.87	4.20 **4.00**	V min
			0.10	0.25 **0.35**	V max
		V^+ = 5V R_L = 600Ω to 2.5V	4.61	4.00 **3.80**	V min
			0.30	0.63 **0.75**	V max
		V^+ = 15V R_L = 2 kΩ to 7.5V	14.63	13.50 **13.00**	V min
			0.26	0.45 **0.55**	V max
		V^+ = 15V R_L = 600Ω to 7.5V	13.90	12.50 **12.00**	V min
			0.79	1.45 **1.75**	V max
I_O	Output Current	V^+ = 5V Sourcing, V_O = 0V	22	13 **9**	mA min
		Sinking, V_O = 5V	21	13 **9**	mA min
		V^+ = 15V Sourcing, V_O = 0V	40	23 **15**	mA min
		Sinking, V_O = 13V (Note 10)	39	23 **15**	mA min
I_S	Supply Current	Both Amplifiers V_O = 1.5V	0.75	1.6 **1.9**	mA max

AC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for T_J = 25°C. **Boldface** limits apply at the temperature extremes. V^+ = 5V, V^- = GND = 0V, V_{CM} = 1.5V, V_{OUT} = 2.5V and R_L > 1M unless otherwise specified.

Symbol	Parameter	Conditions	Typical (Note 5)	LMC6032I Limit (Note 6)	Units
SR	Slew Rate	(Note 8)	1.1	0.8 **0.4**	V/μs min
GBW	Gain-Bandwidth Product		1.4		MHz
ϕ_M	Phase Margin		50		Deg
G_M	Gain Margin		17		dB
	Amp-to-Amp Isolation	(Note 9)	130		dB
e_n	Input-Referred Voltage Noise	F = 1 kHz	22		nV/$\sqrt{Hz}$
i_n	Input-Referred Current Noise	F = 1 kHz	0.0002		pA/$\sqrt{Hz}$
THD	Total Harmonic Distortion	F = 10 kHz, A_V = −10 R_L = 2 kΩ, V_O = 8 V_{PP} ±5V Supply	0.01		%

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to component may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed.

Note 2: Applies to both single-supply and split-supply operation. Continuous short circuit operation at elevated ambient temperature and/or multiple Op Amp shorts can result in exceeding the maximum allowed junction temperature of 150°C. Output currents in excess of ±30 mA over long term may adversely affect reliability.

Note 3: The maximum power dissipation is a function of $T_{J(max)}$, θ_{JA}, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(max)} - T_A)/\theta_{JA}$.

Note 4: Human body model, 100 pF discharged through a 1.5 kΩ resistor.

Note 5: Typical values represent the most likely parametric norm.

Note 6: All limits are guaranteed at room temperature (standard type face) or at operating temperature extremes (**bold type face**).

Note 7: V^+ = 15V, V_{CM} = 7.5V, and R_L connected to 7.5V. For Sourcing tests, 7.5V ≤ V_O ≤ 11.5V. For Sinking tests, 2.5V ≤ V_O ≤ 7.5V.

Note 8: V^+ = 15V. Connected as Voltage Follower with 10V step input. Number specified is the slower of the positive and negative slew rates.

Note 9: Input referred. V^+ = 15V and R_L = 10 kΩ connected to $V^+/2$. Each amp excited in turn with 1 kHz to produce V_O = 13 V_{PP}.

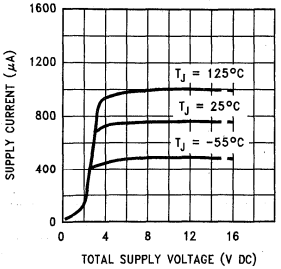
Note 10: Do not connect output to V^+, when V^+ is greater than 13V or reliability may be adversely affected.

Note 11: For operating at elevated temperatures the device must be derated based on the thermal resistance θ_{JA} with $P_D = (T_J - T_A)/\theta_{JA}$.

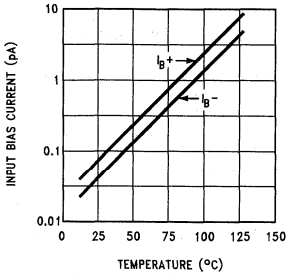
Note 12: All numbers apply for packages soldered directly into a PC board.

Typical Performance Characteristics $V_S = \pm 7.5V$, $T_A = 25°C$ unless otherwise specified

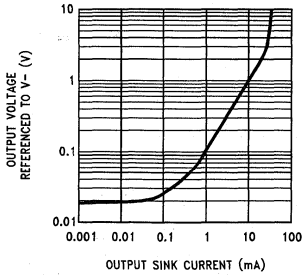
Supply Current vs Supply Voltage



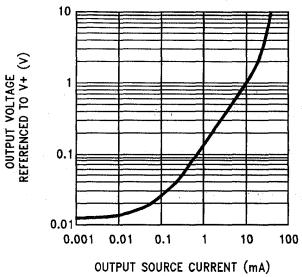
Input Bias Current



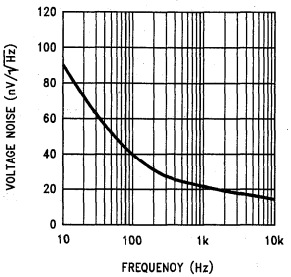
Output Characteristics Current Sinking



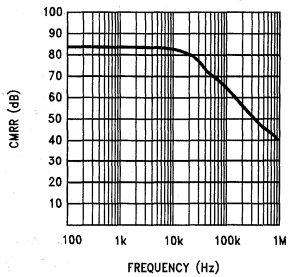
Output Characteristics Current Sourcing



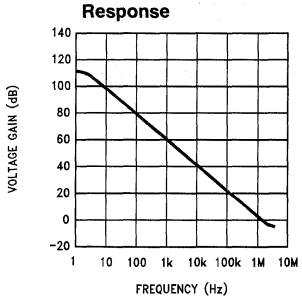
Input Voltage Noise vs Frequency



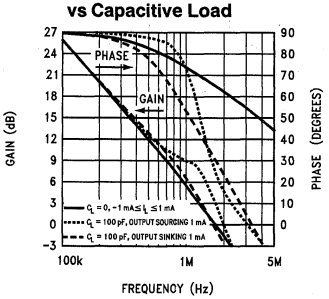
CMRR vs Frequency



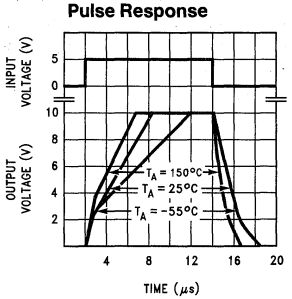
Open-Loop Frequency Response



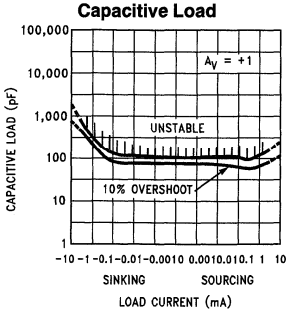
Frequency Response vs Capacitive Load



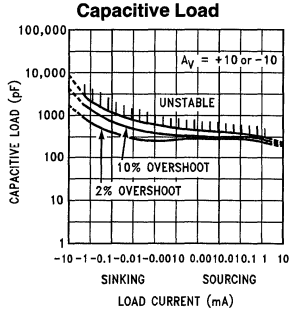
Non-Inverting Large Signal Pulse Response



Stability vs Capacitive Load



Stability vs Capacitive Load



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Note: Avoid resistive loads of less than 500Ω, as they may cause instability.

Application Hints

AMPLIFIER TOPOLOGY

The topology chosen for the LMC6032, shown in *Figure 1*, is unconventional (compared to general-purpose op amps) in that the traditional unity-gain buffer output stage is not used; instead, the output is taken directly from the output of the integrator, to allow a larger output swing. Since the buffer traditionally delivers the power to the load, while maintaining high op amp gain and stability, and must withstand shorts to either rail, these tasks now fall to the integrator.

As a result of these demands, the integrator is a compound affair with an embedded gain stage that is doubly fed forward (via C_f and C_{ff}) by a dedicated unity-gain compensation driver. In addition, the output portion of the integrator is a push-pull configuration for delivering heavy loads. While sinking current the whole amplifier path consists of three gain stages with one stage fed forward, whereas while sourcing the path contains four gain stages with two fed forward.

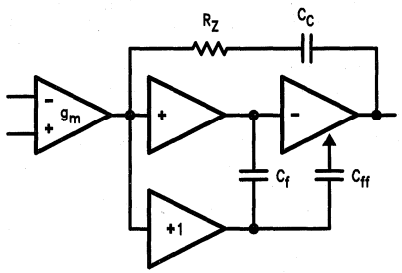

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FIGURE 1. LMC6032 Circuit Topology (Each Amplifier)

The large signal voltage gain while sourcing is comparable to traditional bipolar op amps, even with a 600Ω load. The gain while sinking is higher than most CMOS op amps, due to the additional gain stage; however, under heavy load (600Ω) the gain will be reduced as indicated in the Electrical Characteristics.

COMPENSATING INPUT CAPACITANCE

The high input resistance of the LMC6032 op amps allows the use of large feedback and source resistor values without losing gain accuracy due to loading. However, the circuit will be especially sensitive to its layout when these large-value resistors are used.

Every amplifier has some capacitance between each input and AC ground, and also some differential capacitance between the inputs. When the feedback network around an amplifier is resistive, this input capacitance (along with any additional capacitance due to circuit board traces, the socket, etc.) and the feedback resistors create a pole in the feedback path. In the following General Operational Amplifier Circuit, *Figure 2*, the frequency of this pole is

$$f_p = \frac{1}{2\pi C_S R_P}$$

where C_S is the total capacitance at the inverting input, including amplifier input capacitance and any stray capacitance from the IC socket (if one is used), circuit board traces, etc., and R_P is the parallel combination of R_F and R_{IN}. This formula, as well as all formulae derived below, apply to inverting and non-inverting op-amp configurations.

When the feedback resistors are smaller than a few kΩ, the frequency of the feedback pole will be quite high, since C_S is generally less than 10 pF. If the frequency of the feedback pole is much higher than the "ideal" closed-loop bandwidth (the nominal closed-loop bandwidth in the absence of C_S), the pole will have a negligible effect on stability, as it will add only a small amount of phase shift.

However, if the feedback pole is less than approximately 6 to 10 times the "ideal" −3 dB frequency, a feedback capacitor, C_F, should be connected between the output and the inverting input of the op amp. This condition can also be stated in terms of the amplifier's low-frequency noise gain: To maintain stability, a feedback capacitor will probably be needed if

$$\left(\frac{R_F}{R_{IN}} + 1\right) \leq \sqrt{6 \times 2\pi \times GBW \times R_F \times C_S}$$

where

$$\left(\frac{R_F}{R_{IN}} + 1\right)$$

is the amplifier's low-frequency noise gain and GBW is the amplifier's gain bandwidth product. An amplifier's low-frequency noise gain is represented by the formula

$$\left(\frac{R_F}{R_{IN}} + 1\right)$$

regardless of whether the amplifier is being used in an inverting or non-inverting mode. Note that a feedback capacitor is more likely to be needed when the noise gain is low and/or the feedback resistor is large.

If the above condition is met (indicating a feedback capacitor will probably be needed), and the noise gain is large enough that:

$$\left(\frac{R_F}{R_{IN}} + 1\right) \geq 2\sqrt{GBW \times R_F \times C_S},$$

the following value of feedback capacitor is recommended:

$$C_F = \frac{C_S}{2\left(\frac{R_F}{R_{IN}} + 1\right)}$$

If

$$\left(\frac{R_F}{R_{IN}} + 1\right) < 2\sqrt{GBW \times R_F \times C_S},$$

the feedback capacitor should be:

$$C_F = \sqrt{\frac{C_S}{GBW \times R_F}}$$

Note that these capacitor values are usually significantly smaller than those given by the older, more conservative formula:

$$C_F = \frac{C_S R_{IN}}{R_F}.$$

Application Hints (Continued)

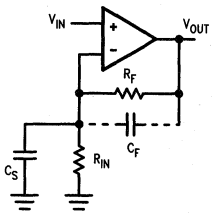

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FIGURE 2. General Operational Amplifier Circuit

C_S consists of the amplifier's input capacitance plus any stray capacitance from the circuit board and socket. C_F compensates for the pole caused by C_S and the feedback resistor.

Using the smaller capacitors will give much higher bandwidth with little degradation of transient response. It may be necessary in any of the above cases to use a somewhat larger feedback capacitor to allow for unexpected stray capacitance, or to tolerate additional phase shifts in the loop, or excessive capacitive load, or to decrease the noise or bandwidth, or simply because the particular circuit implementation needs more feedback capacitance to be sufficiently stable. For example, a printed circuit board's stray capacitance may be larger or smaller than the breadboard's, so the actual optimum value for C_F may be different from the one estimated using the breadboard. In most cases, the value of C_F should be checked on the actual circuit, starting with the computed value.

CAPACITIVE LOAD TOLERANCE

Like many other op amps, the LMC6032 may oscillate when its applied load appears capacitive. The threshold of oscillation varies both with load and circuit gain. The configuration most sensitive to oscillation is a unity-gain follower. See the Typical Performance Characteristics.

The load capacitance interacts with the op amp's output resistance to create an additional pole. If this pole frequency is sufficiently low, it will degrade the op amp's phase margin so that the amplifier is no longer stable at low gains. As shown in *Figure 3a*, the addition of a small resistor (50Ω to 100Ω) in series with the op amp's output, and a capacitor (5 pF to 10 pF) from inverting input to output pins, returns the phase margin to a safe value without interfering with lower-frequency circuit operation. Thus, larger values of capacitance can be tolerated without oscillation. Note that in all cases, the output will ring heavily when the load capacitance is near the threshold for oscillation.

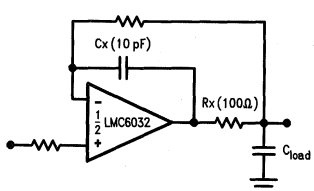

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FIGURE 3a. Rx, Cx Improve Capacitive Load Tolerance

Capacitive load driving capability is enhanced by using a pull up resistor to V^+ (*Figure 3b*). Typically a pull up resistor conducting 500 μA or more will significantly improve capacitive load responses. The value of the pull up resistor must be determined based on the current sinking capability of the amplifier with respect to the desired output swing. Open loop gain of the amplifier can also be affected by the pull up resistor (see Electrical Characteristics).

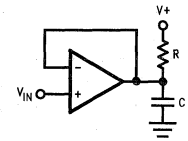

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FIGURE 3b. Compensating for Large Capacitive Loads with a Pull Up Resistor

PRINTED-CIRCUIT-BOARD LAYOUT FOR HIGH-IMPEDANCE WORK

It is generally recognized that any circuit which must operate with less than 1000 pA of leakage current requires special layout of the PC board. When one wishes to take advantage of the ultra-low bias current of the LMC6032, typically less than 0.04 pA, it is essential to have an excellent layout. Fortunately, the techniques for obtaining low leakages are quite simple. First, the user must not ignore the surface leakage of the PC board, even though it may sometimes appear acceptably low, because under conditions of high humidity or dust or contamination, the surface leakage will be appreciable.

To minimize the effect of any surface leakage, lay out a ring of foil completely surrounding the LMC6032's inputs and the terminals of capacitors, diodes, conductors, resistors, relay terminals, etc. connected to the op-amp's inputs. See *Figure 4*. To have a significant effect, guard rings should be placed on both the top and bottom of the PC board. This PC foil must then be connected to a voltage which is at the same voltage as the amplifier inputs, since no leakage current can flow between two points at the same potential. For example, a PC board trace-to-pad resistance of $10^{12}\Omega$, which is normally considered a very large resistance, could leak 5 pA if the trace were a 5V bus adjacent to the pad of an input. This would cause a 100 times degradation from the LMC6032's actual performance. However, if a guard ring is held within 5 mV of the inputs, then even a resistance of $10^{11}\Omega$ would cause only 0.05 pA of leakage current, or perhaps a minor (2:1) degradation of the amplifier's performance. See *Figures 5a, 5b, 5c* for typical connections of guard rings for standard op-amp configurations. If both inputs are active and at high impedance, the guard can be tied to ground and still provide some protection; see *Figure 5d*.

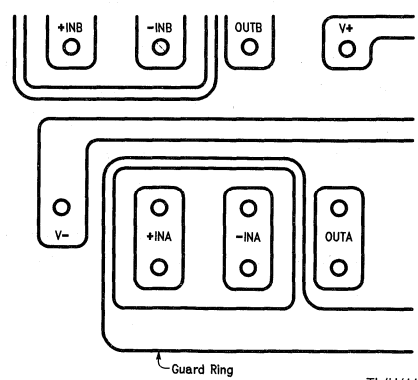

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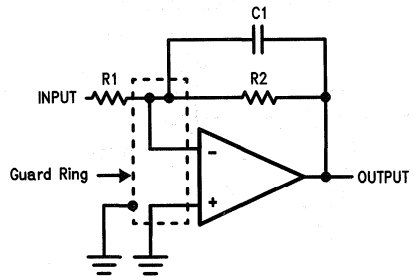
FIGURE 4. Example of Guard Ring in P.C. Board Layout

Application Hints (Continued)



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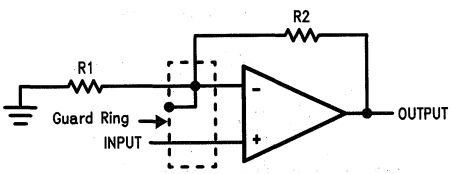
(a) Inverting Amplifier



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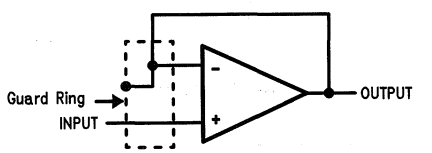
(b) Non-Inverting Amplifier



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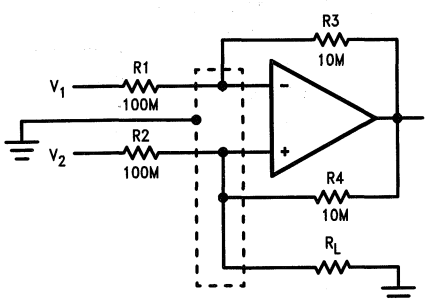
(c) Follower



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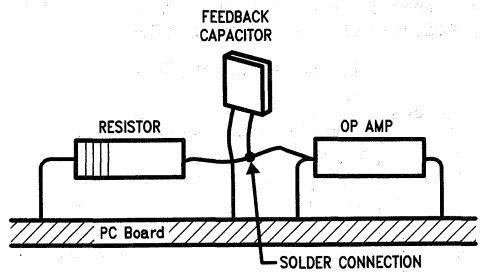
(d) Howland Current Pump

FIGURE 5. Guard Ring Connections

The designer should be aware that when it is inappropriate to lay out a PC board for the sake of just a few circuits, there is another technique which is even better than a guard ring on a PC board: Don't insert the amplifier's input pin into the board at all, but bend it up in the air and use only air as an insulator. Air is an excellent insulator. In this case you may have to forego some of the advantages of PC board construction, but the advantages are sometimes well worth the effort of using point-to-point up-in-the-air wiring. See *Figure 6*.



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(Input pins are lifted out of PC board and soldered directly to components. All other pins connected to PC board.)

FIGURE 6. Air Wiring

BIAS CURRENT TESTING

The test method of *Figure 7* is appropriate for bench-testing bias current with reasonable accuracy. To understand its operation, first close switch S2 momentarily. When S2 is opened, then

$$I_b^- = \frac{dV_{OUT}}{dt} \times C2.$$

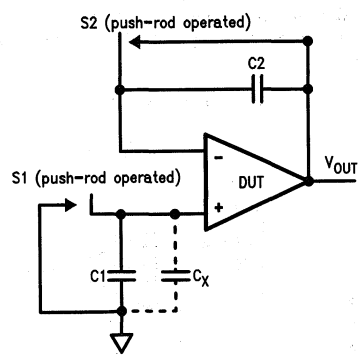

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FIGURE 7. Simple Input Bias Current Test Circuit

A suitable capacitor for C2 would be a 5 pF or 10 pF silver mica, NPO ceramic, or air-dielectric. When determining the magnitude of I_b^-, the leakage of the capacitor and socket must be taken into account. Switch S2 should be left shorted most of the time, or else the dielectric absorption of the capacitor C2 could cause errors.

Similarly, if S1 is shorted momentarily (while leaving S2 shorted)

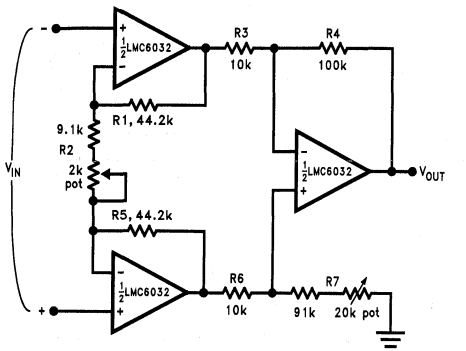
$$I_b^+ = \frac{dV_{OUT}}{dt} \times (C1 + C_X)$$

where C_X is the stray capacitance at the + input.

Typical Single-Supply Applications ($V^+ = 5.0\ V_{DC}$)

Additional single-supply applications ideas can be found in the LM358 datasheet. The LMC6032 is pin-for-pin compatible with the LM358 and offers greater bandwidth and input resistance over the LM358. These features will improve the performance of many existing single-supply applications. Note, however, that the supply voltage range of the LMC6032 is smaller than that of the LM358.

Instrumentation Amplifier



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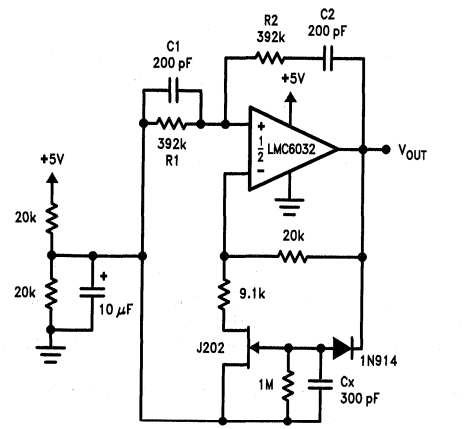
$$\frac{V_{OUT}}{V_{IN}} = \frac{R2 + 2R1}{R2} \times \frac{R4}{R3}$$ if R1 = R5; R3 = R6, and R4 = R7.

= 100 for circuit shown.

For good CMRR over temperature, low drift resistors should be used. Matching of R3 to R6 and R4 to R7 affects CMRR. Gain may be adjusted through R2. CMRR may be adjusted through R7.

Sine-Wave Oscillator



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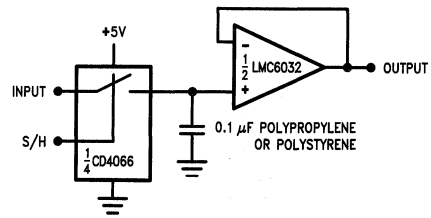
Oscillator frequency is determined by R1, R2, C1, and C2:

$$f_{OSC} = 1/2\pi RC$$

where R = R1 = R2 and C = C1 = C2.

This circuit, as shown, oscillates at 2.0 kHz with a peak-to-peak output swing of 4.0V.

Low-Leakage Sample-and-Hold



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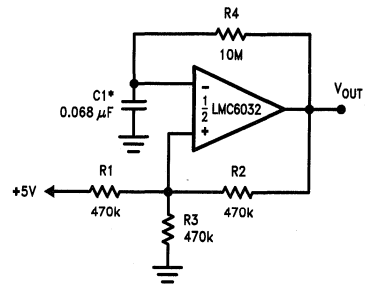
1 Hz Square-Wave Oscillator



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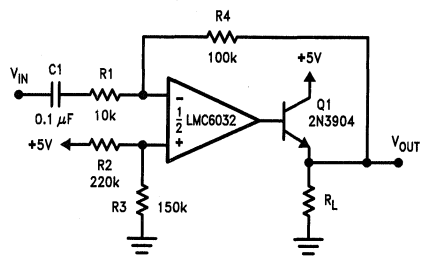
Power Amplifier



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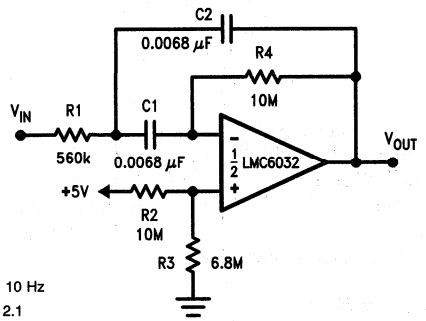
Typical Single-Supply Applications (V^+ = 5.0 V_{DC}) (Continued)

10 Hz Bandpass Filter



f_O = 10 Hz
Q = 2.1
Gain = −8.8

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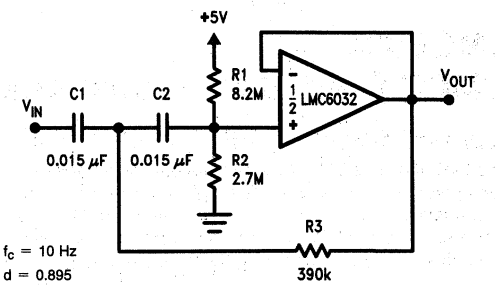
10 Hz High-Pass Filter



f_c = 10 Hz
d = 0.895
Gain = 1
2 dB passband ripple

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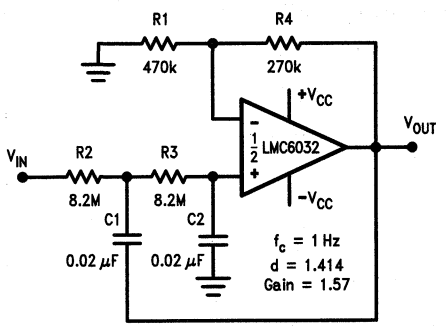
1 Hz Low-Pass Filter (Maximally Flat, Dual Supply Only)



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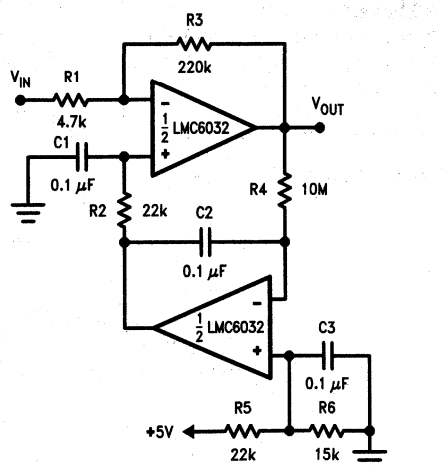
High Gain Amplifier with Offset Voltage Reduction



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Gain = −46.8
Output offset voltage reduced to the level of the input offset voltage of the bottom amplifier (typically 1 mV).

National Semiconductor

LMC6034
CMOS Quad Operational Amplifier

General Description

The LMC6034 is a CMOS quad operational amplifier which can operate from either a single supply or dual supplies. Its performance features include an input common-mode range that reaches ground, low input bias current, and high voltage gain into realistic loads, such as 2 kΩ and 600Ω.

This chip is built with National's advanced Double-Poly Silicon-Gate CMOS process.

See the LMC6032 datasheet for a CMOS dual operational amplifier with these same features. For higher performance characteristics refer to the LMC660.

Features

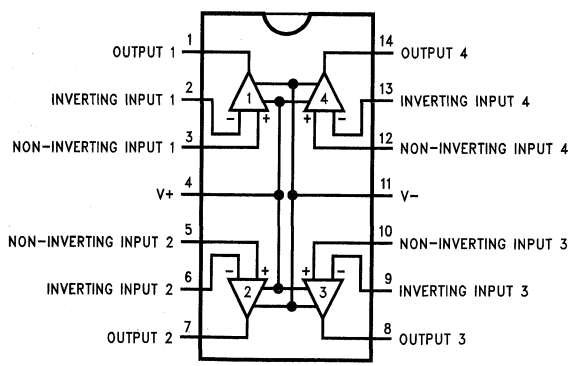
- Specified for 2 kΩ and 600Ω loads
- High voltage gain 126 dB
- Low offset voltage drift 2.3 μV/°C
- Ultra low input bias current 40 fA
- Input common-mode range includes V−
- Operating Range from +5V to +15V supply
- I_{SS} = 400 μA/amplifier; independent of V+
- Low distortion 0.01% at 10 kHz
- Slew rate 1.1 V/μs
- Improved performance over TLC274

Applications

- High-impedance buffer or preamplifier
- Current-to-voltage converter
- Long-term integrator
- Sample-and-hold circuit
- Medical instrumentation

Connection Diagram

14-Pin DIP/SO



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Top View

Ordering Information

Temperature Range Industrial $-40°C \leq T_J \leq +85°C$	Package	NSC Drawing
LMC6034IN	14-Pin Molded DIP	N14A
LMC6034IM	14-Pin Small Outline	M14A

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Differential Input Voltage	±Supply Volt)age
Supply Voltage ($V^+ - V^-$)	16V
Output Short Circuit to V^+	(Note 10)
Output Short Circuit to V^-	(Note 2)
Lead Temperature (Soldering, 10 sec.)	260°C
Storage Temperature Range	−65°C to +150°C
Power Dissipation	(Note 3)
Voltage at Output/Input Pin	(V^+) +0.3V, (V^-) −0.3V
Current at Output Pin	±18 mA
Current at Input Pin	±5 mA
Current at Power Supply Pin	35 mA
Junction Temperature (Note 3)	150°C
ESD Tolerance (Note 4)	500V

Operating Ratings (Note 1)

Temperature Range	$-40°C \le T_J \le +85°C$
Supply Voltage Range	4.75V to 15.5V
Power Dissipation	(Note 11)
Thermal Resistance (θ_{JA}), (Note 12)	
14-Pin DIP	85°C/W
14-Pin SO	115°C/W

DC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for T_J = 25°C. **Boldface** limits apply at the temperature extremes. V^+ = 5V, V^- = GND = 0V, V_{CM} = 1.5V, V_{OUT} = 2.5V, and R_L > 1M unless otherwise specified.

Symbol	Parameter	Conditions	Typical (Note 5)	LMC6034I Limit (Note 6)	Units
V_{OS}	Input Offset Voltage		1	9 **11**	mV max
$\Delta V_{OS}/\Delta T$	Input Offset Voltage Average Drift		2.3		µV/°C
I_B	Input Bias Current		0.04	 **200**	pA max
I_{OS}	Input Offset Current		0.01	 **100**	pA max
R_{IN}	Input Resistance		>1		TeraΩ
CMRR	Common Mode Rejection Ratio	$0V \le V_{CM} \le 12V$ $V^+ = 15V$	83	63 **60**	dB min
+PSRR	Positive Power Supply Rejection Ratio	$5V \le V^+ \le 15V$ $V_O = 2.5V$	83	63 **60**	dB min
−PSRR	Negative Power Supply Rejection Ratio	$0V \le V^- \le -10V$	94	74 **70**	dB min
V_{CM}	Input Common-Mode Voltage Range	$V^+ = 5V$ & 15V For CMRR ≥ 50 dB	−0.4	−0.1 **0**	V max
			$V^+ - 1.9$	$V^+ - 2.3$ $\mathbf{V^+ - 2.6}$	V min
A_V	Large Signal Voltage Gain	$R_L = 2k\Omega$ (Note 7) Sourcing	2000	200 **100**	V/mV min
		Sinking	500	90 **40**	V/mV min
		$R_L = 600\Omega$ (Note 7) Sourcing	1000	100 **75**	V/mV min
		Sinking	250	50 **20**	V/mV min

DC Electrical Characteristics (Continued)

Unless otherwise specified, all limits guaranteed for T_J = 25°C. **Boldface** limits apply at the temperature extremes. V^+ = 5V, V^- = GND = 0V, V_{CM} = 1.5V, V_{OUT} = 2.5V, and R_L > 1M unless otherwise specified.

Symbol	Parameter	Conditions	Typical (Note 5)	LMC6034I Limit (Note 6)	Units
V_O	Output Voltage Swing	V^+ = 5V R_L = 2 kΩ to 2.5V	4.87	4.20 **4.00**	V min
			0.10	0.25 **0.35**	V max
		V^+ = 5V R_L = 600Ω to 2.5V	4.61	4.00 **3.80**	V min
			0.30	0.63 **0.75**	V max
		V^+ = 15V R_L = 2 kΩ to 7.5V	14.63	13.50 **13.00**	V min
			0.26	0.45 **0.55**	V max
		V^+ = 15V R_L = 600Ω to 7.5V	13.90	12.50 **12.00**	V min
			0.79	1.45 **1.75**	V max
I_O	Output Current	V^+ = 5V Sourcing, V_O = 0V	22	13 **9**	mA min
		Sinking, V_O = 5V	21	13 **9**	mA min
		V^+ = 15V Sourcing, V_O = 0V	40	23 **15**	mA min
		Sinking, V_O = 13V (Note 10)	39	23 **15**	mA min
I_S	Supply Current	All Four Amplifiers V_O = 1.5V	1.5	2.7 **3.0**	mA max

AC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for T_J = 25°C. **Boldface** limits apply at the temperature extremes. V^+ = 5V, V^- = GND = 0V, V_{CM} = 1.5V, V_{OUT} = 2.5V, and R_L > 1M unless otherwise specified.

Symbol	Parameter	Conditions	Typical (Note 5)	LMC6034I Limit (Note 6)	Units
SR	Slew Rate	(Note 8)	1.1	0.8 **0.4**	V/μs min
GBW	Gain-Bandwidth Product		1.4		MHz
ϕ_M	Phase Margin		50		Deg
G_M	Gain Margin		17		dB
	Amp-to-Amp Isolation	(Note 9)	130		dB
e_n	Input-Referred Voltage Noise	F = 1 kHz	22		nV/$\sqrt{Hz}$
i_n	Input-Referred Current Noise	F = 1 kHz	0.0002		pA/$\sqrt{Hz}$
THD	Total Harmonic Distortion	F = 10 kHz, A_V = −10 R_L = 2 kΩ, V_O = 8 V_{PP} ±5V Supply	0.01		%

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the component may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed.

Note 2: Applies to both single-supply and split-supply operation. Continuous short circuit operation at elevated ambient temperature and/or multiple Op Amp shorts can result in exceeding the maximum allowed junction temperature of 150°C. Output currents in excess of ±30 mA over long term may adversely affect reliability.

Note 3: The maximum power dissipation is a function of $T_{J(max)}$, θ_{JA}, T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(max)} - T_A)/\theta_{JA}$.

Note 4: Human body model, 100 pF discharged through a 1.5 kΩ resistor.

Note 5: Typical values represent the most likely parametric norm.

Note 6: All limits are guaranteed at room temperature (standard type face) or at operating temperature extremes (**bold type face**).

Note 7: V^+ = 15V, V_{CM} = 7.5V, and R_L connected to 7.5V. For Sourcing tests, 7.5V ≤ V_O ≤ 11.5V. For Sinking tests, 2.5V ≤ V_O ≤ 7.5V.

Note 8: V^+ = 15V. Connected as Voltage Follower with 10V step input. Number specified is the slower of the positive and negative slew rates.

Note 9: Input referred. V^+ = 15V and R_L = 10 kΩ connected to $V^+/2$. Each amp excited in turn with 1 kHz to produce V_O = 13 V_{PP}.

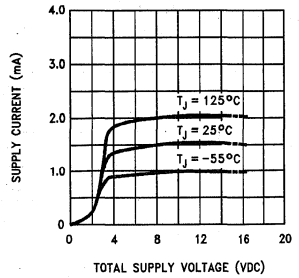
Note 10: Do not connect output to V^+, when V^+ is greater than 13V or reliability may be adversely affected.

Note 11: For operating at elevated temperatures the device must be derated based on the thermal resistance θ_{JA} with $P_D = (T_J - T_A)/\theta_{JA}$.

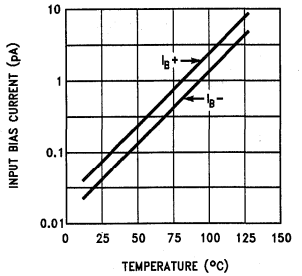
Note 12: All numbers apply for packages soldered directly into a PC board.

Typical Performance Characteristics $V_S = \pm 7.5V$, $T_A = 25°C$ unless otherwise specified

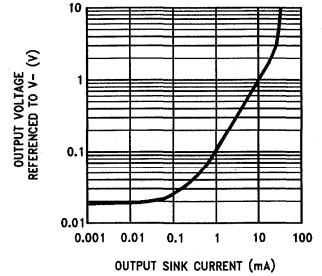
Supply Current vs Supply Voltage



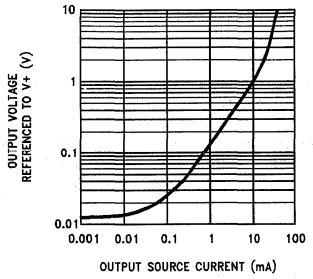
Input Bias Current



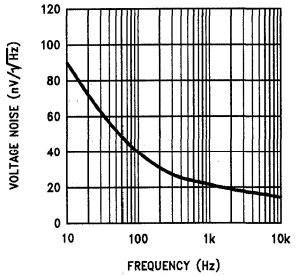
Output Characteristics Current Sinking



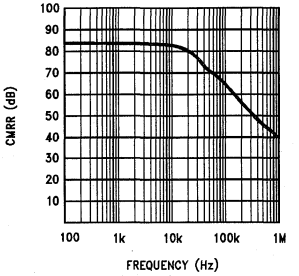
Output Characteristics Current Sourcing



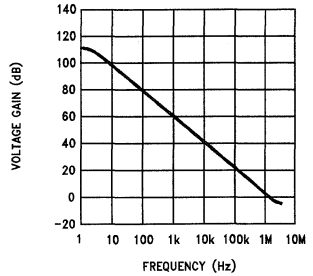
Input Voltage Noise vs Frequency



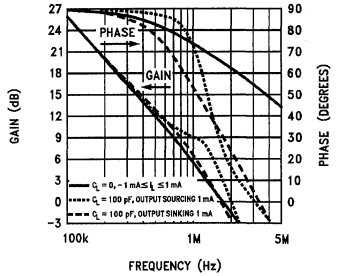
CMRR vs Frequency



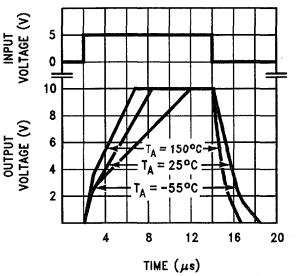
Open-Loop Frequency Response



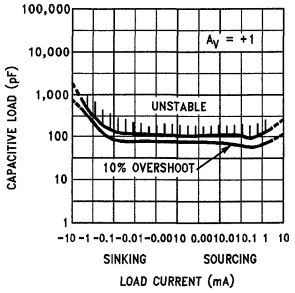
Frequency Response vs Capacitive Load



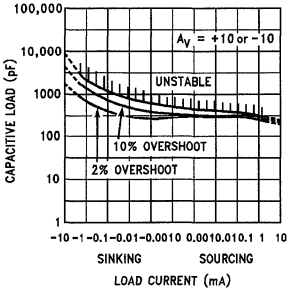
Non-Inverting Large Signal Pulse Response



Stability vs Capacitive Load



Stability vs Capacitive Load



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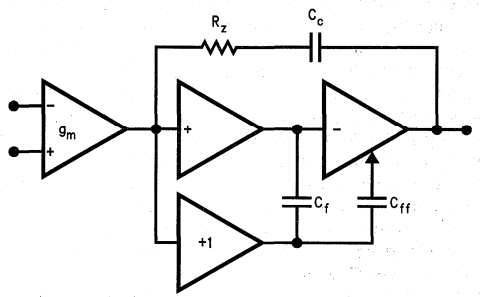
Note: Avoid resistive loads of less than 500Ω, as they may cause instability.

Applications Hint

Amplifier Topolgy

The topology chosen for the LMC6034, shown in *Figure 1*, is unconventional (compared to general-purpose op amps) in that the traditional unity-gain buffer output stage is not used; instead, the output is taken directly from the output of the integrator, to allow a larger output swing. Since the buffer traditionally delivers the power to the load, while maintaining high op amp gain and stability, and must withstand shorts to either rail, these tasks now fall to the integrator.

As a result of these demands, the integrator is a compound affair with an embedded gain stage that is doubly fed forward (via C_f and Cff) by a dedicated unity-gain compensation driver. In addition, the output portion of the integrator is a push-pull configuration for delivering heavy loads. While sinking current the whole amplifier path consists of three gain stages with one stage fed forward, whereas while sourcing the path contains four gain stages with two fed forward.



TL/H/11134–3

FIGURE 1. LMC6034 Circuit Topology (Each Amplifier)

The large signal voltage gain while sourcing is comparable to traditional bipolar op amps, even with a 600Ω load. The gain while sinking is higher than most CMOS op amps, due to the additional gain stage; however, under heavy load (600Ω) the gain will be reduced as indicated in the Electrical Characteristics.

Compensating Input Capacitance

The high input resistance of the LMC6034 op amps allows the use of large feedback and source resistor values without losing gain accuracy due to loading. However, the circuit will be especially sensitive to its layout when these large-value resistors are used.

Every amplifier has some capacitance between each input and AC ground, and also some differential capacitance between the inputs. When the feedback network around an amplifier is resistive, this input capacitance (along with any additional capacitance due to circuit board traces, the socket, etc.) and the feedback resistors create a pole in the feedback path. In the following General Operational Amplifier circuit, *Figure 2* the frequency of this pole is

$$fp = \frac{1}{2\pi C_S R_P}$$

where C_S is the total capacitance at the inverting input, including amplifier input capcitance and any stray capacitance from the IC socket (if one is used), circuit board traces, etc., and R_P is the parallel combination of R_F and R_{IN}. This formula, as well as all formulae derived below, apply to inverting and non-inverting op-amp configurations.

When the feedback resistors are smaller than a few kΩ, the frequency of the feedback pole will be quite high, since C_S is generally less than 10 pF. If the frequency of the feedback pole is much higher than the "ideal" closed-loop bandwidth (the nominal closed-loop bandwidth in the absence of C_S), the pole will have a negligible effect on stability, as it will add only a small amount of phase shift.

However, if the feedback pole is less than approximately 6 to 10 times the "ideal" −3 dB frequency, a feedback capacitor, C_F, should be connected between the output and the inverting input of the op amp. This condition can also be stated in terms of the amplifier's low-frequency noise gain: To maintain stability a feedback capacitor will probably be needed if

$$\left(\frac{R_F}{R_{IN}} + 1\right) \leq \sqrt{6 \times 2\pi \times GBW \times R_F \times C_S}$$

where $\left(\frac{R_F}{R_{IN}} + 1\right)$ is the amplifier's low-frequency noise gain and GBW is the amplifier's gain bandwidth product. An amplifier's low-frequency noise gain is represented by the formula $\left(\frac{R_F}{R_{IN}} + 1\right)$ regardless of whether the amplifier is being used in inverting or non-inverting mode. Note that a feedback capacitor is more likely to be needed when the noise gain is low and/or the feedback resistor is large.

If the above condition is met (indicating a feedback capacitor will probably be needed), and the noise gain is large enough that:

$$\left(\frac{R_F}{R_{IN}} + 1\right) \geq 2\sqrt{GBW \times R_F \times C_S},$$

the following value of feedback capacitor is recommended:

$$C_F = \frac{C_S}{2\left(\frac{R_F}{R_{IN}} + 1\right)}$$

If

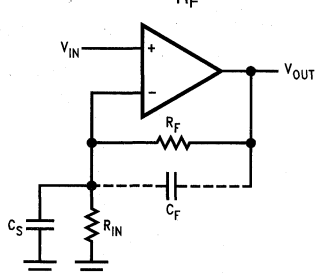
$$\left(\frac{R_F}{R_{IN}} + 1\right) < 2\sqrt{GBW \times R_F \times C_S}$$

the feedback capacitor should be:

$$C_F = \sqrt{\frac{C_S}{GBW \times R_F}}$$

Note that these capacitor values are usually significant smaller than those given by the older, more conservative formula:

$$C_F = \frac{C_S R_{IN}}{R_F}$$



TL/H/11134–4

FIGURE 2. General Operational Amplifier Circuit

C_S consists of the amplifier's input capacitance plus any stray capacitance from the circuit board and socket. C_F compensates for the pole caused by C_S and the feedback resistors.

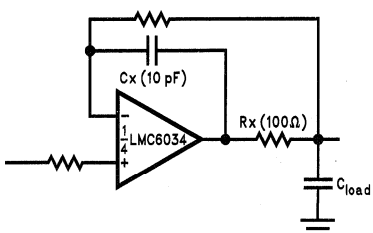
Applications Hint (Continued)

Using the smaller capacitors will give much higher bandwidth with little degradation of transient response. It may be necessary in any of the above cases to use a somewhat larger feedback capacitor to allow for unexpected stray capacitance, or to tolerate additional phase shifts in the loop, or excessive capacitive load, or to decrease the noise or bandwidth, or simply because the particular circuit implementation needs more feedback capacitance to be sufficiently stable. For example, a printed circuit board's stray capacitance may be larger or smaller than the breadboard's, so the actual optimum value for C_F may be different from the one estimated using the breadboard. In most cases, the values of C_F should be checked on the actual circuit, starting with the computed value.

Capacitive Load Tolerance

Like many other op amps, the LMC6034 may oscillate when its applied load appears capacitive. The threshold of oscillation varies both with load and circuit gain. The configuration most sensitive to oscillation is a unity-gain follower. See Typical Performance Characteristics.

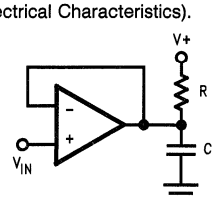
The load capacitance interacts with the op amp's output resistance to create an additional pole. If this pole frequency is sufficiently low, it will degrade the op amp's phase margin so that the amplifier is no longer stable at low gains. As shown in *Figure 3a,* the addition of a small resistor (50Ω to 100Ω) in series with the op amp's output, and a capacitor (5 pF to 10 pF) from inverting input to output pins, returns the phase margin to a safe value without interfering with lower-frequency circuit operation. Thus larger values of capacitance can be tolerated without oscillation. Note that in all cases, the output will ring heavily when the load capacitance is near the threshold for oscillation.



TL/H/11134–5

FIGURE 3a. Rx, Cx Improve Capacitive Load Tolerance

Capacitive load driving capability is enhanced by using a pull up resistor to V^+ (*Figure 3b*). Typically a pull up resistor conducting 500 μA or more will significantly improve capacitive load responses. The value of the pull up resistor must be determined based on the current sinking capability of the amplifier with respect to the desired output swing. Open loop gain of the amplifier can also be affected by the pull up resistor (see Electrical Characteristics).



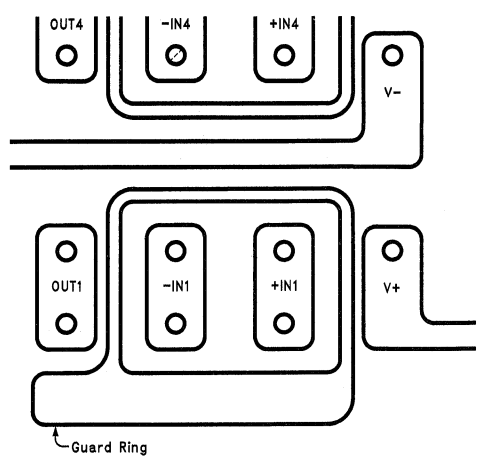
TL/H/11134–22

FIGURE 3b. Compensating for Large Capacitive Loads with a Pull Up Resistor

PRINTED-CIRCUIT-BOARD LAYOUT FOR HIGH-IMPEDANCE WORK

It is generally recognized that any circuit which must operate with less than 1000 pA of leakage current requires special layout of the PC board. When one wishes to take advantage of the ultra-low bias current of the LMC6034, typically less than 0.04 pA, it is essential to have an excellent layout. Fortunately, the techniques for obtaining low leakages are quite simple. First, the user must not ignore the surface leakage of the PC board, even though it may sometimes appear acceptably low, because under conditions of high humidity or dust or contamination, the surface leakage will be appreciable.

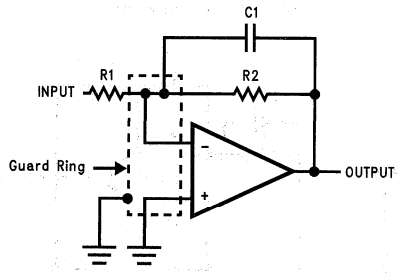
To minimize the effect of any surface leakage, lay out a ring of foil completely surrounding the LMC6034's inputs and the terminals of capacitors, diodes, conductors, resistors, relay terminals, etc. connected to the op-amp's inputs. See *Figure 4.* To have a significant effect, guard rings should be placed on both the top and bottom of the PC board. This PC foil must then be connected to a voltage which is at the same voltage as the amplifier inputs, since no leakage current can flow between two points at the same potential. For example, a PC board trace-to-pad resistance of $10^{12}\Omega$, which is normally considered a very large resistance, could leak 5 pA if the trace were a 5V bus adjacent to the pad of an input. This would cause a 100 times degradation from the LMC6034's actual performance. However, if a guard ring is held within 5 mV of the inputs, then even a resistance of $10^{11}\Omega$ would cause only 0.05 pA of leakage current, or perhaps a minor (2:1) degradation of the amplifier's performance. See *Figures 5a, 5b, 5c* for typical connections of guard rings for standard op-amp configurations. If both inputs are active and at high impedance, the guard can be tied to ground and still provide some protection; see *Figure 5d.*



TL/H/11134–6

FIGURE 4. Example of Guard Ring in P.C. Board Layout

Application Hints (Continued)



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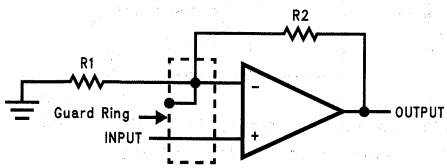
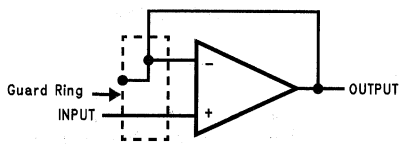
(a) Inverting Amplifier



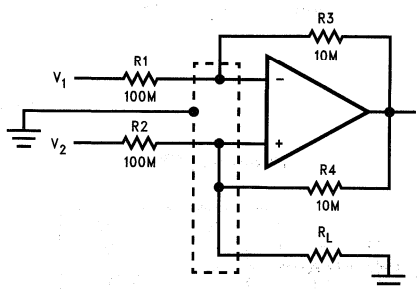
TL/H/11134–8

(b) Non-Inverting Amplifier



TL/H/11134–9

(c) Follower

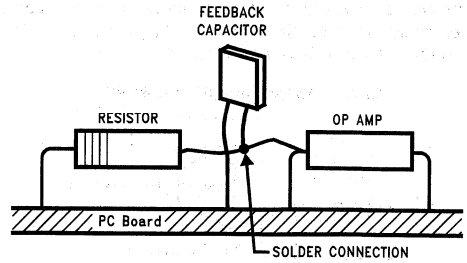


TL/H/11134–10

(d) Howland Current Pump

FIGURE 5. Guard Ring Connections

The designer should be aware that when it is inappropriate to lay out a PC board for the sake of just a few circuits, there is another technique which is even better than a guard ring on a PC board: Don't insert the amplifier's input pin into the board at all, but bend it up in the air and use only air as an insulator. Air is an excellent insulator. In this case you may have to forego some of the advantages of PC board construction, but the advantages are sometimes well worth the effort of using point-to-point up-in-the-air wiring. See *Figure 6*.



TL/H/11134–11

(Input pins are lifted out of PC board and soldered directly to components. All other pins connected to PC board.)

FIGURE 6. Air Wiring

BIAS CURRENT TESTING

The test method of *Figure 7* is appropriate for bench-testing bias current with reasonable accuracy. To understand its operation, first close switch S2 momentarily. When S2 is opened, then

$$I_b^- = \frac{dV_{OUT}}{dt} \times C2.$$

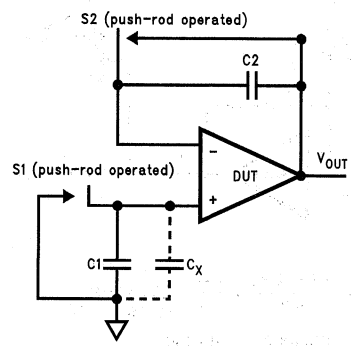


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FIGURE 7. Simple Input Bias Current Test Circuit

A suitable capacitor for C2 would be a 5 pF or 10 pF silver mica, NPO ceramic, or air-dielectric. When determining the magnitude of I_b^-, the leakage of the capacitor and socket must be taken into account. Switch S2 should be left shorted most of the time, or else the dielectric absorption of the capacitor C2 could cause errors.

Similarly, if S1 is shorted momentarily (while leaving S2 shorted)

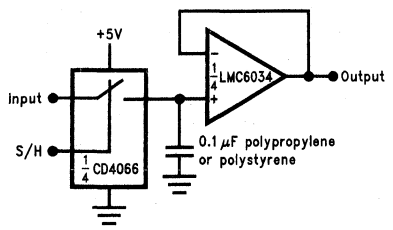
$$I_b^+ = \frac{dV_{OUT}}{dt} \times (C1 + C_X)$$

where C_X is the stray capacitance at the + input.

Typical Single-Supply Applications (V^+ = 5.0 VDC)

Additional single-supply applications ideas can be found in the LM324 datasheet. The LMC6034 is pin-for-pin compatible with the LM324 and offers greater bandwidth and input resistance over the LM324. These features will improve the performance of many existing single-supply applications. Note, however, that the supply voltage range of the LMC6034 is smaller than that of the LM324.

Low-Leakage Sample-and-Hold



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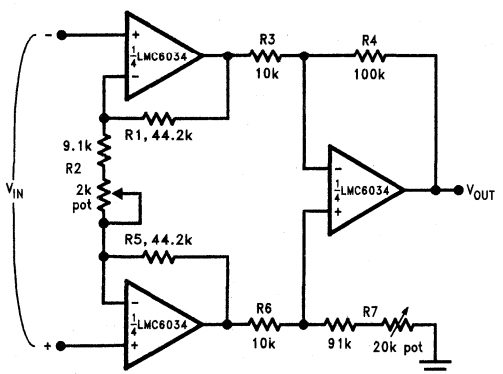
Instrumentation Amplifier



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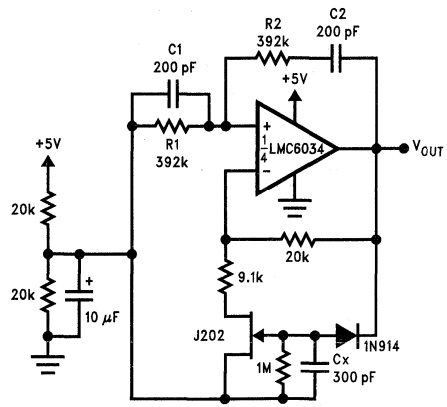
$$\frac{V_{OUT}}{V_{IN}} = \frac{R2 + 2R1}{R2} \times \frac{R4}{R3} \quad \begin{array}{l}\text{if } R1 = R5 \\ R3 = R6, \\ \text{and } R4 = R7.\end{array}$$

$$= 100 \text{ for circuit as shown.}$$

For good CMRR over temperature, low drift resistors should be used. Matching of R3 to R6 and R4 to R7 affect CMRR. Gain may be adjusted through R2. CMRR may be adjusted through R1.

Sine-Wave Oscillator



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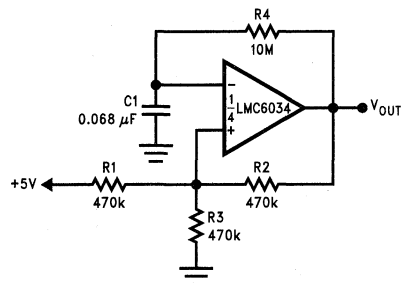
Oscillator frequency is determined by R1, R2, C1, and C2:

$f_{OSC} = 1/2\pi RC$, where $R = R1 = R2$ and $C = C1 = C2$.

This circuit, as shown, oscillates at 2.0 kHz with a peak-to-peak output swing of 4.0V.

1 Hz Square-Wave Oscillator



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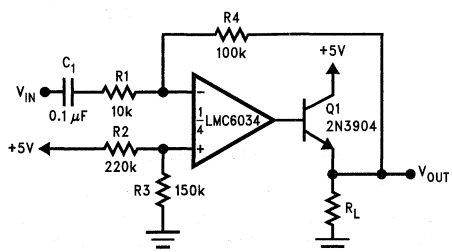
Power Amplifier



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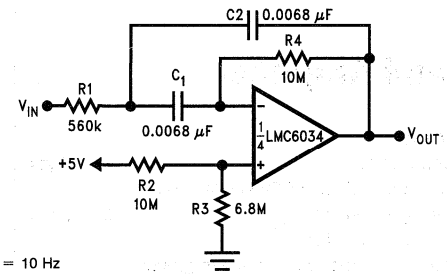
Typical Single-Supply Applications (V^+ = 5.0 VDC) (Continued)

10 Hz Bandpass Filter



f_O = 10 Hz
Q = 2.1
Gain = −8.8

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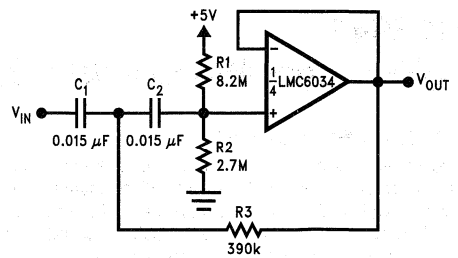
10 Hz High-Pass Filter



f_c = 10 Hz
d = 0.895
Gain = 1
2 dB passband ripple

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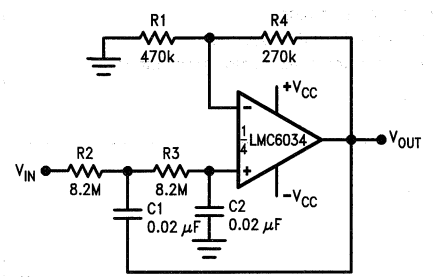
1 Hz Low-Pass Filter (Maximally Flat, Dual Supply Only)



f_c = 1 Hz
d = 1.414
Gain = 1.57

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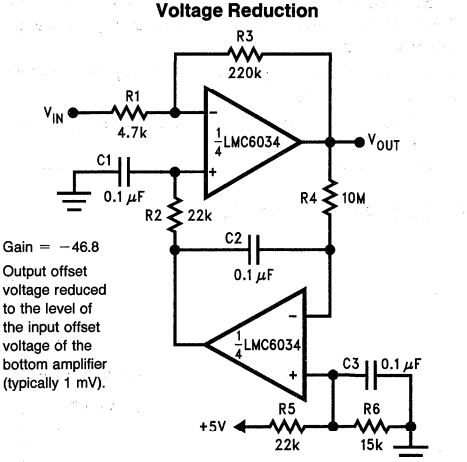
High Gain Amplifier with Offset Voltage Reduction



Gain = −46.8

Output offset voltage reduced to the level of the input offset voltage of the bottom amplifier (typically 1 mV).

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National Semiconductor

LMC6041
CMOS Single Micropower Operational Amplifier

General Description

Ultra-low power consumption and low input-leakage current are the hallmarks of the LMC6041. Providing input currents of only 2 fA typical, the LMC6041 can operate from a single supply, has output swing extending to each supply rail, and an input voltage range that includes ground.

The LMC6041 is ideal for use in systems requiring ultra-low power consumption. In addition, the insensitivity to latch-up, high output drive, and output swing to ground without requiring external pull-down resistors make it ideal for single-supply battery-powered systems.

Other applications for the LMC6041 include bar code reader amplifiers, magnetic and electric field detectors, and hand-held electrometers.

This device is built with National's advanced Double-Poly Silicon-Gate CMOS process.

See the LMC6042 for a dual, and the LMC6044 for a quad amplifier with these features.

Features

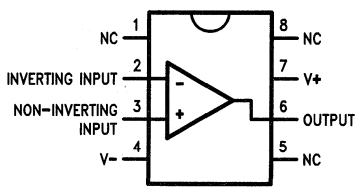
- Low supply current 14 μA (Typ)
- Operates from 4.5V to 15.5V single supply
- Ultra low input current 2 fA (Typ)
- Rail-to-rail output swing
- Input common-mode range includes ground

Applications

- Battery monitoring and power conditioning
- Photodiode and infrared detector preamplifier
- Silicon based transducer systems
- Hand-held analytic instruments
- pH probe buffer amplifier
- Fire and smoke detection systems
- Charge amplifier for piezoelectric transducers

Connection Diagram

8-Pin DIP/SO



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Ordering Information

Package	Temperature Range Industrial −40°C to +85°C	NSC Drawing
8-Pin Small Outline	LMC6041AIM LMC6041IM	M08A
8-Pin Molded DIP	LMC6041AIN LM6041IN	N08E

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Differential Input Voltage	±Supply Voltage
Supply Voltage ($V^+ - V^-$)	16V
Output Short Circuit to V^-	(Note 2)
Output Short Circuit to V^+	(Note 11)
Lead Temperature (Soldering, 10 sec.)	260°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature	110°C
ESD Tolerance (Note 4)	500V
Current at Input Pin	±5 mA
Current at Output Pin	±18 mA
Current at Power Supply Pin	35 mA
Voltage at Input/Output Pin	$(V^+) + 0.3V, (V^-) - 0.3V$
Power Dissipation	(Note 3)

Operating Ratings

Temperature Range	
LMC6041AI, LMC6041I	$-40°C \le T_J \le +85°C$
Supply Voltage	$4.5V \le V^+ \le 15.5V$
Power Dissipation	(Note 9)
Thermal Resistance (θ_{JA}) (Note 10)	
8-Pin DIP	101°C/W
8-Pin SO	165°C/W

Electrical Characteristics

Unless otherwise specified, all limits guaranteed for $T_A = T_J = 25°C$. **Boldface** limits apply at the temperature extremes. $V^+ = 5V$, $V^- = 0V$, $V_{CM} = 1.5V$, $V_O = V^+/2$, and $R_L > 1M$ unless otherwise specified.

Symbol	Parameter	Conditions		Typical (Note 5)	LMC6041AI Limit (Note 6)	LMC6041I Limit (Note 6)	Units (Limit)
V_{OS}	Input Offset Voltage			1	3 **3.3**	6 **6.3**	mV max
TCV_{OS}	Input Offset Voltage Average Drift			1.3			μV/°C
I_B	Input Bias Current			0.002	**4**	**4**	pA max
I_{OS}	Input Offset Current			0.001	**2**	**2**	pA max
R_{IN}	Input Resistance			>10			TeraΩ
CMRR	Common Mode Rejection Ratio	$0V \le V_{CM} \le 12.0V$ $V^+ = 15V$		75	68 **66**	62 **60**	dB min
+PSRR	Positive Power Supply Rejection Ratio	$5V \le V^+ \le 15V$ $V_O = 2.5V$		75	68 **66**	62 **60**	dB min
−PSRR	Negative Power Supply Rejection Ratio	$0V \le V^- \le -10V$ $V_O = 2.5V$		94	84 **83**	74 **73**	dB min
CMR	Input Common-Mode Voltage Range	$V^+ = 5V$ and 15V for CMRR ≥ 50 dB		−0.4	−0.1 **0**	−0.1 **0**	V max
				$V^+ - 1.9V$	$V^+ - 2.3V$ $\mathbf{V^+ - 2.5V}$	$V^+ - 2.3V$ $\mathbf{V^+ - 2.4V}$	V min
A_V	Large Signal Voltage Gain	$R_L = 100 k\Omega$ (Note 7)	Sourcing	1000	400 **300**	300 **200**	V/mV min
			Sinking	500	180 **120**	90 **70**	V/mV min
		$R_L = 25 k\Omega$ (Note 7)	Sourcing	1000	200 **160**	100 **80**	V/mV min
			Sinking	250	100 **60**	50 **40**	V/mV min

Electrical Characteristics

Unless otherwise specified, all limits guaranteed for $T_A = T_J = 25°C$. **Boldface** limits apply at the temperature extremes. $V^+ = 5V$, $V^- = 0V$, $V_{CM} = 1.5V$, $V_O = V^+/2$, and $R_L > 1M$ unless otherwise specified.

Symbol	Parameter	Conditions	Typical (Note 5)	LMC6041AI Limit (Note 6)	LMC6041I Limit (Note 6)	Units (Limit)
V_O	Output Swing	$V^+ = 5V$ $R_L = 100 k\Omega$ to $V^+/2$	4.987	4.970 **4.950**	4.940 **4.910**	V min
			0.004	0.030 **0.050**	0.060 **0.090**	V max
		$V^+ = 5V$ $R_L = 25 k\Omega$ to $V^+/2$	4.980	4.920 **4.870**	4.870 **4.820**	V min
			0.010	0.080 **0.130**	0.130 **0.180**	V max
		$V^+ = 15V$ $R_L = 100 k\Omega$ to $V^+/2$	14.970	14.920 **14.880**	14.880 **14.820**	V min
			0.007	0.030 **0.050**	0.060 **0.090**	V max
		$V^+ = 15V$ $R_L = 25 k\Omega$ to $V^+/2$	14.950	14.900 **14.850**	14.850 **14.800**	V min
			0.022	0.100 **0.150**	0.150 **0.200**	V max
I_{SC}	Output Current $V^+ = 5V$	Sourcing, $V_O = 0V$	22	16 **10**	13 **8**	mA min
		Sinking, $V_O = 5V$	21	16 **8**	13 **8**	mA min
I_{SC}	Output Current $V^+ = 15V$	Sourcing, $V_O = 0V$	40	15 **10**	15 **10**	mA min
		Sinking, $V_O = 13V$ (Note 11)	39	24 **8**	21 **8**	mA min
I_S	Supply Current	$V_O = 1.5V$	14	20 **24**	26 **30**	μA max
		$V^+ = 15V$	18	26 **31**	34 **39**	μA max

AC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for $T_A = T_J = 25°C$. **Boldface** limits apply at the temperature extremes. $V^+ = 5V$, $V^- = 0V$, $V_{CM} = 1.5V$, $V_O = V^+/2$, and $R_L > 1M$ unless otherwise specified.

Symbol	Parameter	Conditions	Typ (Note 5)	LMC6041AI Limit (Note 6)	LMC6041I Limit (Note 6)	Units (Limit)
SR	Slew Rate	(Note 8)	0.02	0.015 **0.010**	0.010 **0.007**	V/μs min
GBW	Gain-Bandwidth Product		75			kHz
ϕ_m	Phase Margin		60			Deg
e_n	Input-Referred Voltage Noise	F = 1 kHz	83			nV/√Hz
i_n	Input-Referred Current Noise	F = 1 kHz	0.0002			pA/√Hz
T.H.D.	Total Harmonic Distortion	F = 1 kHz, $A_V = -5$ $R_L = 100\ k\Omega$, $V_O = 2\ V_{pp}$ ±5V Supply	0.01			%

Note 1: Absolute Maxium Ratings indicate limits beyond which damage to the device may occur. Operating conditions indicate conditions for which the device is intended to be functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed.

Note 2: Applies to both single-supply and split-supply operation. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 110°C. Output currents in excess of ±30 mA over long term may adversely affect reliability.

Note 3: The maximum power dissipation is a function of $T_{J(max)}$, θ_{JA}, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(max)} - T_A)/\theta_{JA}$.

Note 4: Human body model, 1.5 kΩ in series with 100 pF.

Note 5: Typical Values represent the most likely parametric norm.

Note 6: All limits are guaranteed at room temperature (standard type face) or at operating temperature extremes **(bold face type)**.

Note 7: $V^+ = 15V$, $V_{CM} = 7.5V$ and R_L connected to 7.5V. For Sourcing tests, $7.5V \le V_O \le 11.5V$. For Sinking tests, $2.5V \le V_O \le 7.5V$.

Note 8: $V^+ = 15V$. Connected as Voltage Follower with 10V step input. Number specified in the slower of the positive and negative slew rates.

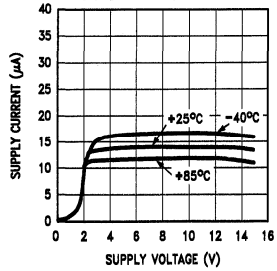
Note 9: For operating at elevated temperatures the device must be derated based on the thermal resistance θ_{JA} with $P_D = (T_J - T_A)/\theta_{JA}$.

Note 10: All numbers apply for packages soldered directly into a PC board.

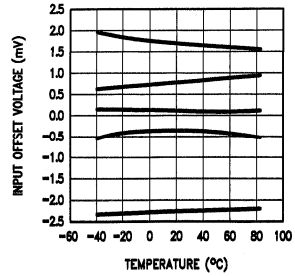
Note 11: Do not connect output to V^+ when V^+ is greater than 13V or reliability may be adversely affected.

Typical Performance Characteristics $V_S = \pm 7.5V$, $T_A = 25°C$ unless otherwise specified

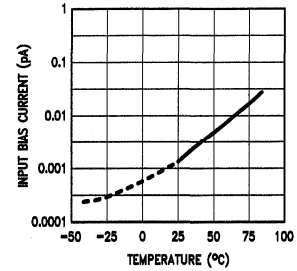
Supply Current vs Supply Voltage



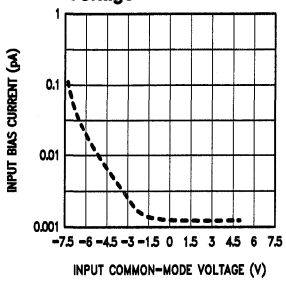
Offset Voltage vs Temperature of Five Representative Units



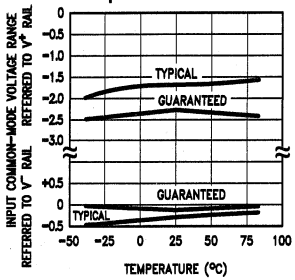
Input Bias Current vs Temperature



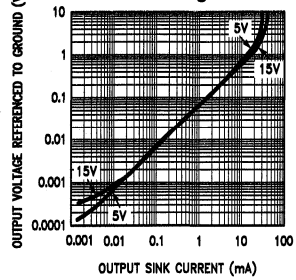
Input Bias Current vs Input Common-Mode Voltage



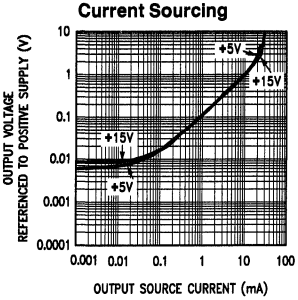
Input Common-Mode Voltage Range vs Temperature



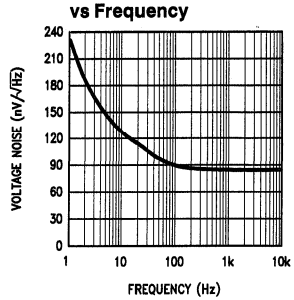
Output Characteristics Current Sinking



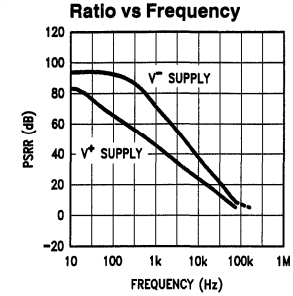
Output Characteristics Current Sourcing



Input Voltage Noise vs Frequency



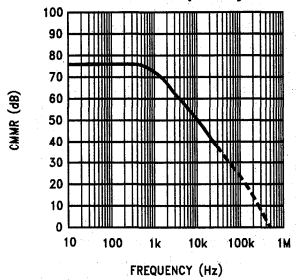
Power Supply Rejection Ratio vs Frequency



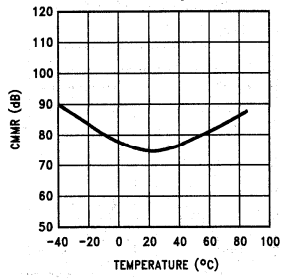
TL/H/11136–2

Typical Performance Characteristics $V_S = \pm 7.5V$, $T_A = 25°C$ unless otherwise specified (Continued)

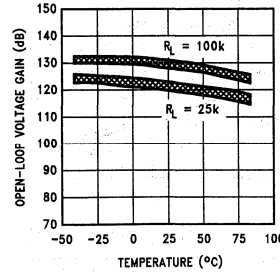
CMRR vs Frequency



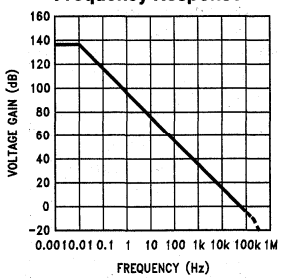
CMRR vs Temperature



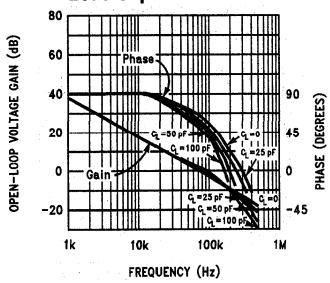
Open-Loop Voltage Gain vs Temperature



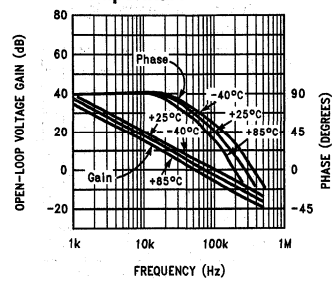
Open-Loop Frequency Response



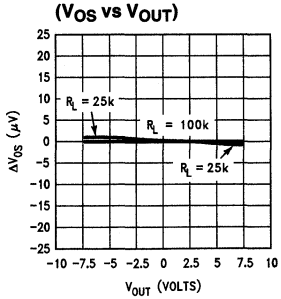
Gain and Phase Responses vs Load Capacitance



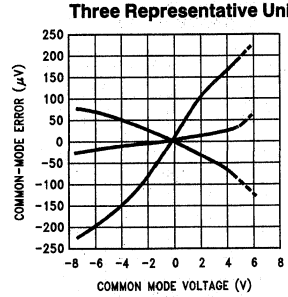
Gain and Phase Responses vs Temperature



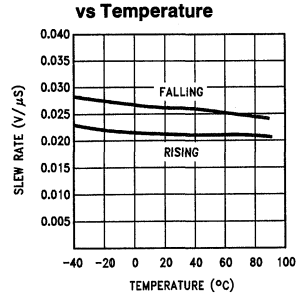
Gain Error (V_{OS} vs V_{OUT})



Common-Mode Error vs Common-Mode Voltage of Three Representative Units



Non-Inverting Slew Rate vs Temperature



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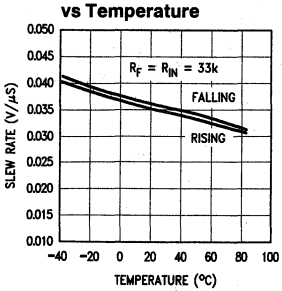
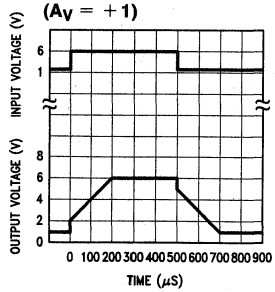
Typical Performance Characteristics $V_S = \pm 7.5V$, $T_A = 25°C$ unless otherwise specified (Continued)

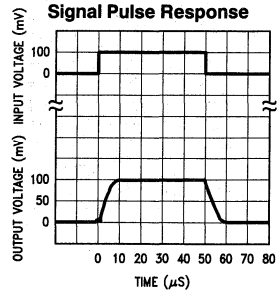
Inverting Slew Rate vs Temperature



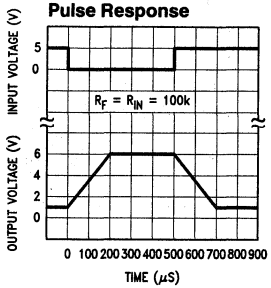
Non-Inverting Large Signal Pulse Response ($A_V = +1$)



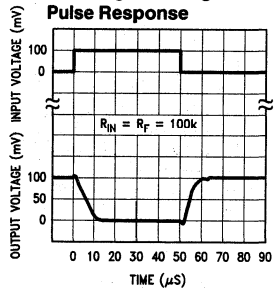
Non-Inverting Small Signal Pulse Response



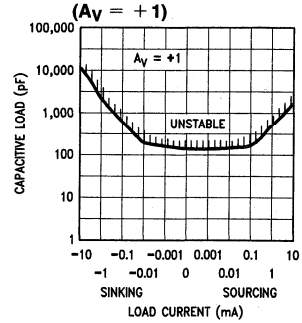
Inverting Large-Signal Pulse Response



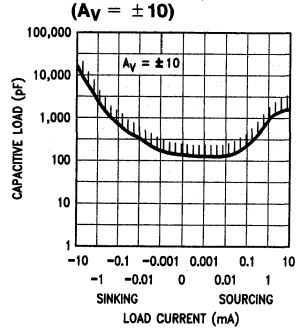
Inverting Small Signal Pulse Response



Stability vs Capacitive Load ($A_V = +1$)



Stability vs Capacitive Load ($A_V = \pm 10$)



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Applications Hints

AMPLIFIER TOPOLOGY

The LMC6041 incorporates a novel op-amp design topology that enables it to maintain rail-rail output swing even when driving a large load. Instead of relying on a push-pull unity gain output buffer stage, the output stage is taken directly from the internal integrator, which provides both low output impedance and large gain. Special feed-forward compensation design techniques are incorporated to maintain stability over a wider range of operating conditions than traditional micropower op-amps. These features make the LMC6041 both easier to design with, and provide higher speed than products typically found in this ultra-low power class.

COMPENSATING FOR INPUT CAPACITANCE

It is quite common to use large values of feedback resistance with amplifiers with ultra-low input current, like the LMC6041.

Although the LMC6041 is highly stable over a wide range of operating conditions, certain precautions must be met to achieve the desired pulse response when a large feedback resistor is used. Large feedback resistors and even small values of input capacitance, due to transducers, photodiodes, and circuits board parasitics, reduce phase margins.

When high input impedance are demanded, guarding of the LMC6041 is suggested. Guarding input lines will not only reduce leakage, but lowers stray input capacitance as well. (See **Printed-Circuit-Board Layout for High Impedance Work.**)

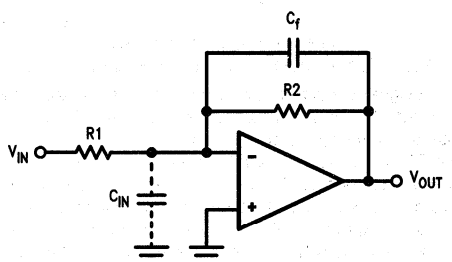

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FIGURE 1. Cancelling the Effect of Input Capacitance

The effect of input capacitance can be compensated for by adding a capacitor. Adding a capacitor, C_f, around the feedback resistor (as in *Figure 1*) such that:

$$\frac{1}{2\pi R_1 C_{IN}} \geq \frac{1}{2\pi R_2 C_f}$$

or

$$R_1 C_{IN} \leq R_2 C_f$$

Since it is often difficult to know the exact value of C_{IN}, C_f can be experimentally adjusted so that the desired pulse response is achieved. Refer to the LMC660 and the LMC662 for a more detailed discussion on compensating for input capacitance.

CAPACITIVE LOAD TOLERANCE

Direct capacitive loading will reduce the phase margin of many op-amps. A pole in the feedback loop is created by the combination of the op-amp's output impedance and the capacitive load. This pole induces phase lag at the unity-gain crossover frequency of the amplifier resulting in either an oscillatory or underdamped pulse response. With a few external components, op amps can easily indirectly drive capacitive loads, as shown in *Figure 2a*.

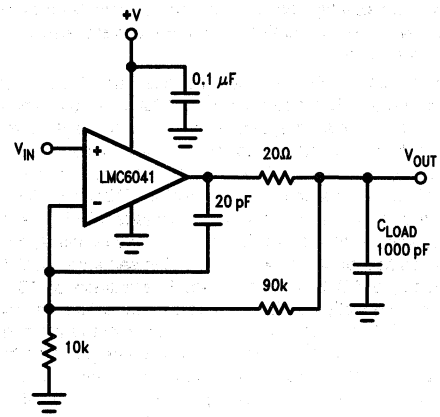

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FIGURE 2a. LMC6041 Noninverting Gain of 10 Amplifier, Compensated to Handle Capacitive Loads

In the circuit of *Figure 2a*, R1 and C1 serve to counteract the loss of phase margin by feeding the high frequency component of the output signal back to the amplifier's inverting input, thereby preserving phase margin in the overall feedback loop.

Capacitive load driving capability is enhanced by using a pull up resistor to V^+ (*Figure 2b*). Typically a pull up resistor conducting 10 μA or more will significantly improve capacitive load responses. The value of the pull up resistor must be determined based on the current sinking capability of the amplifier with respect to the desired output swing. Open loop gain of the amplifier can also be affected by the pull up resistor (see Electrical Characteristics).

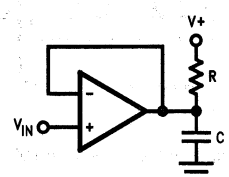

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FIGURE 2b. Compensating for Large Capacitive Loads with a Pull Up Resistor

Application Hints (Continued)

PRINTED-CIRCUIT-BOARD LAYOUT FOR HIGH-IMPEDANCE WORK

It is generally recognized that any circuit which must operate with less than 1000 pA of leakage current requires special layout of the PC board. When one wishes to take advantage of the ultra-low bias current of the LMC6041, typically less than 2fA, it is essential to have an excellent layout. Fortunately, the techniques of obtaining low leakages are quite simple. First, the user must not ignore the surface leakage of the PC board, even though it may sometimes appear acceptably low, because under conditions of high humidity or dust or contamination, the surface leakage will be appreciable.

To minimize the effect of any surface leakage, lay out a ring of foil completely surrounding the LMC6041's inputs and the terminals of capacitors, diodes, conductors, resistors, relay terminals, etc. connected to the op-amp's inputs, as in *Figure 3*. To have a significant effect, guard rings should be placed on both the top and bottom of the PC board. This PC foil must then be connected to a voltage which is at the same voltage as the amplifer inputs, since no leakage current can flow between two points at the same potential. For example, a PC board trace-to-pad resistance of $10^{12}\Omega$, which is normally considered a very large resistance, could leak 5 pA if the trace were a 5V bus adjacent to the pad of the input. This would cause a 100 times degradation from the LMC6041's actual performance. However, if a guard ring is held within 5 mV of the inputs, then even a resistance of $10^{11}\Omega$ would cause only 0.05 pA of leakage current. See *Figures 4a, 4b, 4c* for typical connections of guard rings for standard op-amp configurations.

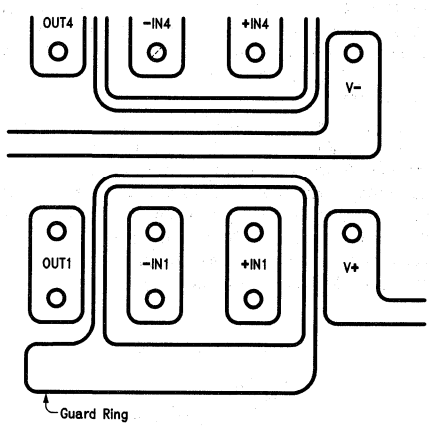

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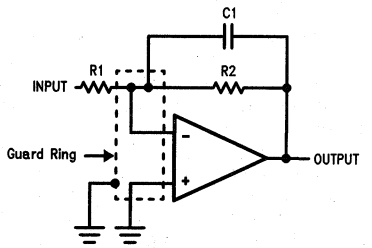
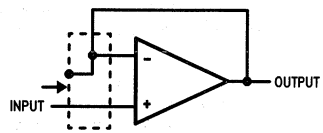
FIGURE 3. Example of Guard Ring in P.C. Board Layout



TL/H/11136–8

(a) Inverting Amplifier



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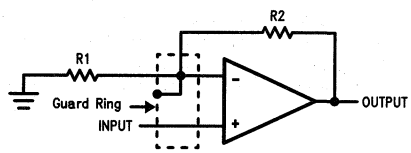
(b) Follower



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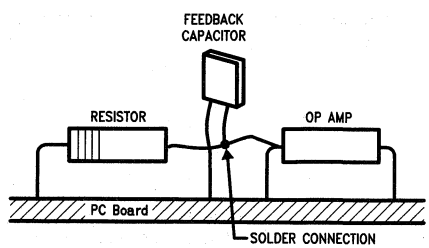
(c) Non-Inverting Amplifier

FIGURE 4. Typical Connections of Guard Rings

The designer should be aware that when it is inappropriate to lay out a PC board for the sake of just a few circuits, there is another technique which is even better than a guard ring on a PC board: Don't insert the amplifier's input pin into the board at all, but bend it up in the air and use only air as an insulator. Air is an excellent insulator. In this case you may have to forego some of the advantages of PC board construction, but the advantages are sometimes well worth the effort of using point-to-point up-in-the-air wiring. See *Figure 5*.



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(Input pins are lifted out of PC board and soldered directly to components. All other pins connected to PC board.)

FIGURE 5. Air Wiring

Typical Single-Supply Applications

(V^+ = 5.0 V_{DC})

The extremely high input impedance, and low power consumption, of the LMC6041 make it ideal for applications that require battery-powered instrumentation amplifiers. Examples of these type of applications are hand-held pH probes, analytic medical instruments, magnetic field detectors, gas detectors, and silicon based pressure transducers.

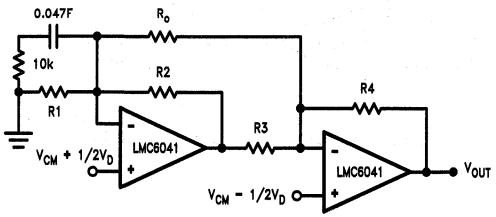

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FIGURE 6. Two Op-Amp Instrumentation Amplifier

The circuit in *Figure 6* is recommended for applications where the common-mode input range is relatively low and the differential gain will be in the range of 10 to 1000. This two op-amp instrumentation amplifier features an independent adjustment of the gain and common-mode rejection trim, and a total quiescent supply current of less than 28 μA. To maintain ultra-high input impedance, it is advisable to use ground rings and consider PC board layout an important part of the overall system design (see Printed-Circuit-Board Layout for High Impedance Work). Referring to *Figure 6*, the input voltages are represented as a common-mode input V_{CM} plus a differential input V_D.

Rejection of the common-mode component of the input is accomplished by making the ratio of R1/R2 equal to R3/R4. So that where,

$$\frac{R3}{R4} = \frac{R2}{R1}$$

$$V_{OUT} = \frac{R4}{R3}\left(1 + \frac{R3}{R4} + \frac{R2 + R3}{R_O}\right) V_D$$

A suggested design guideline is to minimize the difference of value between R1 through R4. This will often result in improved resistor tempco, amplifier gain, and CMRR over temperature. If RN = R1 = R2 = R3 = R4 then the gain equation can be simplified:

$$V_{OUT} = 2\left(1 + \frac{RN}{R_O}\right) V_D$$

Due to the "zero-in, zero-out" performance of the LMC6041, and output swing rail-rail, the dynamic range is only limited to the input common-mode range of 0V to V_S–2.3V, worst case at room temperature. This feature of the LMC6041 makes it an ideal choice for low-power instrumentation systems.

A complete instrumentation amplifier designed for a gain of 100 is shown in *Figure 7*. Provisions have been made for low sensitivity trimming of CMRR and gain.

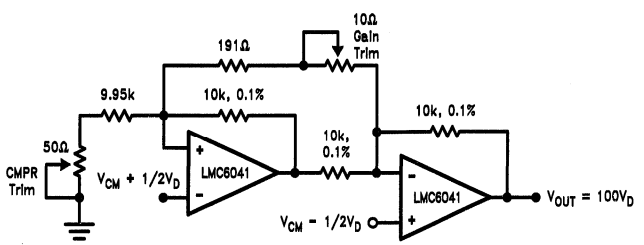

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FIGURE 7. Low-Power Two-Op-Amp Instrumentation Amplifier

Typical Single-Supply Applications ($V^+ = 5.0\ V_{DC}$) (Continued)

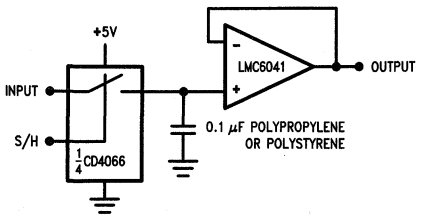

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FIGURE 8. Low-Leakage Sample and Hold

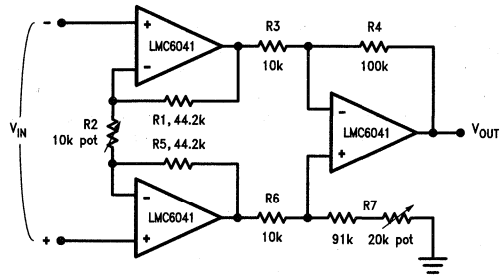

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FIGURE 9. Instrumentation Amplifier

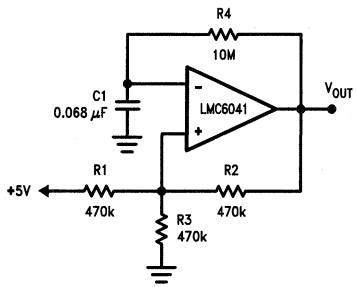

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FIGURE 10. 1 Hz Square-Wave Oscillator

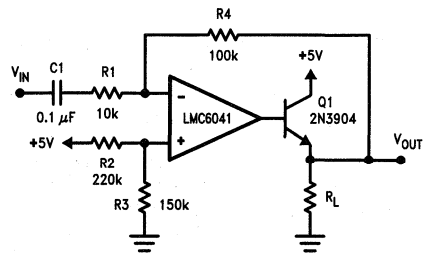

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FIGURE 11. AC Coupled Power Amplifier

National Semiconductor

LMC6042
CMOS Dual Micropower Operational Amplifier

General Description

Ultra-low power consumption and low input-leakage current are the hallmarks of the LMC6042. Providing input currents of only 2 fA typical, the LMC6042 can operate from a single supply, has output swing extending to each supply rail, and an input voltage range that includes ground.

The LMC6042 is ideal for use in systems requiring ultra-low power consumption. In addition, the insensitivity to latch-up, high output drive, and output swing to ground without requiring external pull-down resistors make it ideal for single-supply battery-powered systems.

Other applications for the LMC6042 include bar code reader amplifiers, magnetic and electric field detectors, and hand-held electrometers.

This device is built with National's advanced Double-Poly Silicon-Gate CMOS process.

See the LMC6041 for a single, and the LMC6044 for a quad amplifier with these features.

Features

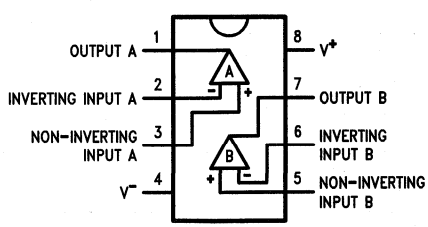
- Low supply current 10 μA/Amp (typ)
- Operates from 4.5V to 15V single supply
- Ultra low input current 2 fA (typ)
- Rail-to-rail output swing
- Input common-mode range includes ground

Applications

- Battery monitoring and power conditioning
- Photodiode and infrared detector preamplifier
- Silicon based transducer systems
- Hand-held analytic instruments
- pH probe buffer amplifier
- Fire and smoke detection systems
- Charge amplifier for piezoelectric transducers

Connection Diagram

8-Pin DIP/SO



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Ordering Information

Package	Temperature Range	NSC Drawing
	Industrial −40°C to +85°C	
8-Pin Small Outline	LMC6042AIM LMC6042IM	M08A
8-Pin Molded DIP	LMC6042AIN LMC6042IN	N08E

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Differential Input Voltage	±Supply Voltage
Supply Voltage ($V^+ - V^-$)	16V
Output Short Circuit to V^+	(Note 12)
Output Short Circuit to V^-	(Note 2)
Lead Temperature (Soldering, 10 seconds)	260°C
Current at Input Pin	±5 mA
Current at Output Pin	±18 mA
Current at Power Supply Pin	35 mA
Power Dissipation	(Note 3)
Storage Temperature Range	−65°C to +150°C
Junction Temperature (Note 3)	110°C
ESD Tolerance (Note 4)	500V
Voltage at Input/Output Pin	$(V^+) + 0.3V, (V^-) - 0.3V$

Operating Ratings

Temperature Range	
LMC6042AI, LMC6042I	$-40°C \le T_J \le +85°C$
Supply Voltage	$4.5V \le V^+ \le 15.5V$
Power Dissipation	(Note 10)
Thermal Resistance (θ_{JA}), (Note 11)	
8-Pin DIP	101°C/W
8-Pin SO	165°C/W

Electrical Characteristics

Unless otherwise specified, all limits guaranteed for $T_A = T_J = 25°C$. **Boldface** limits apply at the temperature extremes. $V^+ = 5V$, $V^- = 0V$, $V_{CM} = 1.5V$, $V_O = V^+/2$ and $R_L > 1M$ unless otherwise specified.

Symbol	Parameter	Conditions		Typical (Note 5)	LMC6042AI Limit (Note 6)	LMC6042I Limit (Note 6)	Units (Limit)
V_{OS}	Input Offset Voltage			1	3 **3.3**	6 **6.3**	mV Max
TCV_{OS}	Input Offset Voltage Average Drift			1.3			μV/°C
I_B	Input Bias Current			0.002	**4**	**4**	pA (Max)
I_{OS}	Input Offset Current			0.001	**2**	**2**	pA (Max)
R_{IN}	Input Resistance			>10			TeraΩ
CMRR	Common Mode Rejection Ratio	$0V \le V_{CM} \le 12.0V$ $V^+ = 15V$		75	68 **66**	62 **60**	dB Min
+PSRR	Positive Power Supply Rejection Ratio	$5V \le V^+ \le 15V$ $V_O = 2.5V$		75	68 **66**	62 **60**	dB Min
−PSRR	Negative Power Supply Rejection Ratio	$0V \le V^- \le -10V$ $V_O = 2.5V$		94	84 **83**	74 **73**	dB Min
CMR	Input Common-Mode Voltage Range	$V^+ = 5V$ and 15V For CMRR ≥ 50 dB		−0.4	−0.1 **0**	−0.1 **0**	V Max
				$V^+ - 1.9V$	$V^+ - 2.3V$ $\mathbf{V^+ - 2.5V}$	$V^+ - 2.3V$ $\mathbf{V^+ - 2.4V}$	V Min
A_V	Large Signal Voltage Gain	$R_L = 100 k\Omega$ (Note 7)	Sourcing	1000	400 **300**	300 **200**	V/mV Min
			Sinking	500	180 **120**	90 **70**	V/mV Min
		$R_L = 25 k\Omega$ (Note 7)	Sourcing	1000	200 **160**	100 **80**	V/mV Min
			Sinking	250	100 **60**	50 **40**	V/mV Min

Electrical Characteristics

Unless otherwise specified, all limits guaranteed for $T_A = T_J = 25°C$. **Boldface** limits apply at the temperature extremes. $V^+ = 5V$, $V^- = 0V$, $V_{CM} = 1.5V$, $V_O = V^+/2$ and $R_L > 1M$ unless otherwise specified. (Continued)

Symbol	Parameter	Conditions	Typical (Note 5)	LMC6042AI Limit (Note 6)	LMC6042I Limit (Note 6)	Units (Limit)
V_O	Output Swing	$V^+ = 5V$ $R_L = 100\ k\Omega$ to $V^+/2$	4.987	4.970 **4.950**	4.940 **4.910**	V Min
			0.004	0.030 **0.050**	0.060 **0.090**	V Max
		$V^+ = 5V$ $R_L = 25\ k\Omega$ to $V^+/2$	4.980	4.920 **4.870**	4.870 **4.820**	V Min
			0.010	0.080 **0.130**	0.130 **0.180**	V Max
		$V^+ = 15V$ $R_L = 100\ k\Omega$ to $V^+/2$	14.970	14.920 **14.880**	14.880 **14.820**	V Min
			0.007	0.030 **0.050**	0.060 **0.090**	V Max
		$V^+ = 15V$ $R_L = 25\ k\Omega$ to $V^+/2$	14.950	14.900 **14.850**	14.850 **14.800**	V Min
			0.022	0.100 **0.150**	0.150 **0.200**	V Max
I_{SC}	Output Current $V^+ = 5V$	Sourcing, $V_O = 0V$	22	16 **10**	13 **8**	mA Min
		Sinking, $V_O = 5V$	21	16 **8**	13 **8**	mA Min
I_{SC}	Output Current $V^+ = 15V$	Sourcing, $V_O = 0V$	40	15 **10**	15 **10**	mA Min
		Sinking, $V_O = 13V$ (Note 12)	39	24 **8**	21 **8**	mA Min
I_S	Supply Current	Both Amplifiers $V_O = 1.5V$	20	34 **39**	45 **50**	μA Max
		Both Amplifiers $V^+ = 15V$	26	44 **51**	56 **65**	μA Max

AC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for $T_A = T_J = 25°C$. **Boldface** limits apply at the temperature extremes. $V^+ = 5V$, $V^- = 0V$, $V_{CM} = 1.5V$, $V_O = V^+/2$ and $R_L > 1M$ unless otherwise specified.

Symbol	Parameter	Conditions	Typ (Note 5)	LMC6042AI Limit (Note 6)	LMC6042I Limit (Note 6)	Units (Limit)
SR	Slew Rate	(Note 8)	0.02	0.015 **0.010**	0.010 **0.007**	V/μs Min
GBW	Gain-Bandwidth Product		100			kHz
ϕ_m	Phase Margin		60			Deg
	Amp-to-Amp Isolation	(Note 9)	115			dB
e_n	Input-Referred Voltage Noise	f = 1 kHz	83			nV/$\sqrt{Hz}$
i_n	Input-Referred Current Noise	f = 1 kHz	0.0002			pA/$\sqrt{Hz}$
T.H.D.	Total Harmonic Distortion	f = 1 kHz, $A_V = -5$ $R_L = 100\ k\Omega$, $V_O = 2\ V_{PP}$ ±5V Supply	0.01			%

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Conditions indicate conditions for which the device is intended to be functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed.

Note 2: Applies to both single-supply operation. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 110°C. Output currents in excess of ±30 mA over long term may adversely affect reliability.

Note 3: The maximum power dissipation is a function of $T_{J(Max)}$, θ_{JA}, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(Max)} - T_A)/\theta_{JA}$.

Note 4: Human body model, 1.5 kΩ in series with 100 pF.

Note 5: Typical values represent the most likely parametric norm.

Note 6: All limits are guaranteed at room temperature (standard type face) or at operating temperature extremes (**bold face type**).

Note 7: $V^+ = 15V$, $V_{CM} = 7.5V$ and R_L connected to 7.5V. For Sourcing tests, $7.5V \le V_O \le 11.5V$. For Sinking tests, $2.5V \le V_O \le 7.5V$.

Note 8: $V^+ = 15V$. Connected as Voltage Follower with 10V step input. Number specified is the slower of the positive and negative slew rates.

Note 9: Input referred $V^+ = 15V$ and $R_L = 100\ k\Omega$ connected to $V^+/2$. Each amp excited in turn with 100 Hz to produce $V_O = 12\ V_{PP}$.

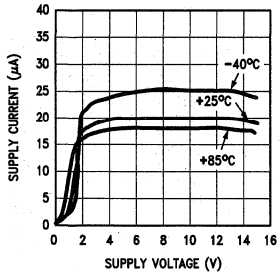
Note 10: For operating at elevated temperatures the device must be derated based on the thermal resistance θ_{JA} with $P_D = (T_J - T_A)/\theta_{JA}$.

Note 11: All numbers apply for packages soldered directly into a PC board.

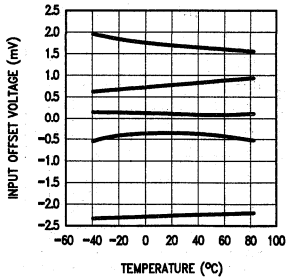
Note 12: Do not connect output to V^+ when V^+ is greater than 13V or reliability may be adversely affected.

Typical Performance Characteristics $V_S = \pm 7.5V$, $T_A = 25°C$ unless otherwise specified

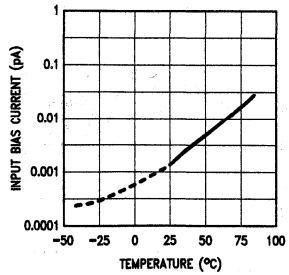
Supply Current vs Supply Voltage



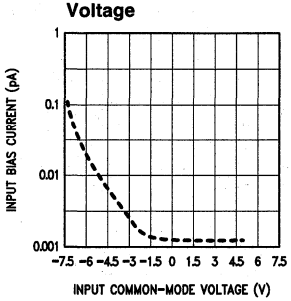
Offset Voltage vs Temperature of Five Representative Units



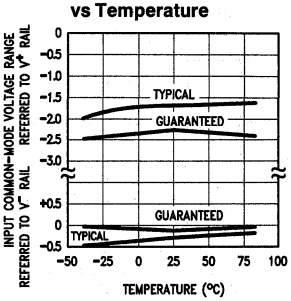
Input Bias Current vs Temperature



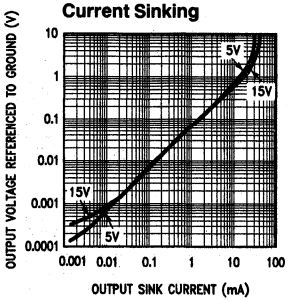
Input Bias Current vs Input Common-Mode Voltage



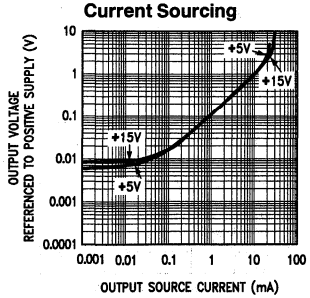
Input Common-Mode Voltage Range vs Temperature



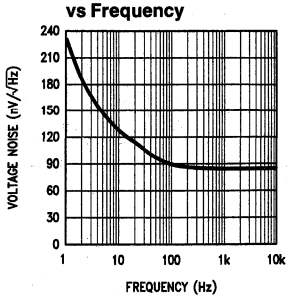
Output Characteristics Current Sinking



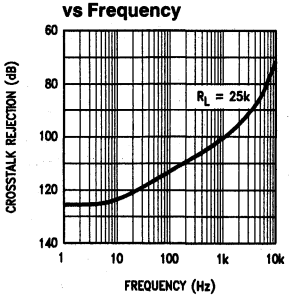
Output Characteristics Current Sourcing



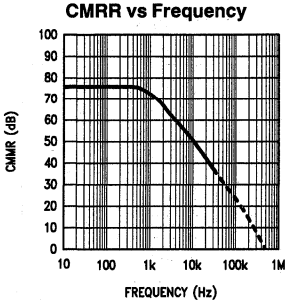
Input Voltage Noise vs Frequency



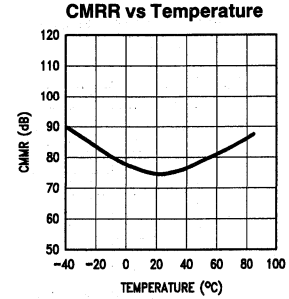
Crosstalk Rejection vs Frequency



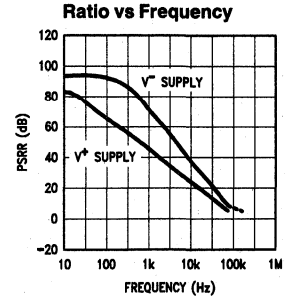
CMRR vs Frequency



CMRR vs Temperature



Power Supply Rejection Ratio vs Frequency



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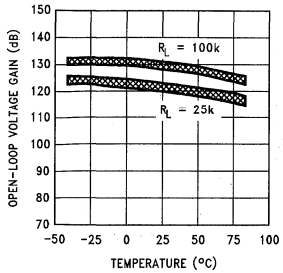
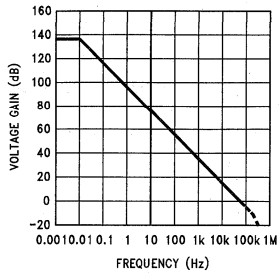
Typical Performance Characteristics

$V_S = \pm 7.5V$, $T_A = 25°C$ unless otherwise specified (Continued)

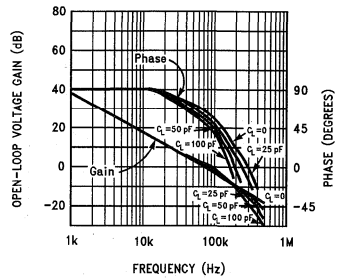
Open-Loop Voltage Gain vs Temperature



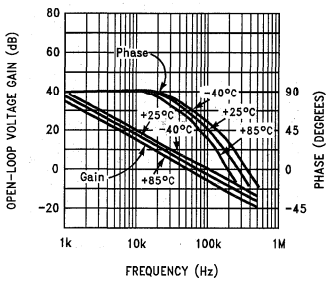
Open-Loop Frequency Response



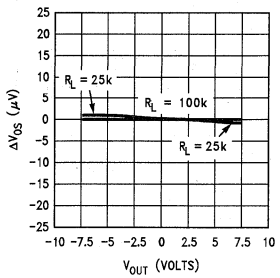
Gain and Phase Responses vs Load Capacitance



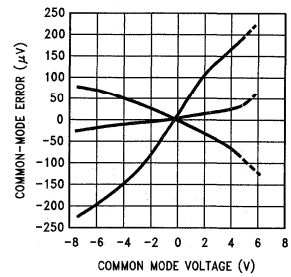
Gain and Phase Response vs Temperature



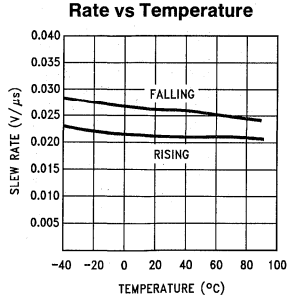
Gain Error (V_{OS} vs V_{OUT})



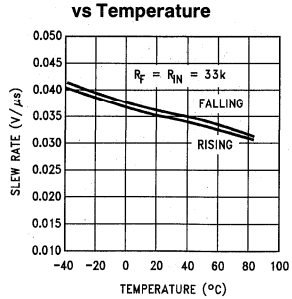
Common-Mode Error vs Common-Mode Voltage of 3 Representative Units



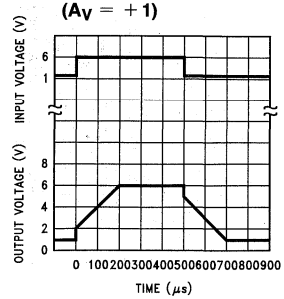
Non-Inverting Slew Rate vs Temperature



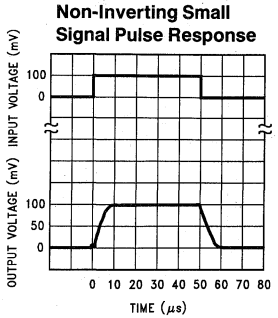
Inverting Slew Rate vs Temperature



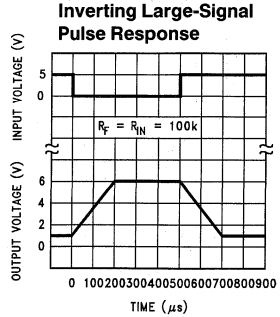
Non-Inverting Large Signal Pulse Response ($A_V = +1$)



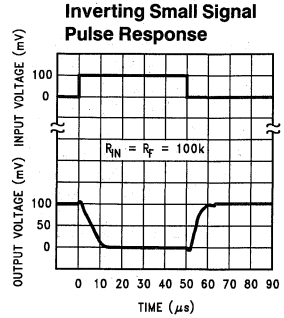
Non-Inverting Small Signal Pulse Response



Inverting Large-Signal Pulse Response



Inverting Small Signal Pulse Response



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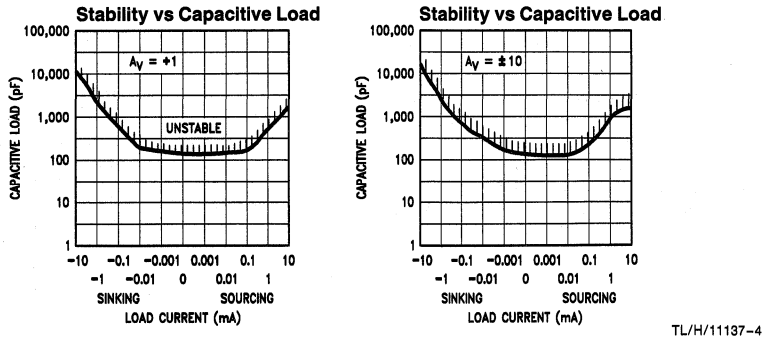
Typical Performance Characteristics

V_S = ±7.5V, T_A = 25°C unless otherwise specified (Continued)



Applications Hints

AMPLIFIER TOPOLOGY

The LMC6042 incorporates a novel op-amp design topology that enables it to maintain rail-rail output swing even when driving a large load. Instead of relying on a push-pull unity gain output buffer stage, the output stage is taken directly from the internal integrator, which provides both low output impedance and large gain. Special feed-forward compensation design techniques are incorporated to maintain stability over a wider range of operating conditions than traditional micropower op-amps. These features make the LMC6042 both easier to design with, and provide higher speed than products typically found in this ultra-low power class.

COMPENSATING FOR INPUT CAPACITANCE

It is quite common to use large values of feedback resistance with amplifiers with ultra-low input curent, like the LMC6042.

Although the LMC6042 is highly stable over a wide range of operating conditions, certain precautions must be met to achieve the desired pulse response when a large feedback resistor is used. Large feedback resistors and even small values of input capacitance, due to transducers, photodiodes, and circuit board parasitics, reduce phase margins.

When high input impedances are demanded, guarding of the LMC6042 is suggested. Guarding input lines will not only reduce leakage, but lowers stray input capacitance as well. (See **Printed-Circuit-Board Layout for High Impedance Work).**

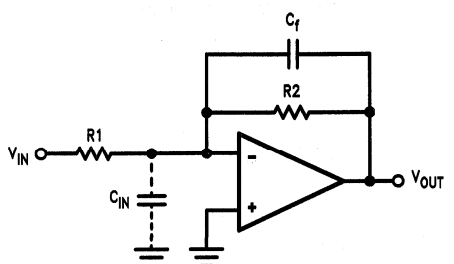


FIGURE 1. Cancelling the Effect of Input Capacitance

The effect of input capacitance can be compensated for by adding a capacitor. Place a capacitor, C_f, around the feedback resistor (as in *Figure 1*) such that:

$$\frac{1}{2\pi R1\, C_{IN}} \geq \frac{1}{2\pi R2\, C_f}$$

or

$$R1\, C_{IN} \leq R2\, C_f$$

Since it is often difficult to know the exact value of C_{IN}, C_f can be experimentally adjusted so that the desired pulse response is achieved. Refer to the LMC660 and the LMC662 for a more detailed discussion on compensating for input capacitance.

CAPACITIVE LOAD TOLERANCE

Direct capacitive loading will reduce the phase margin of many op-amps. A pole in the feedback loop is created by the combination of the op-amp's output impedance and the capacitive load. This pole induces phase lag at the unity-gain crossover frequency of the amplifier resulting in either an oscillatory or underdamped pulse response. With a few external components, op amps can easily indirectly drive capacitive loads, as shown in *Figure 2a*.

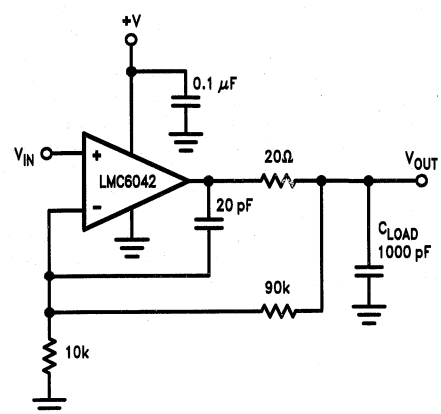


FIGURE 2a. LMC6042 Noninverting Gain of 10 Amplifier, Compensated to Handle Capacitive Loads

Applications Hints (Continued)

In the circuit of *Figure 2a*, R1 and C1 serve to counteract the loss of phase margin by feeding the high frequency component of the output signal back to the amplifier's inverting input, thereby preserving phase margin in the overall feedback loop.

Capacitive load driving capability is enhanced by using a pull up resistor to V^+ *(Figure 2b)*. Typically a pull up resistor conducting 10 μA or more will significantly improve capacitive load responses. The value of the pull up resistor must be determined based on the current sinking capability of the amplifier with respect to the desired output swing. Open loop gain of the amplifier can also be affected by the pull up resistor (see Electrical Characteristics).

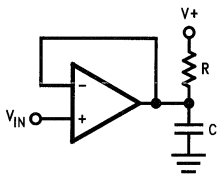


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FIGURE 2b. Compensating for Large Capacitive Loads with a Pull Up Resistor

PRINTED-CIRCUIT-BOARD LAYOUT FOR HIGH-IMPEDANCE WORK

It is generally recognized that any circuit which must operate with less than 1000 pA of leakage current requires special layout of the PC board. When one wishes to take advantage of the ultra-low bias current of the LMC6042, typically less than 2 fA, it is essential to have an excellent layout. Fortunately, the techniques of obtaining low leakages are quite simple. First, the user must not ignore the surface leakage of the PC board, even though it may sometimes appear acceptably low, because under conditions of high humidity or dust or contamination, the surface leakage will be appreciable.

To minimize the effect of any surface leakage, lay out a ring of foil completely surrounding the LMC6042's inputs and the terminals of capacitors, diodes, conductors, resistors, relay terminals etc. connected to the op-amp's inputs, as in *Figure 3*. To have a significant effect, guard rings should be placed on both the top and bottom of the PC board. This PC foil must then be connected to a voltage which is at the same voltage as the amplifier inputs, since no leakage current can flow between two points at the same potential. For example, a PC board trace-to-pad resistance of $10^{12}\Omega$, which is normally considered a very large resistance, could leak 5 pA if the trace were a 5V bus adjacent to the pad of the input. This would cause a 100 times degradation from the LMC6042's actual performance. However, if a guard ring is held within 5 mV of the inputs, then even a resistance of $10^{11}\Omega$ would cause only 0.05 pA of leakage current. See *Figures 4a*, *4b*, *4c* for typical connections of guard rings for standard op-amp configurations.

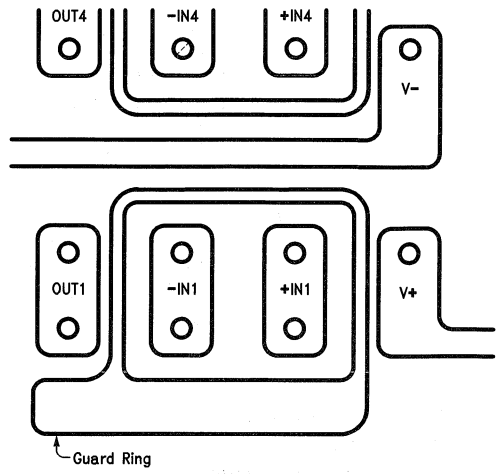

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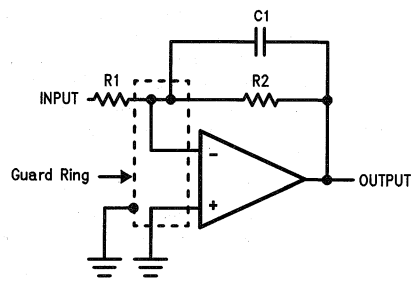
FIGURE 3. Example of Guard Ring in P.C. Board Layout



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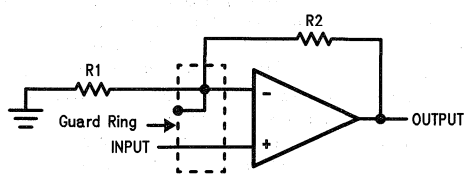
(a) Inverting Amplifier



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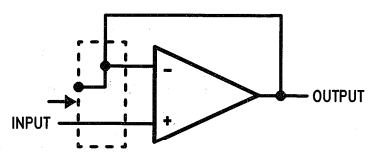
(b) Non-Inverting Amplifier



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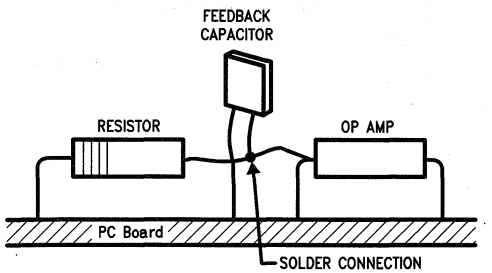
(c) Follower

FIGURE 4. Typical Connections of Guard Rings

Application Hints (Continued)

The designer should be aware that when it is inappropriate to lay out a PC board for the sake of just a few circuits, there is another technique which is even better than a guard ring on a PC board: Don't insert the amplifier's input pin into the board at all, but bend it up in the air and use only air as an insulator. Air is an excellent insulator. In this case you may have to forego some of the advantages of PC board construction, but the advantages are sometimes well worth the effort of using point-to-point up-in-the-air wiring. See *Figure 5*.



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(Input pins are lifted out of PC board and soldered directly to components. All other pins connected to PC board.)

FIGURE 5. Air Wiring

Typical Single-Supply Applications

($V^+ = 5.0\ V_{DC}$)

The extremely high input impedance, and low power consumption, of the LMC6042 make it ideal for applications that require battery-powered instrumentation amplifiers. Examples of these types of applications are hand-held pH probes, analytic medical instruments, magnetic field detectors, gas detectors, and silicon based pressure transducers.

The circuit in *Figure 6* is recommended for applications where the common-mode input range is relatively low and the differential gain will be in the range of 10 to 1000. This two op-amp instrumentation amplifier features an independent adjustment of the gain and common-mode rejection trim, and a total quiescent supply current of less than 20 μA. To maintain ultra-high input impedance, it is advisable to use ground rings and consider PC board layout an important part of the overall system design (see Printed-Circuit-Board Layout for High Impedance Work). Referring to *Figure 6*, the input voltages are represented as a common-mode input V_{CM} plus a differential input V_D.

Rejection of the common-mode component of the input is accomplished by making the ratio of R1/R2 equal to R3/R4. So that where,

$$\frac{R3}{R4} = \frac{R2}{R1}$$

$$V_{OUT} = \frac{R4}{R3}\left(1 + \frac{R3}{R4} + \frac{R2 + R3}{R0}\right) V_D$$

A suggested design guideline is to minimize the difference of value between R1 through R4. This will often result in improved resistor tempco, amplifier gain, and CMRR over temperature. If RN = R1 = R2 = R3 = R4 then the gain equation can be simplified:

$$V_{OUT} = 2\left(1 + \frac{RN}{R0}\right) V_D$$

Due to the "zero-in, zero-out" performance of the LMC6042, and output swing rail-rail, the dynamic range is only limited to the input common-mode range of 0V to $V_S - 2.3V$, worst case at room temperature. This feature of the LMC6042 makes it an ideal choice for low-power instrumentation systems.

A complete instrumentation amplifier designed for a gain of 100 is shown in *Figure 7*. Provisions have been made for low sensitivity trimming of CMRR and gain.

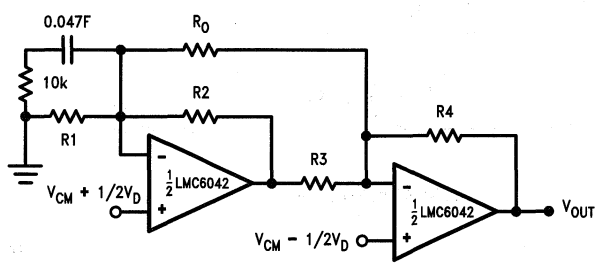

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FIGURE 6. Two Op-Amp Instrumentation Amplifier

Typical Single-Supply Applications ($V^+ = 5.0\ V_{DC}$) (Continued)

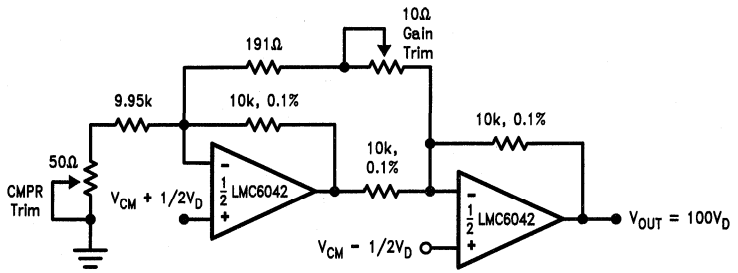

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FIGURE 7. Low-Power Two-Op-Amp Instrumentation Amplifier

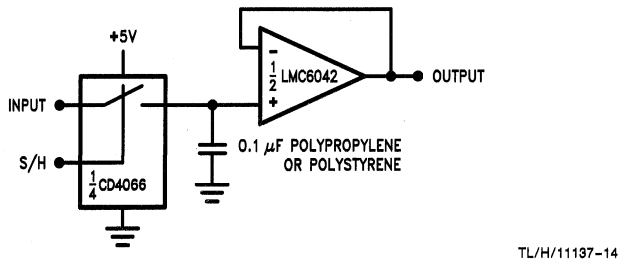

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FIGURE 8. Low-Leakage Sample and Hold

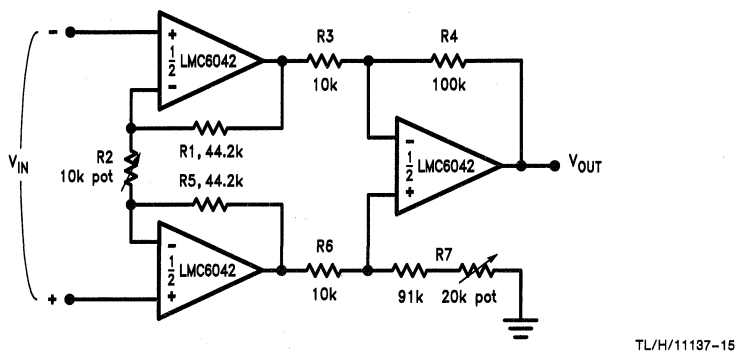

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FIGURE 9. Instrumentation Amplifier

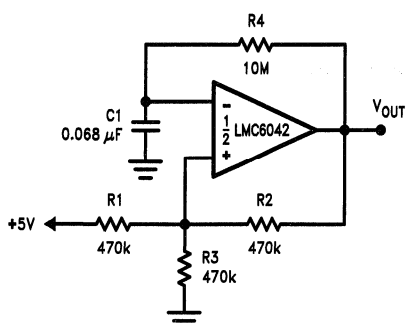

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FIGURE 10. 1 Hz Square Wave Oscillator

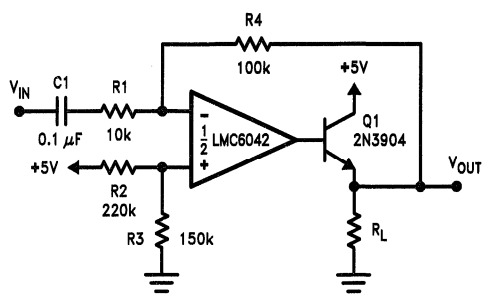

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FIGURE 11. AC Coupled Power Amplifier

National Semiconductor

LMC6044 CMOS Quad Micropower Operational Amplifier

General Description

Ultra-low power consumption and low input-leakage current are the hallmarks of the LMC6044. Providing input currents of only 2 fA typical, the LMC6044 can operate from a single supply, has output swing extending to each supply rail, and an input voltage range that includes ground.

The LMC6044 is ideal for use in systems requiring ultra-low power consumption. In addition, the insensitivity to latch-up, high output drive, and output swing to ground without requiring external pull-down resistors make it ideal for single-supply battery-powered systems.

Other applications for the LMC6044 include bar code reader amplifiers, magnetic and electric field detectors, and hand-held electrometers.

This device is built with National's advanced Double-Poly Silicon-Gate CMOS process.

See the LMC6041 for a single, and the LMC6042 for a dual amplifier with these features.

Features

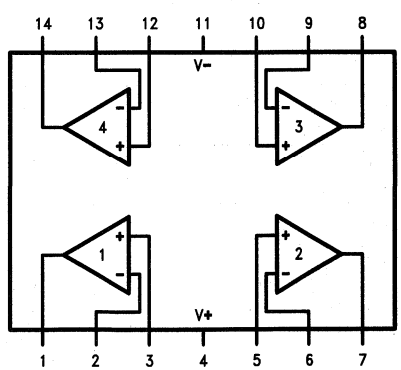
- Low supply current 10 μA/Amp (Typ)
- Operates from 4.5V to 15.5V single supply
- Ultra low input current 2 fA (Typ)
- Rail-to-rail output swing
- Input common-mode range includes ground

Applications

- Battery monitoring and power conditioning
- Photodiode and infrared detector preamplifier
- Silicon based transducer systems
- Hand-held analytic instruments
- pH probe buffer amplifier
- Fire and smoke detection systems
- Charge amplifier for piezoelectric transducers

Connection Diagram

14-Pin DIP/SO



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Ordering Information

Package	Temperature Range: Industrial −40°C to +85°C	NSC Drawing
14-Pin Small Outline	LMC6044AIM LMC6044IM	M14A
14-Pin Molded DIP	LMC6044AIN LMC6044IN	N14A

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Differential Input Voltage	±Supply Voltage
Supply Voltage ($V^+ - V^-$)	16V
Output Short Circuit to V^+	(Note 12)
Output Short Circuit to V^-	(Note 2)
Lead Temperature (Soldering, 10 sec.)	260°C
Current at Input Pin	±5 mA
Current at Output Pin	±18 mA
Current at Power Supply Pin	35 mA
Power Dissipation	(Note 3)
Storage Temperature Range	−65°C to +150°C
Junction Temperature (Note 3)	110°C
ESD Tolerance (Note 4)	500V
Voltage at I/O Pin (V^+)	+0.3V, (V^-) −0.3V

Operating Ratings

Temperature Range	
LMC6044AI, LMC6044I	$-40°C \le T_J \le +85°C$
Supply Voltage	$4.5V \le V+ \le 15.5V$
Power Dissipation	(Note 10)
Thermal Resistance (θ_{JA}), (Note 11)	
14-Pin DIP	85°C/W
14-Pin SO	115°C/W

Electrical Characteristics

Unless otherwise specified, all limits guaranteed for $T_A = T_J = 25°C$. **Boldface** limits apply at the temperature extremes. $V^+ = 5V$, $V^- = 0V$, $V_{CM} = 1.5V$, $V_O = V^+/2$, and $R_L > 1M$ unless otherwise specified.

Symbol	Parameter	Conditions		Typical (Note 5)	LMC6044AI Limit (Note 6)	LMC6044I Limit (Note 6)	Units (Limit)
V_{OS}	Input Offset Voltage			1	3 **3.3**	6 **6.3**	mV max
TCV_{OS}	Input Offset Voltage Average Drift			1.3			µV/°C
I_B	Input Bias Current			0.002	**4**	**4**	pA max
I_{OS}	Input Offset Current			0.001	**2**	**2**	pA max
R_{IN}	Input Resistance			>10			TeraΩ
CMRR	Common Mode Rejection Ratio	$0V \le V_{CM} \le 12.0V$ $V^+ = 15V$		75	68 **66**	62 **60**	dB min
+PSRR	Positive Power Supply Rejection Ratio	$5V \le V^+ \le 15V$ $V_O = 2.5V$		75	68 **66**	62 **60**	dB min
−PSRR	Negative Power Supply Rejection Ratio	$0V \le V^- \le -10V$ $V_O = 2.5V$		94	84 **83**	74 **73**	dB min
CMR	Input Common-Mode Voltage Range	$V^+ = 5V$ & 15V For CMRR ≥ 50 dB		−0.4	−0.1 **0**	−0.1 **0**	V max
				$V^+ - 1.9V$	$V^+ - 2.3V$ $\mathbf{V^+ - 2.5V}$	$V^+ - 2.3V$ $\mathbf{V^+ - 2.4V}$	V min
A_V	Large Signal Voltage Gain	$R_L = 100 k\Omega$ (Note 7)	Sourcing	1000	400 **300**	300 **200**	V/mV min
			Sinking	500	180 **120**	90 **70**	V/mV min
		$R_L = 25 k\Omega$ (Note 7)	Sourcing	1000	200 **160**	100 **80**	V/mV min
			Sinking	250	100 **60**	50 **40**	V/mV min

Electrical Characteristics

Unless otherwise specified, all limits guaranteed for $T_A = T_J = 25°C$. **Boldface** limits apply at the temperature extremes. $V^+ = 5V$, $V^- = 0V$, $V_{CM} = 1.5V$, $V_O = V^+/2$, and $R_L > 1M$ unless otherwise specified. (Continued)

Symbol	Parameter	Conditions	Typical (Note 5)	LMC6044AI Limit (Note 6)	LMC6044I Limit (Note 6)	Units (Limit)
V_O	Output Swing	$V^+ = 5V$ $R_L = 100\ k\Omega$ to 2.5V	4.987	4.970 **4.950**	4.940 **4.910**	V min
			0.004	0.030 **0.050**	0.060 **0.090**	V max
		$V^+ = 5V$ $R_L = 25\ k\Omega$ to 2.5V	4.980	4.920 **4.870**	4.870 **4.820**	V min
			0.010	0.080 **0.130**	0.130 **0.180**	V max
		$V^+ = 15V$ $R_L = 100\ k\Omega$ to $V^+/2$	14.970	14.920 **14.880**	14.880 **14.820**	V min
			0.007	0.030 **0.050**	0.060 **0.090**	V max
		$V^+ = 15V$ $R_L = 25\ k\Omega$ to $V^+/2$	14.950	14.900 **14.850**	14.850 **14.800**	V min
			0.022	0.100 **0.150**	0.150 **0.200**	V max
I_{SC}	Output Current $V^+ = 5V$	Sourcing, $V_O = 0V$	22	16 **10**	13 **8**	mA min
		Sinking, $V_O = 5V$	21	16 **8**	13 **8**	mA min
I_{SC}	Output Current $V^+ = 15V$	Sourcing, $V_O = 0V$	40	15 **10**	15 **10**	mA min
		Sinking, $V_O = 13V$ (Note 12)	39	24 **8**	21 **8**	mA min
I_S	Supply Current	Four Amplifiers $V_O = 1.5V$	40	65 **72**	75 **82**	μA max
		Four Amplifiers $V^+ = 15V$	52	85 **94**	98 **107**	μA max

AC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for $T_A = T_J = 25°C$. **Boldface** limits apply at the temperature extremes. $V^+ = 5V$, $V^- = 0V$, $V_{CM} = 1.5V$, $V_O = V^+/2$, and $R_L > 1M$ unless otherwise specified.

Symbol	Parameter	Conditions	Typical (Note 5)	LMC6044AI Limit (Note 6)	LMC6044I Limit (Note 6)	Units (Limit)
SR	Slew Rate	(Note 8)	0.02	0.015 **0.010**	0.010 **0.007**	V/μs min
GBW	Gain-Bandwidth Product		0.10			MHz
ϕ_m	Phase Margin		60			Deg
	Amp-to-Amp Isolation	(Note 9)	115			dB
e_n	Input-Referred Voltage Noise	F = 1 kHz	83			nV/√Hz
i_n	Input-Referred Current Noise	F = 1 kHz	0.0002			pA/√Hz
T.H.D.	Total Harmonic Distortion	F = 1 kHz, $A_V = -5$ $R_L = 100\ k\Omega$, $V_O = 2\ V_{pp}$ ±5V Supply	0.01			%

Note 1: Absolute Maximum Ratings indicate limts beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed.

Note 2: Applies to both single-supply and split-supply operation. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 110°C. Output currents in excess of ±30 mA over long term may adversely affect reliability.

Note 3: The maximum power dissipation is a function of $T_{J(max)}$, θ_{JA}, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(max)} - T_A)/\theta_{JA}$.

Note 4: Human body model, 1.5 kΩ in series with 100 pF.

Note 5: Typical Values represent the most likely parametric norm.

Note 6: All limits are guaranteed at room temperature (standard type face) or at operating temperature extremes **(bold face type)**.

Note 7: $V^+ = 15V$, $V_{CM} = 7.5V$ and R_L connected to 7.5V. For Sourcing tests, $7.5V \le V_O \le 11.5V$. For Sinking tests, $2.5V \le V_O \le 7.5V$.

Note 8: $V^+ = 15V$. Connected as Voltage Follower with 10V step input. Number specified in the slower of the positive and negative slew rates.

Note 9: Input referred $V^+ = 15V$ and $R_L = 100\ k\Omega$ connected to $V^+/2$. Each amp excited in turn with 100 Hz to produce $V_O = 12\ V_{PP}$.

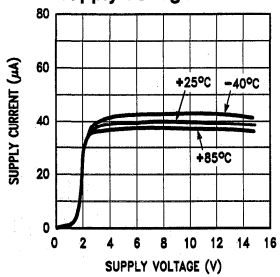
Note 10: For operating at elevated temperatures, the device must be derated based on the thermal resistance θ_{JA} with $P_D = (T_J - T_A)/\theta_{JA}$.

Note 11: All numbers apply for packages soldered directly into a PC board.

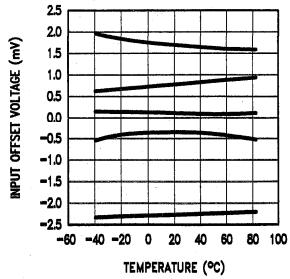
Note 12: Do not connect output to V^+ when V^+ is greater than 13V or reliability may be adversely affected.

Typical Performance Characteristics $V_S = \pm 7.5V$, $T_A = 25°C$ unless otherwise specified

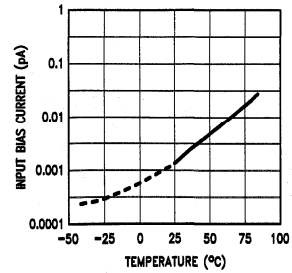
Supply Current vs Supply Voltage



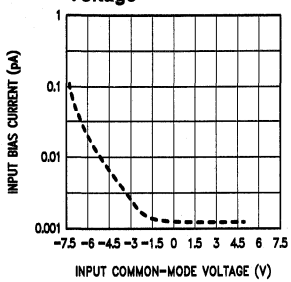
Offset Voltage vs Temperature of Five Representative Units



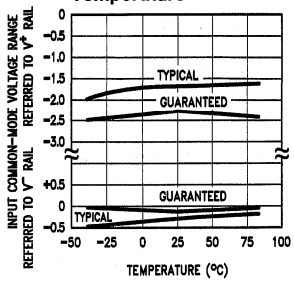
Input Bias Current vs Temperature



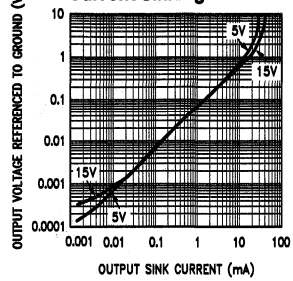
Input Bias Current vs Input Common-Mode Voltage



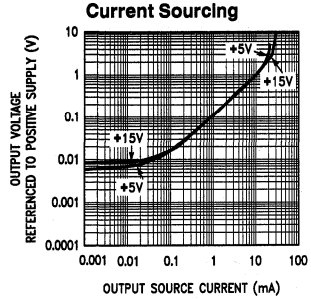
Input Common-Mode Voltage Range vs Temperature



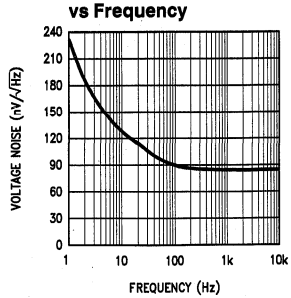
Output Characteristics Current Sinking



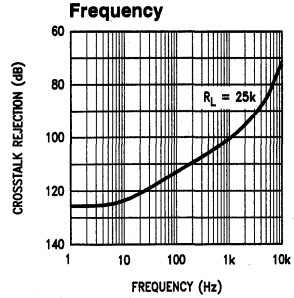
Output Characteristics Current Sourcing



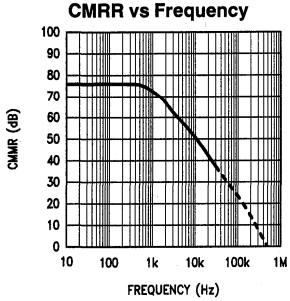
Input Voltage Noise vs Frequency



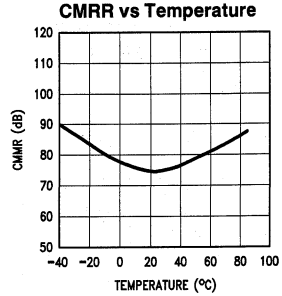
Crosstalk Rejection vs Frequency



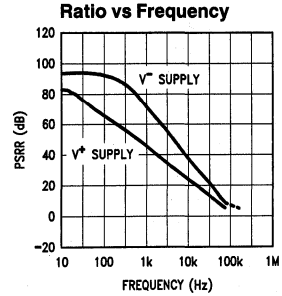
CMRR vs Frequency



CMRR vs Temperature



Power Supply Rejection Ratio vs Frequency

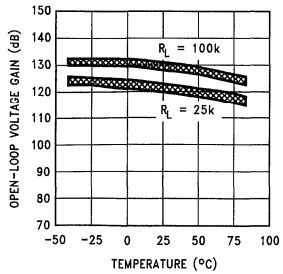


TL/H/11138–2

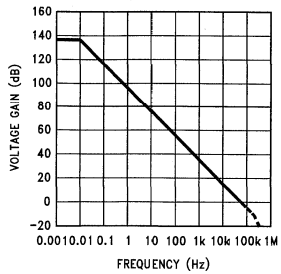
Typical Performance Characteristics

$V_S = \pm 7.5V$, $T_A = 25°C$ unless otherwise specified (Continued)

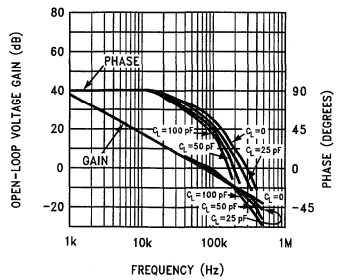
Open-Loop Voltage Gain vs Temperature



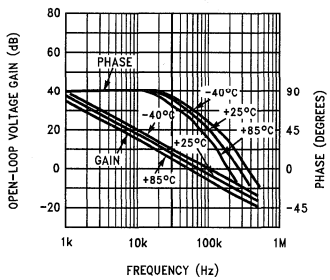
Open-Loop Frequency Response



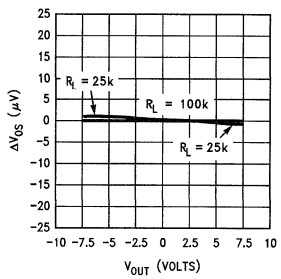
Gain and Phase Responses vs Load Capacitance



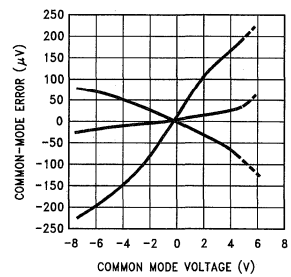
Gain and Phase Responses vs Temperature



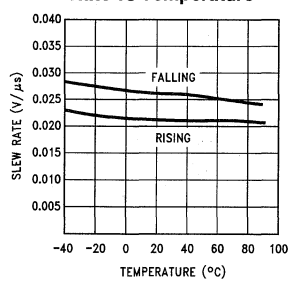
Gain Error (V_{OS} vs V_{OUT})



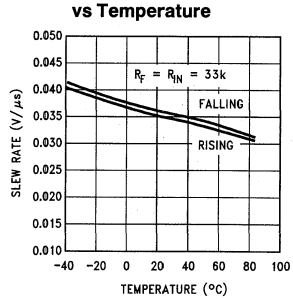
Common-Mode Error vs Common-Mode Voltage of Three Representative Units



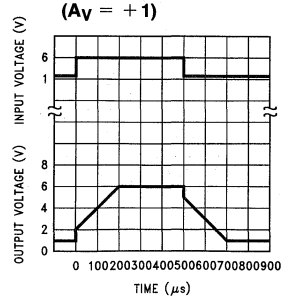
Non-Inverting Slew Rate vs Temperature



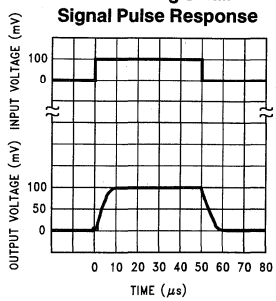
Inverting Slew Rate vs Temperature



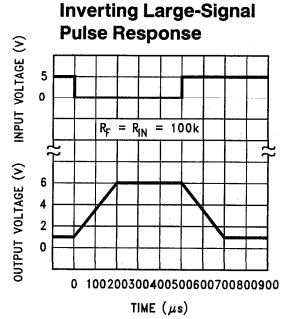
Non-Inverting Large Signal Pulse Response ($A_V = +1$)



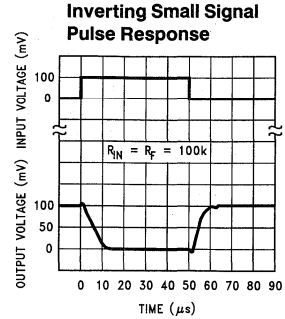
Non-Inverting Small Signal Pulse Response



Inverting Large-Signal Pulse Response



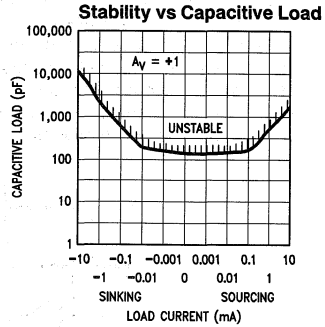
Inverting Small Signal Pulse Response

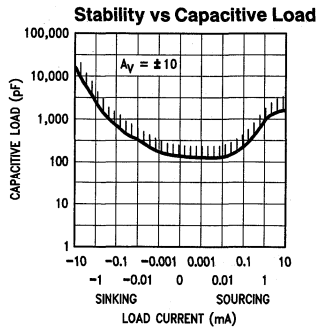


TL/H/11138–3

Typical Performance Characteristics

V_S = ±7.5V, T_A = 25°C unless otherwise specified (Continued)





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Application Hints

AMPLIFIER TOPOLOGY

The LMC6044 incorporates a novel op-amp design topology that enables it to maintain rail-rail output swing even when driving a large load. Instead of relying on a push-pull unity gain outupt buffer stage, the output stage is taken directly from the internal integrator, which provides both low output impedance and large gain. Special feed-forward compensation design techniques are incorporated to maintain stability over a wider range of operating conditions than traditional micropower op-amps. These features make the LMC6044 both easier to design with, and provide higher speed than products typically found in this ultra-low power class.

COMPENSATING FOR INPUT CAPACITANCE

It is quite common to use large values of feedback resistance with amplifiers with ultra-low input current, like the LMC6044.

Although the LMC6044 is highly stable over a wide range of operating conditions, certain precautions must be met to achieve the desired pulse response when a large feedback resistor is used. Large feedback resistors and even small values of input capacitance, due to transducers, photodiodes, and circuits board parasitics, reduce phase margins.

When high input impedance are demanded, guarding of the LMC6044 is suggested. Guarding input lines will not only reduce leakage, but lowers stray input capacitance as well. (See **Printed-Circuit-Board Layout for High Impedance Work.**)

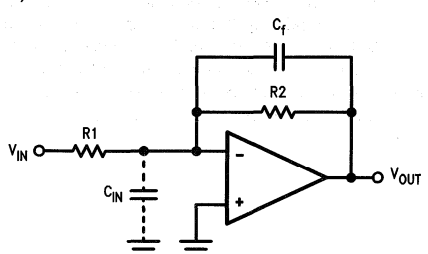

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FIGURE 1. Canceling the Effect of Input Capacitance

The effect of input capacitance can be compensated for by adding a capacitor. Adding a capacitor, C_f, around the feedback resistor (as in *Figure 1*) such that:

$$\frac{1}{2\pi R_1 C_{IN}} \geq \frac{1}{2\pi R_2 C_f}$$

or

$$R_1 C_{IN} \leq R_2 C_f$$

Since it is often difficult to know the exact value of C_{IN}, C_f can be experimentally adjusted so that the desired pulse response is achieved. Refer to the LMC660 and the LMC662 for a more detailed discussion on compensating for input capacitance.

CAPACITIVE LOAD TOLERANCE

Direct capacitive loading will reduce the phase margin of many op-amps. A pole in the feedback loop is created by the combination of the op-amp's output impedance and the capacitive load. This pole induces phase lag at the unity-gain crossover frequency of the amplifier resulting in either an oscillatory or underdamped pulse response. With a few external components, op amps can easily indirectly drive capacitive loads, as shown in *Figure 2a*.

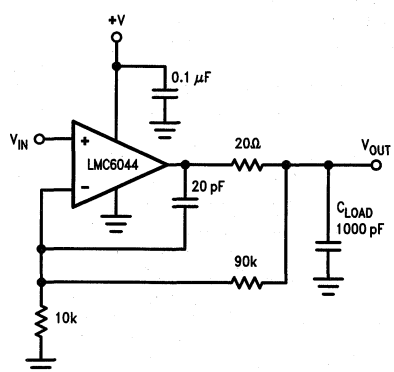

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FIGURE 2a. LMC6044 Noninverting Gain of 10 Amplifier, Compensated to Handle Capacitive Loads

In the circuit of *Figure 2a*, R1 and C1 serve to counteract the loss of phase margin by feeding the high frequency component of the output signal back to the amplifier's inverting input, thereby preserving phase margin in the overall feedback loop.

Application Hints (Continued)

Capacitive load driving capability is enhanced by using a pull up resistor to V^+ *(Figure 2b).* Typically, a pull up resistor conducting 10 μA or more will significantly improve capacitive load responses. The value of the pull up resistor must be determined based on the current sinking capability of the amplifier with respect to the desired output swing. Open loop gain of the amplifier can also be affected by the pull up resistor (see Electrical Characteristics).

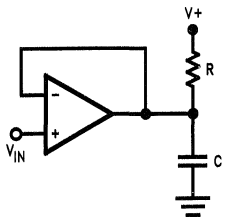

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FIGURE 2b. Compensating for Large Capacitive Loads with a Pull Up Resistor

PRINTED-CIRCUIT-BOARD LAYOUT FOR HIGH-IMPEDANCE WORK

It is generally recognized that any circuit which must operate with less than 1000 pA of leakage current requires special layout of the PC board. When one wishes to take advantage of the ultra-low bias current of the LMC6044, typically less than 2 fA, it is essential to have an excellent layout. Fortunately, the techniques of obtaining low leakages are quite simple. First, the user must not ignore the surface leakage of the PC board, even though it may sometimes appear acceptably low, because under conditions of high humidity or dust or contamination, the surface leakage will be appreciable.

To minimize the effect of any surface leakage, lay out a ring of foil completely surrounding the LMC6044's inputs and the terminals of capacitors, diodes, conductors, resistors, relay terminals, etc. connected to the op-amp's inputs, as in *Figure 3.* To have a significant effect, guard rings should be placed on both the top and bottom of the PC board. This PC foil must then be connected to a voltage which is at the same voltage as the amplifer inputs, since no leakage current can flow between two points at the same potential. For example, a PC board trace-to-pad resistance of $10^{12}\Omega$, which is normally considered a very large resistance, could leak 5 pA if the trace were a 5V bus adjacent to the pad of the input. This would cause a 100 times degradation from the LMC6044's actual performance. However, if a guard ring is held within 5 mV of the inputs, then even a resistance of $10^{11}\Omega$ would cause only 0.05 pA of leakage current. See *Figures 4a, 4b, 4c* for typical connections of guard rings for standard op-amp configurations.

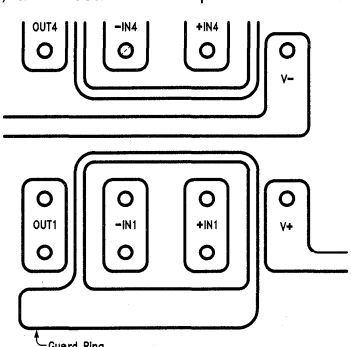

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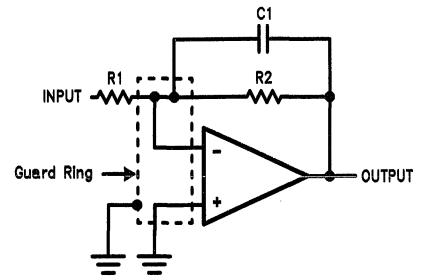
FIGURE 3. Example of Guard Ring in P.C. Board Layout



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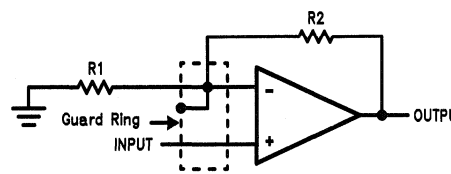
(a) Inverting Amplifier



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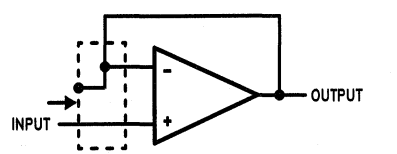
(b) Non-Inverting Amplifier



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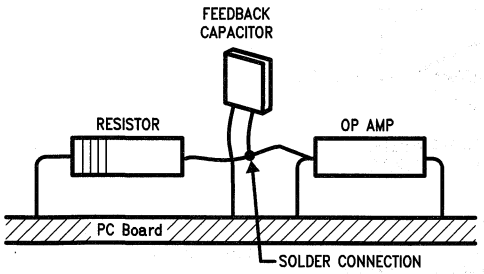
(c) Follower

FIGURE 4. Typical Connections of Guard Rings

The designer should be aware that when it is inappropriate to lay out a PC board for the sake of just a few circuits, there is another technique which is even better than a guard ring on a PC board: Don't insert the amplifier's input pin into the board at all, but bend it up in the air and use only air as an insulator. Air is an excellent insulator. In this case you may have to forego some of the advantages of PC board construction, but the advantages are sometimes well worth the effort of using point-to-point up-in-the-air wiring. See *Figure 5.*

Typical Single-Supply Applications ($V+ = 5.0\ V_{DC}$)



(Input pins are lifted out of PC board and soldered directly to components. All other pins connected to PC board.)

FIGURE 5. Air Wiring

The extremely high input impedance, and low power consumption, of the LMC6044 make it ideal for applications that require battery-powered instrumentation amplifiers. Examples of these type of applications are hand-held pH probes, analytic medical instruments, magnetic field detectors, gas detectors, and silicon based pressure transducers.

The circuit in *Figure 6* is recommended for applications where the common-mode input range is relatively low and the differential gain will be in the range of 10 to 1000. This two op-amp instrumentation amplifier features an independent adjustment of the gain and common-mode rejection trim, and a total quiescent supply current of less than 40 μA. To maintain ultra-high input impedance, it is advisable to use ground rings and consider PC board layout an important part of the overall system design (see Printed-Circuit-Board Layout for High Impedance Work). Referring to *Figure 6*, the input voltages are represented as a common-mode input V_{CM} plus a differential input V_D. Rejection of the common-mode component of the input is accomplished by making the ratio of R1/R2 equal to R3/R4. So that where,

$$\frac{R3}{R4} = \frac{R2}{R1}$$

$$V_{OUT} = \frac{R4}{R3}\left(1 + \frac{R3}{R4} + \frac{R2 + R3}{RO}\right) V_D$$

A suggested design guideline is to minimize the difference of value between R1 through R4. This will often result in improved resistor tempco, amplifier gain, and CMRR over temperature. If RN = R1 = R2 = R3 = R4 then the gain equation can be simplified:

$$V_{OUT} = 2\left(1 + \frac{RN}{RO}\right) V_D$$

Due to the "zero-in, zero-out" performance of the LMC6044, and output swing rail-rail, the dynamic range is only limited to the input common-mode range of 0V to V_S–2.3V, worst case at room temperature. This feature of the LMC6044 makes it an ideal choice for low-power instrumentation systems.

A complete instrumentation amplifier designed for a gain of 100 is shown in *Figure 7*. Provisions have been made for low sensitivity trimming of CMRR and gain.

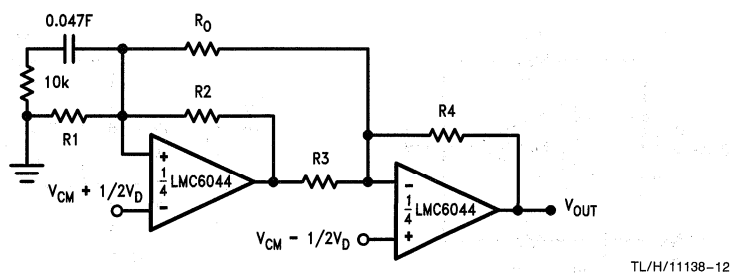


FIGURE 6. Two Op-Amp Instrumentation Amplifier

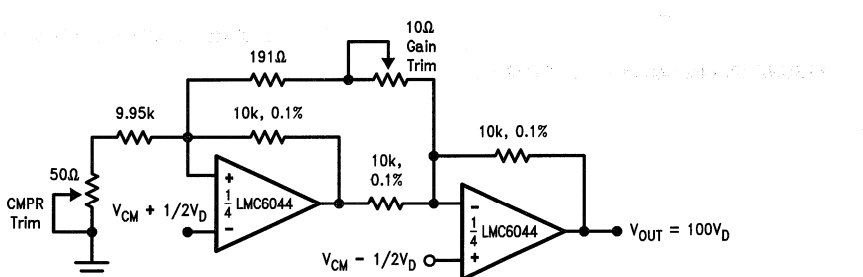


FIGURE 7. Low-Power Two-Op-Amp Instrumentation Amplifier

Typical Single-Supply Applications ($V+ = 5.0\ V_{DC}$) (Continued)

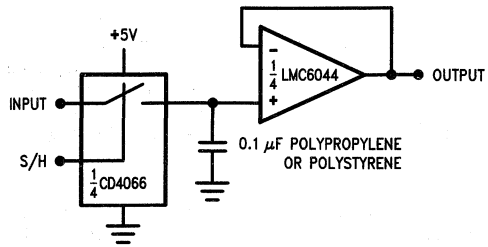


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FIGURE 8. Low-Leakage Sample-and-Hold

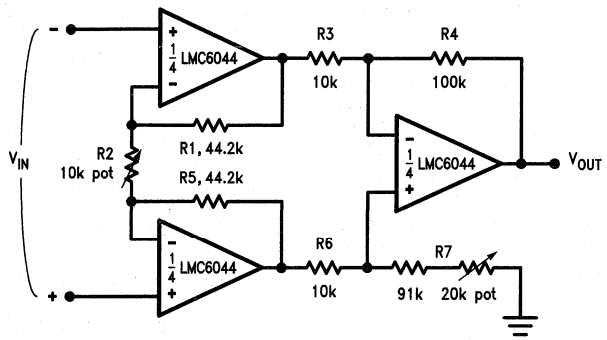

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FIGURE 9. Instrumentation Amplifier

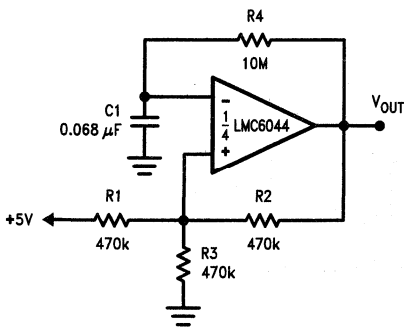

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FIGURE 10. 1 Hz Square-Wave Oscillator

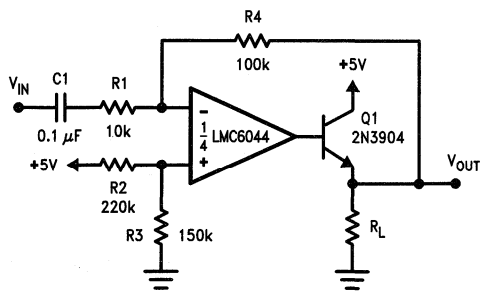

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FIGURE 11. AC Coupled Power Amplifier

National Semiconductor

LMC6061 Precision CMOS Single Micropower Operational Amplifier

General Description

The LMC6061 is a precision single low offset voltage, micropower operational amplifier, capable of precision single supply operation. Performance characteristics include ultra low input bias current, high voltage gain, rail-to-rail output swing, and an input common mode voltage range that includes ground. These features, plus its low power consumption, make the LMC6061 ideally suited for battery powered applications.

Other applications using the LMC6061 include precision full-wave rectifiers, integrators, references, sample-and-hold circuits, and true instrumentation amplifiers.

This device is built with National's advanced double-Poly Silicon-Gate CMOS process.

For designs that require higher speed, see the LMC6081 precision single operational amplifier.

For a dual or quad operational amplifier with similar features, see the LMC6062 or LMC6064 respectively.

PATENT PENDING

Features (Typical Unless Otherwise Noted)

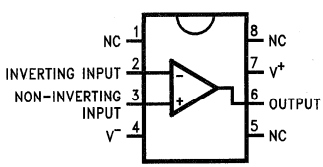
- Low offset voltage 100 μV
- Ultra low supply current 20 μA
- Operates from 4.5V to 15V single supply
- Ultra low input bias current 10 fA
- Output swing within 10 mV of supply rail, 100k load
- Input common-mode range includes V^-
- High voltage gain 140 dB
- Improved latchup immunity

Applications

- Instrumentation amplifier
- Photodiode and infrared detector preamplifier
- Transducer amplifiers
- Hand-held analytic instruments
- Medical instrumentation
- D/A converter
- Charge amplifier for piezoelectric transducers

Connection Diagram

8-Pin DIP/SO



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Top View

Ordering Information

Package	Temperature Range		NSC Drawing
	Military −55°C to +125°C	Industrial −40°C to +85°C	
8-Pin Molded DIP	LMC6061AMN	LMC6061AIN LMC6061IN	N08E
8-Pin Small Outline		LMC6061AIM LMC6061IM	M08A

For MIL-STD-883C qualified products, please contact your local National Semiconductor Sales Office or Distributor for availability and specification information.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Differential Input Voltage	±Supply Voltage
Voltage at Input/Output Pin	(V^+) +0.3V, (V^-) −0.3V
Supply Voltage $(V^+ - V^-)$	16V
Output Short Circuit to V^+	(Note 10)
Output Short Circuit to V^-	(Note 2)
Lead Temperature (Soldering, 10 sec.)	260°C
Storage Temp. Range	−65°C to +150°C
Junction Temperature	150°C
ESD Tolerance (Note 4)	2 kV
Current at Input Pin	±10 mA
Current at Output Pin	±30 mA
Current at Power Supply Pin	40 mA
Power Dissipation	(Note 3)

Operating Ratings (Note 1)

Temperature Range	
LMC6061AM	$-55°C \le T_J \le +125°C$
LMC6061AI, LMC6082I	$-40°C \le T_J \le +85°C$
Supply Voltage	$4.5V \le V^+ \le 15.5V$
Thermal Resistance (θ_{JA}) (Note 11)	
N Package, 8-Pin Molded DIP	115°C/W
M Package, 8-Pin Surface Mount	193°C/W
Power Dissipation	(Note 9)

DC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for $T_J = 25°C$. **Boldface** limits apply at the temperature extremes. $V^+ = 5V$, $V^- = 0V$, $V_{CM} = 1.5V$, $V_O = 2.5V$ and $R_L > 1M$ unless otherwise specified.

Symbol	Parameter	Conditions		Typ (Note 5)	LMC6061AM Limit (Note 6)	LMC6061AI Limit (Note 6)	LMC6061I Limit (Note 6)	Units
V_{OS}	Input Offset Voltage			100	350 **1200**	350 **900**	800 **1300**	μV Max
TCV_{OS}	Input Offset Voltage Average Drift			1.0				μV/°C
I_B	Input Bias Current			0.010	 **100**	 **4**	 **4**	pA Max
I_{OS}	Input Offset Current			0.005	 **100**	 **2**	 **2**	pA Max
R_{IN}	Input Resistance			>10				Tera Ω
CMRR	Common Mode Rejection Ratio	$0V \le V_{CM} \le 12.0V$ $V^+ = 15V$		85	75 **70**	75 **72**	66 **63**	dB Min
+PSRR	Positive Power Supply Rejection Ratio	$5V \le V^+ \le 15V$ $V_O = 2.5V$		85	75 **70**	75 **72**	66 **63**	dB Min
−PSRR	Negative Power Supply Rejection Ratio	$0V \le V^- \le -10V$		100	84 **70**	84 **81**	74 **71**	dB Min
V_{CM}	Input Common-Mode Voltage Range	$V^+ = 5V$ and 15V for CMRR ≥ 60 dB		−0.4	−0.1 **0**	−0.1 **0**	−0.1 **0**	V Max
				$V^+ - 1.9$	$V^+ - 2.3$ $\mathbf{V^+ - 2.6}$	$V^+ - 2.3$ $\mathbf{V^+ - 2.5}$	$V^+ - 2.3$ $\mathbf{V^+ - 2.5}$	V Min
A_V	Large Signal Voltage Gain	$R_L = 100 k\Omega$ (Note 7)	Sourcing	4000	400 **200**	400 **300**	300 **200**	V/mV Min
			Sinking	3000	180 **70**	180 **100**	90 **60**	V/mV Min
		$R_L = 25 k\Omega$ (Note 7)	Sourcing	3000	400 **150**	400 **150**	200 **80**	V/mV Min
			Sinking	2000	100 **35**	100 **50**	70 **35**	V/mV Min

DC Electrical Characteristics (Continued)

Unless otherwise specified, all limits guaranteed for T_J = 25°C. **Boldface** limits apply at the temperature extremes. V^+ = 5V, V^- = 0V, V_{CM} = 1.5V, V_O = 2.5V and R_L > 1M unless otherwise specified.

Symbol	Parameter	Conditions	Typ (Note 5)	LMC6061AM Limit (Note 6)	LMC6061AI Limit (Note 6)	LMC6061I Limit (Note 6)	Units
V_O	Output Swing	V^+ = 5V R_L = 100 kΩ to 2.5V	4.995	4.990 **4.970**	4.990 **4.980**	4.950 **4.925**	V Min
			0.005	0.010 **0.030**	0.010 **0.020**	0.050 **0.075**	V Max
		V^+ = 5V R_L = 25 kΩ to 2.5V	4.990	4.975 **4.955**	4.975 **4.965**	4.950 **4.850**	V Min
			0.010	0.020 **0.045**	0.020 **0.035**	0.050 **0.150**	V Max
		V^+ = 15V R_L = 100 kΩ to 7.5V	14.990	14.975 **14.955**	14.975 **14.965**	14.950 **14.925**	V Min
			0.010	0.025 **0.050**	0.025 **0.035**	0.050 **0.075**	V Max
		V^+ = 15V R_L = 25 kΩ to 7.5V	14.965	14.900 **14.800**	14.900 **14.850**	14.850 **14.800**	V Min
			0.025	0.050 **0.200**	0.050 **0.150**	0.100 **0.200**	V Max
I_O	Output Current V^+ = 5V	Sourcing, V_O = 0V	22	16 **8**	16 **10**	13 **8**	mA Min
		Sinking, V_O = 5V	21	16 **7**	16 **8**	16 **8**	mA Min
I_O	Output Current V^+ = 15V	Sourcing, V_O = 0V	25	15 **9**	15 **10**	15 **10**	mA Min
		Sinking, V_O = 13V (Note 10)	35	24 **7**	24 **8**	24 **8**	mA Min
I_S	Supply Current	V^+ = +5V, V_O = 1.5V	20	24 **35**	24 **32**	32 **40**	μA Max
		V^+ = +15V, V_O = 7.5V	24	30 **40**	30 **38**	40 **48**	μA Max

AC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for T_J = 25°C, **Boldface** limits apply at the temperature extremes. V^+ = 5V, V^- = 0V, V_{CM} = 1.5V, V_O = 2.5V and R_L > 1M unless otherwise specified.

Symbol	Parameter	Conditions	Typ (Note 5)	LMC6061AM Limit (Note 6)	LMC6061AI Limit (Note 6)	LMC6061I Limit (Note 6)	Units
SR	Slew Rate	(Note 8)	35	20 **8**	20 **10**	15 **7**	V/ms Min
GBW	Gain-Bandwidth Product		100				kHz
θ_m	Phase Margin		50				Deg
e_n	Input-Referred Voltage Noise	F = 1 kHz	83				nV/$\sqrt{Hz}$
i_n	Input-Referred Current Noise	F = 1 kHz	0.0002				pA/$\sqrt{Hz}$
T.H.D.	Total Harmonic Distortion	F = 1 kHz, A_V = −5 R_L = 100 kΩ, V_O = 2 V_{PP} ±5V Supply	0.01				%

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed.

Note 2: Applies to both single-supply and split-supply operation. Continous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C. Output currents in excess of ±30 mA over long term may adversely affect reliability.

Note 3: The maximum power dissipation is a function of $T_{J(Max)}$, θ_{JA}, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(Max)} - T_A)/\theta_{JA}$.

Note 4: Human body model, 1.5 kΩ in series with 100 pF.

Note 5: Typical values represent the most likely parametric norm.

Note 6: All limits are guaranteed by testing or statistical analysis.

Note 7: V^+ = 15V, V_{CM} = 7.5V and R_L connected to 7.5V. For Sourcing tests, 7.5V ≤ V_O ≤ 11.5V. For Sinking tests, 2.5V ≤ V_O ≤ 7.5V.

Note 8: V^+ = 15V. Connected as Voltage Follower with 10V step input. Number specified is the slower of the positive and negative slew rates.

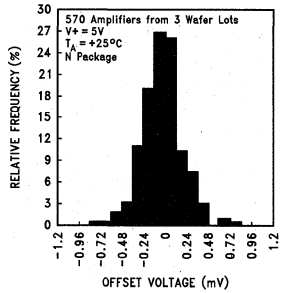
Note 9: For operating at elevated temperatures the device must be derated based on the thermal resistance θ_{JA} with $P_D = (T_J - T_A)/\theta_{JA}$.

Note 10: Do not connect output to V^+, when V^+ is greater than 13V or reliability witll be adversely affected.

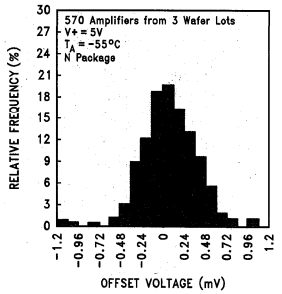
Note 11: All numbers apply for packages soldered directly into a PC board.

Typical Performance Characteristics $V_S = \pm 7.5V$, $T_A = 25°C$, Unless otherwise specified

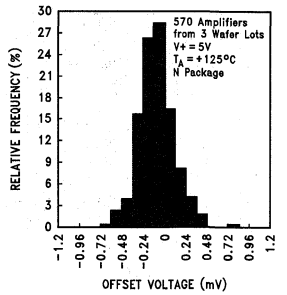
Distribution of LMC6061 Input Offset Voltage ($T_A = +25°C$)



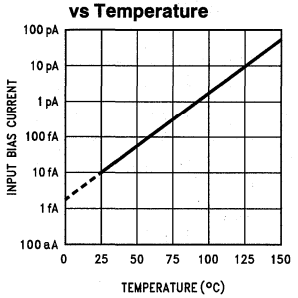
Distribution of LMC6061 Input Offset Voltage ($T_A = -55°C$)



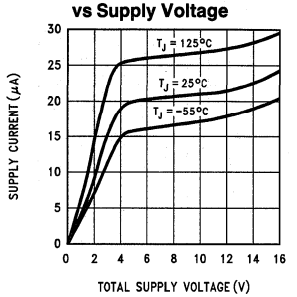
Distribution of LMC6061 Input Offset Voltage ($T_A = +125°C$)



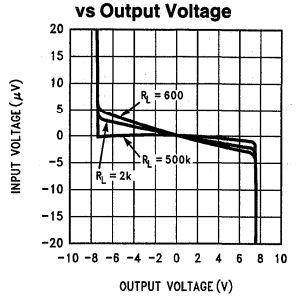
Input Bias Current vs Temperature



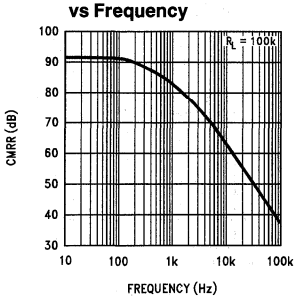
Supply Current vs Supply Voltage



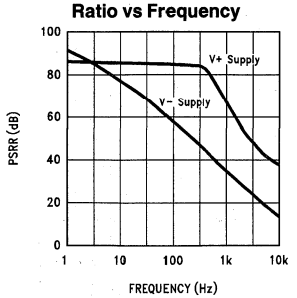
Input Voltage vs Output Voltage



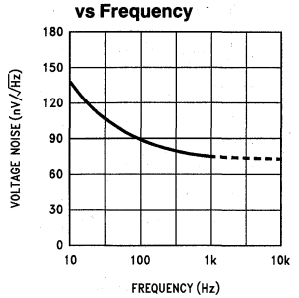
Common Mode Rejection Ratio vs Frequency



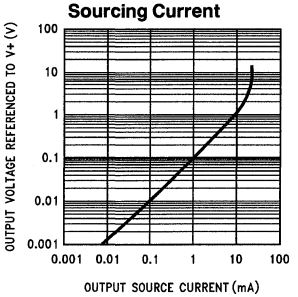
Power Supply Rejection Ratio vs Frequency



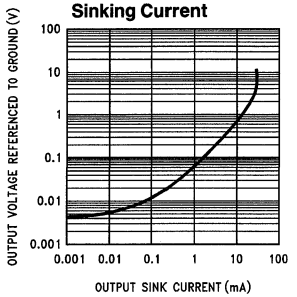
Input Voltage Noise vs Frequency



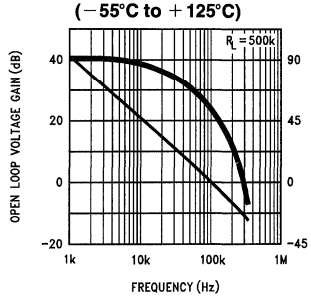
Output Characteristics Sourcing Current



Output Characteristics Sinking Current



Gain and Phase Response vs Temperature (−55°C to +125°C)



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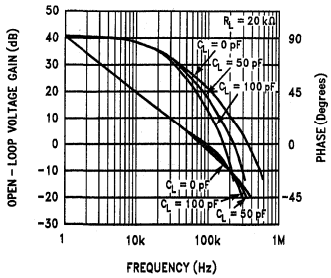
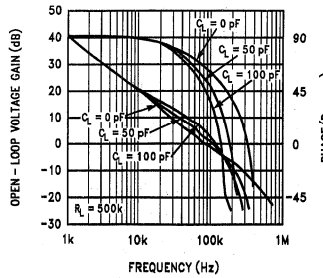
Typical Performance Characteristics $V_S = \pm 7.5V$, $T_A = 25°C$, Unless otherwise specified

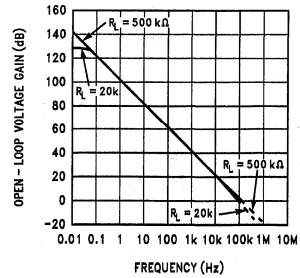
Gain and Phase Response vs Capacitive Load with $R_L = 20\ k\Omega$



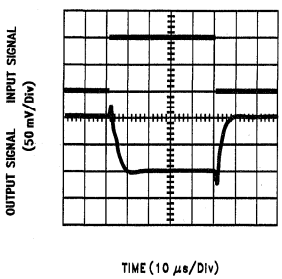
Gain and Phase Response vs Capacitive Load with $R_L = 500\ k\Omega$



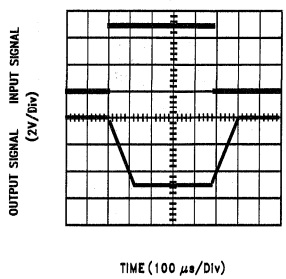
Open Loop Frequency Response



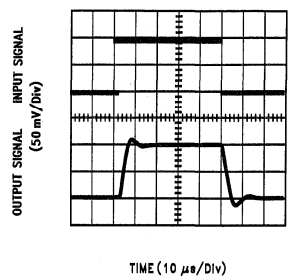
Inverting Small Signal Pulse Response



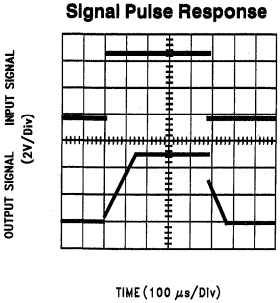
Inverting Large Signal Pulse Response



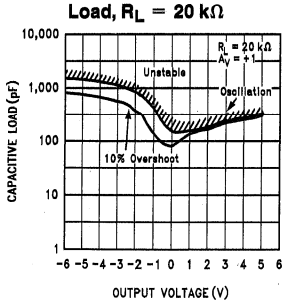
Non-Inverting Small Signal Pulse Response



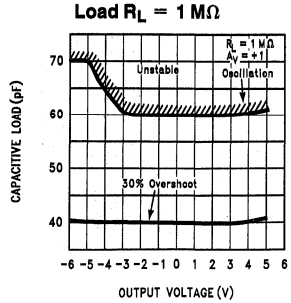
Non-Inverting Large Signal Pulse Response



Stability vs Capacitive Load, $R_L = 20\ k\Omega$



Stability vs Capacitive Load $R_L = 1\ M\Omega$



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Applications Hints

AMPLIFIER TOPOLOGY

The LMC6061 incorporates a novel op-amp design topology that enables it to maintain rail-rail output swing even when driving a large load. Instead of relying on a push-pull unity gain output buffer stage, the output stage is taken directly from the internal integrator, which provides both low output impedance and large gain. Special feed-forward compensation design techniques are incorporated to maintain stability over a wider range of operating conditions than traditional micropower op-amps. These features make the LMC6061 both easier to design with, and provide higher speed than products typically found in this ultra-low power class.

COMPENSATING FOR INPUT CAPACITANCE

It is quite common to use large values of feedback resistance for amplifiers with ultra-low input current, like the LMC6061.

Although the LMC6061 is highly stable over a wide range of operating conditions, certain precautions must be met to achieve the desired pulse response when a large feedback resistor is used. Large feedback resistors and even small values of input capacitance, due to transducers, photodiodes, and circuit board parasitics, reduce phase margins.

When high input impedances are demanded, guarding of the LMC6061 is suggested. Guarding input lines will not only reduce leakage, but lowers stray input capacitance as well. (See ***Printed-Circuit-Board Layout for High Impedance Work***).

The effect of input capacitance can be compensated for by adding a capacitor. Place a capacitor, C_f, around the feedback resistor (as in *Figure 1*) such that:

$$\frac{1}{2\pi R_1 C_{IN}} \geq \frac{1}{2\pi R_2 C_f}$$

or

$$R_1 C_{IN} \leq R_2 C_f$$

Since it is often difficult to know the exact value of C_{IN}, C_f can be experimentally adjusted so that the desired pulse response is achieved. Refer to the LMC660 and the LMC662 for a more detailed discussion on compensating for input capacitance.

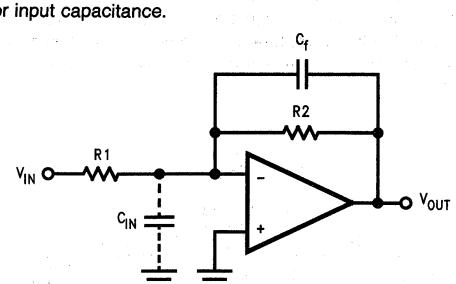

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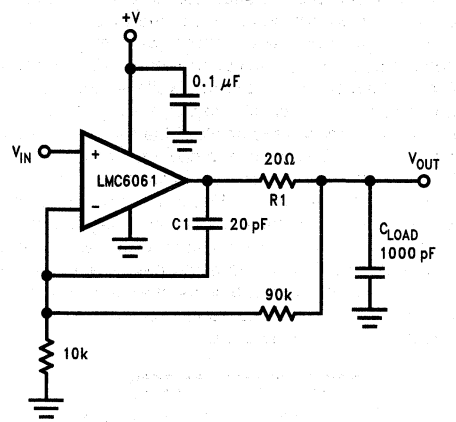
FIGURE 1. Canceling the Effect of Input Capacitance

CAPACITIVE LOAD TOLERANCE

All rail-to-rail output swing operational amplifiers have voltage gain in the output stage. A compensation capacitor is normally included in this integrator stage. The frequency location of the dominate pole is affected by the resistive load on the amplifier. Capacitive load driving capability can be optimized by using an appropriate resistive load in parallel with the capacitive load (see typical curves).

Direct capacitive loading will reduce the phase margin of many op-amps. A pole in the feedback loop is created by the combination of the op-amp's output impedance and the capacitive load. This pole induces phase lag at the unity-gain crossover frequency of the amplifier resulting in either an oscillatory or underdamped pulse response. With a few external components, op amps can easily indirectly drive capacitive loads, as shown in *Figure 2a*.



TL/H/11422–4

FIGURE 2a. LMC6061 Noninverting Gain of 10 Amplifier, Compensated to Handle Capacitive Loads

In the circuit of *Figure 2a*, R1 and C1 serve to counteract the loss of phase margin by feeding the high frequency component of the output signal back to the amplifier's inverting input, thereby preserving phase margin in the overall feedback loop.

Capacitive load driving capability is enhanced by using a pull up resistor to V^+ *(Figure 2b)*. Typically a pull up resistor conducting 10 µA or more will significantly improve capacitive load responses. The value of the pull up resistor must be determined based on the current sinking capability of the amplifier with respect to the desired output swing. Open loop gain of the amplifier can also be affected by the pull up resistor (see electrical characteristics).

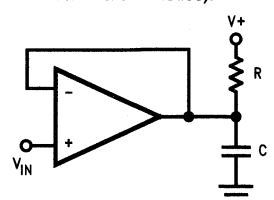


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FIGURE 2b. Compensating for Large Capacitive Loads with a Pull Up Resistor

PRINTED-CIRCUIT-BOARD LAYOUT FOR HIGH-IMPEDANCE WORK

It is generally recognized that any circuit which must operate with less than 1000 pA of leakage current requires special layout of the PC board. When one wishes to take advantage of the ultra-low bias current of the LMC6061, typically less than 10 fA, it is essential to have an excellent layout. Fortunately, the techniques of obtaining low leakages are

Applications Hints (Continued)

quite simple. First, the user must not ignore the surface leakage of the PC board, even though it may sometimes appear acceptably low, because under conditions of high humidity or dust or contamination, the surface leakage will be appreciable.

To minimize the effect of any surface leakage, lay out a ring of foil completely surrounding the LMC6061's inputs and the terminals of capacitors, diodes, conductors, resistors, relay terminals etc. connected to the op-amp's inputs, as in *Figure 3*. To have a significant effect, guard rings should be placed on both the top and bottom of the PC board. This PC foil must then be connected to a voltage which is at the same voltage as the amplifier inputs, since no leakage current can flow between two points at the same potential. For example, a PC board trace-to-pad resistance of $10^{12}\Omega$, which is normally considered a very large resistance, could leak 5 pA if the trace were a 5V bus adjacent to the pad of the input. This would cause a 100 times degradation from the LMC6061's actual performance. However, if a guard ring is held within 5 mV of the inputs, then even a resistance of $10^{11}\Omega$ would cause only 0.05 pA of leakage current. See *Figures 4a, 4b, 4c* for typical connections of guard rings for standard op-amp configurations.

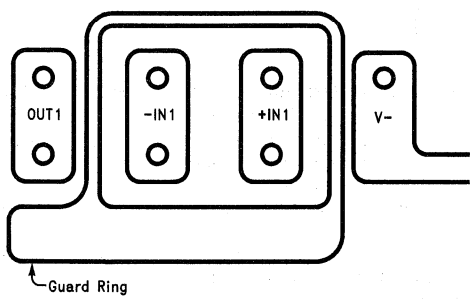

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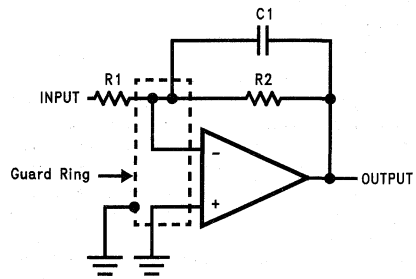
FIGURE 3. Example of Guard Ring in P.C. Board Layout



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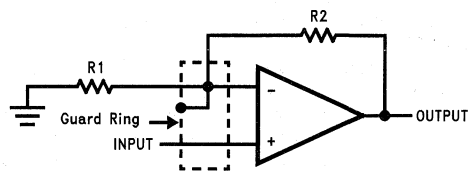
(a) Inverting Amplifier



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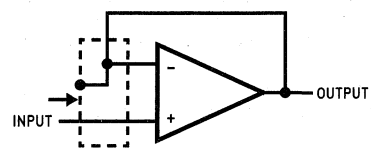
(b) Non-Inverting Amplifier



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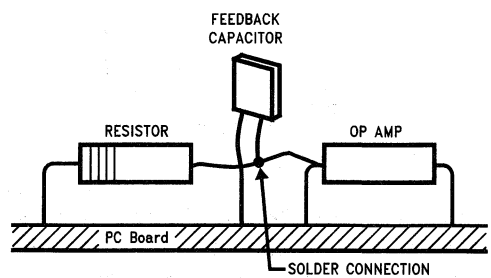
(c) Follower

FIGURE 4. Typical Connections of Guard Rings

The designer should be aware that when it is inappropriate to lay out a PC board for the sake of just a few circuits, there is another technique which is even better than a guard ring on a PC board: Don't insert the amplifier's input pin into the board at all, but bend it up in the air and use only air as an insulator. Air is an excellent insulator. In this case you may have to forego some of the advantages of PC board construction, but the advantages are sometimes well worth the effort of using point-to-point up-in-the-air wiring. See *Figure 5*.



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(Input pins are lifted out of PC board and soldered directly to components. All other pins connected to PC board).

FIGURE 5. Air Wiring

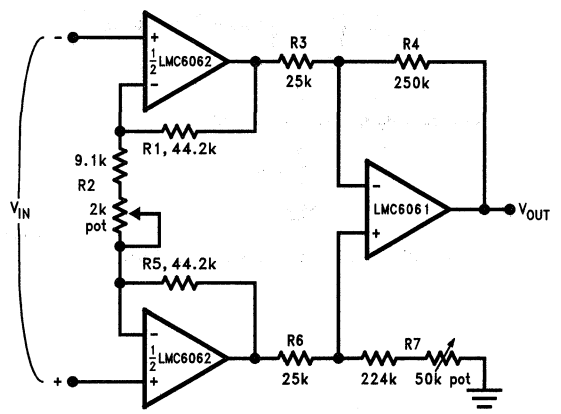
Latchup

CMOS devices tend to be susceptible to latchup due to their internal parasitic SCR effects. The (I/O) input and output pins look similar to the gate of the SCR. There is a minimum current required to trigger the SCR gate lead. The LMC6061 and LMC6081 are designed to withstand 100 mA surge current on the I/O pins. Some resistive method should be used to isolate any capacitance from supplying excess current to the I/O pins. In addition, like an SCR, there is a minimum holding current for any latchup mode. Limiting current to the supply pins will also inhibit latchup susceptibility.

Typical Single-Supply Applications ($V^+ = 5.0\ V_{DC}$)

The extremely high input impedance, and low power consumption, of the LMC6061 make it ideal for applications that require battery-powered instrumentation amplifiers. Examples of these types of applications are hand-held pH probes, analytic medical instruments, magnetic field detectors, gas detectors, and silicon based pressure transducers.

Figure 6 shows an instrumentation amplifier that features high differential and common mode input resistance ($>10^{14}\Omega$), 0.01% gain accuracy at $A_V = 100$, excellent CMRR with 1 kΩ imbalance in bridge source resistance. Input current is less than 100 fA and offset drift is less than 2.5 μV/°C. R_2 provides a simple means of adjusting gain over a wide range without degrading CMRR. R_7 is an initial trim used to maximize CMRR without using super precision matched resistors. For good CMRR over temperature, low drift resistors should be used.



TL/H/11422–11

If $R_1 = R_5$, $R_3 = R_6$, and $R_4 = R_7$; then

$$\frac{V_{OUT}}{V_{IN}} = \frac{R_2 + 2R_1}{R_2} \times \frac{R_4}{R_3}$$

$\therefore A_V \approx 100$ for circuit shown ($R_2 = 9.822$k).

FIGURE 6. Instrumentation Amplifier

Typical Single-Supply Applications ($V^+ = 5.0\ V_{DC}$) (Continued)

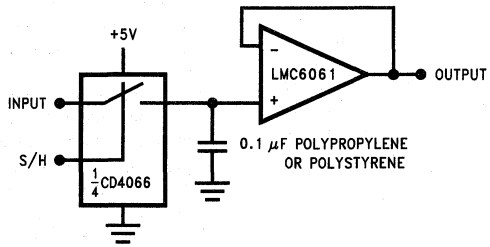


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FIGURE 7. Low-Leakage Sample and Hold

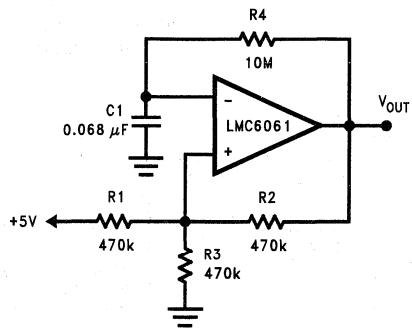

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FIGURE 8. 1 Hz Square Wave Oscillator

National Semiconductor

LMC6062 Precision CMOS Dual Micropower Operational Amplifier

General Description

The LMC6062 is a precision dual low offset voltage, micropower operational amplifier, capable of precision single supply operation. Performance characteristics include ultra low input bias current, high voltage gain, rail-to-rail output swing, and an input common mode voltage range that includes ground. These features, plus its low power consumption, make the LMC6062 ideally suited for battery powered applications.

Other applications using the LMC6062 include precision full-wave rectifiers, integrators, references, sample-and-hold circuits, and true instrumentation amplifiers.

This device is built with National's advanced double-Poly Silicon-Gate CMOS process.

For designs that require higher speed, see the LMC6082 precision dual operational amplifier.

PATENT PENDING

Features (Typical Unless Otherwise Noted)

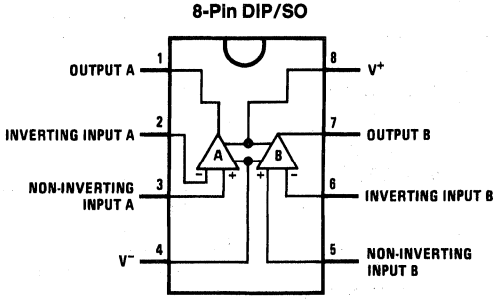
- Low offset voltage 100 μV
- Ultra low supply current 16 μA/Amplifier
- Operates from 4.5V to 15V single supply
- Ultra low input bias current 10 fA
- Output swing within 10 mV of supply rail, 100k load
- Input common-mode range includes V^-
- High voltage gain 140 dB
- Improved latchup immunity

Applications

- Instrumentation amplifier
- Photodiode and infrared detector preamplifier
- Transducer amplifiers
- Hand-held analytic instruments
- Medical instrumentation
- D/A converter
- Charge amplifier for piezoelectric transducers

Connection Diagram

8-Pin DIP/SO



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Top View

Ordering Information

Package	Temperature Range		NSC Drawing
	Military −55°C to +125°C	Industrial −40°C to +85°C	
8-Pin Molded DIP	LMC6062AMN	LMC6062AIN LMC6062IN	N08E
8-Pin Small Outline		LMC6062AIM LMC6062IM	M08A

For MIL-STD-883C qualified products, please contact your local National Semiconductor Sales Office or Distributor for availability and specification information.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Differential Input Voltage	±Supply Voltage
Voltage at Input/Output Pin	$(V^+) + 0.3V$, $(V^-) - 0.3V$
Supply Voltage ($V^+ - V^-$)	16V
Output Short Circuit to V^+	(Note 11)
Output Short Circuit to V^-	(Note 2)
Lead Temperature (Soldering, 10 sec.)	260°C
Storage Temp. Range	−65°C to +150°C
Junction Temperature	150°C
ESD Tolerance (Note 4)	2 kV
Current at Input Pin	±10 mA
Current at Output Pin	±30 mA
Current at Power Supply Pin	40 mA
Power Dissipation	(Note 3)

Operating Ratings (Note 1)

Temperature Range	
LMC6062AM	$-55°C \le T_J \le +125°C$
LMC6062AI, LMC6082I	$-40°C \le T_J \le +85°C$
Supply Voltage	$4.5V \le V^+ \le 15.5V$
Thermal Resistance (θ_{JA}) (Note 12)	
8-Pin Molded DIP	115°C/W
8-Pin SO	193°C/W
Power Dissipation	(Note 10)

DC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for $T_J = 25°C$. **Boldface** limits apply at the temperature extremes. $V^+ = 5V$, $V^- = 0V$, $V_{CM} = 1.5V$, $V_O = 2.5V$ and $R_L > 1M$ unless otherwise specified.

Symbol	Parameter	Conditions		Typ (Note 5)	LMC6062AM Limit (Note 6)	LMC6062AI Limit (Note 6)	LMC6062I Limit (Note 6)	Units
V_{OS}	Input Offset Voltage			100	350 **1200**	350 **900**	800 **1300**	μV Max
TCV_{OS}	Input Offset Voltage Average Drift			1.0				μV/°C
I_B	Input Bias Current			0.010	 **100**	 **4**	 **4**	pA Max
I_{OS}	Input Offset Current			0.005	 **100**	 **2**	 **2**	pA Max
R_{IN}	Input Resistance			>10				Tera Ω
CMRR	Common Mode Rejection Ratio	$0V \le V_{CM} \le 12.0V$ $V^+ = 15V$		85	75 **70**	75 **72**	66 **63**	dB Min
+PSRR	Positive Power Supply Rejection Ratio	$5V \le V^+ \le 15V$ $V_O = 2.5V$		85	75 **70**	75 **72**	66 **63**	dB Min
−PSRR	Negative Power Supply Rejection Ratio	$0V \le V^- \le -10V$		100	84 **70**	84 **81**	74 **71**	dB Min
V_{CM}	Input Common-Mode Voltage Range	$V^+ = 5V$ and 15V for CMRR ≥ 60 dB		−0.4	−0.1 **0**	−0.1 **0**	−0.1 **0**	V Max
				$V^+ - 1.9$	$V^+ - 2.3$ $\mathbf{V^+ - 2.6}$	$V^+ - 2.3$ $\mathbf{V^+ - 2.5}$	$V^+ - 2.3$ $\mathbf{V^+ - 2.5}$	V Min
A_V	Large Signal Voltage Gain	$R_L = 100 k\Omega$ (Note 7)	Sourcing	4000	400 **200**	400 **300**	300 **200**	V/mV Min
			Sinking	3000	180 **70**	180 **100**	90 **60**	V/mV Min
		$R_L = 25 k\Omega$ (Note 7)	Sourcing	3000	400 **150**	400 **150**	200 **80**	V/mV Min
			Sinking	2000	100 **35**	100 **50**	70 **35**	V/mV Min

DC Electrical Characteristics (Continued)

Unless otherwise specified, all limits guaranteed for T_J = 25°C. **Boldface** limits apply at the temperature extremes. V^+ = 5V, V^- = 0V, V_{CM} = 1.5V, V_O = 2.5V and R_L > 1M unless otherwise specified.

Symbol	Parameter	Conditions	Typ (Note 5)	LMC6062AM Limit (Note 6)	LMC6062AI Limit (Note 6)	LMC6062I Limit (Note 6)	Units
V_O	Output Swing	V^+ = 5V R_L = 100 kΩ to 2.5V	4.995	4.990 **4.970**	4.990 **4.980**	4.950 **4.925**	V Min
			0.005	0.010 **0.030**	0.010 **0.020**	0.050 **0.075**	V Max
		V^+ = 5V R_L = 25 kΩ to 2.5V	4.990	4.975 **4.955**	4.975 **4.965**	4.950 **4.850**	V Min
			0.010	0.020 **0.045**	0.020 **0.035**	0.050 **0.150**	V Max
		V^+ = 15V R_L = 100 kΩ to 7.5V	14.990	14.975 **14.955**	14.975 **14.965**	14.950 **14.925**	V Min
			0.010	0.025 **0.050**	0.025 **0.035**	0.050 **0.075**	V Max
		V^+ = 15V R_L = 25 kΩ to 7.5V	14.965	14.900 **14.800**	14.900 **14.850**	14.850 **14.800**	V Min
			0.025	0.050 **0.200**	0.050 **0.150**	0.100 **0.200**	V Max
I_O	Output Current V^+ = 5V	Sourcing, V_O = 0V	22	16 **8**	16 **10**	13 **8**	mA Min
		Sinking, V_O = 5V	21	16 **7**	16 **8**	16 **8**	mA Min
I_O	Output Current V^+ = 15V	Sourcing, V_O = 0V	25	15 **9**	15 **10**	15 **10**	mA Min
		Sinking, V_O = 13V (Note 11)	35	24 **7**	24 **8**	24 **8**	mA Min
I_S	Supply Current	Both Amplifiers V^+ = +5V, V_O = 1.5V	32	38 **60**	38 **46**	46 **56**	μA Max
		Both Amplifiers V^+ = +15V, V_O = 7.5V	40	47 **70**	47 **55**	57 **66**	μA Max

AC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for T_J = 25°C, **Boldface** limits apply at the temperature extremes. V^+ = 5V, V^- = 0V, V_{CM} = 1.5V, V_O = 2.5V and R_L > 1M unless otherwise specified.

Symbol	Parameter	Conditions	Typ (Note 5)	LMC6062AM Limit (Note 6)	LMC6062AI Limit (Note 6)	LMC6062I Limit (Note 6)	Units
SR	Slew Rate	(Note 8)	35	20 **8**	20 **10**	15 **7**	V/ms Min
GBW	Gain-Bandwidth Product		100				kHz
θ_m	Phase Margin		50				Deg
	Amp-to-Amp Isolation	(Note 9)	155				dB
e_n	Input-Referred Voltage Noise	F = 1 kHz	83				nV/$\sqrt{Hz}$
i_n	Input-Referred Current Noise	F = 1 kHz	0.0002				pA/$\sqrt{Hz}$
T.H.D.	Total Harmonic Distortion	F = 1 kHz, A_V = −5 R_L = 100 kΩ, V_O = 2 V_{PP} ±5V Supply	0.01				%

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed.

Note 2: Applies to both single-supply and split-supply operation. Continous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C. Output currents in excess of ±30 mA over long term may adversely affect reliability.

Note 3: The maximum power dissipation is a function of $T_{J(Max)}$, θ_{JA}, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(Max)} - T_A)/\theta_{JA}$.

Note 4: Human body model, 1.5 kΩ in series with 100 pF.

Note 5: Typical values represent the most likely parametric norm.

Note 6: All limits are guaranteed by testing or statistical analysis.

Note 7: V^+ = 15V, V_{CM} = 7.5V and R_L connected to 7.5V. For Sourcing tests, 7.5V ≤ V_O ≤ 11.5V. For Sinking tests, 2.5V ≤ V_O ≤ 7.5V.

Note 8: V^+ = 15V. Connected as Voltage Follower with 10V step input. Number specified is the slower of the positive and negative slew rates.

Note 9: Input referred V^+ = 15V and R_L = 100 kΩ connected to 7.5V. Each amp excited in turn with 100 Hz to produce V_O = 12 V_{PP}.

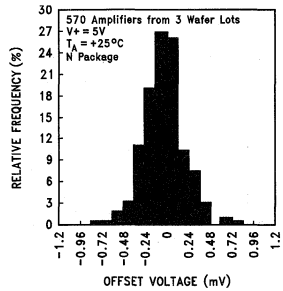
Note 10: For operating at elevated temperatures the device must be derated based on the thermal resistance θ_{JA} with $P_D = (T_J - T_A)/\theta_{JA}$.

Note 11: Do not connect output to V^+, when V^+ is greater than 13V or reliability witll be adversely affected.

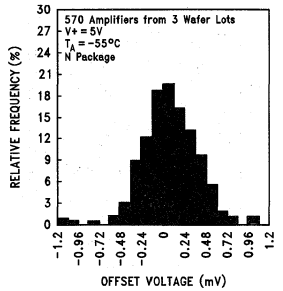
Note 12: All numbers apply for packages soldered directly into a PC board.

Typical Performance Characteristics $V_S = \pm 7.5V$, $T_A = 25°C$, Unless otherwise specified

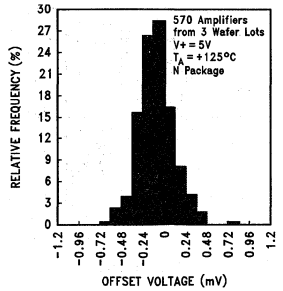
Distribution of LMC6062 Input Offset Voltage ($T_A = +25°C$)



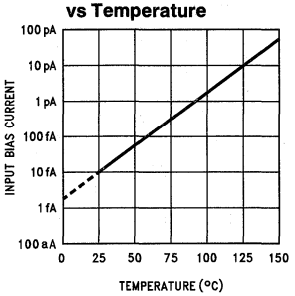
Distribution of LMC6062 Input Offset Voltage ($T_A = -55°C$)



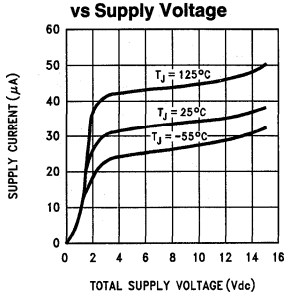
Distribution of LMC6062 Input Offset Voltage ($T_A = +125°C$)



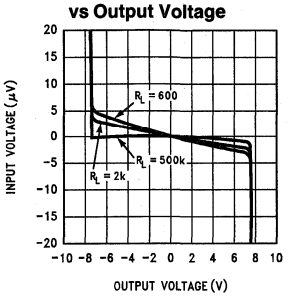
Input Bias Current vs Temperature



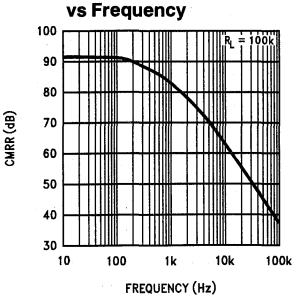
Supply Current vs Supply Voltage



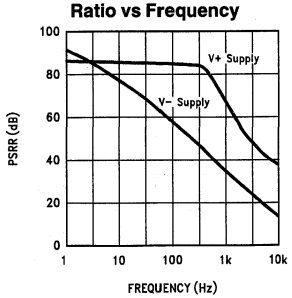
Input Voltage vs Output Voltage



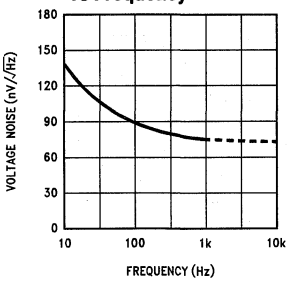
Common Mode Rejection Ratio vs Frequency



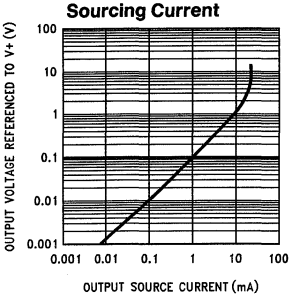
Power Supply Rejection Ratio vs Frequency



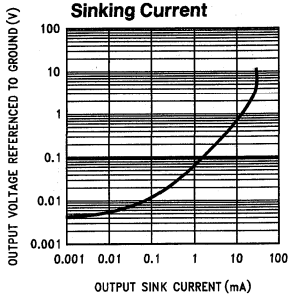
Input Voltage Noise vs Frequency



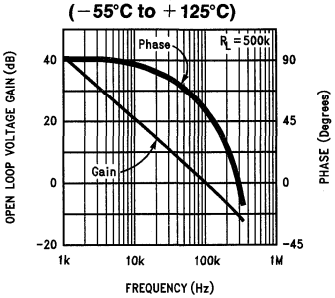
Output Characteristics Sourcing Current



Output Characteristics Sinking Current



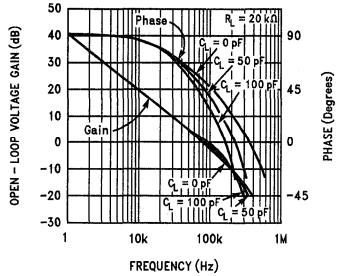
Gain and Phase Response vs Temperature (−55°C to +125°C)



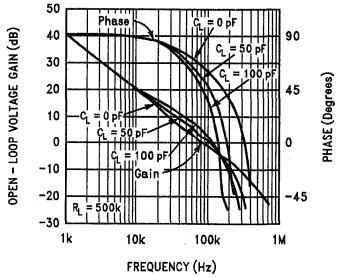
TL/H/11298–2

Typical Performance Characteristics $V_S = \pm 7.5V$, $T_A = 25°C$, Unless otherwise specified

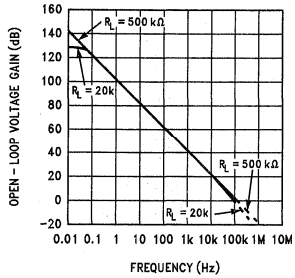
Gain and Phase Response vs Capacitive Load with $R_L = 20\ k\Omega$



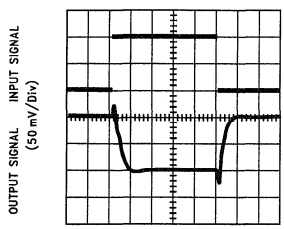
Gain and Phase Response vs Capacitive Load with $R_L = 500\ k\Omega$



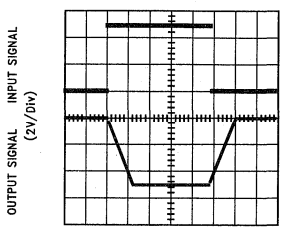
Open Loop Frequency Response



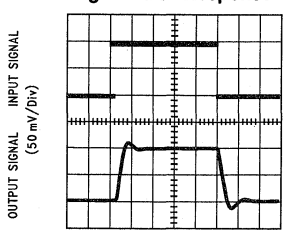
Inverting Small Signal Pulse Response



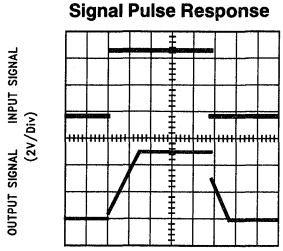
Inverting Large Signal Pulse Response



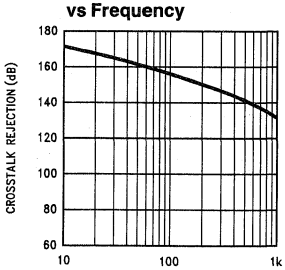
Non-Inverting Small Signal Pulse Response



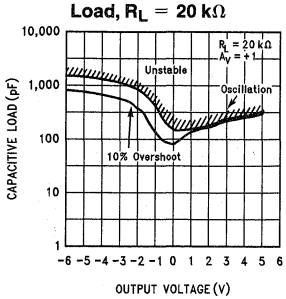
Non-Inverting Large Signal Pulse Response



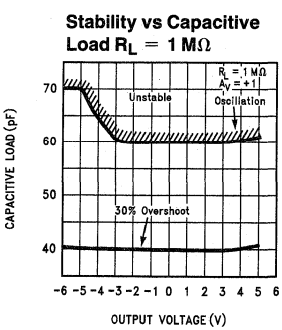
Crosstalk Rejection vs Frequency



Stability vs Capacitive Load, $R_L = 20\ k\Omega$



Stability vs Capacitive Load $R_L = 1\ M\Omega$



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Applications Hints

AMPLIFIER TOPOLOGY

The LMC6062 incorporates a novel op-amp design topology that enables it to maintain rail-rail output swing even when driving a large load. Instead of relying on a push-pull unity gain output buffer stage, the output stage is taken directly from the internal integrator, which provides both low output impedance and large gain. Special feed-forward compensation design techniques are incorporated to maintain stability over a wider range of operating conditions than traditional micropower op-amps. These features make the LMC6062 both easier to design with, and provide higher speed than products typically found in this ultra-low power class.

COMPENSATING FOR INPUT CAPACITANCE

It is quite common to use large values of feedback resistance for amplifiers with ultra-low input current, like the LMC6062.

Although the LMC6062 is highly stable over a wide range of operating conditions, certain precautions must be met to achieve the desired pulse response when a large feedback resistor is used. Large feedback resistors and even small values of input capacitance, due to transducers, photodiodes, and circuit board parasitics, reduce phase margins.

When high input impedances are demanded, guarding of the LMC6062 is suggested. Guarding input lines will not only reduce leakage, but lowers stray input capacitance as well. (See ***Printed-Circuit-Board Layout for High Impedance Work***).

The effect of input capacitance can be compensated for by adding a capacitor. Place a capacitor, C_f, around the feedback resistor (as in *Figure 1*) such that:

$$\frac{1}{2\pi R_1 C_{IN}} \geq \frac{1}{2\pi R_2 C_f}$$

or

$$R_1 C_{IN} \leq R_2 C_f$$

Since it is often difficult to know the exact value of C_{IN}, C_f can be experimentally adjusted so that the desired pulse response is achieved. Refer to the LMC660 and the LMC662 for a more detailed discussion on compensating for input capacitance.

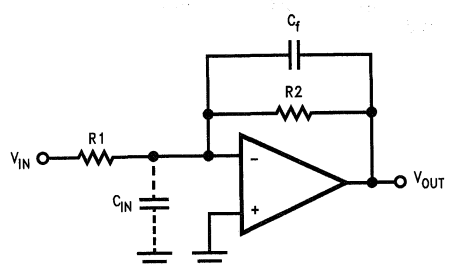

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FIGURE 1. Canceling the Effect of Input Capacitance

CAPACITIVE LOAD TOLERANCE

All rail-to-rail output swing operational amplifiers have voltage gain in the output stage. A compensation capacitor is normally included in this integrator stage. The frequency location of the dominate pole is affected by the resistive load on the amplifier. Capacitive load driving capability can be optimized by using an appropriate resistive load in parallel with the capacitive load (see typical curves).

Direct capacitive loading will reduce the phase margin of many op-amps. A pole in the feedback loop is created by the combination of the op-amp's output impedance and the capacitive load. This pole induces phase lag at the unity-gain crossover frequency of the amplifier resulting in either an oscillatory or underdamped pulse response. With a few external components, op amps can easily indirectly drive capacitive loads, as shown in *Figure 2a*.

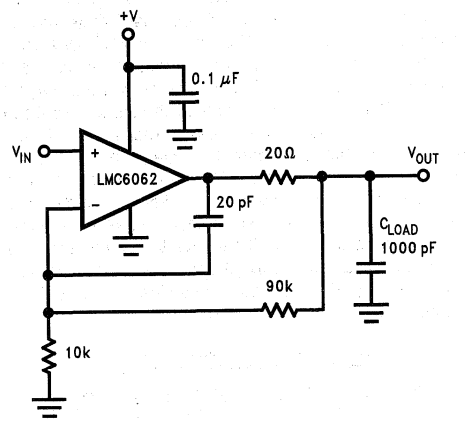

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FIGURE 2a. LMC6062 Noninverting Gain of 10 Amplifier, Compensated to Handle Capacitive Loads

In the circuit of *Figure 2a*, R1 and C1 serve to counteract the loss of phase margin by feeding the high frequency component of the output signal back to the amplifier's inverting input, thereby preserving phase margin in the overall feedback loop.

Capacitive load driving capability is enhanced by using a pull up resistor to V^+ *(Figure 2b)*. Typically a pull up resistor conducting 10 μA or more will significantly improve capacitive load responses. The value of the pull up resistor must be determined based on the current sinking capability of the amplifier with respect to the desired output swing. Open loop gain of the amplifier can also be affected by the pull up resistor (see Electrical Characteristics).

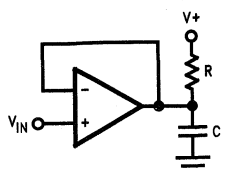

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FIGURE 2b. Compensating for Large Capacitive Loads with a Pull Up Resistor

PRINTED-CIRCUIT-BOARD LAYOUT FOR HIGH-IMPEDANCE WORK

It is generally recognized that any circuit which must operate with less than 1000 pA of leakage current requires special layout of the PC board. When one wishes to take advantage of the ultra-low bias current of the LMC6062, typically less than 10 fA, it is essential to have an excellent layout. Fortunately, the techniques of obtaining low leakages are

Applications Hints (Continued)

quite simple. First, the user must not ignore the surface leakage of the PC board, even though it may sometimes appear acceptably low, because under conditions of high humidity or dust or contamination, the surface leakage will be appreciable.

To minimize the effect of any surface leakage, lay out a ring of foil completely surrounding the LMC6062's inputs and the terminals of capacitors, diodes, conductors, resistors, relay terminals etc. connected to the op-amp's inputs, as in *Figure 3*. To have a significant effect, guard rings should be placed on both the top and bottom of the PC board. This PC foil must then be connected to a voltage which is at the same voltage as the amplifier inputs, since no leakage current can flow between two points at the same potential. For example, a PC board trace-to-pad resistance of $10^{12}\Omega$, which is normally considered a very large resistance, could leak 5 pA if the trace were a 5V bus adjacent to the pad of the input. This would cause a 100 times degradation from the LMC6062's actual performance. However, if a guard ring is held within 5 mV of the inputs, then even a resistance of $10^{11}\Omega$ would cause only 0.05 pA of leakage current. See *Figures 4a*, *4b*, *4c* for typical connections of guard rings for standard op-amp configurations.

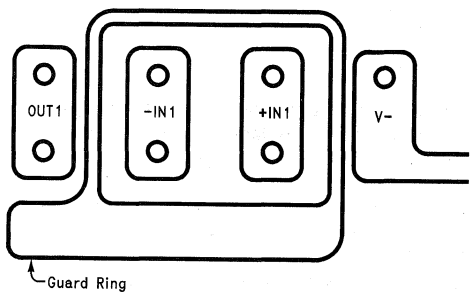

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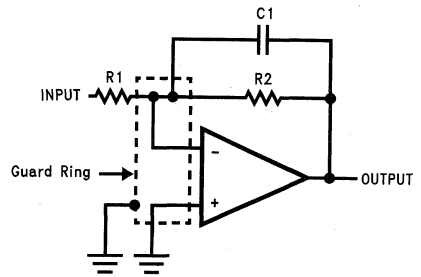
FIGURE 3. Example of Guard Ring in P.C. Board Layout



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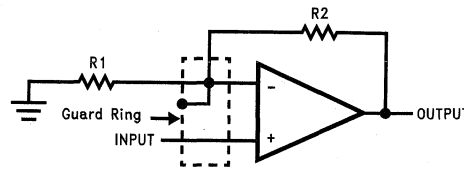
(a) Inverting Amplifier



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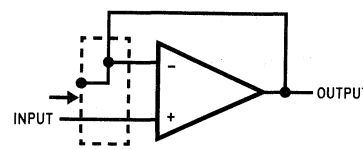
(b) Non-Inverting Amplifier



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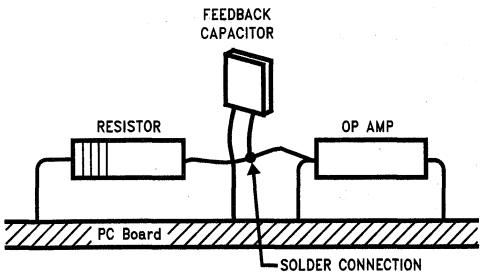
(c) Follower

FIGURE 4. Typical Connections of Guard Rings

The designer should be aware that when it is inappropriate to lay out a PC board for the sake of just a few circuits, there is another technique which is even better than a guard ring on a PC board: Don't insert the amplifier's input pin into the board at all, but bend it up in the air and use only air as an insulator. Air is an excellent insulator. In this case you may have to forego some of the advantages of PC board construction, but the advantages are sometimes well worth the effort of using point-to-point up-in-the-air wiring. See *Figure 5*.

Latchup

CMOS devices tend to be susceptible to latchup due to their internal parasitic SCR effects. The (I/O) input and output pins look similar to the gate of the SCR. There is a minimum current required to trigger the SCR gate lead. The LMC6062 and LMC6082 are designed to withstand 100 mA surge current on the I/O pins. Some resistive method should be used to isolate any capacitance from supplying excess current to the I/O pins. In addition, like an SCR, there is a minimum holding current for any latchup mode. Limiting current to the supply pins will also inhibit latchup susceptibility.



TL/H/11298–10

(Input pins are lifted out of PC board and soldered directly to components. All other pins connected to PC board).

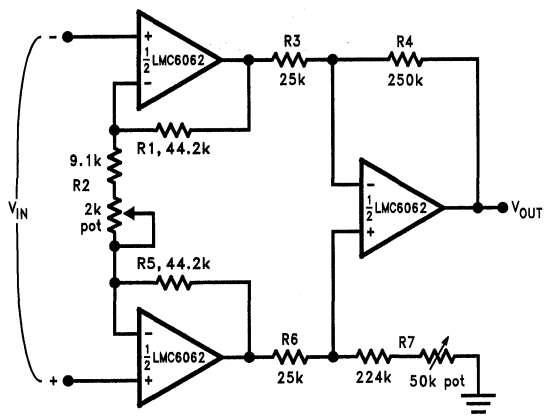
FIGURE 5. Air Wiring

Typical Single-Supply Applications

($V^+ = 5.0\ V_{DC}$)

The extremely high input impedance, and low power consumption, of the LMC6062 make it ideal for applications that require battery-powered instrumentation amplifiers. Examples of these types of applications are hand-held pH probes, analytic medical instruments, magnetic field detectors, gas detectors, and silicon based pressure transducers.

Figure 6 shows an instrumentation amplifier that features high differential and common mode input resistance ($>10^{14}\Omega$), 0.01% gain accuracy at $A_V = 100$, excellent CMRR with 1 kΩ imbalance in bridge source resistance. Input current is less than 100 fA and offset drift is less than 2.5 μV/°C. R_2 provides a simple means of adjusting gain over a wide range without degrading CMRR. R_7 is an initial trim used to maximize CMRR without using super precision matched resistors. For good CMRR over temperature, low drift resistors should be used.



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If $R_1 = R_5$, $R_3 = R_6$, and $R_4 = R_7$; then

$$\frac{V_{OUT}}{V_{IN}} = \frac{R_2 + 2R_1}{R_2} \times \frac{R_4}{R_3}$$

$\therefore A_V \approx 100$ for circuit shown ($R_2 = 9.822k$).

FIGURE 6. Instrumentation Amplifier

Typical Single-Supply Applications ($V^+ = 5.0\ V_{DC}$) (Continued)

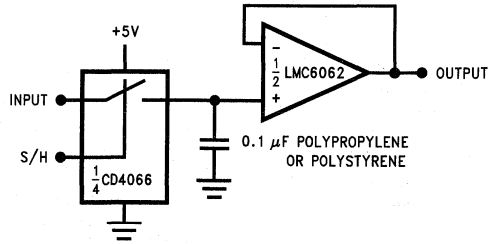

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FIGURE 7. Low-Leakage Sample and Hold

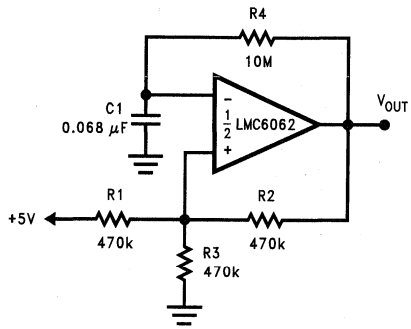

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FIGURE 8. 1 Hz Square Wave Oscillator

National Semiconductor

PRELIMINARY

LMC6064 Precision CMOS Quad Micropower Operational Amplifier

General Description

The LMC6064 is a precision quad low offset voltage, micropower operational amplifier, capable of precision single supply operation. Performance characteristics include ultra low input bias current, high voltage gain, rail-to-rail output swing, and an input common mode voltage range that includes ground. These features, plus its low power consumption make the LMC6064 ideally suited for battery powered applications.

Other applications using the LMC6064 include precision full-wave rectifiers, integrators, references, sample-and-hold circuits, and true instrumentation amplifiers.

This device is built with National's advanced double-Poly Silicon-Gate CMOS process.

For designs that require higher speed, see the LMC6084 precision quad operational amplifier.

For single or dual operational amplifier with similar features, see the LMC6061 or LMC6062 respectively.

PATENT PENDING

Features (Typical Unless Otherwise Noted)

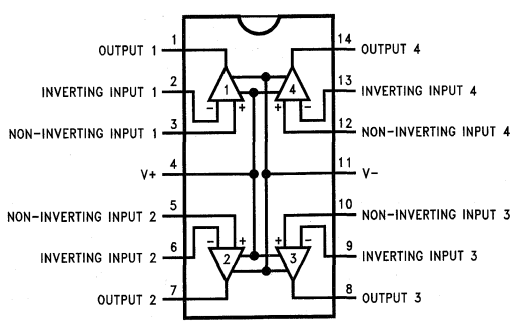
- Low offset voltage 100 μV
- Ultra low supply current 16 μA/Amplifier
- Operates from 4.5V to 15V single supply
- Ultra low input bias current 10 fA
- Output swing within 10 mV of supply rail, 100k load
- Input common-mode range includes V^-
- High voltage gain 140 dB
- Improved latchup immunity

Applications

- Instrumentation amplifier
- Photodiode and infrared detector preamplifier
- Transducer amplifiers
- Hand-held analytic instruments
- Medical instrumentation
- D/A converter
- Charge amplifier for piezoelectric transducers

Connection Diagram

14-Pin DIP/SO



TL/H/11466–1

Top View

Ordering Information

Package	Temperature Range		NSC Drawing
	Military −55°C to +125°C	**Industrial** −40°C to +85°C	
14-Pin Molded DIP	LMC6064AMN	LMC6064AIN LMC60641N	N14A
14-Pin Small Outline		LMC6064AIM LMC6064IM	M14A

For MIL-STD-883C qualified products, please contact your local National Semiconductor Sales Office or Distributor for availability and specification information.

National Semiconductor

LMC6081 Precision CMOS Single Operational Amplifier

General Description

The LMC6081 is a precision low offset voltage operational amplifier, capable of single supply operation. Performance characteristics include ultra low input bias current, high voltage gain, rail-to-rail output swing, and an input common mode voltage range that includes ground. These features, plus its low offset voltage, make the LMC6081 ideally suited for precision circuit applications.

Other applications using the LMC6081 include precision full-wave rectifiers, integrators, references, and sample-and-hold circuits.

This device is built with National's advanced Double-Poly Silicon-Gate CMOS process.

For designs with more critical power demands, see the LMC6061 precision micropower operational amplifier.

For a dual or quad operational amplifier with similar features, see the LMC6082 or LMC6084 respectively.

PATENT PENDING

Features (Typical unless otherwise stated)

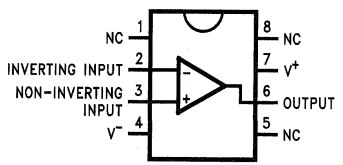
- Low offset voltage 150 μV
- Operates from 4.5V to 15V single supply
- Ultra low input bias current 10 fA
- Output swing to within 20 mV of supply rail, 100k load
- Input common-mode range includes V^-
- High voltage gain 130 dB
- Improved latchup immunity

Applications

- Instrumentation amplifier
- Photodiode and infrared detector preamplifier
- Transducer amplifiers
- Medical instrumentation
- D/A converter
- Charge amplifier for piezoelectric transducers

Connection Diagram

8-Pin DIP/SO



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Top View

Ordering Information

Package	Temperature Range		NSC Drawing
	Military −55°C to +125°C	Industrial −40°C to +85°C	
8-Pin Molded DIP	LMC6081AMN	LMC6081AIN LMC6081IN	N08E
8-Pin Small Outline		LMC6081AIM LMC6081IM	M08A

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Differential Input Voltage	±Supply Voltage
Voltage at Input/Output Pin	$(V^+) + 0.3V$, $(V^-) - 0.3V$
Supply Voltage ($V^+ - V^-$)	16V
Output Short Circuit to V^+	(Note 10)
Output Short Circuit to V^-	(Note 2)
Lead Temperature (Soldering, 10 Sec.)	260°C
Storage Temp. Range	−65°C to +150°C
Junction Temperature	150°C
ESD Tolerance (Note 4)	2 kV
Current at Input Pin	±10 mA
Current at Output Pin	±30 mA
Current at Power Supply Pin	40 mA
Power Dissipation	(Note 3)

Operating Ratings (Note 1)

Temperature Range	
LMC6081AM	$-55°C \le T_J \le +125°C$
LMC6081AI, LMC6081I	$-40°C \le T_J \le +85°C$
Supply Voltage	$4.5V \le V^+ \le 15.5V$
Thermal Resistance (θ_{JA}), (Note 11)	
N Package, 8-Pin Molded DIP	115°C/W
M Package, 8-Pin Surface Mount	193°C/W
Power Dissipation (Note 9)	

DC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for $T_J = 25°C$. **Boldface** limits apply at the temperature extremes. $V^+ = 5V$, $V^- = 0V$, $V_{CM} = 1.5V$, $V_O = 2.5V$ and $R_L > 1M$ unless otherwise specified.

Symbol	Parameter	Conditions		Typ (Note 5)	LMC6081AM Limit (Note 6)	LMC6081AI Limit (Note 6)	LMC6081I Limit (Note 6)	Units
V_{OS}	Input Offset Voltage			150	350 **1000**	350 **800**	800 **1300**	μV Max
TCV_{OS}	Input Offset Voltage Average Drift			1.0				μV/°C
I_B	Input Bias Current			0.010	 **100**	 **4**	 **4**	pA Max
I_{OS}	Input Offset Current			0.005	 **100**	 **2**	 **2**	pA Max
R_{IN}	Input Resistance			>10				Tera Ω
CMRR	Common Mode Rejection Ratio	$0V \le V_{CM} \le 12.0V$ $V^+ = 15V$		85	75 **72**	75 **72**	66 **63**	dB Min
+PSRR	Positive Power Supply Rejection Ratio	$5V \le V^+ \le 15V$ $V_O = 2.5V$		85	75 **72**	75 **72**	66 **63**	dB Min
−PSRR	Negative Power Supply Rejection Ratio	$0V \le V^- \le -10V$		94	84 **81**	84 **81**	74 **71**	dB Min
V_{CM}	Input Common-Mode Voltage Range	$V^+ = 5V$ and 15V for CMRR ≥ 60 dB		−0.4	−0.1 **0**	−0.1 **0**	−0.1 **0**	V Max
				$V^+ - 1.9$	$V^+ - 2.3$ $\mathbf{V^+ - 2.6}$	$V^+ - 2.3$ $\mathbf{V^+ - 2.5}$	$V^+ - 2.3$ $\mathbf{V^+ - 2.5}$	V Min
A_V	Large Signal Voltage Gain	$R_L = 2 k\Omega$ (Note 7)	Sourcing	1400	400 **300**	400 **300**	300 **200**	V/mV Min
			Sinking	350	180 **70**	180 **100**	90 **60**	V/mV Min
		$R_L = 600\Omega$ (Note 7)	Sourcing	1200	400 **150**	400 **150**	200 **80**	V/mV Min
			Sinking	150	100 **35**	100 **50**	70 **35**	V/mV Min

DC Electrical Characteristics (Continued)

Unless otherwise specified, all limits guaranteed for T_J = 25°C. **Boldface** limits apply at the temperature extremes. V^+ = 5V, V^- = 0V, V_{CM} = 1.5V, V_O = 2.5V and R_L > 1M unless otherwise specified.

Symbol	Parameter	Conditions	Typ (Note 5)	LMC6081AM Limit (Note 6)	LMC6081AI Limit (Note 6)	LMC6081I Limit (Note 6)	Units
V_O	Output Swing	V^+ = 5V R_L = 2 kΩ to 2.5V	4.87	4.80 **4.70**	4.80 **4.73**	4.75 **4.67**	V Min
			0.10	0.13 **0.19**	0.13 **0.17**	0.20 **0.24**	V Max
		V^+ = 5V R_L = 600Ω to 2.5V	4.61	4.50 **4.24**	4.50 **4.31**	4.40 **4.21**	V Min
			0.30	0.40 **0.63**	0.40 **0.50**	0.50 **0.63**	V Max
		V^+ = 15V R_L = 2 kΩ to 7.5V	14.63	14.50 **14.30**	14.50 **14.34**	14.37 **14.25**	V Min
			0.26	0.35 **0.48**	0.35 **0.45**	0.44 **0.56**	V Max
		V^+ = 15V R_L = 600Ω to 7.5V	13.90	13.35 **12.80**	13.35 **12.86**	12.92 **12.44**	V Min
			0.79	1.16 **1.42**	1.16 **1.32**	1.33 **1.58**	V Max
I_O	Output Current V^+ = 5V	Sourcing, V_O = 0V	22	16 **8**	16 **10**	13 **8**	mA Min
		Sinking, V_O = 5V	21	16 **11**	16 **13**	13 **10**	mA Min
I_O	Output Current V^+ = 15V	Sourcing, V_O = 0V	30	28 **18**	28 **22**	23 **18**	mA Min
		Sinking, V_O = 13V (Note 10)	34	28 **19**	28 **22**	23 **18**	mA Min
I_S	Supply Current	V^+ = +5V, V_O = 1.5V	450	750 **900**	750 **900**	750 **900**	μA Max
		V^+ = +15V, V_O = 7.5V	550	850 **950**	850 **950**	850 **950**	μA Max

AC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for T_J = 25°C, **Boldface** limits apply at the temperature extremes. V^+ = 5V, V^- = 0V, V_{CM} = 1.5V, V_O = 2.5V and R_L > 1M unless otherwise specified.

Symbol	Parameter	Conditions	Typ (Note 5)	LMC6081AM Limit (Note 6)	LMC6081AI Limit (Note 6)	LMC6081 Limit (Note 6)	Units
SR	Slew Rate	(Note 8)	1.5	1.2 **0.6**	1.2 **0.8**	1.0 **0.7**	V/μs Min
GBW	Gain-Bandwidth Product		1.3				MHz
ϕ_m	Phase Margin		50				Deg
e_n	Input-Referred Voltage Noise	F = 1 kHz	22				nV/$\sqrt{Hz}$
i_n	Input-Referred Current Noise	F = 1 kHz	0.0002				pA/$\sqrt{Hz}$
T.H.D.	Total Harmonic Distortion	F = 10 kHz, A_V = −10 R_L = 2 kΩ, V_O = 8 V_{PP} ±5V Supply	0.01				%

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed.

Note 2: Applies to both single-supply and split-supply operation. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C. Output currents in excess of ±30 mA over long term may adversely affect reliability.

Note 3: The maximum power dissipation is a function of $T_{J(Max)}$, θ_{JA}, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(Max)} - T_A) / \theta_{JA}$.

Note 4: Human body model, 1.5 kΩ in series with 100 pF.

Note 5: Typical values represent the most likely parametric norm.

Note 6: All limits are guaranteed by testing or statistical analysis.

Note 7: V^+ = 15V, V_{CM} = 7.5V and R_L connected to 7.5V. For Sourcing tests, 7.5V ≤ V_O ≤ 11.5V. For Sinking tests, 2.5V ≤ V_O ≤ 7.5V.

Note 8: V^+ = 15V. Connected as Voltage Follower with 10V step input. Number specified is the slower of the positive and negative slew rates.

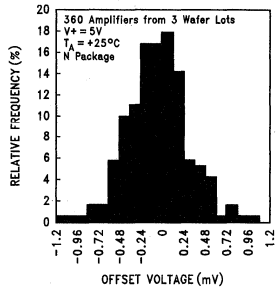
Note 9: For operating at elevated temperatures the device must be derated based on the thermal resistance θ_{JA} with $P_D = (T_J - T_A)/\theta_{JA}$.

Note 10: Do not connect output to V^+, when V^+ is greater than 13V or reliability will be adversely affected.

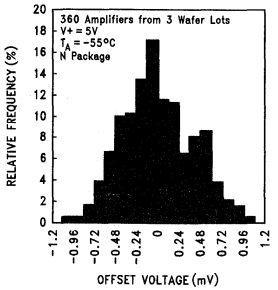
Note 11: All numbers apply for packages soldered directly into a PC board.

Typical Performance Characteristics $V_S = \pm 7.5V$, $T_A = 25°C$, Unless otherwise specified

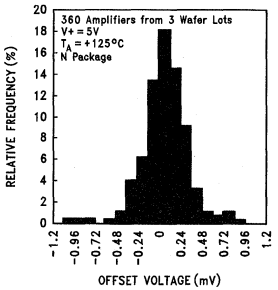
Distribution of LMC6081 Input Offset Voltage ($T_A = +25°C$)



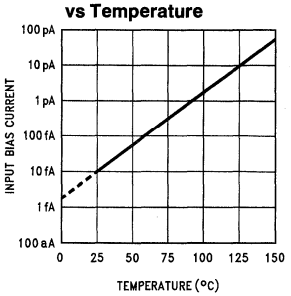
Distribution of LMC6081 Input Offset Voltage ($T_A = -55°C$)



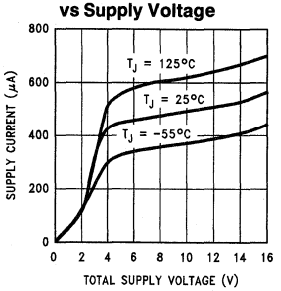
Distribution of LMC6081 Input Offset Voltage ($T_A = +125°C$)



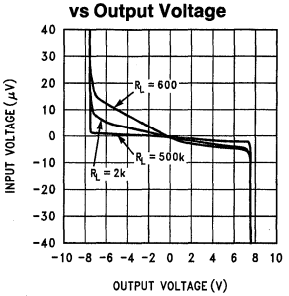
Input Bias Current vs Temperature



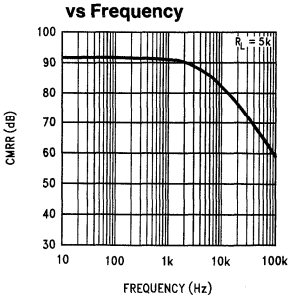
Supply Current vs Supply Voltage



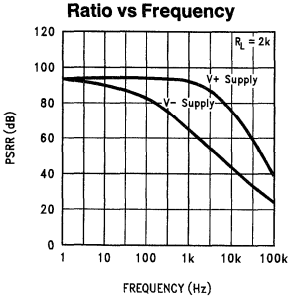
Input Voltage vs Output Voltage



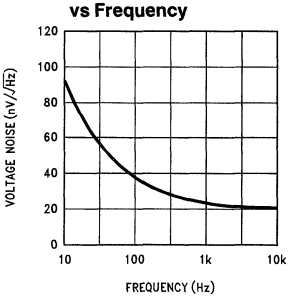
Common Mode Rejection Ratio vs Frequency



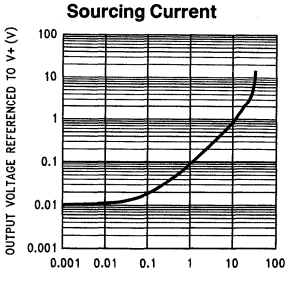
Power Supply Rejection Ratio vs Frequency



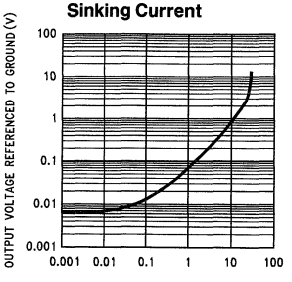
Input Voltage Noise vs Frequency



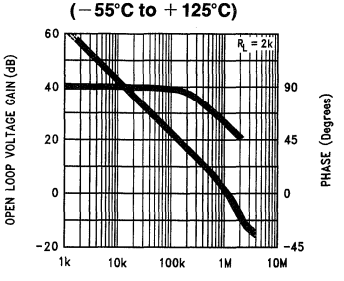
Output Characteristics Sourcing Current



Output Characteristics Sinking Current



Gain and Phase Response vs Temperature (−55°C to +125°C)



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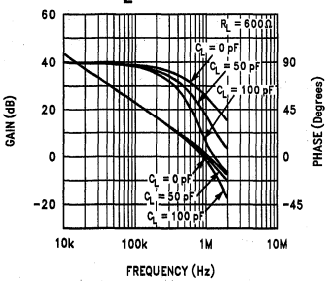
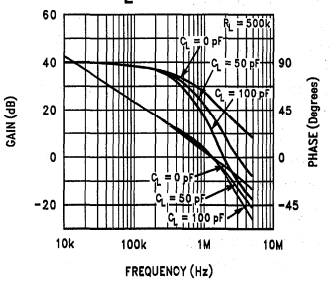
Typical Performance Characteristics $V_S = \pm 7.5V$, $T_A = 25°C$, Unless otherwise specified

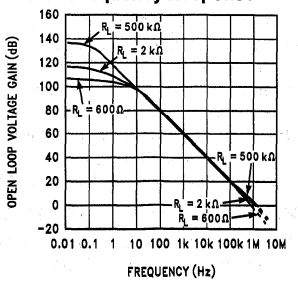
Gain and Phase Response vs Capacitive Load with $R_L = 600\Omega$



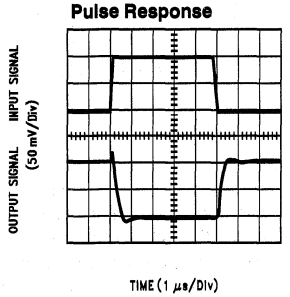
Gain and Phase Response vs Capacitive Load with $R_L = 500\ k\Omega$



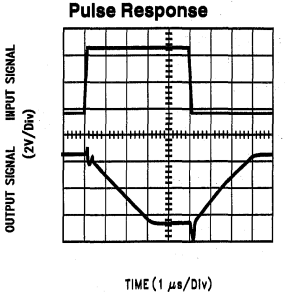
Open Loop Frequency Response



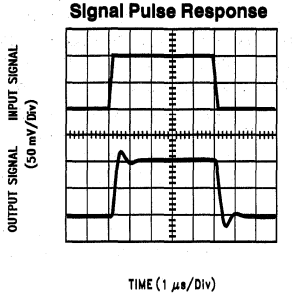
Inverting Small Signal Pulse Response



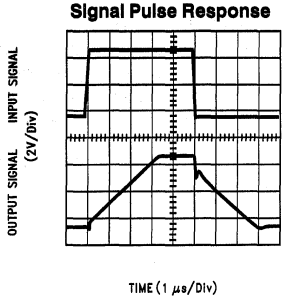
Inverting Large Signal Pulse Response



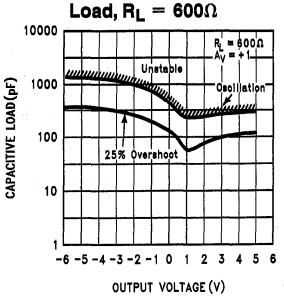
Non-Inverting Small Signal Pulse Response



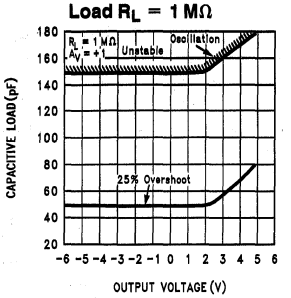
Non-Inverting Large Signal Pulse Response



Stability vs Capacitive Load, $R_L = 600\Omega$



Stability vs Capacitive Load $R_L = 1\ M\Omega$



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Applications Hints

AMPLIFIER TOPOLOGY

The LMC6081 incorporates a novel op-amp design topology that enables it to maintain rail-rail output swing even when driving a large load. Instead of relying on a push-pull unity gain output buffer stage, the output stage is taken directly from the internal integrator, which provides both low output impedance and large gain. Special feed-forward compensation design techniques are incorporated to maintain stability over a wider range of operating conditions than traditional micropower op-amps. These features make the LMC6081 both easier to design with, and provide higher speed than products typically found in this ultra-low power class.

COMPENSATING FOR INPUT CAPACITANCE

It is quite common to use large values of feedback resistance for amplifiers with ultra-low input current, like the LMC6081.

Although the LMC6081 is highly stable over a wide range of operating conditions, certain precautions must be met to achieve the desired pulse response when a large feedback resistor is used. Large feedback resistors and even small values of input capacitance, due to transducers, photodiodes, and circuit board parasitics, reduce phase margins.

When high input impedances are demanded, guarding of the LMC6081 is suggested. Guarding input lines will not only reduce leakage, but lowers stray input capacitance as well. (See *Printed-Circuit-Board Layout for High Impedance Work).*

The effect of input capacitance can be compensated for by adding a capacitor, C_f, around the feedback resistors (as in *Figure 1*) such that:

$$\frac{1}{2\pi R_1 C_{IN}} \geq \frac{1}{2\pi R_2 C_f}$$

or

$$R_1 C_{IN} \leq R_2 C_f$$

Since it is often difficult to know the exact value of C_{IN}, C_f can be experimentally adjusted so that the desired pulse response is achieved. Refer to the LMC660 and LMC662 for a more detailed discussion on compensating for input capacitance.

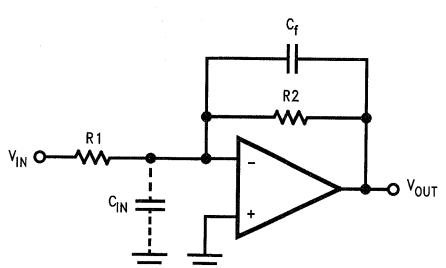

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FIGURE 1. Cancelling the Effect of Input Capacitance

CAPACITIVE LOAD TOLERANCE

All rail-to-rail output swing operational amplifiers have voltage gain in the output stage. A compensation capacitor is normally included in this integrator stage. The frequency location of the dominant pole is affected by the resistive load on the amplifier. Capacitive load driving capability can be optimized by using an appropriate resistive load in parallel with the capacitive load (see typical curves).

Direct capacitive loading will reduce the phase margin of many op-amps. A pole in the feedback loop is created by the combination of the op-amp's output impedance and the capacitive load. This pole induces phase lag at the unity-gain crossover frequency of the amplifier resulting in either an oscillatory or underdamped pulse response. With a few external components, op amps can easily indirectly drive capacitive loads, as shown in *Figure 2a*.

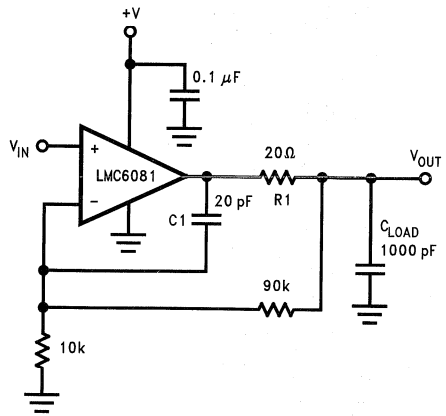

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FIGURE 2a. LMC6081 Noninverting Gain of 10 Amplifier, Compensated to Handle Capacitive Loads

In the circuit of *Figure 2a*, R1 and C1 serve to counteract the loss of phase margin by feeding the high frequency component of the output signal back to the amplifier's inverting input, thereby preserving phase margin in the overall feedback loop.

Capacitive load driving capability is enhanced by using a pull up resistor to V^+ *(Figure 2b)*. Typically a pull up resistor conducting 500 μA or more will significantly improve capacitive load responses. The value of the pull up resistor must be determined based on the current sinking capability of the amplifier with respect to the desired output swing. Open loop gain of the amplifier can also be affected by the pull up resistor (see electrical characteristics).

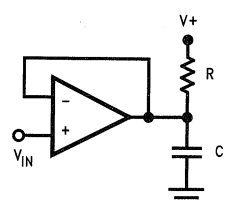

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FIGURE 2b: Compensating for Large Capacitive Loads with a Pull Up Resistor

PRINTED-CIRCUIT-BOARD LAYOUT FOR HIGH-IMPEDANCE WORK

It is generally recognized that any circuit which must operate with less than 1000 pA of leakage current requires special layout of the PC board. When one wishes to take advantage of the ultra-low bias current of the LMC6081, typically less than 10 fA, it is essential to have an excellent layout. Fortunately, the techniques of obtaining low leakages are quite simple. First, the user must not ignore the surface

Applications Hints

leakage of the PC board, even though it may sometimes appear acceptably low, because under conditions of high humidity or dust or contamination, the surface leakage will be appreciable.

To minimize the effect of any surface leakage, lay out a ring of foil completely surrounding the LMC6081's inputs and the terminals of capacitors, diodes, conductors, resistors, relay terminals, etc. connected to the op-amp's inputs, as in *Figure 3*. To have a significant effect, guard rings should be placed on both the top and bottom of the PC board. This PC foil must then be connected to a voltage which is at the same voltage as the amplifier inputs, since no leakage current can flow between two points at the same potential. For example, a PC board trace-to-pad resistance of $10^{12}\Omega$, which is normally considered a very large resistance, could leak 5 pA if the trace were a 5V bus adjacent to the pad of the input. This would cause a 100 times degradation from the LMC6081's actual performance. However, if a guard ring is held within 5 mV of the inputs, then even a resistance of $10^{11}\Omega$ would cause only 0.05 pA of leakage current. See *Figures 4a*, *4b*, *4c* for typical connections of guard rings for standard op-amp configurations.

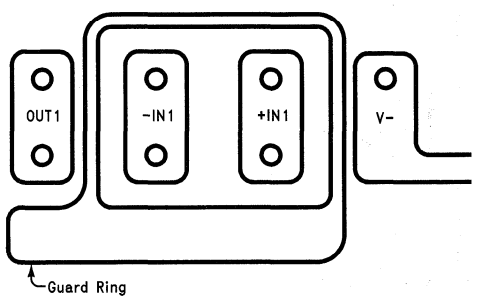

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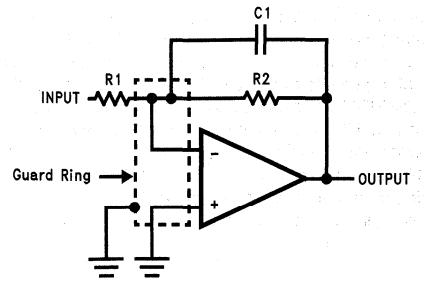
FIGURE 3. Example of Guard Ring in P.C. Board Layout



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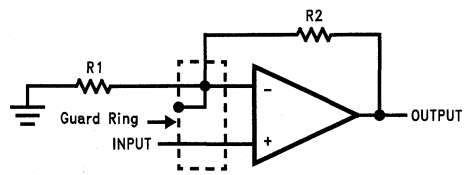
(a) Inverting Amplifier



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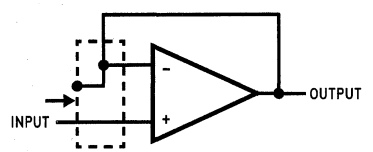
(b) Non-Inverting Amplifier



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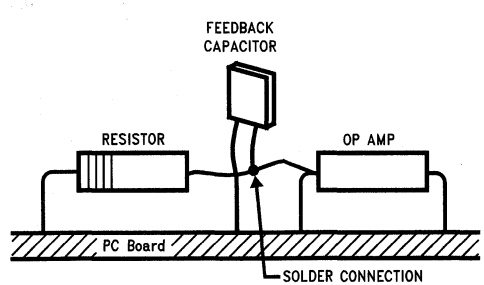
(c) Follower

FIGURE 4. Typical Connections of Guard Rings

The designer should be aware that when it is inappropriate to lay out a PC board for the sake of just a few circuits, there is another technique which is even better than a guard ring on a PC board: Don't insert the amplifier's input pin into the board at all, but bend it up in the air and use only air as an insulator. Air is an excellent insulator. In this case you may have to forego some of the advantages of PC board construction, but the advantages are sometimes well worth the effort of using point-to-point up-in-the-air wiring. See *Figure 5*.



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(Input pins are lifted out of PC board and soldered directly to components. All other pins connected to PC board).

FIGURE 5. Air Wiring

Latchup

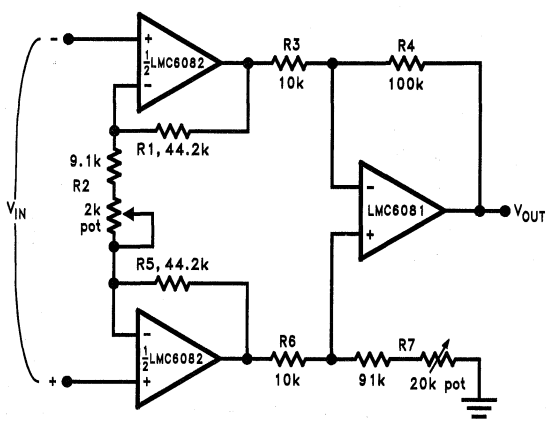
CMOS devices tend to be susceptible to latchup due to their internal parasitic SCR effects. The (I/O) input and output pins look similar to the gate of the SCR. There is a minimum current required to trigger the SCR gate lead. The LMC6061 and LMC6081 are designed to withstand 100 mA surge current on the I/O pins. Some resistive method should be used to isolate any capacitance from supplying excess current to the I/O pins. In addition, like an SCR, there is a minimum holding current for any latchup mode. Limiting current to the supply pins will also inhibit latchup susceptibility.

Typical Single-Supply Applications

($V^+ = 5.0\ V_{DC}$)

The extremely high input impedance, and low power consumption, of the LMC6081 make it ideal for applications that require battery-powered instrumentation amplifiers. Examples of these types of applications are hand-held pH probes, analytic medical instruments, magnetic field detectors, gas detectors, and silicon based pressure transducers.

Figure 6 shows an instrumentation amplifier that features high differential and common mode input resistance ($>10^{14}\Omega$), 0.01% gain accuracy at $A_V = 1000$, excellent CMRR with 1 kΩ imbalance in bridge source resistance. Input current is less than 100 fA and offset drift is less than 2.5 μV/°C. R_2 provides a simple means of adjusting gain over a wide range without degrading CMRR. R_7 is an initial trim used to maximize CMRR without using super precision matched resistors. For good CMRR over temperature, low drift resistors should be used.



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If $R_1 = R_5$, $R_3 = R_6$, and $R_4 = R_7$; then

$$\frac{V_{OUT}}{V_{IN}} = \frac{R_2 + 2R_1}{R_2} \times \frac{R_4}{R_3}$$

$\therefore A_V \approx 100$ for circuit shown ($R_2 = 9.822k$).

FIGURE 6. Instrumentation Amplifier

Typical Single-Supply Applications ($V^+ = 5.0\ V_{DC}$)

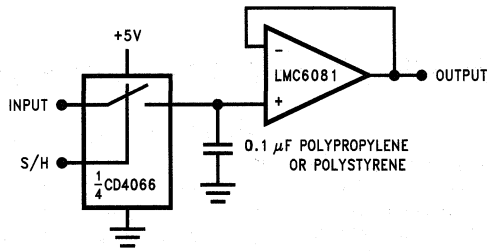

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FIGURE 7. Low-Leakage Sample and Hold

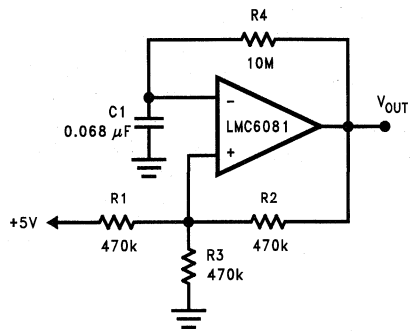

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FIGURE 8. 1 Hz Square Wave Oscillator

National Semiconductor

LMC6082 Precision CMOS Dual Operational Amplifier

General Description

The LMC6082 is a precision dual low offset voltage operational amplifier, capable of single supply operation. Performance characteristics include ultra low input bias current, high voltage gain, rail-to-rail output swing, and an input common mode voltage range that includes ground. These features, plus its low offset voltage, make the LMC6082 ideally suited for precision circuit applications.

Other applications using the LMC6082 include precision full-wave rectifiers, integrators, references, and sample-and-hold circuits.

This device is built with National's advanced Double-Poly Silicon-Gate CMOS process.

For designs with more critical power demands, see the LMC6062 precision dual micropower operational amplifier.

PATENT PENDING

Features (Typical unless otherwise stated)

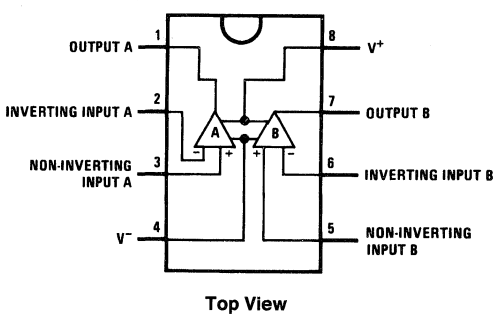
- Low offset voltage 150 μV
- Operates from 4.5V to 15V single supply
- Ultra low input bias current 10 fA
- Output swing to within 20 mV of supply rail, 100k load
- Input common-mode range includes V^-
- High voltage gain 130 dB
- Improved latchup immunity

Applications

- Instrumentation amplifier
- Photodiode and infrared detector preamplifier
- Transducer amplifiers
- Medical instrumentation
- D/A converter
- Charge amplifier for piezoelectric transducers

Connection Diagram

8-Pin DIP/SO



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Top View

Ordering Information

Package	Temperature Range		NSC Drawing
	Military −55°C to +125°C	Industrial −40°C to +85°C	
8-Pin Molded DIP	LMC6082AMN	LMC6082AIN LMC6082IN	N08E
8-Pin Small Outline		LMC6082AIM LMC6082IM	M08A

For MIL-STD-883C qualified products, please contact your local National Semiconductor Sales Office or Distributor for availability and specification information.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Differential Input Voltage	±Supply Voltage
Voltage at Input/Output Pin	(V^+) +0.3V, (V^-) −0.3V
Supply Voltage $(V^+ - V^-)$	16V
Output Short Circuit to V^+	(Note 11)
Output Short Circuit to V^-	(Note 2)
Lead Temperature (Soldering, 10 Sec.)	260°C
Storage Temp. Range	−65°C to +150°C
Junction Temperature	150°C
ESD Tolerance (Note 4)	2 kV
Current at Input Pin	±10 mA
Current at Output Pin	±30 mA
Current at Power Supply Pin	40 mA
Power Dissipation	(Note 3)

Operating Ratings (Note 1)

Temperature Range	
LMC6082AM	$-55°C \le T_J \le +125°C$
LMC6082AI, LMC6082I	$-40°C \le T_J \le +85°C$
Supply Voltage	$4.5V \le V^+ \le 15.5V$
Thermal Resistance (θ_{JA}) (Note 12)	
8-Pin Molded DIP	115°C/W
8-Pin SO	193°C/W
Power Dissipation	(Note 10)

DC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for T_J = 25°C. **Boldface** limits apply at the temperature extremes. V^+ = 5V, V^- = 0V, V_{CM} = 1.5V, V_O = 2.5V and R_L > 1M unless otherwise specified.

Symbol	Parameter	Conditions		Typ (Note 5)	LMC6082AM Limit (Note 6)	LMC6082AI Limit (Note 6)	LMC6082I Limit (Note 6)	Units
V_{OS}	Input Offset Voltage			150	350 **1000**	350 **800**	800 **1300**	μV Max
TCV_{OS}	Input Offset Voltage Average Drift			1.0				μV/°C
I_B	Input Bias Current			0.010	 **100**	 **4**	 **4**	pA Max
I_{OS}	Input Offset Current			0.005	 **100**	 **2**	 **2**	pA Max
R_{IN}	Input Resistance			>10				Tera Ω
CMRR	Common Mode Rejection Ratio	$0V \le V_{CM} \le 12.0V$ $V^+ = 15V$		85	75 **72**	75 **72**	66 **63**	dB Min
+PSRR	Positive Power Supply Rejection Ratio	$5V \le V^+ \le 15V$ $V_O = 2.5V$		85	75 **72**	75 **72**	66 **63**	dB Min
−PSRR	Negative Power Supply Rejection Ratio	$0V \le V^- \le -10V$		94	84 **81**	84 **81**	74 **71**	dB Min
V_{CM}	Input Common-Mode Voltage Range	V^+ = 5V and 15V for CMRR ≥ 60 dB		−0.4	−0.1 **0**	−0.1 **0**	−0.1 **0**	V Max
				$V^+ - 1.9$	$V^+ - 2.3$ $\mathbf{V^+ - 2.6}$	$V^+ - 2.3$ $\mathbf{V^+ - 2.5}$	$V^+ - 2.3$ $\mathbf{V^+ - 2.5}$	V Min
A_V	Large Signal Voltage Gain	R_L = 2 kΩ (Note 7)	Sourcing	1400	400 **300**	400 **300**	300 **200**	V/mV Min
			Sinking	350	180 **70**	180 **100**	90 **60**	V/mV Min
		R_L = 600Ω (Note 7)	Sourcing	1200	400 **150**	400 **150**	200 **80**	V/mV Min
			Sinking	150	100 **35**	100 **50**	70 **35**	V/mV Min

DC Electrical Characteristics (Continued)

Unless otherwise specified, all limits guaranteed for T_J = 25°C. **Boldface** limits apply at the temperature extremes. V^+ = 5V, V^- = 0V, V_{CM} = 1.5V, V_O = 2.5V and R_L > 1M unless otherwise specified.

Symbol	Parameter	Conditions	Typ (Note 5)	LMC6082AM Limit (Note 6)	LMC6082AI Limit (Note 6)	LMC6082I Limit (Note 6)	Units
V_O	Output Swing	V^+ = 5V R_L = 2 kΩ to 2.5V	4.87	4.80 **4.70**	4.80 **4.73**	4.75 **4.67**	V Min
			0.10	0.13 **0.19**	0.13 **0.17**	0.20 **0.24**	V Max
		V^+ = 5V R_L = 600Ω to 2.5V	4.61	4.50 **4.24**	4.50 **4.31**	4.40 **4.21**	V Min
			0.30	0.40 **0.63**	0.40 **0.50**	0.50 **0.63**	V Max
		V^+ = 15V R_L = 2 kΩ to 7.5V	14.63	14.50 **14.30**	14.50 **14.34**	14.37 **14.25**	V Min
			0.26	0.35 **0.48**	0.35 **0.45**	0.44 **0.56**	V Max
		V^+ = 15V R_L = 600Ω to 7.5V	13.90	13.35 **12.80**	13.35 **12.86**	12.92 **12.44**	V Min
			0.79	1.16 **1.42**	1.16 **1.32**	1.33 **1.58**	V Max
I_O	Output Current V^+ = 5V	Sourcing, V_O = 0V	22	16 **8**	16 **10**	13 **8**	mA Min
		Sinking, V_O = 5V	21	16 **11**	16 **13**	13 **10**	mA Min
I_O	Output Current V^+ = 15V	Sourcing, V_O = 0V	30	28 **18**	28 **22**	23 **18**	mA Min
		Sinking, V_O = 13V (Note 11)	34	28 **19**	28 **22**	23 **18**	mA Min
I_S	Supply Current	Both Amplifiers V^+ = +5V, V_O = 1.5V	0.9	1.5 **1.8**	1.5 **1.8**	1.5 **1.8**	mA Max
		Both Amplifiers V^+ = +15V, V_O = 7.5V	1.1	1.7 **2**	1.7 **2**	1.7 **2**	mA Max

AC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for T_J = 25°C, **Boldface** limits apply at the temperature extremes. V^+ = 5V, V^- = 0V, V_{CM} = 1.5V, V_O = 2.5V and R_L > 1M unless otherwise specified.

Symbol	Parameter	Conditions	Typ (Note 5)	LMC6082AM Limit (Note 6)	LMC6082AI Limit (Note 6)	LMC6082I Limit (Note 6)	Units
SR	Slew Rate	(Note 8)	1.5	1.2 **0.6**	1.2 **0.8**	1.0 **0.7**	V/μs Min
GBW	Gain-Bandwidth Product		1.3				MHz
ϕ_m	Phase Margin		50				Deg
	Amp-to-Amp Isolation	(Note 9)	140				dB
e_n	Input-Referred Voltage Noise	F = 1 kHz	22				nV/$\sqrt{Hz}$
i_n	Input-Referred Current Noise	F = 1 kHz	0.0002				pA/$\sqrt{Hz}$
T.H.D.	Total Harmonic Distortion	F = 10 kHz, A_V = −10 R_L = 2 kΩ, V_O = 8 V_{PP} ±5V Supply	0.01				%

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed.

Note 2: Applies to both single-supply and split-supply operation. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C. Output currents in excess of ±30 mA over long term may adversely affect reliability.

Note 3: The maximum power dissipation is a function of $T_{J(Max)}$, θ_{JA}, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(Max)} - T_A)/\theta_{JA}$.

Note 4: Human body model, 1.5 kΩ in series with 100 pF.

Note 5: Typical values represent the most likely parametric norm.

Note 6: All limits are guaranteed by testing or statistical analysis.

Note 7: V^+ = 15V, V_{CM} = 7.5V and R_L connected to 7.5V. For Sourcing tests, 7.5V ≤ V_O ≤ 11.5V. For Sinking tests, 2.5V ≤ V_O ≤ 7.5V.

Note 8: V^+ = 15V. Connected as Voltage Follower with 10V step input. Number specified is the slower of the positive and negative slew rates.

Note 9: Input referred V^+ = 15V and R_L = 100 kΩ connected to 7.5V. Each amp excited in turn with 1 kHz to produce V_O = 12 V_{PP}.

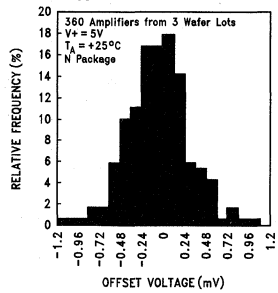
Note 10: For operating at elevated temperatures the device must be derated based on the thermal resistance θ_{JA} with $P_D = (T_J - T_A)/\theta_{JA}$. All numbers apply for packages soldered directly into a PC board.

Note 11: Do not connect output to V^+, when V^+ is greater than 13V or reliability will be adversely affected.

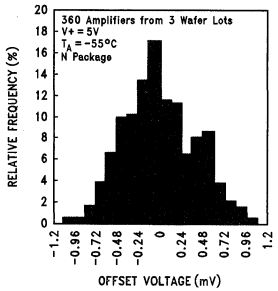
Note 12: All numbers apply for packages soldered directly into a PC board.

Typical Performance Characteristics $V_S = \pm 7.5V$, $T_A = 25°C$, Unless otherwise specified

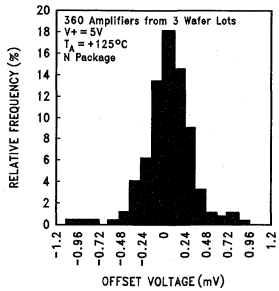
Distribution of LMC6082 Input Offset Voltage ($T_A = +25°C$)



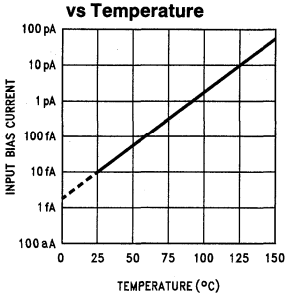
Distribution of LMC6082 Input Offset Voltage ($T_A = -55°C$)



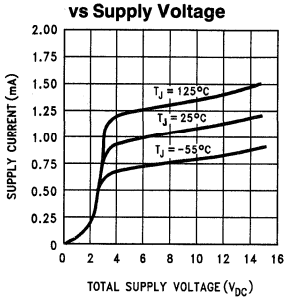
Distribution of LMC6082 Input Offset Voltage ($T_A = +125°C$)



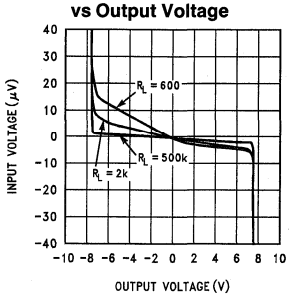
Input Bias Current vs Temperature



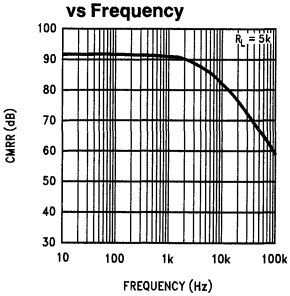
Supply Current vs Supply Voltage



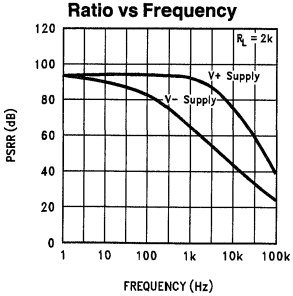
Input Voltage vs Output Voltage



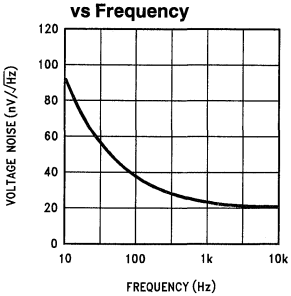
Common Mode Rejection Ratio vs Frequency



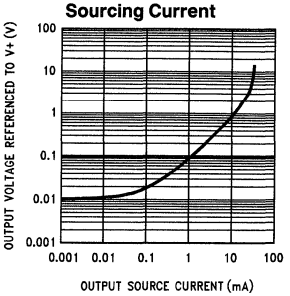
Power Supply Rejection Ratio vs Frequency



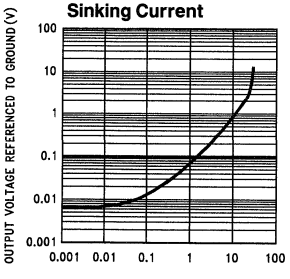
Input Voltage Noise vs Frequency



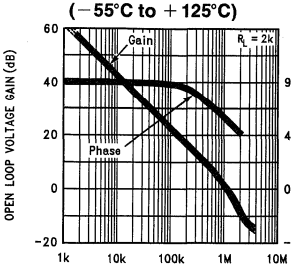
Output Characteristics Sourcing Current



Output Characteristics Sinking Current



Gain and Phase Response vs Temperature (−55°C to +125°C)



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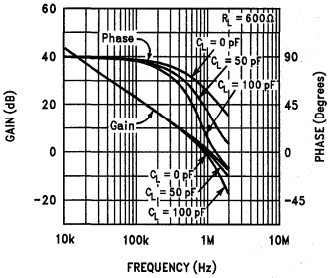
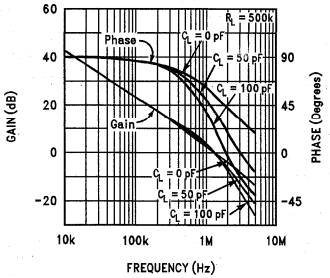
Typical Performance Characteristics $V_S = \pm 7.5V$, $T_A = 25°C$, Unless otherwise specified

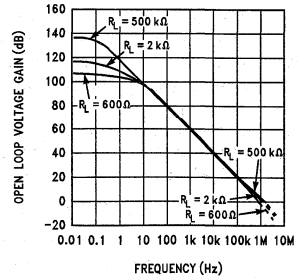
Gain and Phase Response vs Capacitive Load with $R_L = 600\Omega$



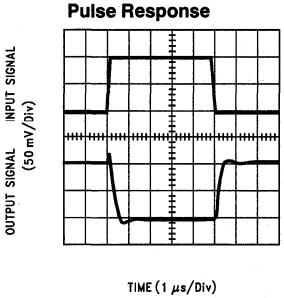
Gain and Phase Response vs Capacitive Load with $R_L = 500\ k\Omega$



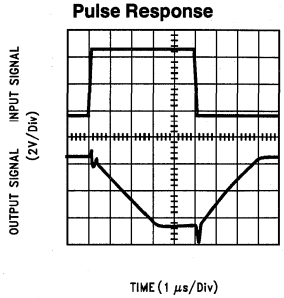
Open Loop Frequency Response



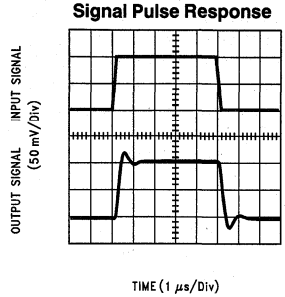
Inverting Small Signal Pulse Response



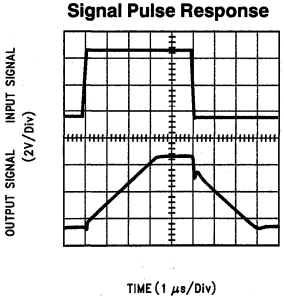
Inverting Large Signal Pulse Response



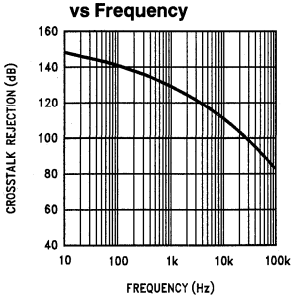
Non-Inverting Small Signal Pulse Response



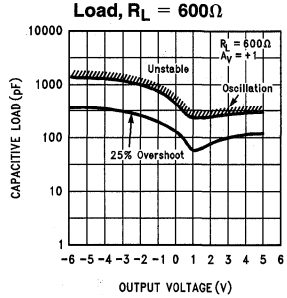
Non-Inverting Large Signal Pulse Response



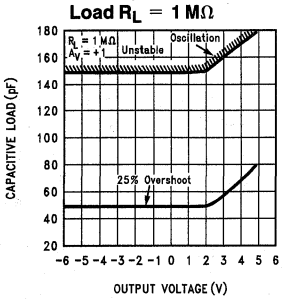
Crosstalk Rejection vs Frequency



Stability vs Capacitive Load, $R_L = 600\Omega$



Stability vs Capacitive Load $R_L = 1\ M\Omega$



TL/H/11297–3

Applications Hints

AMPLIFIER TOPOLOGY

The LMC6082 incorporates a novel op-amp design topology that enables it to maintain rail-rail output swing even when driving a large load. Instead of relying on a push-pull unity gain output buffer stage, the output stage is taken directly from the internal integrator, which provides both low output impedance and large gain. Special feed-forward compensation design techniques are incorporated to maintain stability over a wider range of operating conditions than traditional micropower op-amps. These features make the LMC6082 both easier to design with, and provide higher speed than products typically found in this ultra-low power class.

COMPENSATING FOR INPUT CAPACITANCE

It is quite common to use large values of feedback resistance for amplifiers with ultra-low input current, like the LMC6082.

Although the LMC6082 is highly stable over a wide range of operating conditions, certain precautions must be met to achieve the desired pulse response when a large feedback resistor is used. Large feedback resistors and even small values of input capacitance, due to transducers, photodiodes, and circuit board parasitics, reduce phase margins.

When high input impedances are demanded, guarding of the LMC6082 is suggested. Guarding input lines will not only reduce leakage, but lowers stray input capacitance as well. (See *Printed-Circuit-Board Layout for High Impedance Work).*

The effect of input capacitance can be compensated for by adding a capacitor, C_f, around the feedback resistors (as in *Figure 1*) such that:

$$\frac{1}{2\pi R_1 C_{IN}} \geq \frac{1}{2\pi R_2 C_f}$$

or

$$R_1 C_{IN} \leq R_2 C_f$$

Since it is often difficult to know the exact value of C_{IN}, C_f can be experimentally adjusted so that the desired pulse response is achieved. Refer to the LMC660 and LMC662 for a more detailed discussion on compensating for input capacitance.

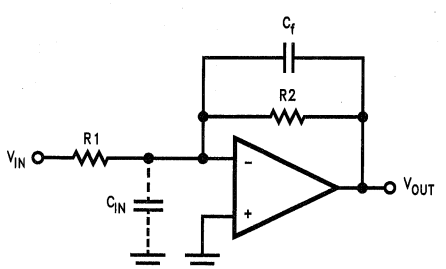


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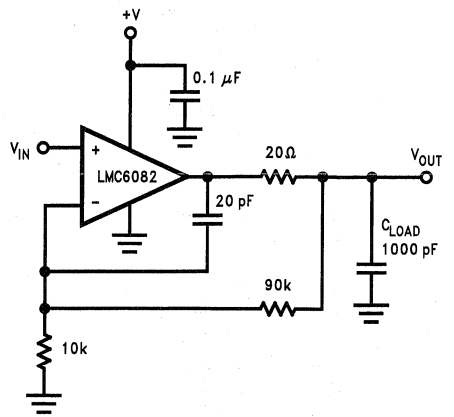
FIGURE 1. Cancelling the Effect of Input Capacitance

CAPACITIVE LOAD TOLERANCE

All rail-to-rail output swing operational amplifiers have voltage gain in the output stage. A compensation capacitor is normally included in this integrator stage. The frequency location of the dominant pole is affected by the resistive load on the amplifier. Capacitive load driving capability can be optimized by using an appropriate resistive load in parallel with the capacitive load (see typical curves).

Direct capacitive loading will reduce the phase margin of many op-amps. A pole in the feedback loop is created by the combination of the op-amp's output impedance and the capacitive load. This pole induces phase lag at the unity-gain crossover frequency of the amplifier resulting in either an oscillatory or underdamped pulse response. With a few external components, op amps can easily indirectly drive capacitive loads, as shown in *Figure 2a.*



TL/H/11297–5

FIGURE 2a. LMC6082 Noninverting Gain of 10 Amplifier, Compensated to Handle Capacitive Loads

In the circuit of *Figure 2a*, R1 and C1 serve to counteract the loss of phase margin by feeding the high frequency component of the output signal back to the amplifier's inverting input, thereby preserving phase margin in the overall feedback loop.

Capacitive load driving capability is enhanced by using a pull up resistor to V^+ *(Figure 2b).* Typically a pull up resistor conducting 500 μA or more will significantly improve capacitive load responses. The value of the pull up resistor must be determined based on the current sinking capability of the amplifier with respect to the desired output swing. Open loop gain of the amplifier can also be affected by the pull up resistor (see Electrical Characteristics).

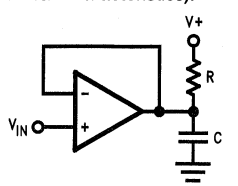


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FIGURE 2b. Compensating for Large Capacitive Loads with a Pull Up Resistor

PRINTED-CIRCUIT-BOARD LAYOUT FOR HIGH-IMPEDANCE WORK

It is generally recognized that any circuit which must operate with less than 1000 pA of leakage current requires special layout of the PC board. When one wishes to take advantage of the ultra-low bias current of the LMC6082, typically less than 10 fA, it is essential to have an excellent layout. Fortunately, the techniques of obtaining low leakages are quite simple. First, the user must not ignore the surface

Applications Hints

leakage of the PC board, even though it may sometimes appear acceptably low, because under conditions of high humidity or dust or contamination, the surface leakage will be appreciable.

To minimize the effect of any surface leakage, lay out a ring of foil completely surrounding the LMC6082's inputs and the terminals of capacitors, diodes, conductors, resistors, relay terminals, etc. connected to the op-amp's inputs, as in *Figure 3*. To have a significant effect, guard rings should be placed on both the top and bottom of the PC board. This PC foil must then be connected to a voltage which is at the same voltage as the amplifier inputs, since no leakage current can flow between two points at the same potential. For example, a PC board trace-to-pad resistance of $10^{12}\Omega$, which is normally considered a very large resistance, could leak 5 pA if the trace were a 5V bus adjacent to the pad of the input. This would cause a 100 times degradation from the LMC6082's actual performance. However, if a guard ring is held within 5 mV of the inputs, then even a resistance of $10^{11}\Omega$ would cause only 0.05 pA of leakage current. See *Figures 4a*, *4b*, *4c* for typical connections of guard rings for standard op-amp configurations.

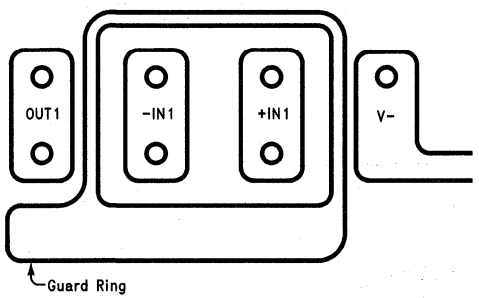

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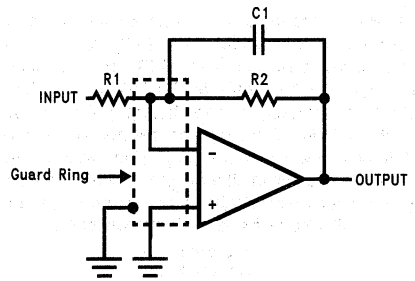
FIGURE 3. Example of Guard Ring in P.C. Board Layout



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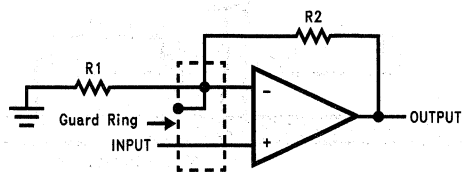
(a) Inverting Amplifier



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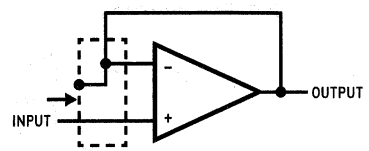
(b) Non-Inverting Amplifier



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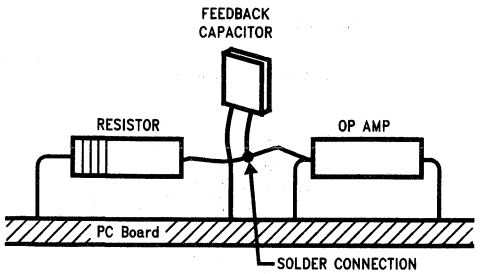
(c) Follower

FIGURE 4. Typical Connections of Guard Rings

The designer should be aware that when it is inappropriate to lay out a PC board for the sake of just a few circuits, there is another technique which is even better than a guard ring on a PC board: Don't insert the amplifier's input pin into the board at all, but bend it up in the air and use only air as an insulator. Air is an excellent insulator. In this case you may have to forego some of the advantages of PC board construction, but the advantages are sometimes well worth the effort of using point-to-point up-in-the-air wiring. See *Figure 5*.

Latchup

CMOS devices tend to be susceptible to latchup due to their internal parasitic SCR effects. The (I/O) input and output pins look similar to the gate of the SCR. There is a minimum current required to trigger the SCR gate lead. The LMC6062 and LMC6082 are designed to withstand 100 mA surge current on the I/O pins. Some resistive method should be used to isolate any capacitance from supplying excess current to the I/O pins. In addition, like an SCR, there is a minimum holding current for any latchup mode. Limiting current to the supply pins will also inhibit latchup susceptibility.



(Input pins are lifted out of PC board and soldered directly to components. All other pins connected to PC board).

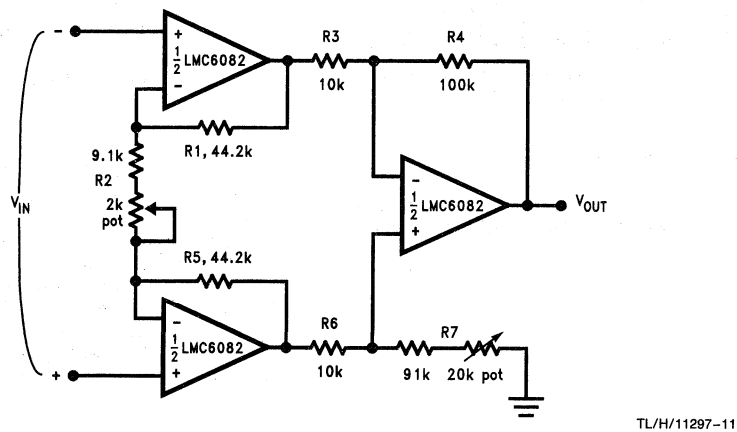
FIGURE 5. Air Wiring

Typical Single-Supply Applications

($V^+ = 5.0\ V_{DC}$)

The extremely high input impedance, and low power consumption, of the LMC6082 make it ideal for applications that require battery-powered instrumentation amplifiers. Examples of these types of applications are hand-held pH probes, analytic medical instruments, magnetic field detectors, gas detectors, and silicon based pressure transducers.

Figure 6 shows an instrumentation amplifier that features high differential and common mode input resistance ($>10^{14}\Omega$), 0.01% gain accuracy at $A_V = 1000$, excellent CMRR with 1 kΩ imbalance in bridge source resistance. Input current is less than 100 fA and offset drift is less than 2.5 μV/°C. R_2 provides a simple means of adjusting gain over a wide range without degrading CMRR. R_7 is an initial trim used to maximize CMRR without using super precision matched resistors. For good CMRR over temperature, low drift resistors should be used.



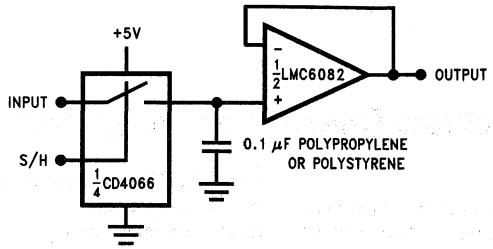
If $R_1 = R_5$, $R_3 = R_6$, and $R_4 = R_7$; then

$$\frac{V_{OUT}}{V_{IN}} = \frac{R_2 + 2R_1}{R_2} \times \frac{R_4}{R_3}$$

$\therefore A_V \approx 100$ for circuit shown ($R_2 = 9.822k$).

FIGURE 6. Instrumentation Amplifier

Typical Single-Supply Applications ($V^+ = 5.0\ V_{DC}$)



TL/H/11297–12

FIGURE 7. Low-Leakage Sample and Hold

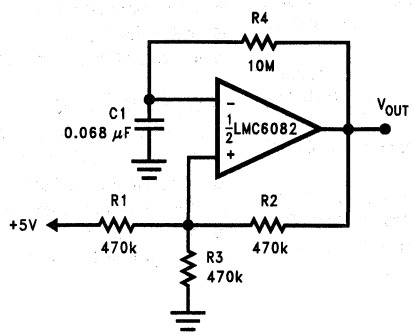


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FIGURE 8. 1 Hz Square Wave Oscillator

National Semiconductor

PRELIMINARY

LMC6084
Precision CMOS Quad Operational Amplifier

General Description

The LMC6084 is a precision quad low offset voltage operational amplifier, capable of single supply operation. Performance characteristics include ultra low input bias current, high voltage gain, rail-to-rail output swing, and an input common mode voltage range that includes ground. These features, plus its low offset voltage, make the LMC6084 ideally suited for precision circuit applications.

Other applications using the LMC6084 include precision full-wave rectifiers, integrators, references, and sample-and-hold circuits.

This device is built with National's advanced Double-Poly Silicon-Gate CMOS process.

For designs with more critical power demands, see the LMC6064 precision quad micropower operational amplifier.

For a single or dual operational amplifier with similar features, see the LMC6081 or LMC6082 respectively.

PATENT PENDING

Features (Typical unless otherwise stated)

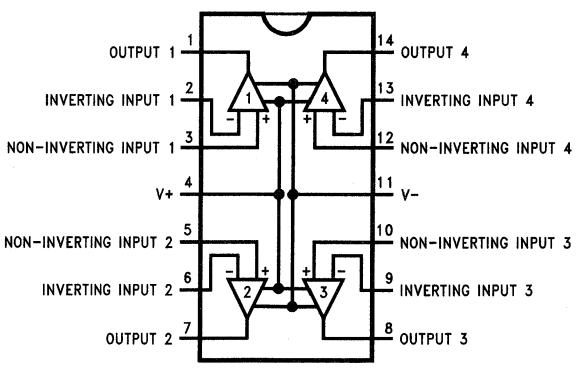
- Low offset voltage 150 μV
- Operates from 4.5V to 15V single supply
- Ultra low input bias current 10 fA
- Output swing to within 20 mV of supply rail, 100k load
- Input common-mode range includes V−
- High voltage gain 130 dB
- Improved latchup immunity

Applications

- Instrumentation amplifier
- Photodiode and infrared detector preamplifier
- Transducer amplifiers
- Medical instrumentation
- D/A converter
- Charge amplifier for piezoelectric transducers

Connection Diagram

14-Pin DIP/SO



TL/H/11467–1

Top View

Ordering Information

Package	Temperature Range		NSC Drawing
	Military −55°C to +125°C	Industrial −40°C to +85°C	
14-Pin Molded DIP	LMC6084AMN	LMC6084AIN LMC6084IN	N14A
14-Pin Small Outline		LMC6084AIM LMC6084IM	M14A

For MIL-STD-883C qualified products, please contact your local National Semiconductor Sales Office or Distributor for availability and specification information.

National Semiconductor

PRELIMINARY

LMC6482
CMOS Dual Rail-to-Rail Input and Output Operational Amplifier

General Description

The LMC6482 low power amplifier offers the advantage of both rail-to-rail input common-mode voltage range and rail-to-rail output swing. This performance is important when designing systems with a single-supply voltage range from 3V to 15V. Special design techniques provide an excellent common-mode rejection ratio of 85 dB. CMRR is an often overlooked parameter for amplifiers in this class. For an example of where this performance is critical, consider single-supply data acquisition systems. The LMC6482 will maintain the linearity performance of single-supply data acquisition systems because of its high CMRR that extends across the full input common-mode range.

Applications of the LMC6482 include signal conditioning circuits, peak detectors, low-droop sample and holds, pH detectors, wide dynamic-range current sources and low supply voltage transducer applications.

See the LMC6484 data sheet for a Quad CMOS operational amplifier with these same features.

Features (Typical unless otherwise noted)

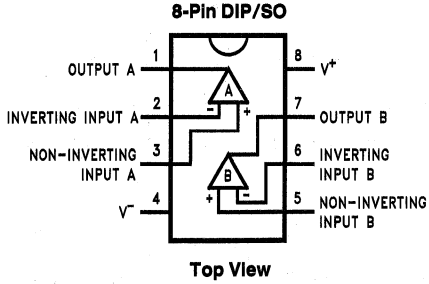
- Rail-to-Rail input common-mode voltage range
- Rail-to-Rail output swing
- Operates from 3V to 15V Supply
- Large capacitive load capability up to 500 pF
- Excellent Rail-to-Rail CMRR 85 dB
- Low input offset voltage 0.5 mV
- Low offset voltage drift 1.5 μV/°C
- Ultra low input current 20 fA
- High voltage gain (R_L = 100 kΩ) 120 dB
- Low current consumption 500 μA/Amplifier
- Specified for loads to 600Ω

Applications

- Transducer amplifier
- Portable analytic equipment (medical)
- Signal conditioning circuits

Connection Diagram

8-Pin DIP/SO



TL/H/11474–1

Top View

Ordering Information

Package	Temperature Range		
	Military −55°C to +125°C	Industrial −40°C to +85°C	NSC Drawing
8-Pin Molded DIP	LMC6482MN	LMC6482AIN LMC6482IN	N08E
8-Pin Small Outline		LMC6482AIM LMC6482IM	M08A

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office or Distributors for availability and specifications.

National Semiconductor

PRELIMINARY

LMC6484
CMOS Quad Rail-to-Rail Input and Output Operational Amplifier

General Description

The LMC6484 low power amplifier offers the advantage of both rail-to-rail input common-mode voltage range and rail-to-rail output swing. This performance is important when designing systems with a single-supply voltage range from 3V to 15V. Special design techniques provide an excellent common-mode rejection ratio of 85 dB. CMRR is an often overlooked parameter for amplifiers in this class. For an example of where this performance is critical, consider single-supply data acquisition systems. The LMC6484 will maintain the linearity performance of single-supply data acquisition systems because of its high CMRR that extends across the full input common-mode range.

Applications of the LMC6484 include signal conditioning circuits, peak detectors, low-droop sample and holds, pH detectors, wide dynamic-range current sources and low supply voltage transducer applications.

See the LMC6482 data sheet for a Dual CMOS operational amplifier with these same features.

Features (Typical unless otherwise noted)

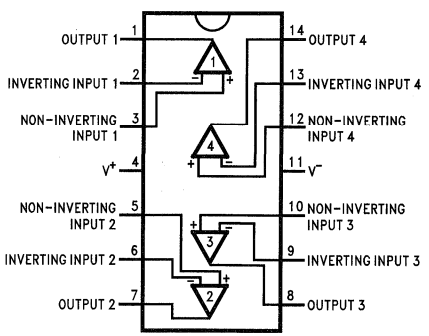
- Rail-to-Rail input common-mode voltage range
- Rail-to-Rail output swing
- Operates from 3V to 15V Supply
- Excellent Rail-to-Rail CMRR — 85 dB
- Low input offset voltage — 0.5 mV
- Low offset voltage drift — 1.5 μV/°C
- Ultra low input current — 20 fA
- High voltage gain (R_L = 100 kΩ) — 120 dB
- Low current consumption — 500 μA/Amplifier
- Specified for loads to 600Ω

Applications

- Transducer amplifier
- Portable analytic equipment (medical)
- Signal conditioning circuits

Connection Diagram

14-Pin DIP/SO



TL/H/11395–1

Ordering Information

Package	Temperature Range		
	Military −55°C to +125°C	Industrial −40°C to +85°C	NSC Drawing
14-Pin Molded DIP	LMC6484MN	LMC6484AIN LMC6484IN	N14A
14-Pin Small Outline		LMC6484AIM LMC6484IM	M14A

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office or Distributors for availability and specifications.

National Semiconductor

LP124/LP2902/LP324 Micropower Quad Operational Amplifier

General Description

The LP124 series consists of four independent, high gain internally compensated micropower operational amplifiers. These amplifiers are specially suited for operation in battery systems while maintaining good input specifications, and extremely low supply current drain. In addition, the LP124 has an input common mode range, and output source range which includes ground, making it ideal in single supply applications.

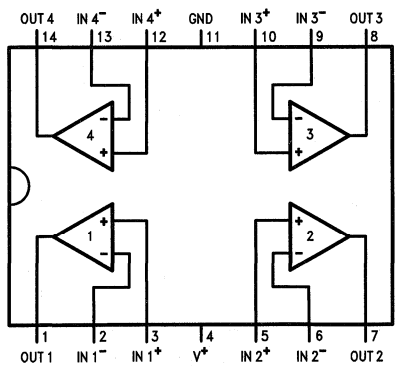
These amplifiers are ideal in applications which include portable instrumentation, battery backup equipment, and other circuits which require good DC performance and low supply current.

Features

- Low supply current — 125 μA (max)
- Low offset voltage — 2 mV (max)
- Low input bias current — 4 nA (max)
- Input common mode to GND
- Interfaces to CMOS logic
- Wide supply range — 3V < V+ < 32V
- Small Outline Package available
- Pin-for-pin compatible with LM124

Connection Diagram

Dual-in-Line (J, N) and SO (M)



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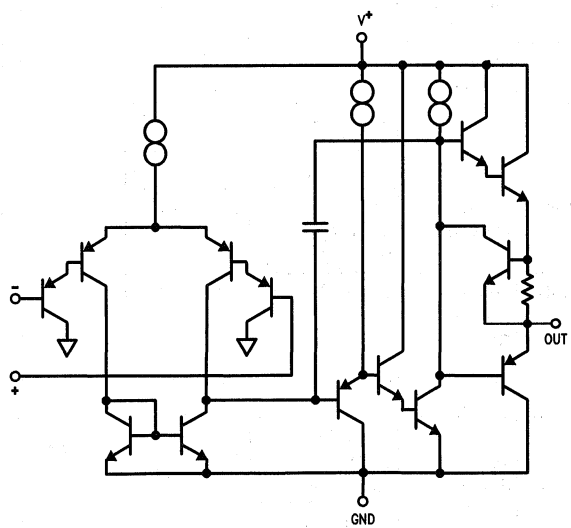
Order Number LP124J or LP324J
See NS Package Number J14A

Order Number LP324M or LP2902M
See NS Package Number M14A

Order Number LP324N or LP2902N
See NS Package Number N14A

Simplified Schematic



TL/H/8562–2

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	32V or ± 16V
LP2902	26V or ± 13V
Differential Input Voltage	32V
LP2902	26V
Input Voltage (Note 1)	−0.3V to 32V
LP2902	−0.3V to 26V
Output Short-Circuit to GND (One Amplifier) (Note 2) $V^+ \leq 15V$ and $T_A = 25°C$	Continuous
ESD Susceptibility (Note 9)	±500V

Operating Conditions

	Package J	Package N	Package M
Power Dissipation (Note 3)	500 mW	500 mW	500 mW
T_j Max	150°C	150°C	150°C
θ_{ja}	90°C/W	90°C/W	140°C/W
Operating Temp. Range	(Note 4)	(Note 4)	(Note 4)
Storage Temp. Range	−65°C ≤ T ≤ 150°C		
Soldering Information (10 sec.)	300°C	260°C	
Vapor Phase (60 sec.)			215°C
Infrared (15 sec.)			220°C

Electrical Characteristics (Note 5)

Symbol	Parameter	Conditions	LP124 Typ	LP124 Tested Limit (Note 6)	LP124 Design Limit (Note 7)	LP2902 (Note 8) Typ	LP2902 (Note 8) Tested Limit (Note 6)	LP2902 (Note 8) Design Limit (Note 7)	LP324 Typ	LP324 Tested Limit (Note 6)	LP324 Design Limit (Note 7)	Units Limits
V_{os}	Input Offset Voltage		1	2 **4**	**7**	2	4	**10**	2	4	**9**	mV (Max)
I_b	Input Bias Current		1	4 **8**	**8**	2	20	**40**	2	10	**20**	nA (Max)
I_{os}	Input Offset Current		0.1	1 **2**	**2**	0.5	4	**8**	0.2	2	**4**	nA (Max)
A_{vol}	Voltage Gain	R_L = 10k to GND V^+ = 30V	100	70 **60**	**60**	70	40	**30**	100	50	**40**	V/mV (Min)
CMRR	Common Mode Rej. Ratio	V^+ = 30V $0V \leq V_{cm}$ $V_{cm} < V^+ - 1.5$	100	85 **80**	**75**	90	80	**75**	90	80	**75**	dB (Min)
PSRR	Power Supply Rej. Ratio	V^+ = 5V to 30V	100	85 **80**	**75**	90	80	**75**	90	80	**75**	dB (Min)
I_s	Supply Current	$R_L = \infty$	85	125 **150**	**200**	85	150	**250**	85	150	**250**	μA (Max)
V_o	Output Voltage Swing	I_L = 350 μA to GND. V_{cm} = 0V	3.6	3.4 3.1	**$V^+ - 1.9V$**	3.6	3.4	**$V^+ - 1.9V$**	3.6	3.4	**$V^+ - 1.9V$**	V (Min)
		I_L = 350 μA to V^+ V_{cm} = 0V	0.7	0.8 **1.0**	**1.0**	0.7	0.8	**1.0**	0.7	0.8	**1.0**	V (Max)
I_{out} Source	Output Source Current	V_o = 3V V_{in} (diff) = 1V	11	9 **4**	**4**	10	7	**4**	10	7	**4**	mA (Min)
I_{out} Sink	Output Sink Current	V_o = 1.5V V_{in} (diff) = 1V	6	5 **4**	**4**	5	4	**3**	5	4	**3**	mA (Min)
I_{out} Sink	Output Sink Current	V_o = 1.5V V_{cm} = 0V	5	3 **0.5**	**1.5**	4	2	**1**	4	2	**1**	mA (Min)
I_{source}	Output Short to GND	V_{in} (diff) = 1V	20	25 **35**	**35**	20	25 **35**	**35**	20	25 **35**	**35**	mA (Max)

Electrical Characteristics (Note 5) (Continued)

Symbol	Parameter	Conditions	LP124			LP2902 (Note 8)			LP324			Units Limits
			Typ	Tested Limit (Note 6)	Design Limit (Note 7)	Typ	Tested Limit (Note 6)	Design Limit (Note 7)	Typ	Tested Limit (Note 6)	Design Limit (Note 7)	
I_{sink}	Output Short to V^+	V_{in} (diff) = 1V	15	30 **40**	**45**	15	30	**45**	15	30	**45**	mA (Max)
V_{os} Drift			7			10			10			μV/C°
I_{os} Drift			5			10			10			pA/C°
GBW	Gain Bandwidth Product		100			100			100			KHz
S_r	Slew Rate		50			50			50			V/mS

Note 1: The input voltage is not allowed to go more than −0.3V below V^- (GND) as this will turn on a parasitic transistor causing large currents to flow through the device.

Note 2: Short circuits from the output to GND can cause excessive heating and eventual destruction. The maximum sourcing output current is approximately 30 mA independent of the magnitude of V^+. At values of supply voltage in excess of 15 V_{DC}, continuous short-circuit to GND can exceed the power dissipation ratings (particularly at elevated temperatures) and cause eventual destruction. Destructive dissipation can result from simultaneous shorts on all amplifiers.

Note 3: For operation at elevated temperatures, these devices must be derated based on a thermal resistance of θ_{ja} and T_j max. $T_j = T_A + \theta_{ja}P_D$.

Note 4: The LP124 may be operated from $-55°C \le T_A \le +125°C$. The LP2902 may be operated from $-40°C \le T_A \le +85°C$, and the LP324 may be operated from $0°C \le T_A \le +70°C$.

Note 5: Boldface numbers apply at temperature extremes. All other numbers apply only at $T_A = T_j = 25°C$, $V^+ = 5V$, $V_{cm} = V/2$, and $R_L = 100k$ connected to GND unless otherwise specified.

Note 6: Guaranteed and 100% production tested.

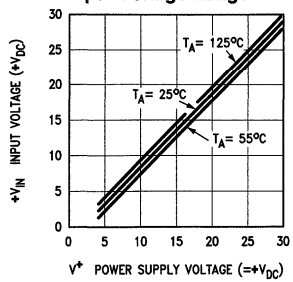
Note 7: Guaranteed (but not 100% production tested) over the operating supply voltage range (3.0V to 32V for the LP124, LP324, and 3.0V to 26V for the LP2902), and the common mode range (0V to $V^+ - 1.5V$), unless otherwise specified. These limits are not used to calculate outgoing quality levels.

Note 8: The LP2902 operating supply range is 3V to 26V, and is not tested above 26V.

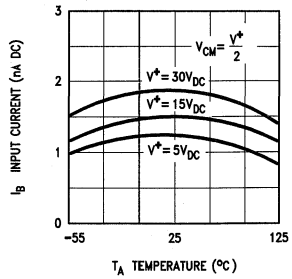
Note 9: The test circuit used consists of the human body model of 100 pF in series with 1500Ω.

Typical Performance Curves

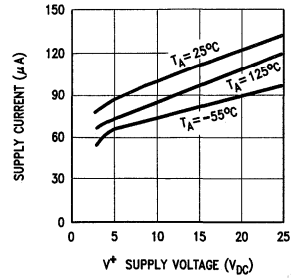
Input Voltage Range



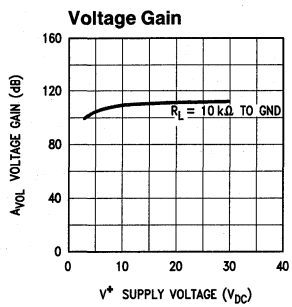
Input Current



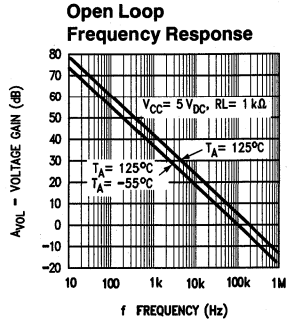
Supply Current



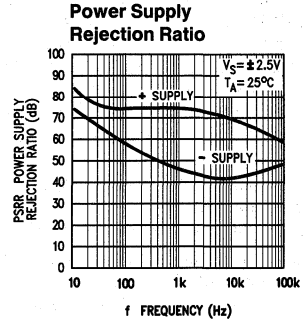
Voltage Gain



Open Loop Frequency Response



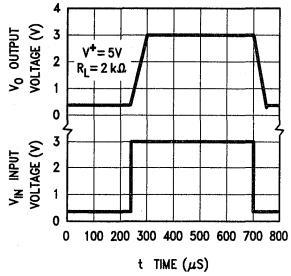
Power Supply Rejection Ratio



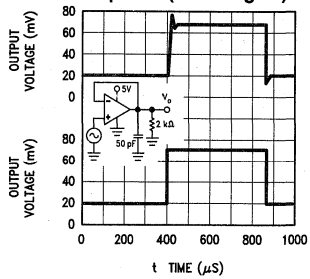
TL/H/8562–18

Typical Performance Curves (Continued)

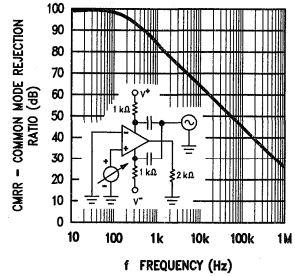
Voltage Follower Pulse Response



Voltage Follower Pulse Response (Small Signal)

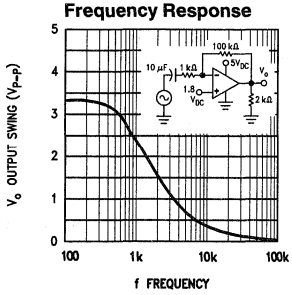


Common Mode Rejection Ratio

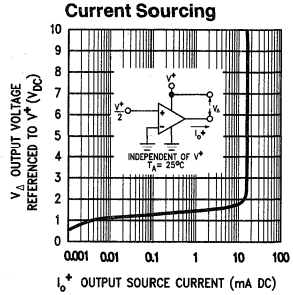


TL/H/8562–20

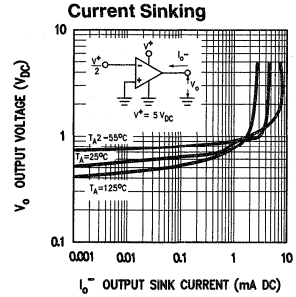
Large Signal Frequency Response



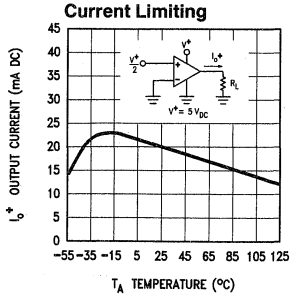
Output Characteristics Current Sourcing



Output Characteristics Current Sinking



Current Limiting



TL/H/8562–19

Application Hints

The LP124 series is a micro-power pin-for-pin equivalent to the LM124 op amps. Power supply current, input bias current, and input offset current have all been reduced by a factor of 10 over the LM124. Like its predecessor, the LP124 series op amps can operate on single supply, have true-differential inputs, and remain in the linear mode with an input common-mode voltage of 0 V_{DC}.

The pinouts of the package have been designed to simplify PC board layouts. Inverting inputs are adjacent to outputs for all of the amplifiers and the outputs have also been placed at the corners of the package (pins 1, 7, 8, and 14).

Precautions should be taken to insure that the power supply for the integrated circuit never becomes reversed in polarity or the unit is not inadvertently installed backwards in the test socket as an unlimited current surge through the resulting forward diode within the IC could destroy the unit.

Large differential input voltages can be easily accommodated and, as input differential voltage protection diodes are not needed, no large input currents result from large differential input voltages. The differential input voltage may be larger than V^+ without damaging the device. Protection should be provided to prevent the input voltages from going negative more than -0.3 V_{DC} (at 25°C). An input clamp diode with a resistor to the IC input terminal can be used.

The amplifiers have a class B output stage which allows the amplifiers to both source and sink output currents. In applications where crossover distortion is undesirable, a resistor

Application Hints (Continued)

should be used from the output of the amplifier to ground. The resistor biases the output into class A operation.

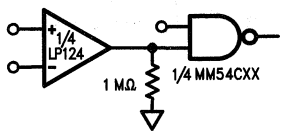
The LP124 has improved stability margin for driving capacitive loads. No special precautions are needed to drive loads in the 50 pF to 1000 pF range. It should be noted however that since the power supply current has been reduced by a factor of 10, so also has the slew rate and gain bandwidth product. This reduction can cause reduced performance in AC applications where the LM124 is being replaced by an LP124. Such situations usually occur when the LM124 has been operated near its power bandwidth.

Output short circuits either to ground or to the positive power supply should be of short time duration. Units can be destroyed, not as a result of the short circuit current causing metal fusing, but rather due to the large increase in IC chip dissipation which will cause eventual failure due to excessive junction temperatures. For example: If all four amplifiers were simultaneously shorted to ground on a 10V supply the junction temperature would rise by 110°C.

Exceeding the negative common-mode limit on either input will cause a reversal of phase to the output and force the amplifier to the corresponding high or low state. Exceeding the negative common-mode limit on both inputs will force the amplifier output to a high state. Exceeding the positive common-mode limit on a single input will not change the phase of the output. However, if both inputs exceed the limit, the output of the amplifier will be forced to a low state. In neither case does a latch occur since returning the input within the common mode range puts the input stage and thus the amplifier in a normal operating mode.

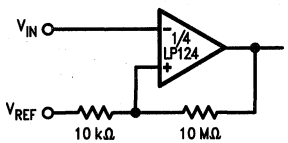
The circuits presented in the section on typical applications emphasize operation on only a single power supply voltage. If complementary power supplies are available, all of the standard op amp circuits can be used. In general, introducing a pseudo-ground (a bias voltage reference to $V^+/2$) will allow operation above and below this value in single power supply systems. Many application circuits are shown which take advantage of the wide input common-mode voltage range which includes ground. In most cases, input biasing is not required and input voltages which range to ground can easily be accommodated.

Driving CMOS



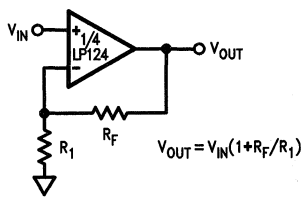
TL/H/8562–3

Comparator with Hysteresis



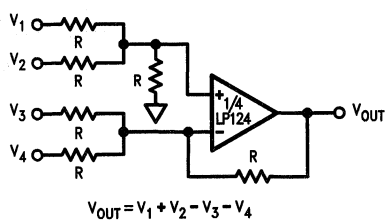
TL/H/8562–6

Non-Inverting Amplifier



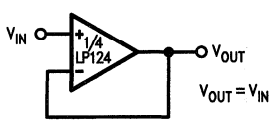
TL/H/8562–4

Adder/Subtractor



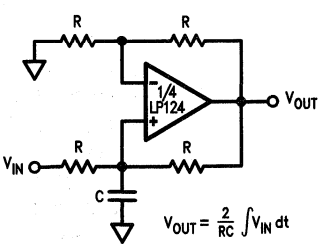
TL/H/8562–7

Unity Gain Buffer



TL/H/8562–5

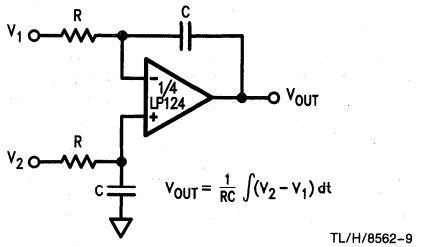
Positive Integrator



TL/H/8562–8

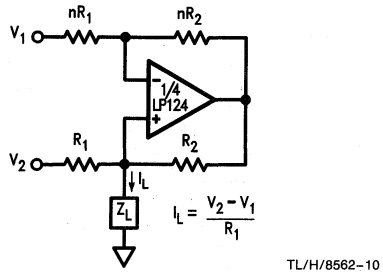
Application Hints (Continued)

Differential Integrator



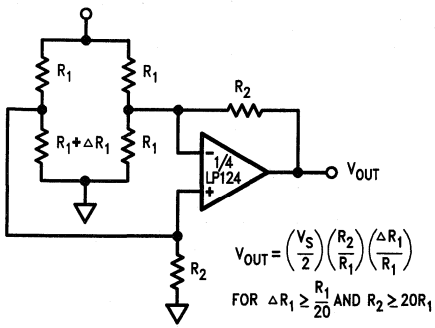
TL/H/8562–9

Howland Current Pump



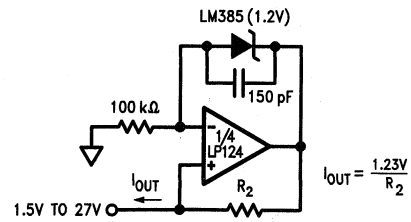
TL/H/8562–10

Bridge Current Amplifier



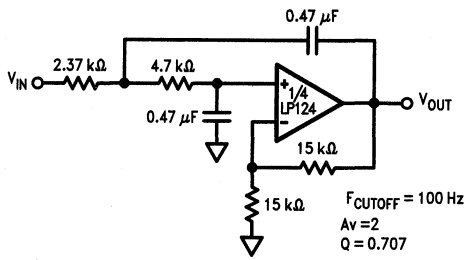
TL/H/8562–11

μ Power Current Source



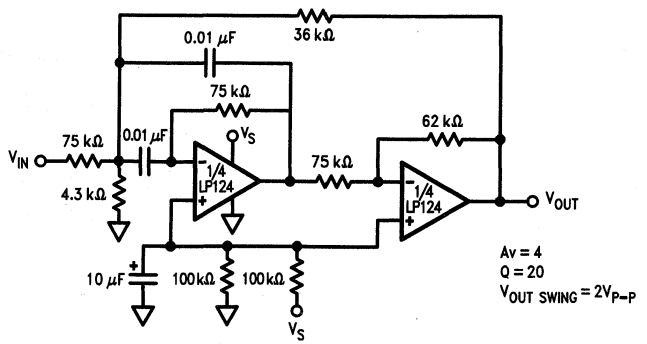
TL/H/8562–12

Lowpass Filter



TL/H/8562–13

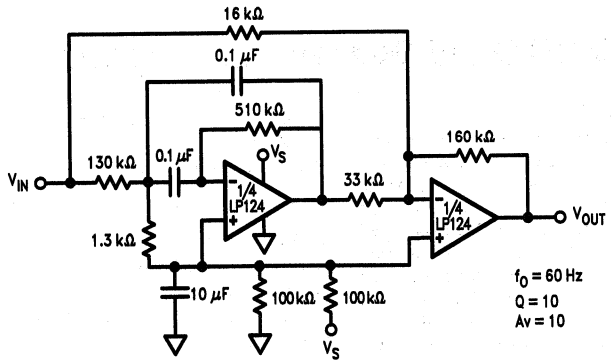
1 kHz Bandpass Active Filter



TL/H/8562–14

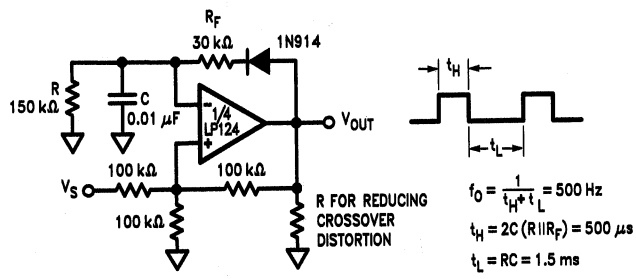
Application Hints (Continued)

Band-Reject Filter



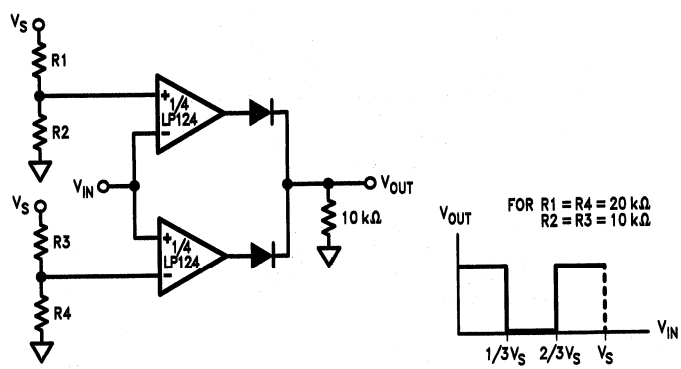
TL/H/8562–15

Pulse Generator



TL/H/8562–16

Window Comparator



TL/H/8562–17

National Semiconductor

LPC660
Low Power CMOS Quad Operational Amplifier

General Description

The LPC660 CMOS Quad operational amplifier is ideal for operation from a single supply. It features a wide range of operating voltage from +5V to +15V and features rail-to-rail output swing in addition to an input common-mode range that includes ground. Performance limitations that have plagued CMOS amplifiers in the past are not a problem with this design. Input V_{OS}, drift, and broadband noise as well as voltage gain (into 100 kΩ and 5 kΩ) are all equal to or better than widely accepted bipolar equivalents, while the power supply requirement is typically less than 1 mW.

This chip is built with National's advanced Double-Poly Silicon-Gate CMOS process.

See the LPC662 datasheet for a Dual CMOS operational amplifier and LPC661 datasheet for a single CMOS operational amplifier with these same features.

Applications

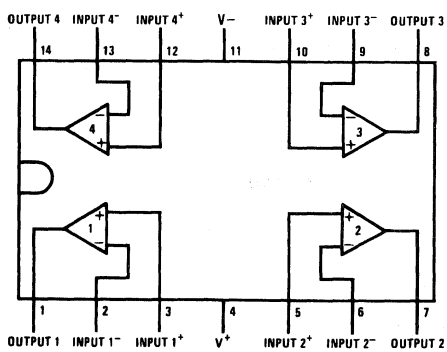
- High-impedance buffer
- Precision current-to-voltage converter
- Long-term integrator
- High-impedance preamplifier
- Active filter
- Sample-and-Hold circuit
- Peak detector

Features

- Rail-to-rail output swing
- Micropower operation (1 mW)
- Specified for 100 kΩ and 5 kΩ loads
- High voltage gain 120 dB
- Low input offset voltage 3 mV
- Low offset voltage drift 1.3 μV/°C
- Ultra low input bias current 2 fA
- Input common-mode includes V−
- Operation range from +5V to +15V
- Low distortion 0.01% at 1 kHz
- Slew rate 0.11 V/μs
- Full military temp. range available

Connection Diagram

14-Pin DIP/SO



TL/H/10547–1

Top View

Ordering Information

Package	Temperature Range		NSC Drawing
	Military	Industrial	
14-Pin Side Brazed Ceramic DIP	LPC660AMD		D14E
14-Pin Small Outline		LPC660AIM or LPC660IM	M14A
14-Pin Molded DIP		LPC660AIN or LPC660IN	N14A
14-Pin Ceramic DIP	LPC660AMJ/883		J14A

Absolute Maximum Ratings (Note 3)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Differential Input Voltage	±Supply Voltage
Supply Voltage ($V^+ - V^-$)	16V
Output Short Circuit to V^+	(Note 11)
Output Short Circuit to V^-	(Note 1)
Lead Temperature (Soldering, 10 sec.)	260°C
Storage Temp. Range	−65°C to +150°C
Junction Temperature (Note 2)	150°C
ESD Rating (C = 100 pF, R = 1.5 kΩ)	500V
Power Dissipation	(Note 2)
Current at Input Pin	±5 mA
Current at Output Pin	±18 mA
Voltage at Input/Output Pin	$(V^+) + 0.3V, (V^-) - 0.3V$
Current at Power Supply Pin	35 mA

Operating Ratings (Note 3)

Temperature Range	
LPC660AM	$-55°C \le T_J \le +125°C$
LPC660AI	$-40°C \le T_J \le +85°C$
LPC660I	$-40°C \le T_J \le +85°C$
Supply Range	4.75V to 15.5V
Power Dissipation	(Note 9)
Thermal Resistance (θ_{JA}), (Note 10)	
14-Pin Ceramic DIP	90°C/W
14-Pin Molded DIP	85°C/W
14-Pin SO	115°C/W
14-Pin Side Brazed Ceramic DIP	90°C/W

DC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for $T_J = 25°C$. **Boldface** limits apply at the temperature extremes. $V^+ = 5V$, $V^- = 0V$, $V_{CM} = 1.5V$, $V_O = 2.5V$, and $R_L > 1M$ unless otherwise specified.

Parameter	Conditions	Typ	LPC660AM LPC660AMJ/883	LPC660AI	LPC660I	Units
			Limit (Notes 4, 8)	Limit (Note 4)	Limit (Note 4)	
Input Offset Voltage		1	3	3	6	mV
			3.5	**3.3**	**6.3**	max
Input Offset Voltage Average Drift		1.3				µV/°C
Input Bias Current		0.002	20			pA
			100	**4**	**4**	max
Input Offset Current		0.001	20			pA
			100	**2**	**2**	max
Input Resistance		>1				Tera Ω
Common Mode Rejection Ratio	$0V \le V_{CM} \le 12.0V$ $V^+ = 15V$	83	70	70	63	dB
			68	**68**	**61**	min
Positive Power Supply Rejection Ratio	$5V \le V^+ \le 15V$	83	70	70	63	dB
			68	**68**	**61**	min
Negative Power Supply Rejection Ratio	$0V \le V^- \le -10V$	94	84	84	74	dB
			82	**83**	**73**	min
Input Common Mode Voltage Range	$V^+ = 5V$ & 15V For CMRR > 50 dB	−0.4	−0.1	−0.1	−0.1	V
			0	**0**	**0**	max
		$V^+ - 1.9$	$V^+ - 2.3$	$V^+ - 2.3$	$V^+ - 2.3$	V
			$\mathbf{V^+ - 2.6}$	$\mathbf{V^+ - 2.5}$	$\mathbf{V^+ - 2.5}$	min

DC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for T_J = 25°C. **Boldface** limits apply at the temperature extremes. V^+ = 5V, V^- = 0V, V_{CM} = 1.5V, V_O = 2.5V, and R_L > 1M unless otherwise specified. (Continued)

Parameter	Conditions	Typ	LPC660AM LPC660AMJ/883	LPC660AI	LPC660I	Units
			Limit (Notes 4, 8)	Limit (Note 4)	Limit (Note 4)	
Large Signal Voltage Gain	R_L = 100 kΩ (Note 5) Sourcing	1000	400	400	300	V/mV min
			250	**300**	**200**	
	Sinking	500	180	180	90	V/mV min
			70	**120**	**70**	
	R_L = 5 kΩ (Note 5) Sourcing	1000	200	200	100	V/mV min
			150	**160**	**80**	
	Sinking	250	100	100	50	V/mV min
			35	**60**	**40**	
Output Swing	V^+ = 5V R_L = 100 kΩ to $V^+/2$	4.987	4.970	4.970	4.940	V min
			4.950	**4.950**	**4.910**	
		0.004	0.030	0.030	0.060	V max
			0.050	**0.050**	**0.090**	
	V^+ = 5V R_L = 5 kΩ to $V^+/2$	4.940	4.850	4.850	4.750	V min
			4.750	**4.750**	**4.650**	
		0.040	0.150	0.150	0.250	V max
			0.250	**0.250**	**0.350**	
	V^+ = 15V R_L = 100 kΩ to $V^+/2$	14.970	14.920	14.920	14.880	V min
			14.880	**14.880**	**14.820**	
		0.007	0.030	0.030	0.060	V max
			0.050	**0.050**	**0.090**	
	V^+ = 15V R_L = 5 kΩ to $V^+/2$	14.840	14.680	14.680	14.580	V min
			14.600	**14.600**	**14.480**	
		0.110	0.220	0.220	0.320	V max
			0.300	**0.300**	**0.400**	
Output Current V^+ = 5V	Sourcing, V_O = 0V	22	16	16	13	mA min
			12	**14**	**11**	
	Sinking, V_O = 5V	21	16	16	13	mA min
			12	**14**	**11**	
Output Current V^+ = 15V	Sourcing, V_O = 0V	40	19	28	23	mA min
			19	**25**	**20**	
	Sinking, V_O = 13V (Note 11)	39	19	28	23	mA min
			19	**24**	**19**	
Supply Current	All Four Amplifiers V_O = 1.5V	160	200	200	240	μA max
			250	**230**	**270**	

AC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for T_J = 25°C. **Boldface** limits apply at the temperature extremes. V^+ = 5V, V^- = 0V, V_{CM} = 1.5V, V_O = 2.5, and R_L > 1M unless otherwise specified.

Parameter	Conditions	Typ	LPC660AM LPC660AMJ/883	LPC660AI	LPC660I	Units
			Limit (Notes 4, 8)	Limit (Note 4)	Limit (Note 4)	
Slew Rate	(Note 6)	0.11	0.07	0.07	0.05	V/μs min
			0.04	**0.05**	**0.03**	
Gain-Bandwidth Product		0.35				MHz
Phase Margin		50				Deg
Gain Margin		17				dB
Amp-to-Amp Isolation	(Note 7)	130				dB
Input Referred Voltage Noise	F = 1 kHz	42				nV/√Hz
Input Referred Current Noise	F = 1 kHz	0.0002				pA/√Hz
Total Harmonic Distortion	F = 1 kHz, A_V = −10 R_L = 100 kΩ, V_O = 8 V_{PP}	0.01				%

Note 1: Applies to both single supply and split supply operation. Continuous short circuit operation at elevated ambient temperature and/or multiple Op Amp shorts can result in exceeding the maximum allowed junction temperature of 150°C. Output currents in excess of ±30 mA over long term may adversely affect reliability.

Note 2: The maximum power dissipation is a function of $T_{J(max)}$, θ_{JA} and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(max)}-T_A)\theta_{JA}$.

Note 3: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed.

Note 4: Limits are guaranteed by testing or correlation.

Note 5: V^+ = 15V, V_{CM} = 7.5V and R_L connected to 7.5V. For Sourcing tests, 7.5V ≤ V_O ≤ 11.5V. For Sinking tests, 2.5V ≤ V_O ≤ 7.5V.

Note 6: V^+ = 15V. Connected as Voltage Follower with 10V step input. Number specified is the slower of the positive and negative slew rates.

Note 7: Input referred. V^+ = 15V and R_L = 100 kΩ connected to $V^+/2$. Each amp excited in turn with 1 kHz to produce V_O = 13 V_{PP}.

Note 8: A military RETS electrical test specification is available on request. At the time of printing, the LPC660AMJ/883 RETS specification complied fully with the boldface limits in this column. The LPC660AMJ/883 may also be procured to a Standard Military Drawing specification.

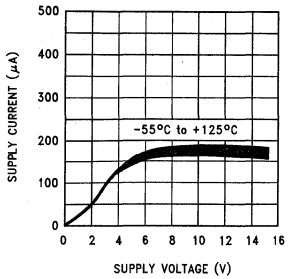
Note 9: For operating at elevated temperatures, the device must be derated based on the thermal resistance θ_{JA} with $P_D = (T_J-T_A)/\theta_{JA}$.

Note 10: All numbers apply for packages soldered directly into a PC board.

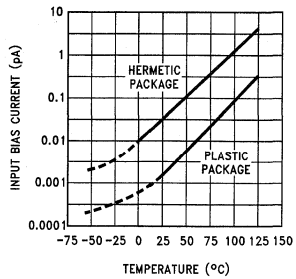
Note 11: Do not connect output to V^+ when V^+ is greater than 13V or reliability may be adversely affected.

Typical Performance Characteristics $V_S = \pm 7.5V$, $T_A = 25°C$ unless otherwise specified

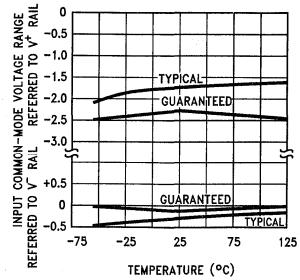
Supply Current vs Supply Voltage



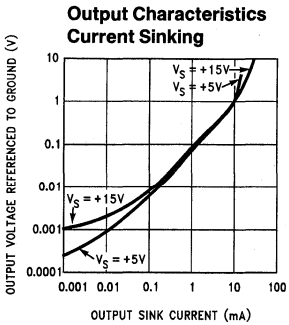
Input Bias Current vs Temperature



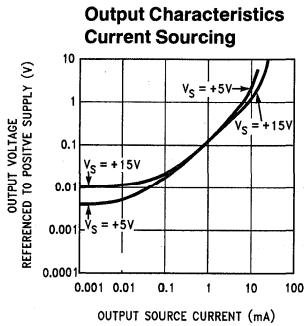
Common-Mode Voltage Range vs Temperature



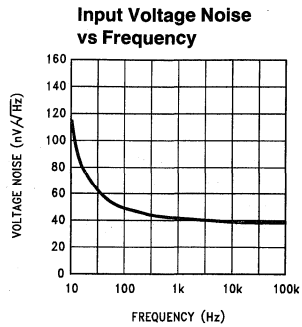
Output Characteristics Current Sinking



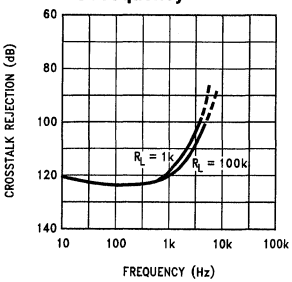
Output Characteristics Current Sourcing



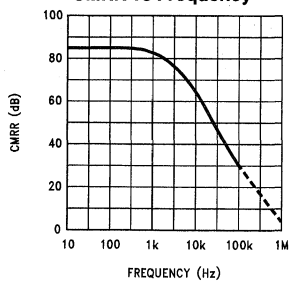
Input Voltage Noise vs Frequency



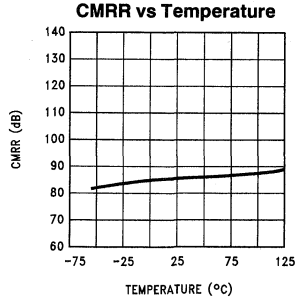
Crosstalk Rejection vs Frequency



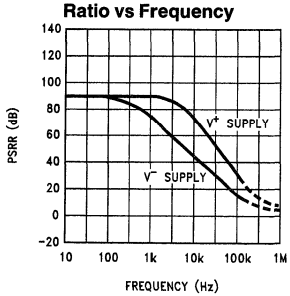
CMRR vs Frequency



CMRR vs Temperature



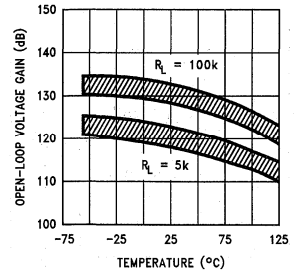
Power Supply Rejection Ratio vs Frequency



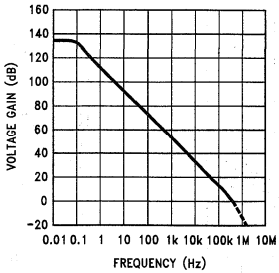
TL/H/10547–2

Typical Performance Characteristics $V_S = \pm 7.5V$, $T_A = 25°C$ unless otherwise specified (Continued)

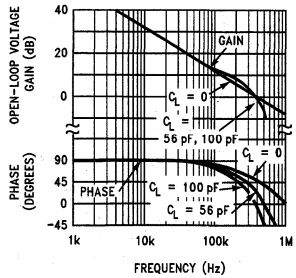
Open-Loop Voltage Gain vs Temperature



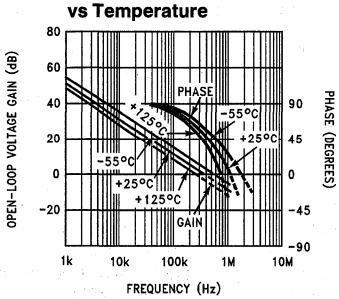
Open-Loop Frequency Response



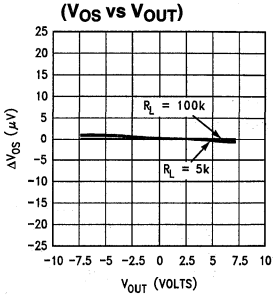
Gain and Phase Responses vs Load Capacitance



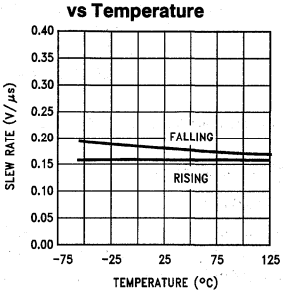
Gain and Phase Responses vs Temperature



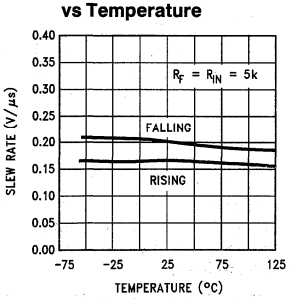
Gain Error (V_{OS} vs V_{OUT})



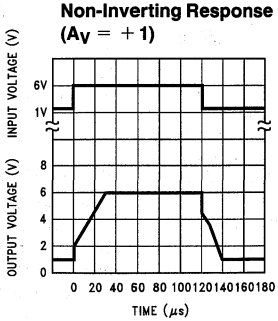
Non-Inverting Slew Rate vs Temperature



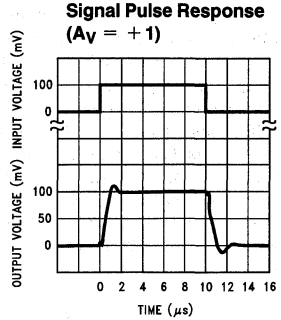
Inverting Slew Rate vs Temperature



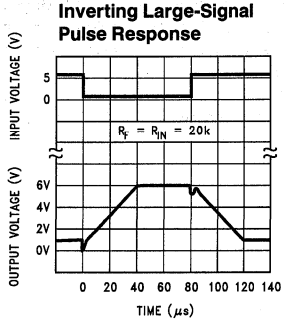
Large-Signal Pulse Non-Inverting Response ($A_V = +1$)



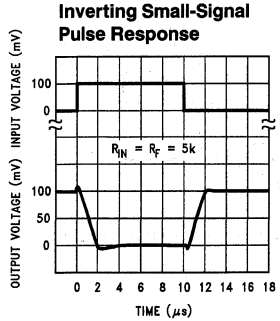
Non-Inverting Small Signal Pulse Response ($A_V = +1$)



Inverting Large-Signal Pulse Response

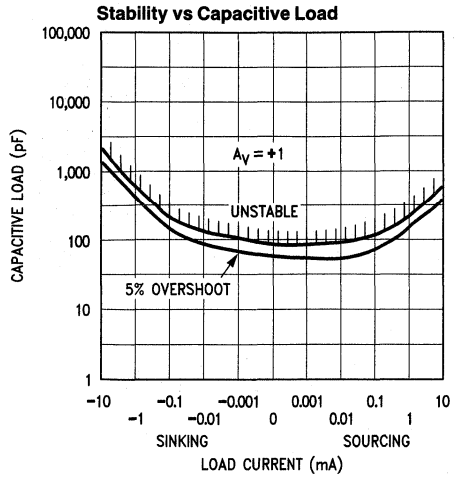


Inverting Small-Signal Pulse Response

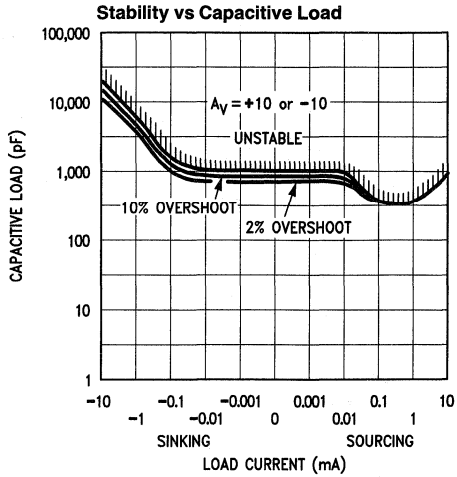


TL/H/10547–3

Typical Performance Characteristics $V_S = \pm 7.5V$, $T_A = 25°C$ (Continued)



TL/H/10547–4



TL/H/10547–5

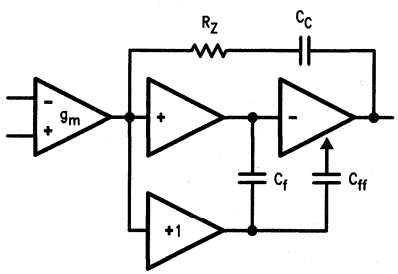
Note: Avoid resistive loads of less than 500Ω, as they may cause instability.

Application Hints

AMPLIFIER TOPOLOGY

The topology chosen for the LPC660 is unconventional (compared to general-purpose op amps) in that the traditional unity-gain buffer output stage is not used; instead, the output is taken directly from the output of the integrator, to allow rail-to-rail output swing. Since the buffer traditionally delivers the power to the load, while maintaining high op amp gain and stability, and must withstand shorts to either rail, these tasks now fall to the integrator.

As a result of these demands, the integrator is a compound affair with an embedded gain stage that is doubly fed forward (via C_f and C_{ff}) by a dedicated unity-gain compensation driver. In addition, the output portion of the integrator is a push-pull configuration for delivering heavy loads. While sinking current the whole amplifier path consists of three gain stages with one stage fed forward, whereas while sourcing the path contains four gain stages with two fed forward.



TL/H/10547–6

FIGURE 1. LPC660 Circuit Topology (Each Amplifier)

The large signal voltage gain while sourcing is comparable to traditional bipolar op amps, for load resistance of at least 5 kΩ. The gain while sinking is higher than most CMOS op amps, due to the additional gain stage; however, when driving load resistance of 5 kΩ or less, the gain will be reduced as indicated in the Electrical Characteristics. The op amp can drive load resistance as low as 500Ω without instability.

COMPENSATING INPUT CAPACITANCE

Refer to the LMC660 or LMC662 datasheets to determine whether or not a feedback capacitor will be necessary for compensation and what the value of that capacitor would be.

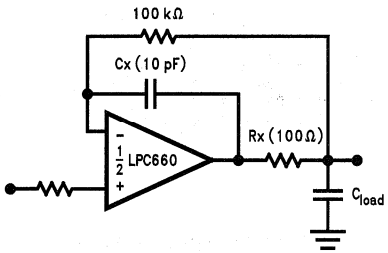
CAPACITIVE LOAD TOLERANCE

Like many other op amps, the LPC660 may oscillate when its applied load appears capacitive. The threshold of oscillation varies both with load and circuit gain. The configuration most sensitive to oscillation is a unity-gain follower. See the Typical Performance Characteristics.

The load capacitance interacts with the op amp's output resistance to create an additional pole. If this pole frequency is sufficiently low, it will degrade the op amp's phase margin so that the amplifier is no longer stable at low gains. The addition of a small resistor (50Ω to 100Ω) in series with the op amp's output, and a capacitor (5 pF to 10 pF) from inverting input to output pins, returns the phase margin to a safe value without interfering with lower-frequency circuit

Application Hints (Continued)

operation. Thus, larger values of capacitance can be tolerated without oscillation. Note that in all cases, the output will ring heavily when the load capacitance is near the threshold for oscillation.



TL/H/10547–7

FIGURE 2a. Rx, Cx Improve Capacitive Load Tolerance

Capacitive load driving capability is enhanced by using a pull up resistor to V^+ *(Figure 2b)*. Typically a pull up resistor conducting 50 μA or more will significantly improve capacitive load responses. The value of the pull up resistor must be determined based on the current sinking capability of the amplifier with respect to the desired output swing. Open loop gain of the amplifier can also be affected by the pull up resistor (see Electrical Characteristics).

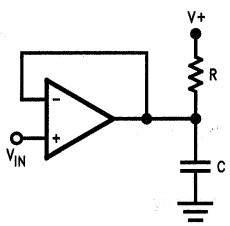


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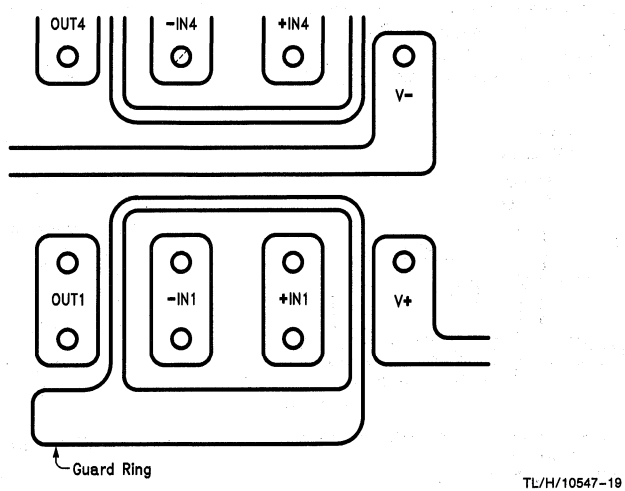
FIGURE 2b. Compensating for Large Capacitive Loads with A Pull Up Resistor

PRINTED-CIRCUIT-BOARD LAYOUT FOR HIGH-IMPEDANCE WORK

It is generally recognized that any circuit which must operate with less than 1000 pA of leakage current requires special layout of the PC board. When one wishes to take advantage of the ultra-low bias current of the LPC660, typically less than 0.04 pA, it is essential to have an excellent layout. Fortunately, the techniques for obtaining low leakages are quite simple. First, the user must not ignore the surface leakage of the PC board, even though it may sometimes appear acceptably low, because under conditions of high humidity or dust or contamination, the surface leakage will be appreciable.

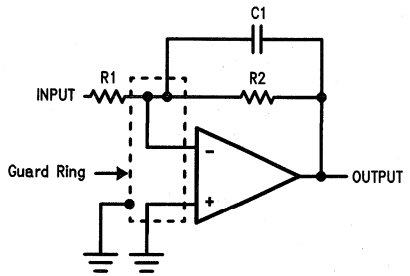
To minimize the effect of any surface leakage, lay out a ring of foil completely surrounding the LPC660's inputs and the terminals of capacitors, diodes, conductors, resistors, relay terminals, etc. connected to the op-amp's inputs. See *Figure 3*. To have a significant effect, guard rings should be placed on both the top and bottom of the PC board. This PC foil must then be connected to a voltage which is at the same voltage as the amplifier inputs, since no leakage current can flow between two points at the same potential. For example, a PC board trace-to-pad resistance of 10^{12} ohms, which is normally considered a very large resistance, could leak 5 pA if the trace were a 5V bus adjacent to the pad of an input. This would cause a 100 times degradation from the LPC660's actual performance. However, if a guard ring is held within 5 mV of the inputs, then even a resistance of 10^{11} ohms would cause only 0.05 pA of leakage current, or perhaps a minor (2:1) degradation of the amplifier's performance. See *Figures 4a, 4b, 4c* for typical connections of guard rings for standard op-amp configurations. If both inputs are active and at high impedance, the guard can be tied to ground and still provide some protection; see *Figure 4d*.



TL/H/10547–19

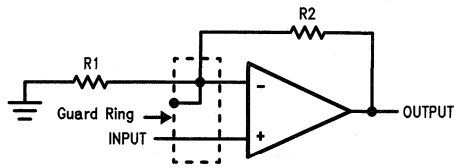
FIGURE 3. Example of Guard Ring in P.C. Board Layout using the LPC660

Application Hints (Continued)



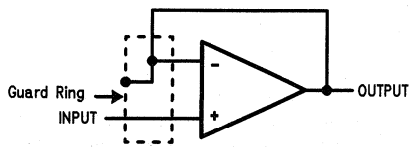
TL/H/10547–20

(a) Inverting Amplifier



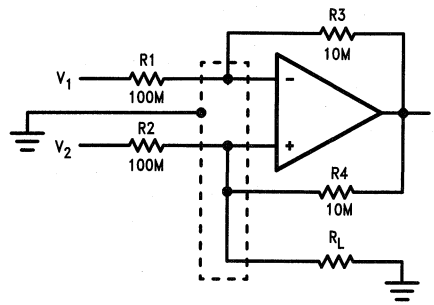
TL/H/10547–21

(b) Non-Inverting Amplifier



TL/H/10547–22

(c) Follower

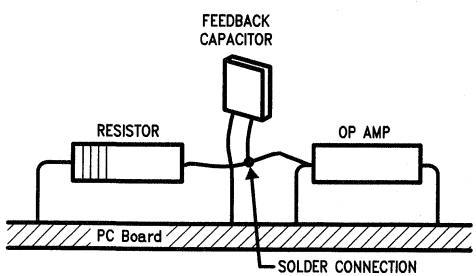


TL/H/10547–23

(d) Howland Current Pump

FIGURE 4. Guard Ring Connections

The designer should be aware that when it is inappropriate to lay out a PC board for the sake of just a few circuits, there is another technique which is even better than a guard ring on a PC board: Don't insert the amplifier's input pin into the board at all, but bend it up in the air and use only air as an insulator. Air is an excellent insulator. In this case you may have to forego some of the advantages of PC board construction, but the advantages are sometimes well worth the effort of using point-to-point up-in-the-air wiring. See *Figure 5*.



TL/H/10547–24

(Input pins are lifted out of PC board and soldered directly to components. All other pins connected to PC board.)

FIGURE 5. Air Wiring

BIAS CURRENT TESTING

The test method of *Figure 6* is appropriate for bench-testing bias current with reasonable accuracy. To understand its operation, first close switch S2 momentarily. When S2 is opened, then $I^- = \frac{dV_{OUT}}{dt} \times C2$.

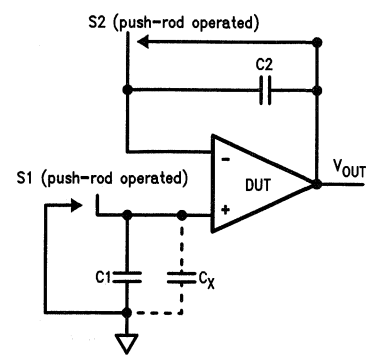


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FIGURE 6. Simple Input Bias Current Test Circuit

Application Hints (Continued)

A suitable capacitor for C2 would be a 5 pF or 10 pF silver mica, NPO ceramic, or air-dielectric. When determining the magnitude of I^-, the leakage of the capacitor and socket must be taken into account. Switch S2 should be left shorted most of the time, or else the dielectric absorption of the capacitor C2 could cause errors.

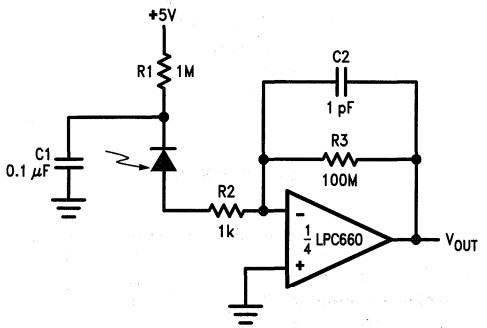
Similarly, if S1 is shorted momentarily (while leaving S2 shorted)

$$I^+ = \frac{dV_{OUT}}{dt} \times (C1 + C_x)$$

where C_x is the stray capacitance at the + input.

Typical Single-Supply Applications ($V^+ = 5.0\ V_{DC}$)

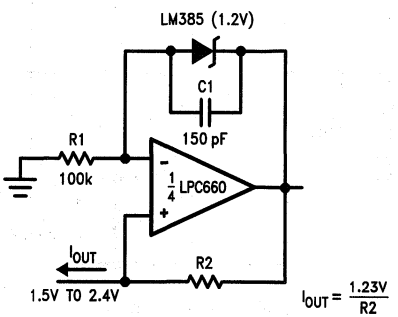
Photodiode Current-to-Voltage Converter



TL/H/10547–17

Note: A 5V bias on the photodiode can cut its capacitance by a factor of 2 or 3, leading to improved response and lower noise. However, this bias on the photodiode will cause photodiode leakage (also known as its dark current).

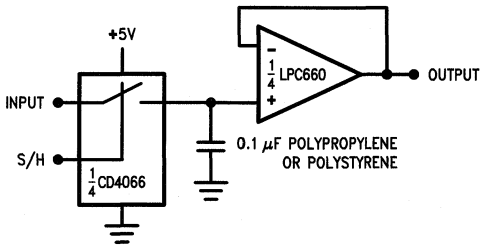
Micropower Current Source



TL/H/10547–18

(Upper limit of output range dictated by input common-mode range; lower limit dictated by minimum current requirement of LM385.)

Low-Leakage Sample-and-Hold



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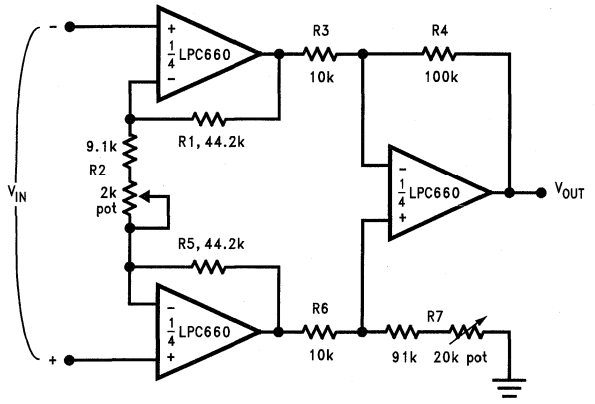
Instrumentation Amplifier



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If R1 = R5, R3 = R6, and R4 = R7;

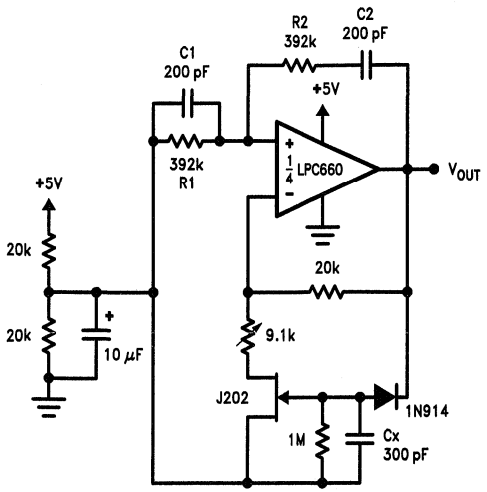
then $\frac{V_{OUT}}{V_{IN}} = \frac{R2 + 2R1}{R1} \times \frac{R4}{R3}$

$\therefore A_V \simeq 100$ for circuits shown.

For good CMRR over temperature, low drift resistors should be used. Matching of R3 to R6 and R4 to R7 affects CMRR. Gain may be adjusted through R2. CMRR may be adjusted through R7.

Typical Single-Supply Applications (V^+ = 5.0 V_{DC}) (Continued)

Sine-Wave Oscillator



TL/H/10547–10

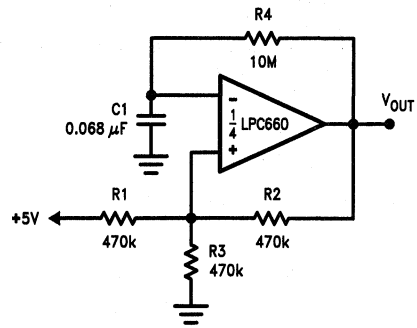
Oscillator frequency is determined by R1, R2, C1, and C2:

$$f_{OSC} = 1/2\pi RC$$

where R = R1 = R2 and C = C1 = C2.

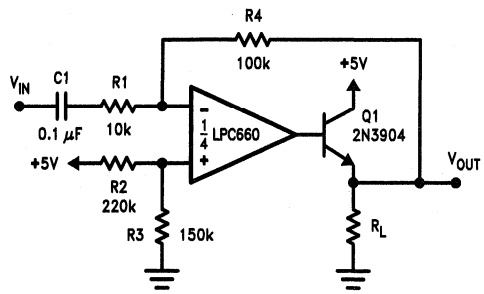
This circuit, as shown, oscillates at 2.0 kHz with a peak-to-peak output swing of 4.5V

1 Hz Square-Wave Oscillator



TL/H/10547–11

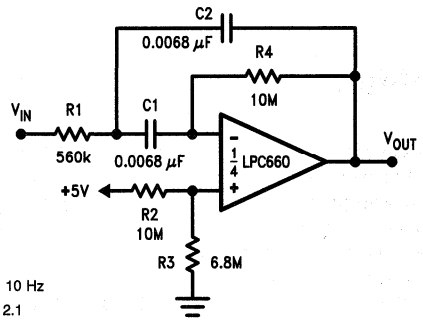
Power Amplifier



TL/H/10547–12

Typical Single-Supply Applications (V^+ = 5.0 V_{DC}) (Continued)

10 Hz Bandpass Filter



f_O = 10 Hz
Q = 2.1
Gain = −8.8

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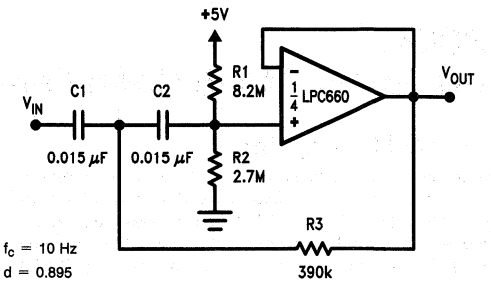
10 Hz High-Pass Filter (2 dB Dip)



f_c = 10 Hz
d = 0.895
Gain = 1

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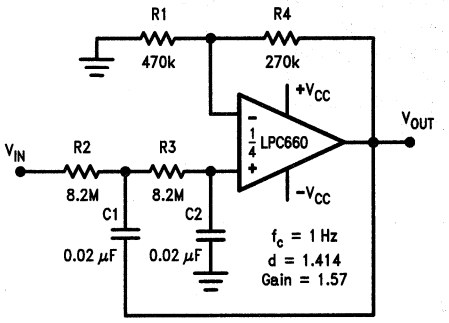
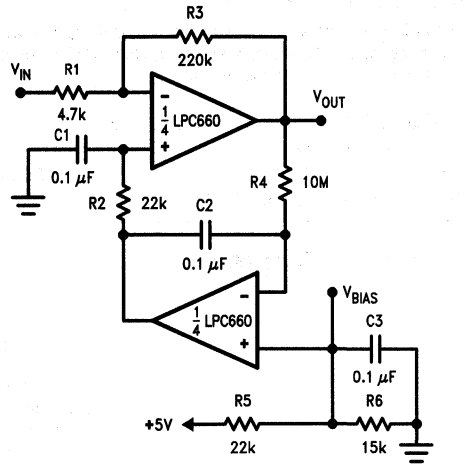
1 Hz Low-Pass Filter (Maximally Flat, Dual Supply Only)



TL/H/10547–15

High Gain Amplifier with Offset Voltage Reduction



Gain = −46.8

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Output offset voltage reduced to the level of the input offset voltage of the bottom amplifier (typically 1 mV), referred to V_{BIAS}.

National Semiconductor

LPC661
Low Power CMOS Operational Amplifier

General Description

The LPC661 CMOS operational amplifier is ideal for operation from a single supply. It features a wide range of operating supply voltage from +5V to +15V, rail-to-rail output swing and an input common-mode range that includes ground. Performance limitations that have plagued CMOS amplifiers in the past are not a problem with this design. Input V_{OS}, drift, and broadband noise as well as voltage gain (into 100 kΩ and 5 kΩ) are all equal to or better than widely accepted bipolar equivalents, while the supply current requirement is typically 55 μA.

This chip is built with National's advanced Double-Poly Silicon-Gate CMOS process.

See the LPC660 datasheet for a Quad CMOS operational amplifier or the LPC662 data sheet for a Dual CMOS operational amplifier with these same features.

Features (Typical unless otherwise noted)

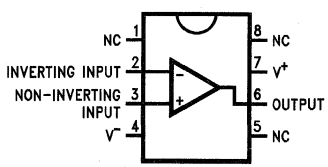
- Rail-to-rail output swing
- Low supply current 55 μA
- Specified for 100 kΩ and 5 kΩ loads
- High voltage gain 120 dB
- Low input offset voltage 3 mV
- Low offset voltage drift 1.3 μV/°C
- Ultra low input bias current 2 fA
- Input common-mode range includes GND
- Operating range from +5V to +15V
- Low distortion 0.01% at 1 kHz
- Slew rate 0.11 V/μs

Applications

- High-impedance buffer
- Precision current-to-voltage converter
- Long-term integrator
- High-impedance preamplifier
- Active filter
- Sample-and-Hold circuit
- Peak detector

Connection Diagram

8-Pin DIP/SO



TL/H/11227–1

Ordering Information

Package	Temperature Range		NSC Drawing
	Military −55°C to +125°C	Industrial −40°C to +85°C	
8-Pin Small Outline		LPC661AIM LPC661IM	M08A
8-Pin Molded DIP	LPC661AMN	LPC661AIN LPC661IN	N08E

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage ($V^+ - V^-$)	16V
Differential Input Voltage	±Supply Voltage
Output Short Circuit to V^+	(Note 9)
Output Short Circuit to V^-	(Note 2)
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec.)	260°C
Junction Temperature (Note 3)	150°C
Power Dissipation	(Note 3)
ESD Rating (C = 100 pF, R = 1.5 kΩ)	500V
Current at Input Pin	±5 mA
Current at Output Pin	±18 mA
Voltage Input/Output Pin	(V^+) +0.3V, (V^-) −0.3V
Current at Power Supply Pin	35 mA

Operating Ratings (Note 1)

Supply Voltage	$4.75V \le V^+ \le 15.5V$
Junction Temperature Range	
LPC661AM	$-55°C \le T_J \le +125°C$
LPC661AI	$-40°C \le T_J \le +85°C$
LPC661I	$-40°C \le T_J \le +85°C$
Power Dissipation	(Note 7)
Thermal Resistance (θ_{JA}) (Note 8)	
8-Pin DIP	101°C/W
8-Pin SO	165°C/W

DC Electrical Characteristics

The following specifications apply for $V^+ = 5V$, $V^- = 0V$, $V_{CM} = 1.5V$, $V_O = 2.5V$, and $R_L = 1M$ unless otherwise noted. **Boldface** limits apply at the temperature extremes; all other limits $T_J = 25°C$.

Symbol	Parameter	Conditions	Typ	LPC661AM Limit (Note 4)	LPC661AI Limit (Note 4)	LPC661I Limit (Note 4)	Units (Limit)
V_{OS}	Input Offset Voltage		1	3 **3.5**	3 **3.3**	6 **6.3**	mV
TCV_{OS}	Input Offset Voltage Average Drift		1.3				µV/°C
I_B	Input Bias Current		0.002	20 **100**	 **4**	 **4**	pA max
I_{OS}	Input Offset Current		0.001	20 **100**	 **2**	 **2**	pA max
R_{IN}	Input Resistance		>1				Tera Ω
CMRR	Common Mode Rejection Ratio	$0V \le V_{CM} \le 12.0V$ $V^+ = 15V$	83	70 **68**	70 **68**	63 **61**	dB min
+PSRR	Positive Power Supply Rejection Ratio	$5V \le V^+ \le 15V$	83	70 **68**	70 **68**	63 **61**	dB min
−PSRR	Negative Power Supply Rejection Ratio	$0V \le V^- \le -10V$	94	84 **82**	84 **83**	74 **73**	dB min
V_{CM}	Input Common Mode Voltage Range	$V^+ = 5V$ and 15V for CMRR ≥ 50 dB	−0.4	−0.1 **0**	−0.1 **0**	−0.1 **0**	V max
			$V^+ - 1.9$	$V^+ - 2.3$ $V^+ - 2.6$	$V^+ - 2.3$ $V^+ - 2.5$	$V^+ - 2.3$ $V^+ - 2.5$	V min
A_V	Large Signal Voltage Gain	Sourcing $R_L = 100 k\Omega$ (Note 5)	1000	400 **250**	400 **300**	300 **200**	V/mV min
		Sinking $R_L = 100 k\Omega$ (Note 5)	500	180 **70**	180 **120**	90 **70**	V/mV min
		Sourcing $R_L = 5 k\Omega$ (Note 5)	1000	200 **150**	200 **160**	100 **80**	V/mV min
		Sinking $R_L = 5 k\Omega$ (Note 5)	250	100 **35**	100 **60**	50 **40**	V/mV min

DC Electrical Characteristics

The following specifications apply for $V^+ = 5V$, $V^- = 0V$, $V_{CM} = 1.5V$, $V_O = 2.5V$, and $R_L = 1M$ unless otherwise noted. **Boldface** limits apply at the temperature extremes; all other limits $T_J = 25°C$. (Continued)

Symbol	Parameter	Conditions	Typ	LPC661AM Limit (Note 4)	LPC661AI Limit (Note 4)	LPC661I Limit (Note 4)	Units (Limit)
V_O	Output Swing	$V^+ = 5V$ $R_L = 100\ k\Omega$ to 2.5V	4.987	4.970 **4.950**	4.970 **4.950**	4.940 **4.910**	V min
			0.004	0.030 **0.050**	0.030 **0.050**	0.060 **0.090**	V max
		$V^+ = 5V$ $R_L = 5\ k\Omega$ to 2.5V	4.940	4.850 **4.750**	4.850 **4.750**	4.750 **4.650**	V min
			0.040	0.150 **0.250**	0.150 **0.250**	0.250 **0.350**	V max
		$V^+ = 15V$ $R_L = 100\ k\Omega$ to 7.5V	14.970	14.920 **14.880**	14.920 **14.880**	14.880 **14.820**	V min
			0.007	0.030 **0.050**	0.030 **0.050**	0.060 **0.090**	V max
		$V^+ = 15V$ $R_L = 5\ k\Omega$ to 7.5V	14.840	14.680 **14.600**	14.680 **14.600**	14.580 **14.480**	V min
			0.110	0.220 **0.300**	0.220 **0.300**	0.320 **0.400**	V max
I_O	Output Current $V^+ = 5V$	Sourcing, $V_O = 0V$	22	16 **12**	16 **14**	13 **11**	mA min
		Sinking, $V_O = 5V$	21	16 **12**	16 **14**	13 **11**	mA min
I_O	Output Current $V^+ = 15V$	Sourcing, $V_O = 0V$	40	19 **19**	28 **25**	23 **20**	mA min
		Sinking, $V_O = 13V$ (Note 9)	39	19 **19**	28 **24**	23 **19**	mA min
I_S	Supply Current	$V^+ = 5V$, $V_O = 1.5V$	55	60 **70**	60 **70**	70 **85**	μA max
		$V^+ = 15V$, $V_O = 1.5V$	58	75 **85**	75 **85**	90 **105**	μA max

AC Electrical Characteristics

The following specifications apply for $V^+ = 5V$, $V^- = 0V$, $V_{CM} = 1.5V$, $V_O = 2.5V$, and $R_L = 1M$ unless otherwise noted. **Boldface** limits apply at the temperature extremes; all other limits $T_J = 25°C$.

Symbol	Parameter	Conditions	Typ	LPC661AM Limit (Note 4)	LPC661AI Limit (Note 4)	LPC661I Limit (Note 4)	Units (Limit)
SR	Slew Rate	(Note 6)	0.11	0.07 **0.04**	0.07 **0.05**	0.05 **0.03**	V/μs min
GBW	Gain-Bandwidth Product		350				kHz
ϕm	Phase Margin		50				Deg
G_M	Gain Margin		17				dB
e_n	Input Referred Voltage Noise	F = 1 kHz	42				nV/√Hz
i_n	Input Referred Current Noise	F = 1 kHz	0.0002				pA/√Hz
T.H.D.	Total Harmonic Distortion	F = 1 kHz, $A_V = -10$ $R_L = 100\ k\Omega$, $V_O = 8\ V_{PP}$ $V^+ = 15V$	0.01				%

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed.

Note 2: Applies to both single supply and split supply operation. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C. Output currents in excess of ±30 mA over long term may adversely affect reliability.

Note 3: The maximum power dissipation is a function of $T_{J(max)}$, θ_{JA} and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(max)} - T_A)/\theta_{JA}$.

Note 4: Limits are guaranteed by testing or correlation.

Note 5: $V^+ = 15V$, $V_{CM} = 7.5V$ and R_L connected to 7.5V. For sourcing tests, $7.5V \le V_O \le 11.5V$. For sinking tests, $2.5V \le V_O \le 7.5V$.

Note 6: $V^+ = 15V$. Connected as Voltage Follower with 10V step input. Number specified is the slower of the positive and negative slew rates.

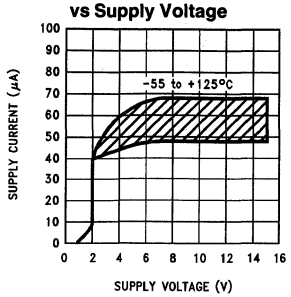
Note 7: For operating at elevated temperatures the device must be derated based on the thermal resistance θ_{JA} with $P_D = (T_J - T_A)/\theta_{JA}$.

Note 8: All numbers apply for packages soldered directly into a PC board.

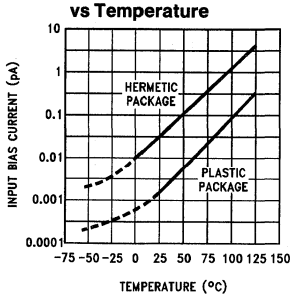
Note 9: Do not connect output to V^+ when V^+ is greater than 13V or reliability may be adversely affected.

Typical Performance Characteristics $V_S = \pm 7.5V$, $T_A = 25°C$ unless otherwise specified

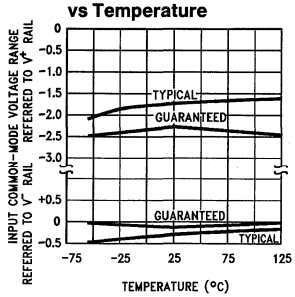
Supply Current vs Supply Voltage



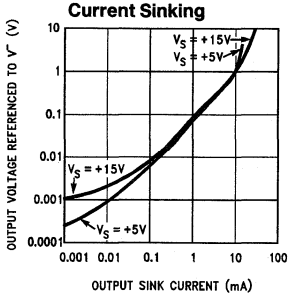
Input Bias Current vs Temperature



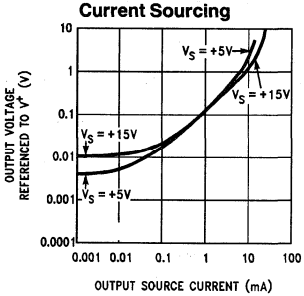
Common-Mode Voltage Range vs Temperature



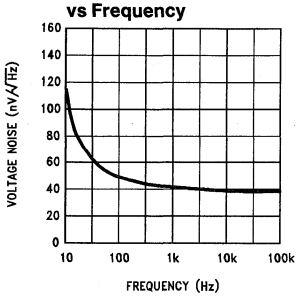
Output Characteristics Current Sinking



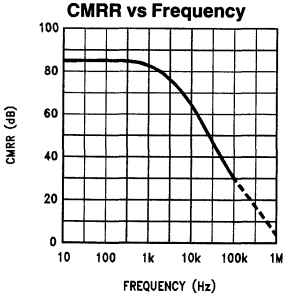
Output Characteristics Current Sourcing



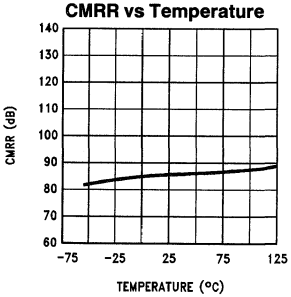
Input Voltage Noise vs Frequency



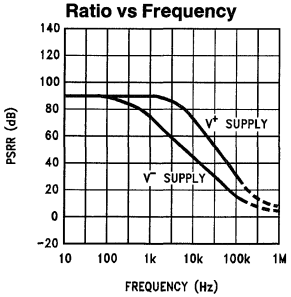
CMRR vs Frequency



CMRR vs Temperature



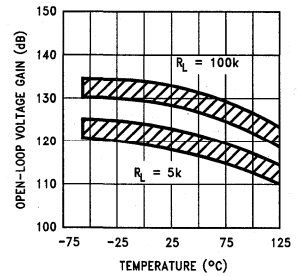
Power Supply Rejection Ratio vs Frequency



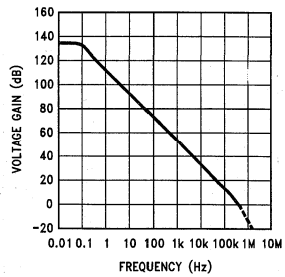
TL/H/11227–2

Typical Performance Characteristics $V_S = \pm 7.5V, T_A = 25°C$ unless otherwise specified (Continued)

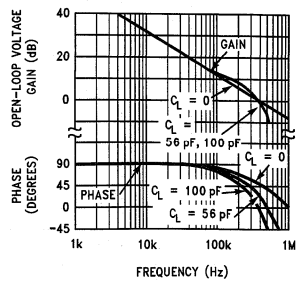
Open-Loop Voltage Gain vs Temperature



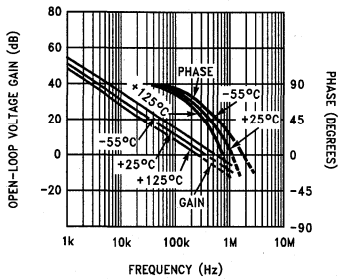
Open-Loop Frequency Response



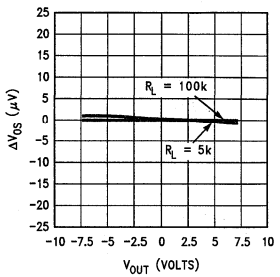
Gain and Phase Responses vs Load Capacitance



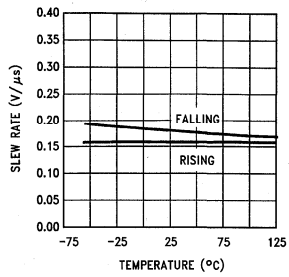
Gain and Phase Responses vs Temperature



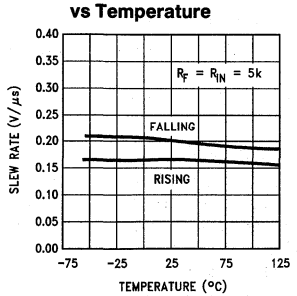
Gain Error (V_{OS} vs V_{OUT})



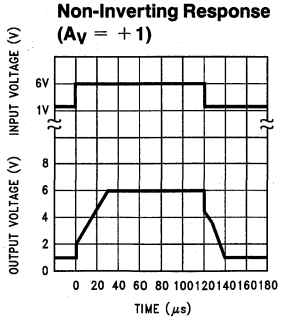
Non-Inverting Slew Rate vs Temperature



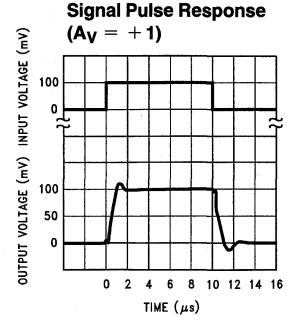
Inverting Slew Rate vs Temperature



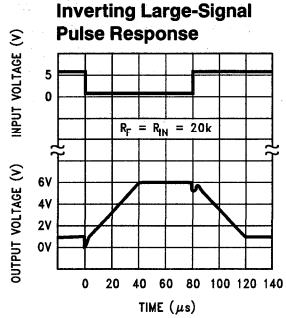
Large-Signal Pulse Non-Inverting Response ($A_V = +1$)



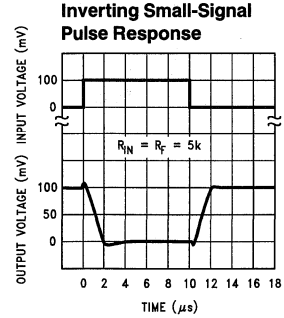
Non-Inverting Small Signal Pulse Response ($A_V = +1$)



Inverting Large-Signal Pulse Response

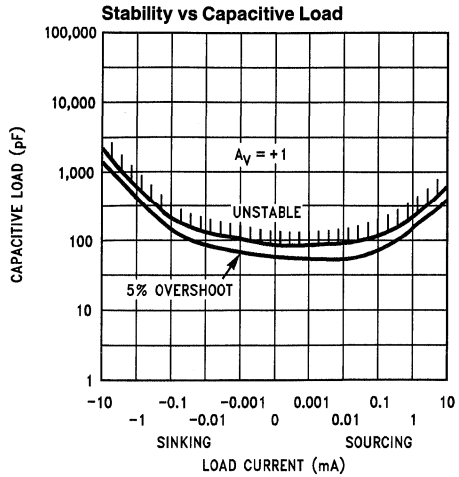


Inverting Small-Signal Pulse Response

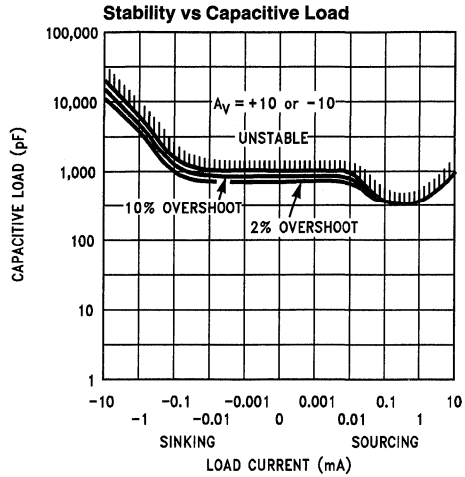


TL/H/11227–3

Typical Performance Characteristics $V_S = \pm 7.5V$, $T_A = 25°C$ (Continued)



TL/H/11227–4



TL/H/11227–5

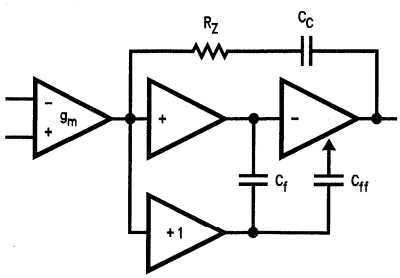
Note: Avoid resistive loads of less than 500Ω, as they may cause instability.

Application Hints

AMPLIFIER TOPOLOGY

The topology chosen for the LPC661 is unconventional (compared to general-purpose op amps) in that the traditional unity-gain buffer output stage is not used; instead, the output is taken directly from the output of the integrator, to allow rail-to-rail output swing. Since the buffer traditionally delivers the power to the load, while maintaining high op amp gain and stability, and must withstand shorts to either rail, these tasks now fall to the integrator.

As a result of these demands, the integrator is a compound affair with an embedded gain stage that is doubly fed forward (via C_f and C_{ff}) by a dedicated unity-gain compensation driver. In addition, the output portion of the integrator is a push-pull configuration for delivering heavy loads. While sinking current the whole amplifier path consists of three gain stages with one stage fed forward, whereas while sourcing the path contains four gain stages with two fed forward.



TL/H/11227–6

FIGURE 1. LPC661 Circuit Topology

The large signal voltage gain while sourcing is comparable to traditional bipolar op amps, for load resistance of at least 5 kΩ. The gain while sinking is higher than most CMOS op amps, due to the additional gain stage; however, when driving load resistance of 5 kΩ or less, the gain will be reduced as indicated in the Electrical Characteristics. The op amp can drive load resistance as low as 500Ω without instability.

COMPENSATING INPUT CAPACITANCE

Refer to the LMC660 or LMC662 datasheets to determine whether or not a feedback capacitor will be necessary for compensation and what the value of that capacitor would be.

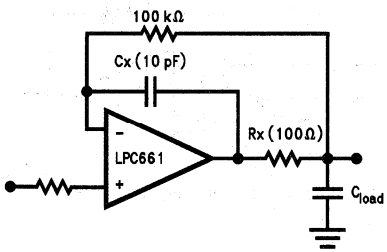
CAPACITIVE LOAD TOLERANCE

Like many other op amps, the LPC661 may oscillate when its applied load appears capacitive. The threshold of oscillation varies both with load and circuit gain. The configuration most sensitive to oscillation is a unity-gain follower. See the Typical Performance Characteristics.

The load capacitance interacts with the op amp's output resistance to create an additional pole. If this pole frequency is sufficiently low, it will degrade the op amp's phase margin so that the amplifier is no longer stable at low gains. The addition of a small resistor (50Ω to 100Ω) in series with the op amp's output, and a capacitor (5 pF to 10 pF) from inverting input to output pins, returns the phase margin to a safe value without interfering with lower-frequency circuit

Application Hints (Continued)

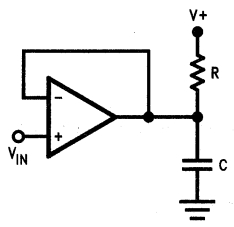
operation. Thus, larger values of capacitance can be tolerated without oscillation. Note that in all cases, the output will ring heavily when the load capacitance is near the threshold for oscillation.



TL/H/11227–7

FIGURE 2a. Rx, Cx Improve Capacitive Load Tolerance

Capacitive load driving capability is enhanced by using a pull up resistor to V^+ *(Figure 2b)*. Typically a pull up resistor conducting 50 μA or more will significantly improve capacitive load responses. The value of the pull up resistor must be determined based on the current sinking capability of the amplifier with respect to the desired output swing. Open loop gain of the amplifier can also be affected by the pull up resistor (see Electrical Characteristics).



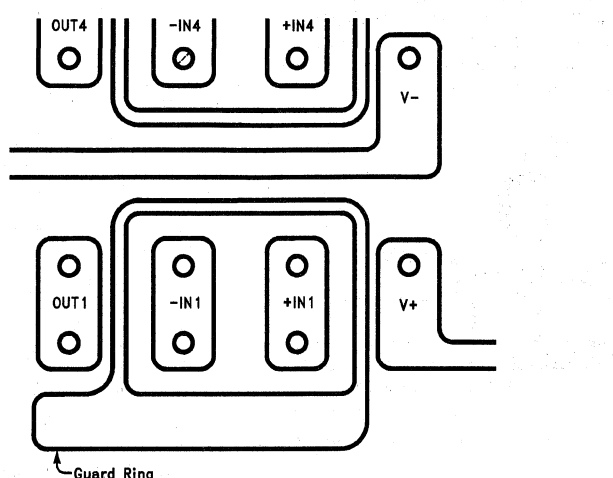
TL/H/11227–24

FIGURE 2b. Compensating for Large Capacitive Loads with A Pull Up Resistor

PRINTED-CIRCUIT-BOARD LAYOUT FOR HIGH-IMPEDANCE WORK

It is generally recognized that any circuit which must operate with less than 1000 pA of leakage current requires special layout of the PC board. When one wishes to take advantage of the ultra-low bias current of the LPC661, typically less than 0.04 pA, it is essential to have an excellent layout. Fortunately, the techniques for obtaining low leakages are quite simple. First, the user must not ignore the surface leakage of the PC board, even though it may sometimes appear acceptably low, because under conditions of high humidity or dust or contamination, the surface leakage will be appreciable.

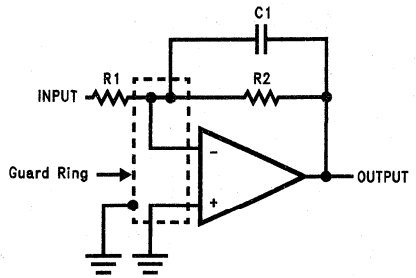
To minimize the effect of any surface leakage, lay out a ring of foil completely surrounding the LPC661's inputs and the terminals of capacitors, diodes, conductors, resistors, relay terminals, etc. connected to the op-amp's inputs. See *Figure 3*. To have a significant effect, guard rings should be placed on both the top and bottom of the PC board. This PC foil must then be connected to a voltage which is at the same voltage as the amplifier inputs, since no leakage current can flow between two points at the same potential. For example, a PC board trace-to-pad resistance of $10^{12}\Omega$, which is normally considered a very large resistance, could leak 5 pA if the trace were a 5V bus adjacent to the pad of an input. This would cause a 100 times degradation from the LPC660's actual performance. However, if a guard ring is held within 5 mV of the inputs, then even a resistance of $10^{11}\Omega$ would cause only 0.05 pA of leakage current, or perhaps a minor (2:1) degradation of the amplifier's performance. See *Figures 4a, 4b, 4c* for typical connections of guard rings for standard op-amp configurations. If both inputs are active and at high impedance, the guard can be tied to ground and still provide some protection; see *Figure 4d*.



TL/H/11227–8

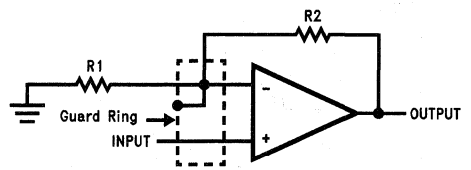
FIGURE 3. Example of Guard Ring in P.C. Board Layout, Using the LPC660

Application Hints (Continued)



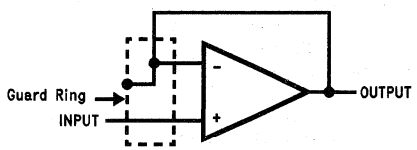
TL/H/11227–9

(a) Inverting Amplifier



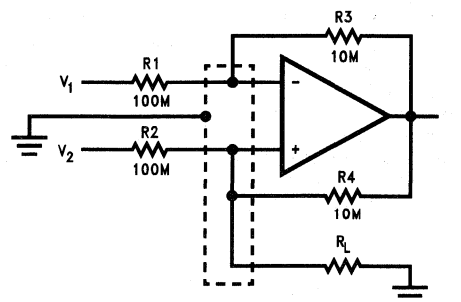
TL/H/11227–10

(b) Non-Inverting Amplifier



TL/H/11227–11

(c) Follower

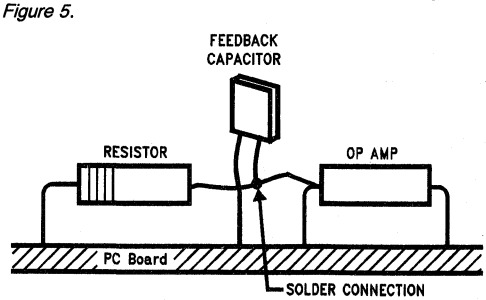


TL/H/11227–12

(d) Howland Current Pump

FIGURE 4. Guard Ring Connections

The designer should be aware that when it is inappropriate to lay out a PC board for the sake of just a few circuits, there is another technique which is even better than a guard ring on a PC board: Don't insert the amplifier's input pin into the board at all, but bend it up in the air and use only air as an insulator. Air is an excellent insulator. In this case you may have to forego some of the advantages of PC board construction, but the advantages are sometimes well worth the effort of using point-to-point up-in-the-air wiring. See *Figure 5*.



TL/H/11227–13

(Input pins are lifted out of PC board and soldered directly to components. All other pins connected to PC board.)

FIGURE 5. Air Wiring

BIAS CURRENT TESTING

The test method of *Figure 6* is appropriate for bench-testing bias current with reasonable accuracy. To understand its operation, first close switch S2 momentarily. When S2 is opened, then

$$I^- = \frac{dV_{OUT}}{dt} \times C2.$$

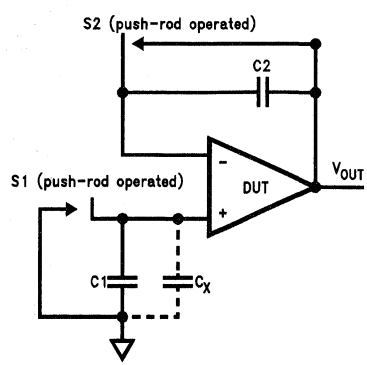


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FIGURE 6. Simple Input Bias Current Test Circuit

Application Hints (Continued)

A suitable capacitor for C2 would be a 5 pF or 10 pF silver mica, NPO ceramic, or air-dielectric. When determining the magnitude of I^-, the leakage of the capacitor and socket must be taken into account. Switch S2 should be left shorted most of the time, or else the dielectric absorption of the capacitor C2 could cause errors.

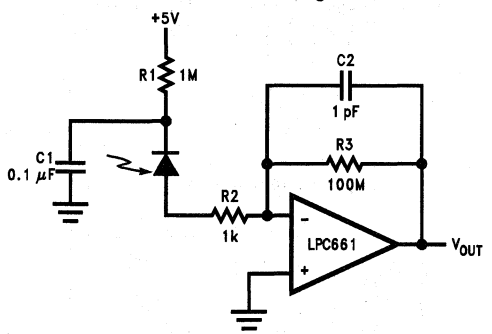
Similarly, if S1 is shorted momentarily (while leaving S2 shorted)

$$I^+ = \frac{dV_{OUT}}{dt} \times (C1 + C_X)$$

where C_X is the stray capacitance at the + input.

Typical Single-Supply Applications ($V^+ = 5.0\ V_{DC}$)

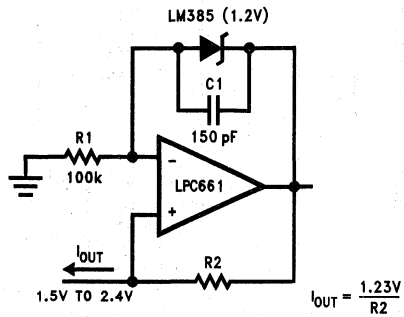
Photodiode Current-to-Voltage Converter



TL/H/11227–15

Note: A 5V bias on the photodiode can cut its capacitance by a factor of 2 or 3, leading to improved response and lower noise. However, this bias on the photodiode will cause photodiode leakage (also known as its dark current).

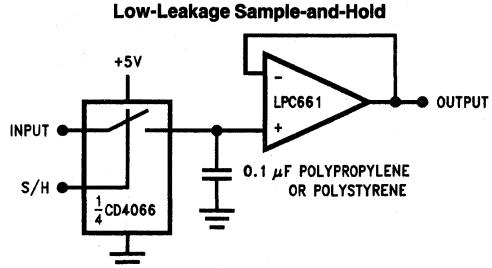
Micropower Current Source



TL/H/11227–16

(Upper limit of output range dictated by input common-mode range; lower limit dictated by minimum current requirement of LM385.)

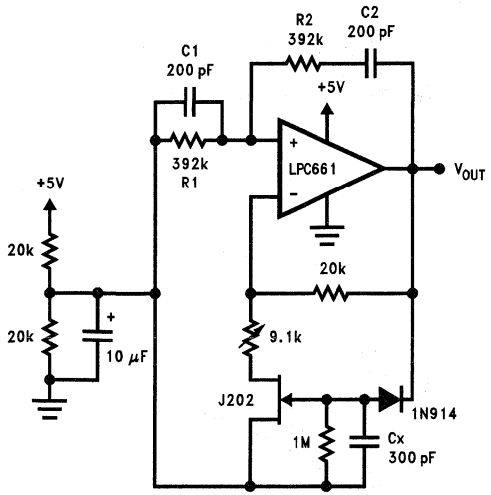
Low-Leakage Sample-and-Hold



TL/H/11227–17

Typical Single-Supply Applications (V^+ = 5.0 V_{DC}) (Continued)

Sine-Wave Oscillator



TL/H/11227–18

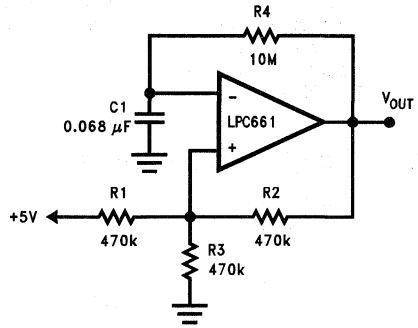
Oscillator frequency is determined by R1, R2, C1, and C2:

$$f_{OSC} = 1/2\pi RC$$

where R = R1 = R2 and C = C1 = C2.

This circuit, as shown, oscillates at 2.0 kHz with a peak-to-peak output swing of 4.5V

1 Hz Square-Wave Oscillator



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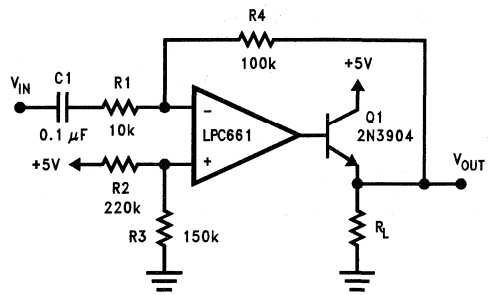
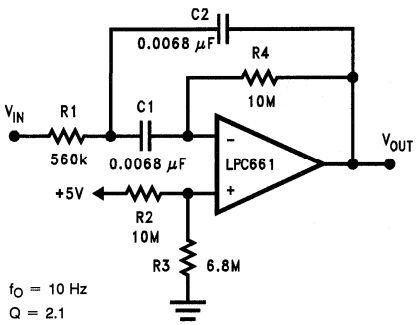
Power Amplifier



TL/H/11227–20

Typical Single-Supply Applications (V^+ = 5.0 V_{DC}) (Continued)

10 Hz Bandpass Filter



f_O = 10 Hz
Q = 2.1
Gain = 18.9 dB

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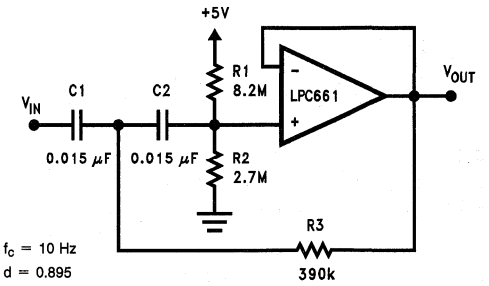
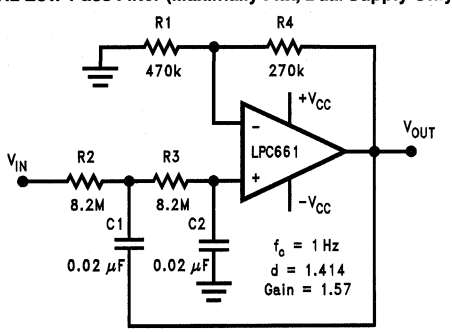
10 Hz High-Pass Filter (2 dB Dip)



f_C = 10 Hz
d = 0.895
Gain = 1

TL/H/11227–22

1 Hz Low-Pass Filter (Maximally Flat, Dual Supply Only)



TL/H/11227–23

National Semiconductor

LPC662
Low Power CMOS Dual Operational Amplifier

General Description

The LPC662 CMOS Dual operational amplifier is ideal for operation from a single supply. It features a wide range of operating voltage from +5V to +15V, rail-to-rail output swing in addition to an input common-mode range that includes ground. Performance limitations that have plagued CMOS amplifiers in the past are not a problem with this design. Input V_{OS}, drift, and broadband noise as well as voltage gain (into 100 kΩ and 5 kΩ) are all equal to or better than widely accepted bipolar equivalents, while the power supply requirement is typically less than 0.5 mW.

This chip is built with National's advanced Double-Poly Silicon-Gate CMOS process.

See the LPC660 datasheet for a Quad CMOS operational amplifier and LPC661 for a single CMOS operational amplifier with these same features.

Applications

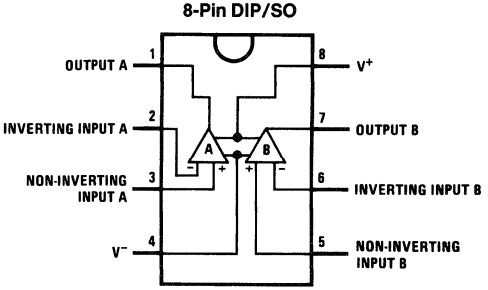
- High-impedance buffer
- Precision current-to-voltage converter
- Long-term integrator
- High-impedance preamplifier
- Active filter
- Sample-and-Hold circuit
- Peak detector

Features

- Rail-to-rail output swing
- Micropower operation (<0.5 mW)
- Specified for 100 kΩ and 5 kΩ loads
- High voltage gain 120 dB
- Low input offset voltage 3 mV
- Low offset voltage drift 1.3 μV/°C
- Ultra low input bias current 2 fA
- Input common-mode includes GND
- Operating range from +5V to +15V
- Low distortion 0.01% at 1 kHz
- Slew rate 0.11 V/μs
- Full military temperature range available

Connection Diagram

8-Pin DIP/SO



TL/H/10548–1

Top View

Ordering Information

Package	Temperature Range		NSC Drawing
	Military	Industrial	
8-Pin Side Brazed Ceramic DIP	LPC662AMD		D08C
8-Pin Small Outline		LPC662AIM or LPC662IM	M08A
8-Pin Molded DIP		LPC662AIN or LPC662IN	N08E
8-Pin Ceramic DIP	LPC662AMJ/883		J08A

Absolute Maximum Ratings (Note 3)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Differential Input Voltage	±Supply Voltage
Supply Voltage ($V^+ - V^-$)	16V
Output Short Circuit to V^+	(Note 11)
Output Short Circuit to V^-	(Note 1)
Lead Temperature (Soldering, 10 sec.)	260°C
Storage Temp. Range	−65°C to +150°C
Junction Temperature	150°C
ESD Rating (C = 100 pF, R = 1.5 kΩ)	500V
Power Dissipation	(Note 2)
Current at Input Pin	±5 mA
Current at Output Pin	±18 mA
Current at Power Supply Pin	35 mA
Voltage at Input/Output Pin	$(V^+) + 0.3V, (V^-) - 0.3V$

Operating Ratings (Note 3)

Temperature Range	
LPC662AMJ/883	$-55°C \le T_J \le +125°C$
LPC662AM	$-55°C \le T_J \le +125°C$
LPC662AI	$-40°C \le T_J \le +85°C$
LPC662I	$-40°C \le T_J \le +85°C$
Supply Range	4.75V to 15.5V
Power Dissipation	(Note 9)
Thermal Resistance (θ_{JA}) (Note 10)	
8-Pin Ceramic DIP	100°C/W
8-Pin Molded DIP	101°C/W
8-Pin SO	165°C/W
8-Pin Side Brazed Ceramic DIP	100°C/W

DC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for $T_J = 25°C$. **Boldface** limits apply at the temperature extremes. $V^+ = 5V$, $V^- = 0V$, $V_{CM} = 1.5V$, $V_O = 2.5V$ and $R_L > 1M$ unless otherwise specified.

Parameter	Conditions	Typ	LPC662AM LPC662AMJ/883 Limit (Notes 4, 8)	LPC662AI Limit (Note 4)	LPC662I Limit (Note 4)	Units
Input Offset Voltage		1	3	3	6	mV
			3.5	**3.3**	**6.3**	max
Input Offset Voltage Average Drift		1.3				μV/°C
Input Bias Current		0.002	20			pA
			100	**4**	**4**	max
Input Offset Current		0.001	20			pA
			100	**2**	**2**	max
Input Resistance		>1				Tera Ω
Common Mode Rejection Ratio	$0V \le V_{CM} \le 12.0V$ $V^+ = 15V$	83	70	70	63	dB
			68	**68**	**61**	min
Positive Power Supply Rejection Ratio	$5V \le V^+ \le 15V$ $V_O = 2.5V$	83	70	70	63	dB
			68	**68**	**61**	min
Negative Power Supply Rejection Ratio	$0V \le V^- \le -10V$	94	84	84	74	dB
			82	**83**	**73**	min
Input Common-Mode Voltage Range	$V^+ = 5V$ and 15V For CMRR ≥ 50 dB	−0.4	−0.1	−0.1	−0.1	V
			0	**0**	**0**	max
		$V^+ - 1.9$	$V^+ - 2.3$	$V^+ - 2.3$	$V^+ - 2.3$	V
			$\mathbf{V^+ - 2.6}$	$\mathbf{V^+ - 2.5}$	$\mathbf{V^+ - 2.5}$	min

DC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for T_J = 25°C. **Boldface** limits apply at the temperature extremes. V^+ = 5V, V^- = 0V, V_{CM} = 1.5V, V_O = 2.5V and R_L > 1M unless otherwise specified. (Continued)

Parameter	Conditions	Typ	LPC662AM LPC662AMJ/883 Limit (Notes 4, 8)	LPC662AI Limit (Note 4)	LPC662I Limit (Note 4)	Units
Large Signal Voltage Gain	R_L = 100 kΩ (Note 5) Sourcing	1000	400	400	300	V/mV min
			250	**300**	**200**	
	Sinking	500	180	180	90	V/mV min
			70	**120**	**70**	
	R_L = 5 kΩ (Note 5) Sourcing	1000	200	200	100	V/mV min
			150	**160**	**80**	
	Sinking	250	100	100	50	V/mV min
			35	**60**	**40**	
Output Swing	V^+ = 5V R_L = 100 kΩ to $V^+/2$	4.987	4.970	4.970	4.940	V min
			4.950	**4.950**	**4.910**	
		0.004	0.030	0.030	0.060	V max
			0.050	**0.050**	**0.090**	
	V^+ = 5V R_L = 5 kΩ to $V^+/2$	4.940	4.850	4.850	4.750	V min
			4.750	**4.750**	**4.650**	
		0.040	0.150	0.150	0.250	V max
			0.250	**0.250**	**0.350**	
	V^+ = 15V R_L = 100 kΩ to $V^+/2$	14.970	14.920	14.920	14.880	V min
			14.880	**14.880**	**14.820**	
		0.007	0.030	0.030	0.060	V max
			0.050	**0.050**	**0.090**	
	V^+ = 15V R_L = 5 kΩ to $V^+/2$	14.840	14.680	14.680	14.580	V min
			14.600	**14.600**	**14.480**	
		0.110	0.220	0.220	0.320	V max
			0.300	**0.300**	**0.400**	
Output Current V^+ = 5V	Sourcing, V_O = 0V	22	16	16	13	mA min
			12	**14**	**11**	
	Sinking, V_O = 5V	21	16	16	13	mA min
			12	**14**	**11**	
Output Current V^+ = 15V	Sourcing, V_O = 0V	40	19	28	23	mA min
			19	**25**	**20**	
	Sinking, V_O = 13V (Note 11)	39	19	28	23	mA min
			19	**24**	**19**	
Supply Current	Both Amplifiers V_O = 1.5V	86	120	120	140	μA max
			145	**140**	**160**	

AC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for T_J = 25°C. **Boldface** limits apply at the temperature extremes. V^+ = 5V, V^- = 0V, V_{CM} = 1.5V, V_O = 2.5V and R_L > 1M unless otherwise specified.

Parameter	Conditions	Typ	LPC662AM LPC662AMJ/883 Limit (Notes 4, 8)	LPC662AI Limit (Note 4)	LPC662I Limit (Note 4)	Units
Slew Rate	(Note 6)	0.11	0.07	0.07	0.05	V/μs
			0.04	**0.05**	**0.03**	min
Gain-Bandwidth Product		0.35				MHz
Phase Margin		50				Deg
Gain Margin		17				dB
Amp-to-Amp Isolation	(Note 7)	130				dB
Input Referred Voltage Noise	F = 1 kHz	42				nV/$\sqrt{Hz}$
Input Referred Current Noise	F = 1 kHz	0.0002				pA/$\sqrt{Hz}$
Total Harmonic Distortion	F = 1 kHz, A_V = −10, V^+ = 15V R_L = 100 kΩ, V_O = 8 V_{PP}	0.01				%

Note 1: Applies to both single supply and split supply operation. Continuous short circuit operation at elevated ambient temperature and/or multiple Op Amp shorts can result in exceeding the maximum allowed junction temperature of 150°C. Output currents in excess of ±30 mA over long term may adversely affect reliability.

Note 2: The maximum power dissipation is a function of $T_{J(max)}$, θ_{JA}, and T_A. The maximum allowable power dissipation of any ambient temperature is $P_D = (T_{J(max)} - T_A)/\theta_{JA}$.

Note 3: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed.

Note 4: Limits are guaranteed by testing or correlation.

Note 5: V^+ = 15V, V_{CM} = 7.5V and R_L connected to 7.5V. For Sourcing tests, 7.5V ≤ V_O ≤ 11.5V. For Sinking tests, 2.5V ≤ V_O ≤ 7.5V.

Note 6: V^+ = 15V. Connected as Voltage Follower with 10V step input. Number specified is the slower of the positive and negative slew rates.

Note 7: Input referred. V^+ = 15V and R_L = 100 kΩ connected to $V^+/2$. Each amp excited in turn with 1 kHz to produce V_O = 13 V_{PP}.

Note 8: A military RETS electrical test specification is available on request. At the time of printing, the LPC662AMJ/883 RETS specification complied fully with the **boldface** limits in this column. The LPC662AMJ/883 may also be procured to a Standard Military Drawing specification.

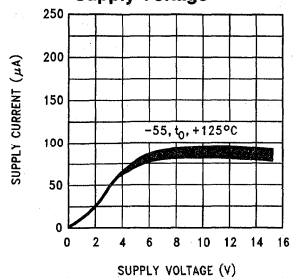
Note 9: For operating at elevated temperatures the device must be derated based on the thermal resistance θ_{JA} with $P_D = (T_J - T_A)/\theta_{JA}$.

Note 10: All numbers apply for packages soldered directly into a PC board.

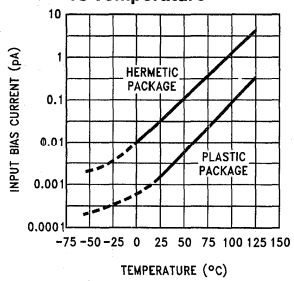
Note 11: Do not connect output to V^+ when V^+ is greater than 13V or reliability may be adversely affected.

Typical Performance Characteristics $V_S = \pm 7.5V$, $T_A = 25°C$ unless otherwise specified

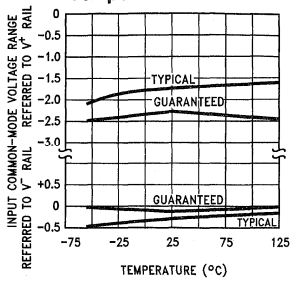
Supply Current vs Supply Voltage



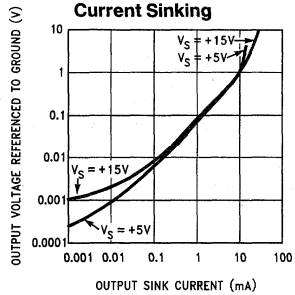
Input Bias Current vs Temperature



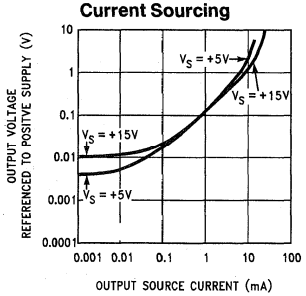
Input Common-Mode Voltage Range vs Temperature



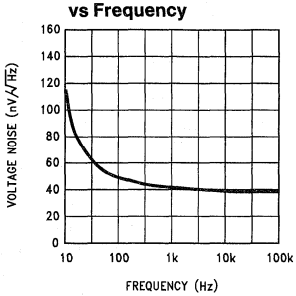
Output Characteristics Current Sinking



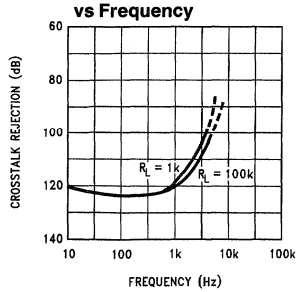
Output Characteristics Current Sourcing



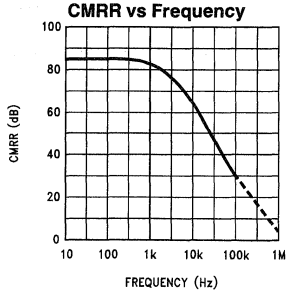
Input Voltage Noise vs Frequency



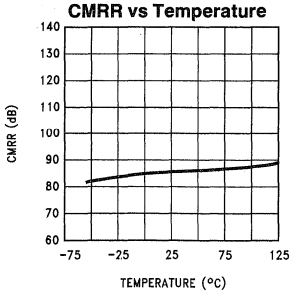
Crosstalk Rejection vs Frequency



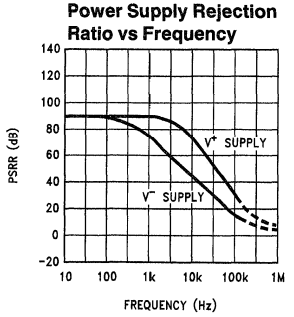
CMRR vs Frequency



CMRR vs Temperature



Power Supply Rejection Ratio vs Frequency



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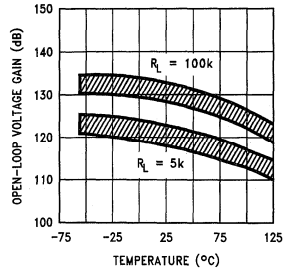
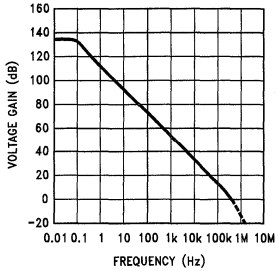
Typical Performance Characteristics $V_S = \pm 7.5V$, $T_A = 25°C$ unless otherwise specified (Continued)

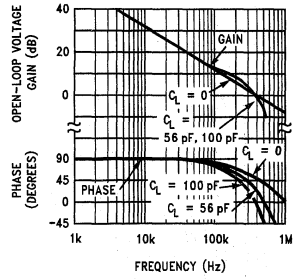
Open-Loop Voltage Gain vs Temperature



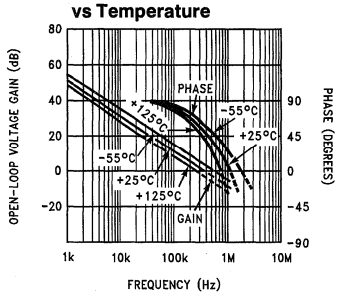
Open-Loop Frequency Response



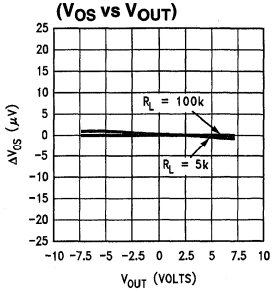
Gain and Phase Responses vs Load Capacitance



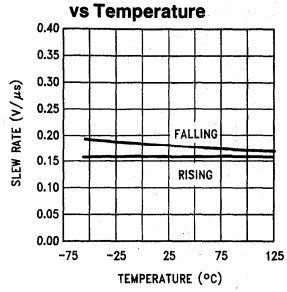
Gain and Phase Responses vs Temperature



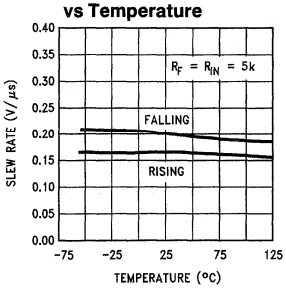
Gain Error (V_{OS} vs V_{OUT})



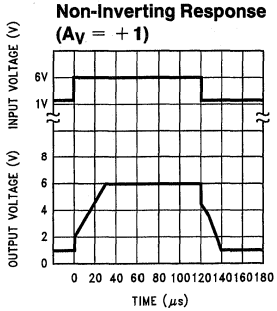
Non-Inverting Slew Rate vs Temperature



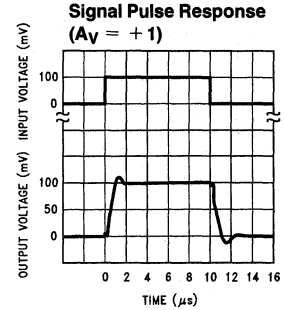
Inverting Slew Rate vs Temperature



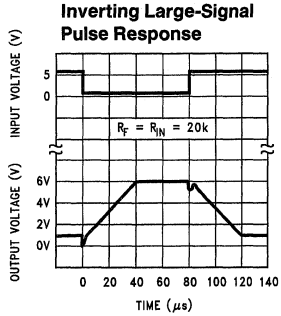
Large-Signal Pulse Non-Inverting Response ($A_V = +1$)



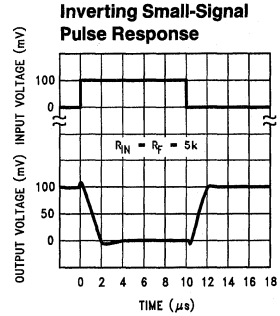
Non-Inverting Small Signal Pulse Response ($A_V = +1$)



Inverting Large-Signal Pulse Response



Inverting Small-Signal Pulse Response



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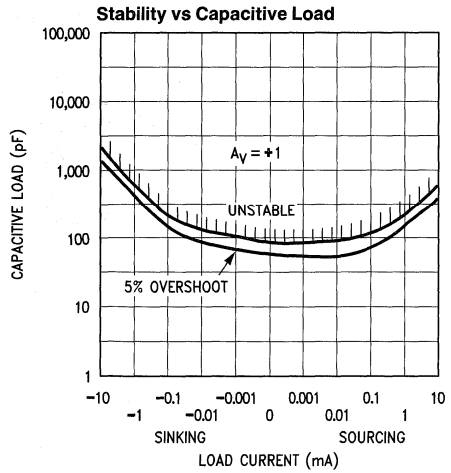
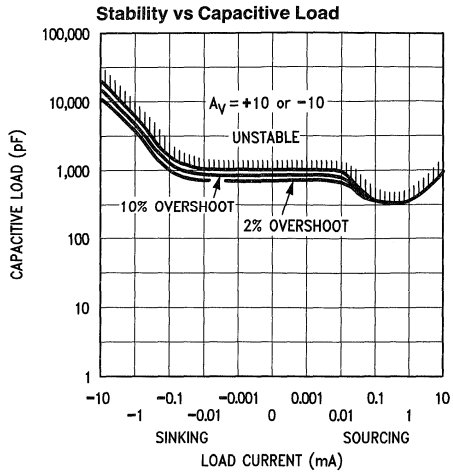
Typical Performance Characteristics $V_S = \pm 7.5V$, $T_A = 25°C$ (Continued)



TL/H/10548–4



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Note: Avoid resistive loads of less than 500Ω, as they may cause instability.

Application Hints

AMPLIFIER TOPOLOGY

The topology chosen for the LPC662 is unconventional (compared to general-purpose op amps) in that the traditional unity-gain buffer output stage is not used; instead, the output is taken directly from the output of the integrator, to allow rail-to-rail output swing. Since the buffer traditionally delivers the power to the load, while maintaining high op amp gain and stability, and must withstand shorts to either rail, these tasks now fall to the integrator.

As a result of these demands, the integrator is a compound affair with an embedded gain stage that is doubly fed forward (via C_f and C_{ff}) by a dedicated unity-gain compensation driver. In addition, the output portion of the integrator is a push-pull configuration for delivering heavy loads. While sinking current the whole amplifier path consists of three gain stages with one stage fed forward, whereas while sourcing the path contains four gain stages with two fed forward.

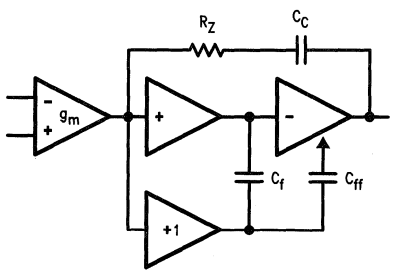

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FIGURE 1. LPC662 Circuit Topology (Each Amplifier)

The large signal voltage gain while sourcing is comparable to traditional bipolar op amps for load resistance of at least 5 kΩ. The gain while sinking is higher than most CMOS op amps, due to the additional gain stage; however, when driving load resistance of 5 kΩ or less, the gain will be reduced as indicated in the Electrical Characteristics. The op amp can drive load resistance as low as 500Ω without instability.

COMPENSATING INPUT CAPACITANCE

Refer to the LMC660 or LMC662 datasheets to determine whether or not a feedback capacitor will be necessary for compensation and what the value of that capacitor would be.

CAPACITIVE LOAD TOLERANCE

Like many other op amps, the LPC662 may oscillate when its applied load appears capacitive. The threshold of oscillation varies both with load and circuit gain. The configuration most sensitive to oscillation is a unity-gain follower. See the Typical Performance Characteristics.

The load capacitance interacts with the op amp's output resistance to create an additional pole. If this pole frequency is sufficiently low, it will degrade the op amp's phase margin so that the amplifier is no longer stable at low gains. The addition of a small resistor (50Ω to 100Ω) in series with the op amp's output, and a capacitor (5 pF to 10 pF) from inverting input to output pins, returns the phase margin to a safe value without interfering with lower-frequency circuit

Application Hints (Continued)

operation. Thus, larger values of capacitance can be tolerated without oscillation. Note that in all cases, the output will ring heavily when the load capacitance is near the threshold for oscillation.

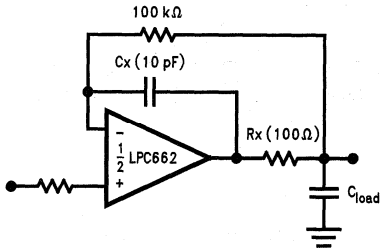

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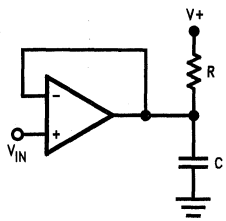
FIGURE 2a. Rx, Cx Improve Capacitive Load Tolerance

Capacitive load driving capability is enhanced by using a pull up resistor to V^+ *(Figure 2b)*. Typically a pull up resistor conducting 50 μA or more will significantly improve capacitive load responses. The value of the pull up resistor must be determined based on the current sinking capability of the amplifier with respect to the desired output swing. Open loop gain of the amplifier can also be affected by the pull up resistor (see Electrical Characteristics).



TL/H/10548–26

FIGURE 2b. Compensating for Large Capacitive Loads with A Pull Up Resistor

PRINTED-CIRCUIT-BOARD LAYOUT FOR HIGH-IMPEDANCE WORK

It is generally recognized that any circuit which must operate with less than 1000 pA of leakage current requires special layout of the PC board. When one wishes to take advantage of the ultra-low bias current of the LPC662, typically less than 0.04 pA, it is essential to have an excellent layout. Fortunately, the techniques for obtaining low leakages are quite simple. First, the user must not ignore the surface leakage of the PC board, even though it may sometimes appear acceptably low, because under conditions of high humidity or dust or contamination, the surface leakage will be appreciable.

To minimize the effect of any surface leakage, lay out a ring of foil completely surrounding the LPC662's inputs and the terminals of capacitors, diodes, conductors, resistors, relay terminals, etc. connected to the op-amp's inputs. See *Figure 3*. To have a significant effect, guard rings should be placed on both the top and bottom of the PC board. This PC foil must then be connected to a voltage which is at the same voltage as the amplifier inputs, since no leakage current can flow between two points at the same potential. For example, a PC board trace-to-pad resistance of 10^{12} ohms, which is normally considered a very large resistance, could leak 5 pA if the trace were a 5V bus adjacent to the pad of an input. This would cause a 100 times degradation from the LPC662's actual performance. However, if a guard ring is held within 5 mV of the inputs, then even a resistance of 10^{11} ohms would cause only 0.05 pA of leakage current, or perhaps a minor (2:1) degradation of the amplifier's performance. See *Figures 4a*, *4b*, *4c* for typical connections of guard rings for standard op-amp configurations. If both inputs are active and at high impedance, the guard can be tied to ground and still provide some protection; see *Figure 4d*.

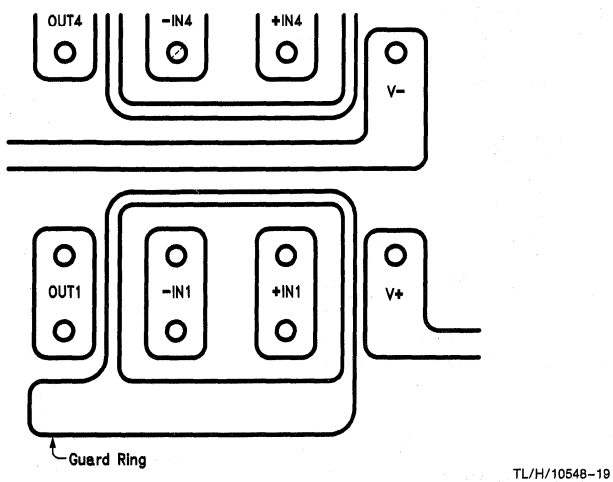


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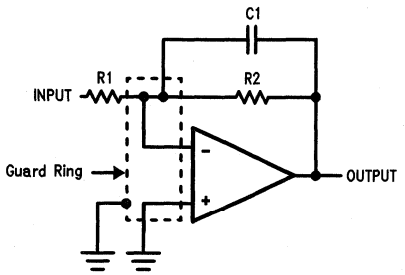
FIGURE 3. Example of Guard Ring in P.C. Board Layout, using the LPC660

Application Hints (Continued)



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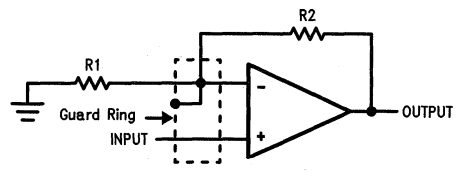
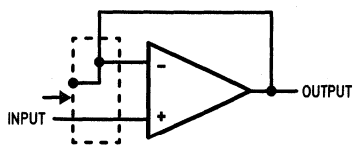
(a) Inverting Amplifier



TL/H/10548–21

(b) Non-Inverting Amplifier



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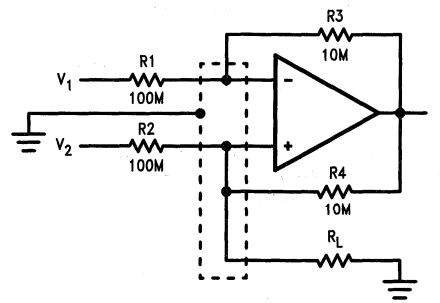
(c) Follower

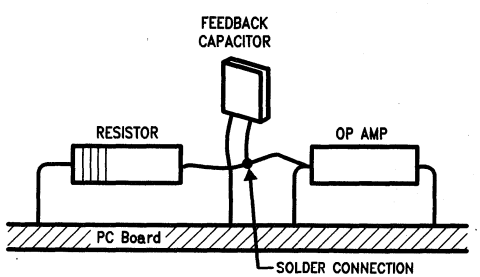


TL/H/10548–23

(d) Howland Current Pump

FIGURE 4. Guard Ring Connections

The designer should be aware that when it is inappropriate to lay out a PC board for the sake of just a few circuits, there is another technique which is even better than a guard ring on a PC board: Don't insert the amplifier's input pin into the board at all, but bend it up in the air and use only air as an insulator. Air is an excellent insulator. In this case you may have to forego some of the advantages of PC board construction, but the advantages are sometimes well worth the effort of using point-to-point up-in-the-air wiring. See *Figure 5*.



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(Input pins are lifted out of PC board and soldered directly to components. All other pins connected to PC board.)

FIGURE 5. Air Wiring

BIAS CURRENT TESTING

The test method of *Figure 6* is appropriate for bench-testing bias current with reasonable accuracy. To understand its operation, first close switch S2 momentarily. When S2 is opened, then

$$I^- = \frac{dV_{OUT}}{dt} \times C2.$$

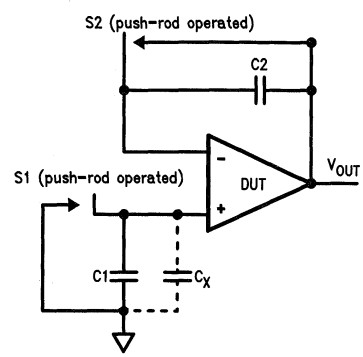

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FIGURE 6. Simple Input Bias Current Test Circuit

Application Hints (Continued)

A suitable capacitor for C2 would be a 5 pF or 10 pF silver mica, NPO ceramic, or air-dielectric. When determining the magnitude of I^-, the leakage of the capacitor and socket must be taken into account. Switch S2 should be left shorted most of the time, or else the dielectric absorption of the capacitor C2 could cause errors.

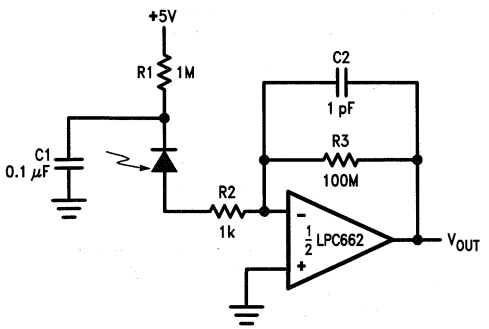
Similarly, if S1 is shorted momentarily (while leaving S2 shorted)

$$I^+ = \frac{dV_{OUT}}{dt} \times (C1 + C_X)$$

where C_X is the stray capacitance at the + input.

Typical Single-Supply Applications ($V^+ = 5.0\ V_{DC}$)

Photodiode Current-to-Voltage Converter



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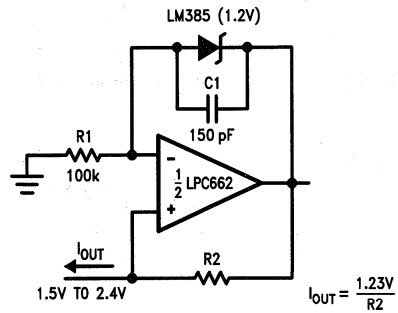
Note: A 5V bias on the photodiode can cut its capacitance by a factor of 2 or 3, leading to improved response and lower noise. However, this bias on the photodiode will cause photodiode leakage (also known as its dark current).

Micropower Current Source



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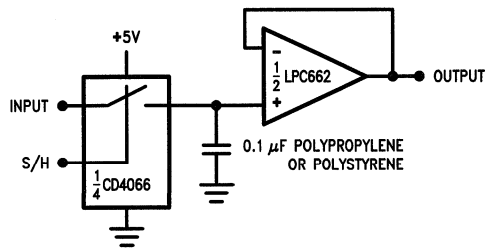
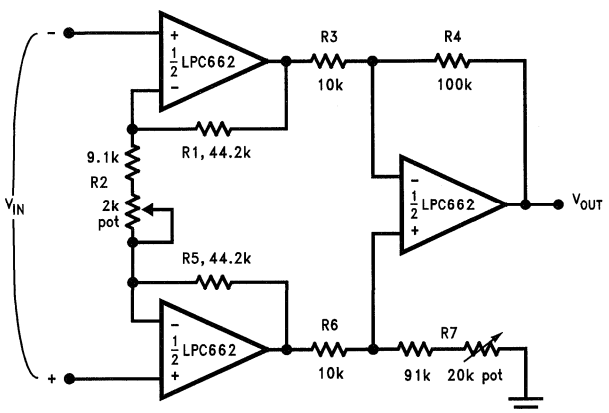
(Upper limit of output range dictated by input common-mode range; lower limit dictated by minimum current requirement of LM385.)

Low-Leakage Sample-and-Hold



TL/H/10548–8

Instrumentation Amplifier



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If R1 = R5, R3 = R6 and R4 = R7; then

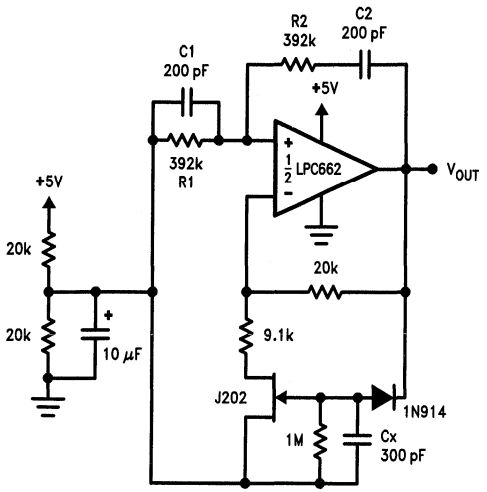
$$\frac{V_{OUT}}{V_{IN}} = \frac{R2 + 2R1}{R2} \times \frac{R4}{R3}$$

$\therefore A_V \approx 100$ for circuit shown.

For good CMRR over temperature, low drift resistors should be used. Matching of R3 to R6 and R4 to R7 affects CMRR. Gain may be adjusted through R2. CMRR may be adjusted through R7.

Typical Single-Supply Applications (V^+ = 5.0 V_{DC}) (Continued)

Sine-Wave Oscillator



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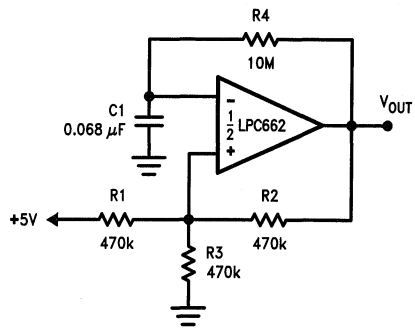
Oscillator frequency is determined by R1, R2, C1, and C2:

$$f_{OSC} = 1/2\pi RC$$

where R = R1 = R2 and C = C1 = C2.

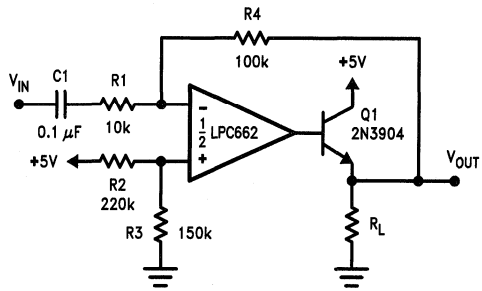
This circuit, as shown, oscillates at 2.0 kHz with a peak-to-peak output swing of 4.5V

1 Hz Square-Wave Oscillator



TL/H/10548–11

Power Amplifier



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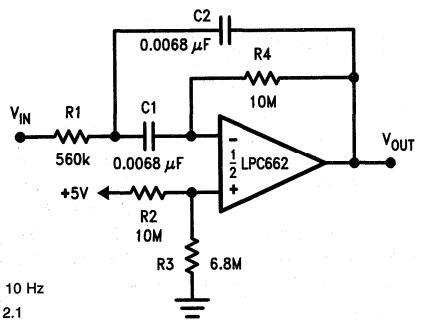
Typical Single-Supply Applications (V^+ = 5.0 V_{DC}) (Continued)

10 Hz Bandpass Filter



f_O = 10 Hz
Q = 2.1
Gain = −8.8

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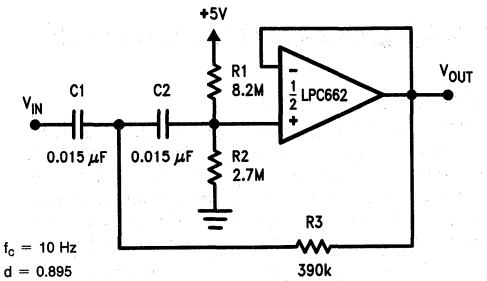
10 Hz High-Pass Filter (2 dB Dip)



f_c = 10 Hz
d = 0.895
Gain = 1

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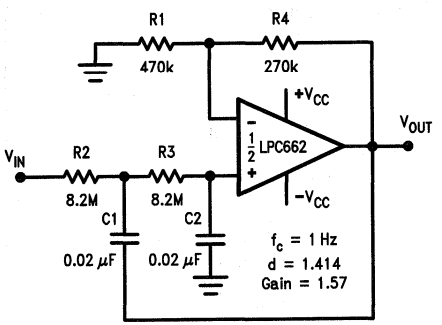
1 Hz Low-Pass Filter (Maximally Flat, Dual Supply Only)



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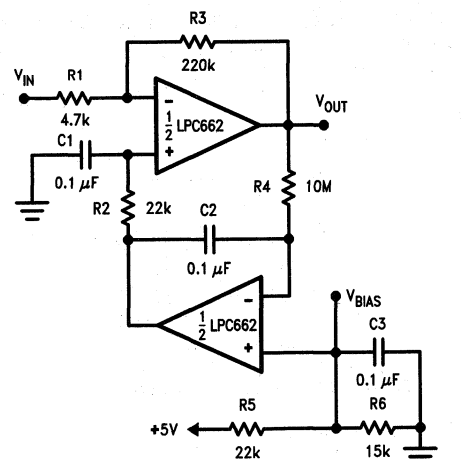
High Gain Amplifier with Offset Voltage Reduction



Gain = −46.8

Output offset voltage reduced to the level of the input offset voltage of the bottom amplifier (typically 1 mV), referred to V_{BIAS}.

TL/H/10548–16

National Semiconductor

OP-07 Low Offset, Low Drift Operational Amplifier

General Description

The OP-07 has very low input offset voltage which is obtained by trimming at the wafer stage. These low offset voltages generally eliminate any need for external nulling. The OP-07 also features low input bias current and high open-loop gain. The low offsets and high open-loop gain make the OP-07 particularly useful for high-gain applications.

The wide input voltage range of ±13V minimum combined with high CMRR of 110 dB and high input impedance provide high accuracy in the non-inverting circuit configuration. Excellent linearity and gain accuracy can be maintained even at high closed-loop gains.

Stability of offsets and gain with time or variation in temperature is excellent.

The OP-07 is available in TO-99 metal can, ceramic or molded DIP.

For improved specifications, see the LM607.

Features

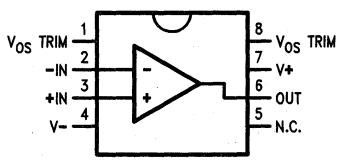
- Low V_{OS} — 75 μV Max
- Low V_{OS} Drift — 0.6 μV/°C Max
- Ultra-Stable vs Time — 1.0 μV/Month Max
- Low Noise — 0.6 μVp-p Max
- Wide Input Voltage Range — ±14V
- Wide Supply Voltage Range — ±3V to ±18V
- Fits 725/108A/308A, 741, AD510 Sockets
- Replaces the μA714

Applications

- Strain Gauge Amplifiers
- Thermocouple Amplifiers
- Precision Reference Buffer
- Analog Computing Functions

Connection Diagrams

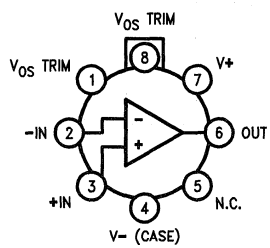
Dual-In-Line Package



TL/H/10550–1

See NS Package Number J08A or N08E

Metal Can Package



TL/H/10550–2

See NS Package Number H08C

Ordering Information

T_A = 25°C V_{OS}Max (μV)	H08C TO-99	Package J08A CERDIP	N08E Plastic	Operating Temperature Range
75	OP07EJ	OP07EZ	OP07EP	COM
75	OP07J*	OP07Z		MIL
150	OP07CJ	OP07CZ	OP07CP	COM
150	OP07DJ		OP07DP	COM

*Also available per SMD #8203602

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	±22V
Internal Power Dissipation (Note 5)	500 mW
Differential Input Voltage	±30V
Input Voltage (Note 6)	±22V
Output Short-Circuit Duration	Continuous
Storage Temperature Range	
J and Z Packages	−65°C to +150°C
P Package	−65°C to +125°C
Lead Temperature (Soldering, 60 sec.)	260°C
Junction Temperature	−65°C to +150°C

Operating Temperature Range

OP-07	−55°C to +125°C
OP-07E, OP-07C, OP-07D	0°C to +70°C

Electrical Characteristics

Unless otherwise specified, V_S = ±15V, T_A = 25°C. **Boldface** type refers to limits over −55°C ≤ T_A ≤ +125°C

Symbol	Parameter	Conditions	OP-07			Units
			Min	Typ	Max	
V_{OS}	Input Offset Voltage	(Note 1) (Note 1)		30 **60**	75 **200**	µV
$\Delta V_{OS/t}$	Long-Term Input Offset Voltage Stability	(Note 2)		0.2	1.0	µV/Mo
I_{OS}	Input Offset Current			0.4 **1.2**	2.8 **5.6**	nA
I_B	Input Bias Current			±1.0 ±**2**	±3.0 ±**6**	nA
e_{np-p}	Input Noise Voltage	0.1 Hz to 10 Hz (Note 3)		0.35	0.6	μV_{p-p}
e_n	Input Noise Voltage Density	f_O = 10 Hz (Note 3) f_O = 100 Hz (Note 3) f_O = 1000 Hz (Note 3)		10.3 10.0 9.6	18.0 13.0 11.0	$nV/\sqrt{Hz}$
i_{np-p}	Input Noise Current	0.1 Hz to 10 Hz (Note 3)		14	30	pA_{p-p}
i_n	Input Noise Current Density	f_O = 10 Hz (Note 3) f_O = 100 Hz (Note 3) f_O = 1000 Hz (Note 3)		0.32 0.14 0.12	0.80 0.23 0.17	$pA/\sqrt{Hz}$
R_{IN}	Input Resistance Differential-Mode	(Note 4)	20	60		MΩ
R_{INCM}	Input Resistance Common-Mode			200		GΩ
IVR	Input Voltage Range		±13.0 ±**13.0**	±14.0 ±**13.5**		V
CMRR	Common-Mode Rejection Ratio	V_{CM} = ±13V	110 **106**	126 **123**		dB
PSRR	Power Supply Rejection Ratio	V_S = ±3V to ±18V		4 **5**	10 **20**	µV/V
A_{VO}	Large-Signal Voltage Gain	R_L ≥ 2 kΩ, V_O = ±10V R_L ≥ 2 kΩ, V_O = ±10V R_L ≥ 500Ω, V_O = ±0.5V, V_S = ±3V (Note 4)	200 **150** 150	500 **400** 400		V/mV
V_O	Output Voltage Swing	R_L ≥ 10 kΩ R_L ≥ 2 kΩ R_L ≥ 2 kΩ R_L ≥ 1 kΩ	±12.5 ±12.0 ±**12.0** ±10.5	±13.0 ±12.8 ±**12.6** ±12.0		V

Electrical Characteristics (Continued)

Unless otherwise specified, $V_S = \pm 15V$, $T_A = 25°C$. **Boldface** type refers to limits over $-55°C \leq T_A \leq +125°C$

Symbol	Parameter	Conditions	OP-07			Units
			Min	Typ	Max	
SR	Slew Rate	$R_L \geq 2\,k\Omega$ (Note 3)	0.1	0.3		V/μs
BW	Closed-Loop Bandwidth	$A_{VCL} = +1$ (Note 3)	0.4	0.6		MHz
R_O	Open-Loop Output Resistance	$V_O = 0$, $I_O = 0$		60		Ω
P_d	Power Consumption	$V_S = \pm 15V$, No Load $V_S = \pm 3V$, No Load		75 4	120 6	mW
	Offset Adj. Range	$R_P = 20\,k\Omega$		±4		mV
TCV_{OS}	Average Input Offset Voltage Drift Without External Trim	(Note 3)		**0.3**	**1.3**	μV/°C
TCV_{OSn}	With External Trim	$R_P = 20\,k\Omega$ (Note 4)		**0.3**	**1.3**	
TCI_{OS}	Average Input Offset Current Drift	(Note 3)		**8**	**50**	pA/°C
TCI_B	Average Input Bias Drift	(Note 3)		**13**	**50**	pA/°C

Note 1: V_{OS} is measured approximately 0.5 second after application of power.

Note 2: Long-Term Offset Voltage Stability refers to the averaged trend line of V_{OS} vs time over extended periods after the first 30 days of operation. Excluding the initial hour of operation, changes in V_{OS} during the first 30 operating days are typically 2.5 μV. Parameter is sample tested.

Note 3: Sample tested.

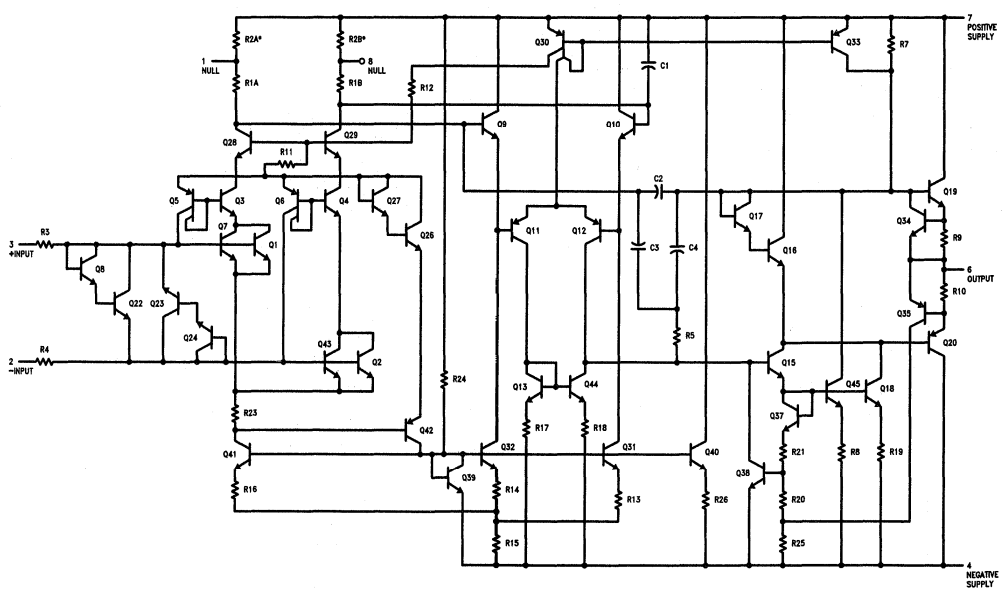
Note 4: Guaranteed by design.

Note 5: The typical θ_{JA} of the H08 (TO-99) package is 155°C/W, the J08 (CERDIP) package is 92° C/W and the N08 (Molded DIP) is 100° C/W. The typical θ_{JC} of the H08 package is 17.5° C/W. All numbers apply for packages soldered directly into an etched circuit board.

Note 6: For supply voltages of less than ±22V, the maximum input voltage is 0.5V beyond either supply.

Note 7: See RETSOPO7X for the OP07H military specifications.

Simplified Schematic



TL/H/10550–3

*R2A and R2B are electronically trimmed on chip at the factory for minimum offset voltage.

Electrical Characteristics

Unless otherwise specified, $V_S = \pm 15V$, $T_A = 25°C$. **Boldface** type refers to limits over $0°C \le T_A \le 70°C$

Symbol	Parameter	Conditions	OP-07E			OP-07C			Units
			Min	Typ	Max	Min	Typ	Max	
V_{OS}	Input Offset Voltage	(Note 1)		30 **45**	75 **130**		60 **85**	150 **250**	μV
$V_{OS/t}$	Long-Term V_{OS} Stability	(Note 2)		0.3	1.5		0.4	2.0	μV/Mo
I_{OS}	Input Offset Current			0.5 **0.9**	3.8 **5.3**		0.8 **1.6**	6.0 **8.0**	nA
I_B	Input Bias Current			±1.2 **±1.5**	±4.0 **±5.5**		±1.8 **±2.2**	±7.0 **±9.0**	nA
e_{np-p}	Input Noise Voltage	0.1 Hz to 10 Hz (Note 3)		0.35	0.6		0.38	0.65	μV_{p-p}
e_n	Input Noise Voltage Density	f_O = 10 Hz f_O = 100 Hz (Note 3) f_O = 1000 Hz		10.3 10.0 9.6	18.0 13.0 11.0		10.5 10.2 9.8	20.0 13.5 11.5	$nV/\sqrt{Hz}$
i_{np-p}	Input Noise Current	0.1 Hz to 10 Hz (Note 3)		14	30		15	35	pA_{p-p}
i_n	Input Noise Current Density	f_O = 10 Hz f_O = 100 Hz (Note 3) f_O = 1000 Hz		0.32 0.14 0.12	0.80 0.23 0.17		0.35 0.15 0.13	0.90 0.27 0.18	$pA/\sqrt{Hz}$
R_{IN}	Input Resistance Differential-Mode	(Note 4)	15	50		8	33		MΩ
R_{INCM}	Input Resistance Common-Mode			160			120		GΩ
IVR	Input Voltage Range		±13.0	±14.0		±13	±14		V
CMRR	Common-Mode Rejection Ratio	V_{CM} = ±13V	106 **103**	123 **123**		100 **97**	120 **120**		dB
PSRR	Power Supply Rejection Ratio	V_S = ±3V to ±18V V_S = ±3V to ±18V		5 **7**	20 **32**		7 **10**	32 **51**	μV/V
A_{VO}	Large Signal Voltage Gain	$R_L \ge 2 k\Omega$, V_O = ±10V $R_L \ge 2 k\Omega$ $R_L \ge 500\Omega$, V_O = ±0.5V, V_S = ±3V (Note 4)	200 **180** 150	500 **450** 400		120 **100** 100	400 **400** 400		V/mV
V_O	Output Voltage Swing	$R_L \ge 10 k\Omega$ $R_L \ge 2 k\Omega$ $R_L \ge 2 k\Omega$ $R_L \ge 1 k\Omega$	±12.5 ±12.0 **±12.0** ±10.5	±13.0 ±12.8 **±12.6** ±12.0		±12.0 ±11.5 **±11.0**	±13.0 ±12.8 **±12.6** ±12.0		V
SR	Slew Rate	$R_L \ge 2 k\Omega$ (Note 3)	0.1	0.3		0.1	0.3		V/μs
BW	Closed-Loop Bandwidth	A_{VCL} = +1 (Note 3)	0.4	0.6		0.4	0.6		MHz
R_O	Output Resistance	V_O = 0, I_O = 0		60			60		Ω
P_d	Power Consumption	V_S = ±15V, No Load V_S = ±3V, No Load		75 4	120 6		80 4	150 8	mW
	Offset Adj. Range	R_P = 20 kΩ		±4			±4		mV
TCV_{OS} TCV_{OSn}	Average Input Offset Voltage Drift Without External Trim With External Trim	(Note 4) R_P = 20 kΩ (Note 4)		**0.3** **0.3**	**1.3** **1.3**		**0.5** **0.4**	**1.8** **1.6**	μV/°C
TCI_{OS}	Average Input Offset Current Drift	(Note 3)		**8**	**35**		**12**	**50**	pA/°C
TCI_B	Average Input Bias Current Drift	(Note 3)		**13**	**35**		**18**	**50**	pA/°C

Electrical Characteristics

Unless otherwise specified, $V_S = \pm 15V$, $T_A = 25°C$. **Boldface** type refers to limits over $0°C \leq T_A \leq +70°C$

Symbol	Parameter	Conditions	OP-07D			Units
			Min	Typ	Max	
V_{OS}	Input Offset Voltage	(Note 1)		60 **85**	150 **250**	μV
$V_{OS/t}$	Long-Term V_{OS} Stability	(Note 2)		0.5	3.0	μV/Mo
I_{OS}	Input Offset Current			0.8 **1.6**	6.0 **8.0**	nA
I_B	Input Bias Current			±2.0 ±**3.0**	±12.0 ±**14.0**	nA
e_{np-p}	Input Noise Voltage	0.1 Hz to 10 Hz (Note 3)		0.38	0.65	μVp-p
e_n	Input Noise Voltage Density	f_O = 10 Hz f_O = 100 Hz (Note 3) f_O = 1000 Hz		10.5 10.3 9.8	20.0 13.5 11.5	nV/√Hz
i_{np-p}	Input Noise Current	0.1 Hz to 10 Hz (Note 3)		15	35	pAp-p
i_n	Input Noise Current Density	f_O = 10 Hz f_O = 100 Hz (Note 3) f_O = 1000 Hz		0.35 0.15 0.13	0.90 0.27 0.18	pA/√Hz
R_{IN}	Input Resistance Differential-Mode	(Note 4)	7	31		MΩ
R_{INCM}	Input Resistance Common-Mode			120		GΩ
iVR	Input Voltage Range		±13	±14		V
CMRR	Common-Mode Rejection Ratio	$V_{CM} = \pm 13V$	94 **94**	110 **106**		dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 3V$ to $\pm 18V$		7 **10**	32 **51**	μV/V
A_{VO}	Large Signal Voltage Gain	$R_L \leq 2 k\Omega$, $V_O = \pm 10V$ $R_L = 2 k\Omega$, $V_O = \pm 10V$ $R_L \geq 500\Omega$, $V_O = \pm 0.5V$, V_S ±3V (Note 4)	120 **100**	400 **400** 400		V/mV
V_O	Output Voltage Swing	$R_L \geq 10 k\Omega$ $R_L \geq 2 k\Omega$ $R_L \geq 2 k\Omega$ $R_L \geq 1 k\Omega$	±12.0 ±11.5 ±**11.0**	±13.0 ±12.8 ±**12.6** ±12.0		V
SR	Slew Rate	$R_L \geq 2 k\Omega$ (Note 3)	0.1	0.3		V/μs
BW	Closed-Loop Bandwidth	$A_{VCL} = +1$ (Note 3)	0.4	0.6		MHz
RO	Output Resistance	$V_O = 0$, $I_O = 0$		60		Ω
P_d	Power Consumption	$V_S = \pm 15V$, No Load $V_S = \pm 3V$, No Load		80 4	150 8	mW
	Offset Adj. Range	$R_P = 20 k\Omega$		±4		mV
TCV_{OS}	Average Input Offset Voltage Drift Without External Trim	(Note 4)		**0.7**	**2.5**	μV/°C
$TCV_{OS}n$	With External Trim	$R_P = 20 k\Omega$ (Note 4)		**0.7**	**2.5**	μV/°C
TCI_{OS}	Average Input Offset Current Drift	(Note 3)		**12**	**50**	pA/°C
TCI_B	Average Input Bias Current Drift	(Note 3)		**18**	**50**	pA/°C

Note 1: V_{OS} is measured approximately 0.5 second after application of power.

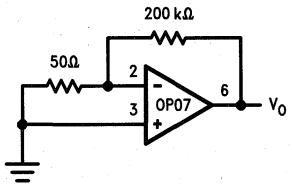
Note 2: Long-Term Offset Voltage Stability refers to the averaged trend line of V_{OS} vs Time over extended periods after the first 30 days of operation. Excluding the initial hour of operation, changes in V_{OS} during the first 30 operating days are typically 2.5 μV. Parameter is sample tested.

Note 3: Sample Tested.

Note 4: Guaranteed by design.

Test Circuits

Offset Voltage Test Circuit



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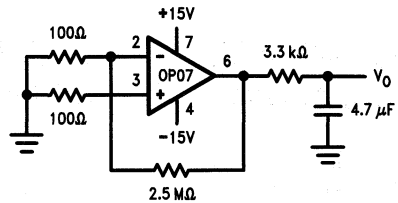
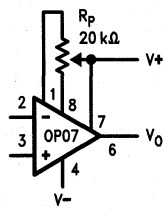
Low Frequency Noise Test Circuit



TL/H/10550–5

Optional Offset Nulling Circuit



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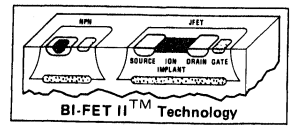
National Semiconductor



TL081 Wide Bandwidth JFET Input Operational Amplifier

General Description

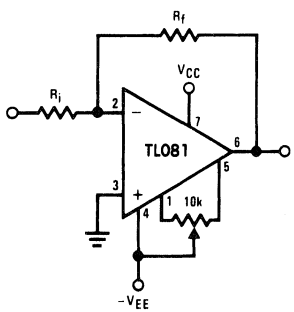
The TL081 is a low cost high speed JFET input operational amplifier with an internally trimmed input offset voltage (BI-FET II™ technology). The device requires a low supply current and yet maintains a large gain bandwidth product and a fast slew rate. In addition, well matched high voltage JFET input devices provide very low input bias and offset currents. The TL081 is pin compatible with the standard LM741 and uses the same offset voltage adjustment circuitry. This feature allows designers to immediately upgrade the overall performance of existing LM741 designs.

The TL081 may be used in applications such as high speed integrators, fast D/A converters, sample-and-hold circuits and many other circuits requiring low input offset voltage, low input bias current, high input impedance, high slew rate and wide bandwidth. The devices has low noise and offset voltage drift, but for applications where these requirements are critical, the LF356 is recommended. If maximum supply current is important, however, the TL081C is the better choice.

Features

■ Internally trimmed offset voltage	15 mV
■ Low input bias current	50 pA
■ Low input noise voltage	25 nV/$\sqrt{\text{Hz}}$
■ Low input noise current	0.01 pA/$\sqrt{\text{Hz}}$
■ Wide gain bandwidth	4 MHz
■ High slew rate	13 V/μs
■ Low supply current	1.8 mA
■ High input impedance	$10^{12}\Omega$
■ Low total harmonic distortion A_V = 10, R_L = 10k, V_O = 20 Vp-p, BW = 20 Hz–20 kHz	<0.02%
■ Low 1/f noise corner	50 Hz
■ Fast settling time to 0.01%	2 μs

Typical Connection



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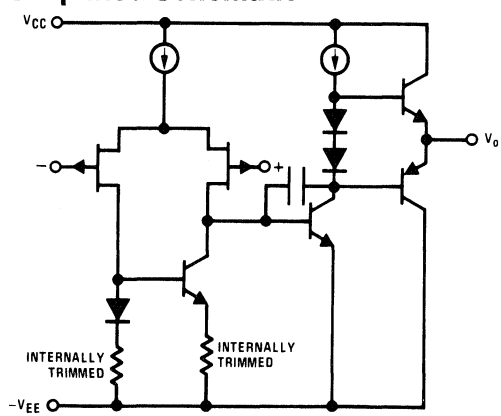
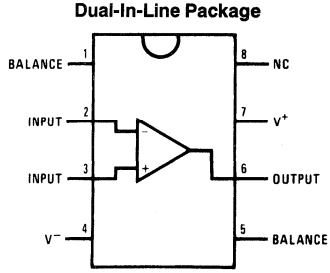
Simplified Schematic



TL/H/8358–2

Connection Diagram

Dual-In-Line Package



TL/H/8358–4

Order Number TL081CP
See NS Package Number N08E

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	±18V
Power Dissipation (Notes 1 and 6)	670 mW
Operating Temperature Range	0°C to +70°C
$T_{j(MAX)}$	115°C
Differential Input Voltage	±30V
Input Voltage Range (Note 2)	±15V
Output Short Circuit Duration	Continuous
Storage Temperature Range	−65°C to +150°C
Lead Temp. (Soldering, 10 seconds)	260°C
θ_{jA}	120°C/W

ESD rating to be determined.

DC Electrical Characteristics (Note 3)

Symbol	Parameter	Conditions	TL081C			Units
			Min	Typ	Max	
V_{OS}	Input Offset Voltage	R_S = 10 kΩ, T_A = 25°C Over Temperature		5	15 20	mV mV
$\Delta V_{OS}/\Delta T$	Average TC of Input Offset Voltage	R_S = 10 kΩ		10		µV/°C
I_{OS}	Input Offset Current	T_j = 25°C, (Notes 3, 4) $T_j \leq$ 70°C		25	100 4	pA nA
I_B	Input Bias Current	T_j = 25°C, (Notes 3, 4) $T_j \leq$ 70°C		50	200 8	pA nA
R_{IN}	Input Resistance	T_j = 25°C		10^{12}		Ω
A_{VOL}	Large Signal Voltage Gain	V_S = ±15V, T_A = 25°C V_O = ±10V, R_L = 2 kΩ Over Temperature	25 15	100		V/mV V/mV
V_O	Output Voltage Swing	V_S = ±15V, R_L = 10 kΩ	±12	±13.5		V
V_{CM}	Input Common-Mode Voltage Range	V_S = ±15V	±11	+15 −12		V V
CMRR	Common-Mode Rejection Ratio	$R_S \leq$ 10 kΩ	70	100		dB
PSRR	Supply Voltage Rejection Ratio	(Note 5)	70	100		dB
I_S	Supply Current			1.8	2.8	mA

AC Electrical Characteristics (Note 3)

Symbol	Parameter	Conditions	TL081C			Units
			Min	Typ	Max	
SR	Slew Rate	V_S = ±15V, T_A = 25°C		13		V/µs
GBW	Gain Bandwidth Product	V_S = ±15V, T_A = 25°C		4		MHz
e_n	Equivalent Input Noise Voltage	T_A = 25°C, R_S = 100Ω, f = 1000 Hz		25		nV/√Hz
i_n	Equivalent Input Noise Current	T_j = 25°C, f = 1000 Hz		0.01		pA/√Hz

Note 1: For operating at elevated temperature, the device must be derated based on a thermal resistance of 120°C/W junction to ambient for N package.

Note 2: Unless otherwise specified the absolute maximum negative input voltage is equal to the negative power supply voltage.

Note 3: These specifications apply for V_S = ±15V and 0°C ≤ T_A ≤ +70°C. V_{OS}, I_B and I_{OS} are measured at V_{CM} = 0.

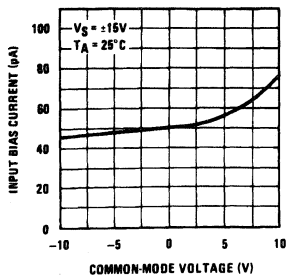
Note 4: The input bias currents are junction leakage currents which approximately double for every 10°C increase in the junction temperature, T_j. Due to the limited production test time, the input bias currents measured are correlated to junction temperature. In normal operation the junction temperature rises above the ambient temperature as a result of internal power dissipation, P_D. $T_j = T_A + \theta_{jA} P_D$ where θ_{jA} is the thermal resistance from junction to ambient. Use of a heat sink is recommended if input bias current is to be kept to a minimum.

Note 5: Supply voltage rejection ratio is measured for both supply magnitudes increasing or decreasing simultaneously in accordance with common practice from V_S = ±5V to ±15V.

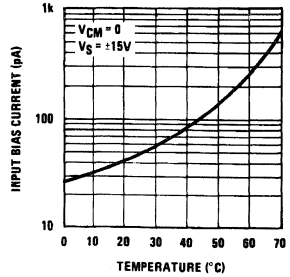
Note 6: Max. Power Dissipation is defined by the package characteristics. Operating the part near the Max. Power Dissipation may cause the part to operate outside guaranteed limits.

Typical Performance Characteristics

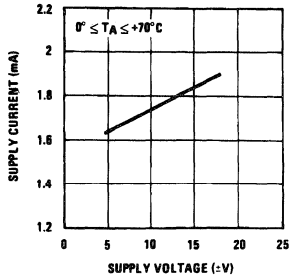
Input Bias Current



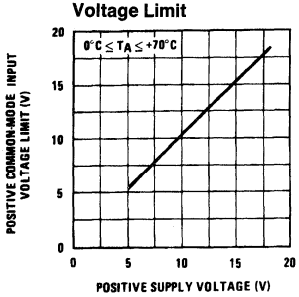
Input Bias Current



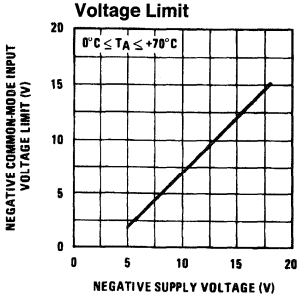
Supply Current



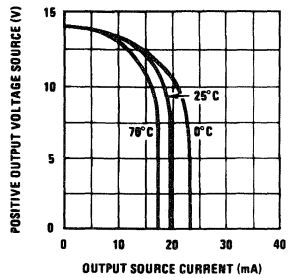
Positive Common-Mode Input Voltage Limit



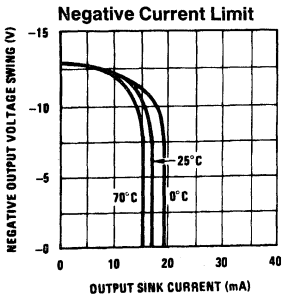
Negative Common-Mode Input Voltage Limit



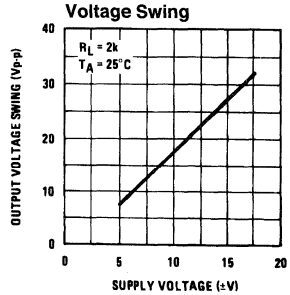
Positive Current Limit



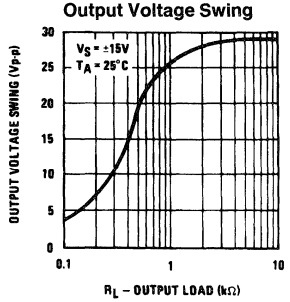
Negative Current Limit



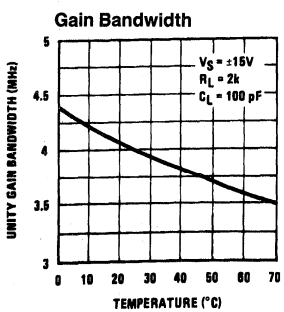
Voltage Swing



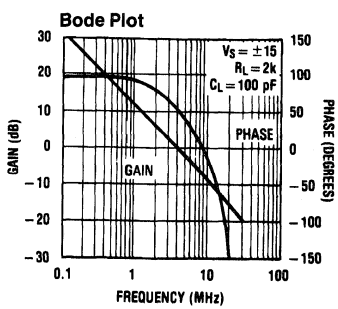
Output Voltage Swing



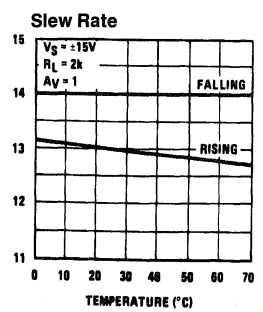
Gain Bandwidth



Bode Plot



Slew Rate



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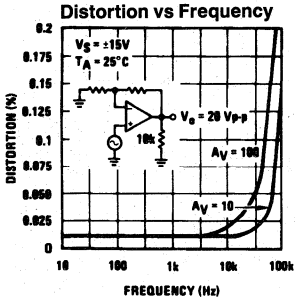
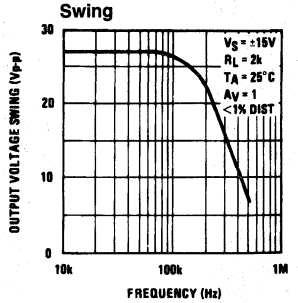
Typical Performance Characteristics (Continued)

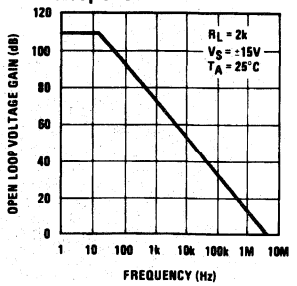
Distortion vs Frequency



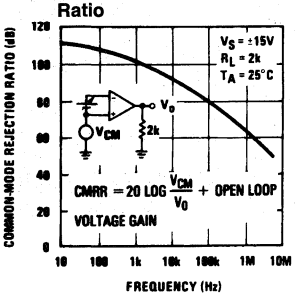
Undistorted Output Voltage Swing



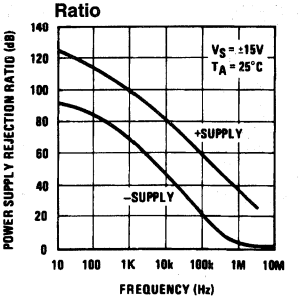
Open Loop Frequency Response



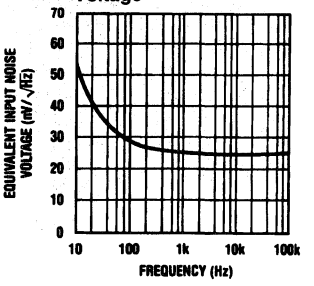
Common-Mode Rejection Ratio



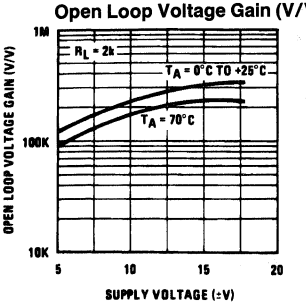
Power Supply Rejection Ratio



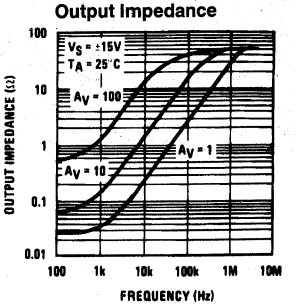
Equivalent Input Noise Voltage



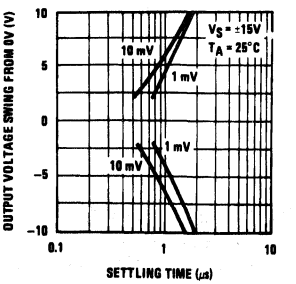
Open Loop Voltage Gain (V/V)



Output Impedance



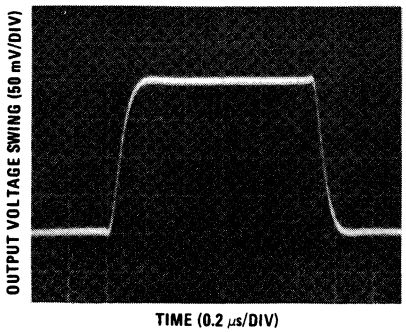
Inverter Settling Time



TL/H/8358–6

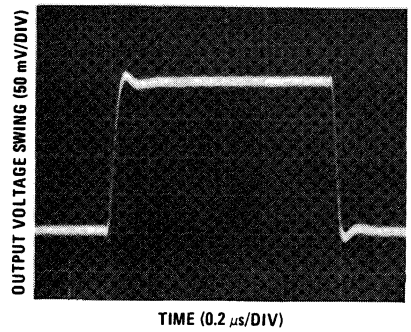
Pulse Response

Small Signal Inverting



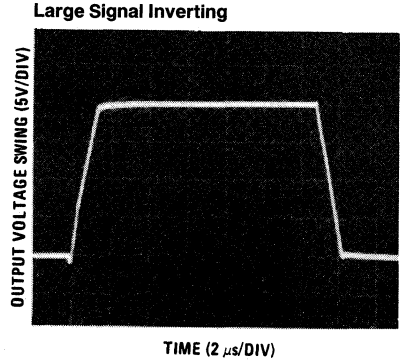
TL/H/8358-7

Small Signal Non-Inverting



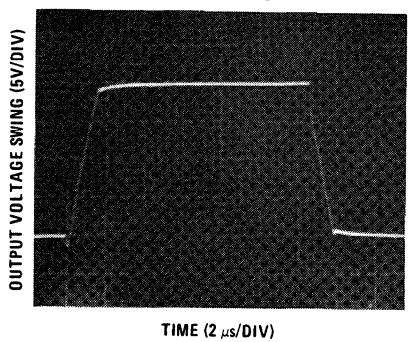
TL/H/8358-13

Large Signal Inverting



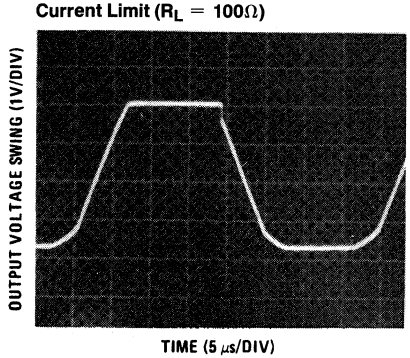
TL/H/8358-14

Large Signal Non-Inverting



TL/H/8358-15

Current Limit (R_L = 100Ω)



TL/H/8358-16

Application Hints

The TL081 is an op amp with an internally trimmed input offset voltage and JFET input devices (BI-FET II). These JFETs have large reverse breakdown voltages from gate to source and drain eliminating the need for clamps across the inputs. Therefore, large differential input voltages can easily be accommodated without a large increase in input current. The maximum differential input voltage is independent of the supply voltages. However, neither of the input voltages should be allowed to exceed the negative supply as this will cause large currents to flow which can result in a destroyed unit.

Exceeding the negative common-mode limit on either input will force the output to a high state, potentially causing a reversal of phase to the output.

Exceeding the negative common-mode limit on both inputs will force the amplifier output to a high state. In neither case does a latch occur since raising the input back within the

Application Hints (Continued)

common-mode range again puts the input stage and thus the amplifier in a normal operating mode.

Exceeding the positive common-mode limit on a single input will not change the phase of the output; however, if both inputs exceed the limit, the output of the amplifier will be forced to a high state.

The amplifier will operate with a common-mode input voltage equal to the positive supply; however, the gain bandwidth and slew rate may be decreased in this condition. When the negative common-mode voltage swings to within 3V of the negative supply, an increase in input offset voltage may occur.

The TL081 is biased by a zener reference which allows normal circuit operation on ±4V power supplies. Supply voltages less than these may result in lower gain bandwidth and slew rate.

The TL081 will drive a 2 kΩ load resistance to ±10V over the full temperature range of 0°C to +70°C. If the amplifier is forced to drive heavier load currents, however, an increase in input offset voltage may occur on the negative voltage swing and finally reach an active current limit on both positive and negative swings.

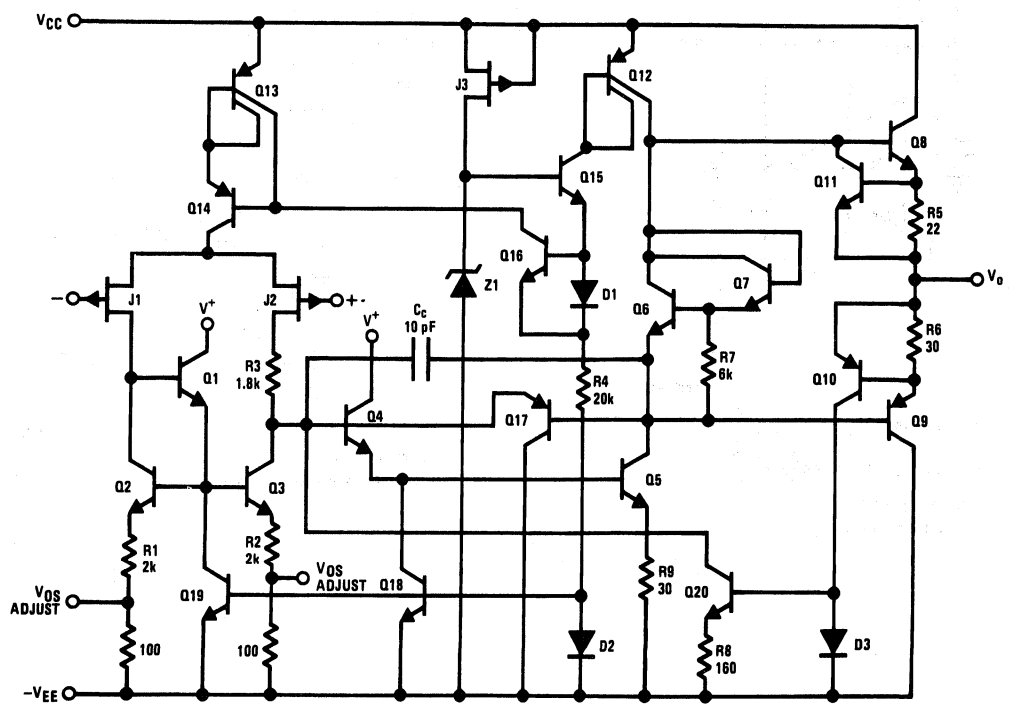
Precautions should be taken to ensure that the power supply for the integrated circuit never becomes reversed in polarity or that the unit is not inadvertently installed backwards in a socket as an unlimited current surge through the resulting forward diode within the IC could cause fusing of the internal conductors and result in a destroyed unit.

Because these amplifiers are JFET rather than MOSFET input op amps they do not require special handling.

As with most amplifiers, care should be taken with lead dress, component placement and supply decoupling in order to ensure stability. For example, resistors from the output to an input should be placed with the body close to the input to minimize "pick-up" and maximize the frequency of the feedback pole by minimizing the capacitance from the input to ground.

A feedback pole is created when the feedback around any amplifier is resistive. The parallel resistance and capacitance from the input of the device (usually the inverting input) to AC ground set the frequency of the pole. In many instances the frequency of this pole is much greater than the expected 3 dB frequency of the closed loop gain and consequently there is negligible effect on stability margin. However, if the feedback pole is less than approximately 6 times the expected 3 dB frequency a lead capacitor should be placed from the output to the input of the op amp. The value of the added capacitor should be such that the RC time constant of this capacitor and the resistance it parallels is greater than or equal to the original feedback pole time constant.

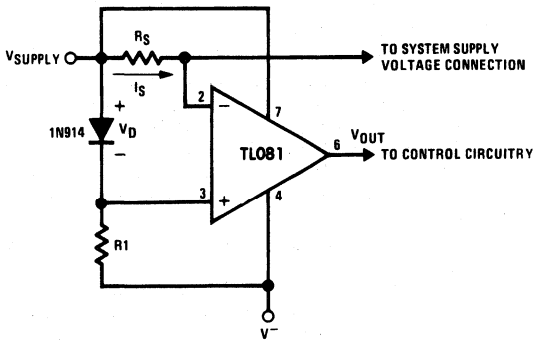
Detailed Schematic



TL/H/8358–8

Typical Applications

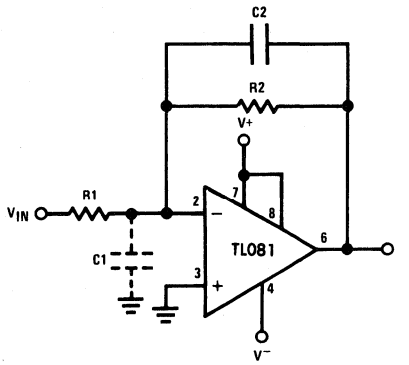
Supply Current Indicator/Limiter



TL/H/8358–9

• V_{OUT} switches high when $R_S I_S > V_D$

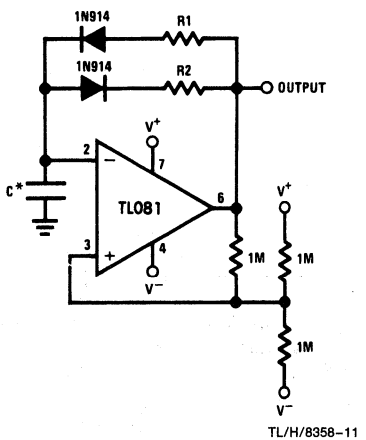
Hi-Z_{IN} Inverting Amplifier



TL/H/8358–10

Parasitic input capacitance C1 ≅ (3 pF for TL081 plus any additional layout capacitance) interacts with feedback elements and creates undesirable high frequency pole. To compensate, add C2 such that: R2C2 ≅ R1C1.

Ultra-Low (or High) Duty Cycle Pulse Generator



TL/H/8358–11

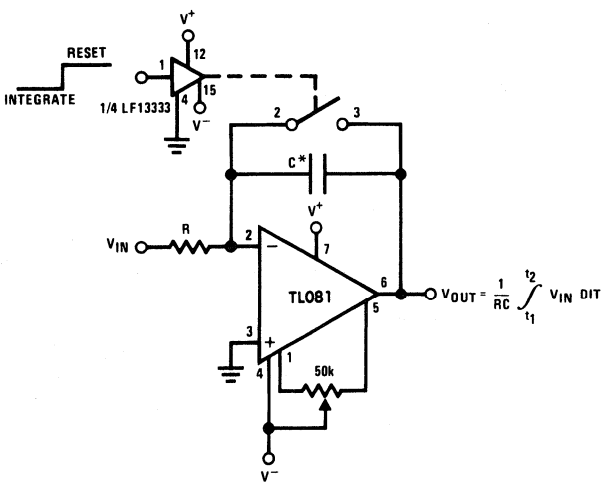
• $t_{OUTPUT\ HIGH} \approx R1C\ \ell n \frac{4.8 - 2V_S}{4.8 - V_S}$

• $t_{OUTPUT\ LOW} \approx R2C\ \ell n \frac{2V_S - 7.8}{V_S - 7.8}$

where $V_S = V^+ + |V^-|$

*low leakage capacitor

Long Time Integrator

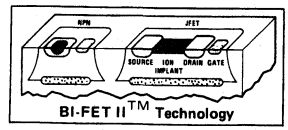


TL/H/8358–12

* Low leakage capacitor

• 50k pot used for less sensitive V_{OS} adjust

National Semiconductor



TL082 Wide Bandwidth Dual JFET Input Operational Amplifier

General Description

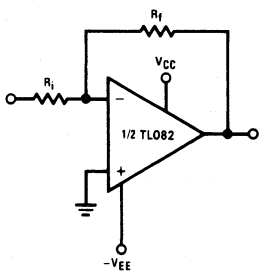
These devices are low cost, high speed, dual JFET input operational amplifiers with an internally trimmed input offset voltage (BI-FET II™ technology). They require low supply current yet maintain a large gain bandwidth product and fast slew rate. In addition, well matched high voltage JFET input devices provide very low input bias and offset currents. The TL082 is pin compatible with the standard LM1558 allowing designers to immediately upgrade the overall performance of existing LM1558 and most LM358 designs.

These amplifiers may be used in applications such as high speed integrators, fast D/A converters, sample and hold circuits and many other circuits requiring low input offset voltage, low input bias current, high input impedance, high slew rate and wide bandwidth. The devices also exhibit low noise and offset voltage drift.

Features

■ Internally trimmed offset voltage	15 mV
■ Low input bias current	50 pA
■ Low input noise voltage	16nV/√Hz
■ Low input noise current	0.01 pA/√Hz
■ Wide gain bandwidth	4 MHz
■ High slew rate	13 V/μs
■ Low supply current	3.6 mA
■ High input impedance	$10^{12}\Omega$
■ Low total harmonic distortion A_V = 10, R_L = 10k, V_O = 20 Vp − p, BW = 20 Hz−20 kHz	<0.02%
■ Low 1/f noise corner	50 Hz
■ Fast settling time to 0.01%	2 μs

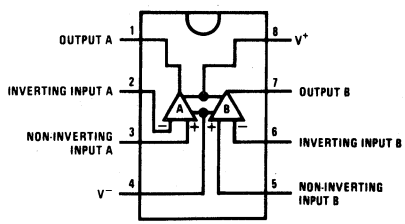
Typical Connection



TL/H/8357–1

Connection Diagram

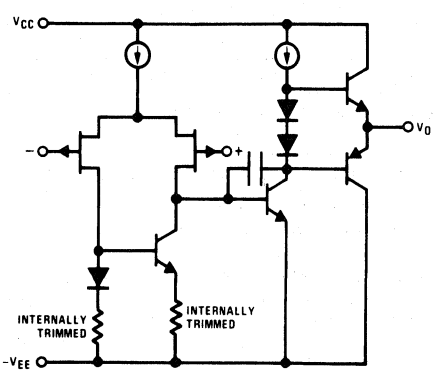
DIP/SO Package (Top View)



TL/H/8357–3

Order Number TL082CM or TL082CP
See NS Package Number M08A or N08E

Simplified Schematic



TL/H/8357–2

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	±18V
Power Dissipation	(Note 1)
Operating Temperature Range	0°C to +70°C
$T_{j(MAX)}$	150°C
Differential Input Voltage	±30V
Input Voltage Range (Note 2)	±15V
Output Short Circuit Duration	Continuous
Storage Temperature Range	−65°C to +150°C
Lead Temp. (Soldering, 10 seconds)	260°C

ESD rating to be determined.

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	TL082C			Units
			Min	Typ	Max	
V_{OS}	Input Offset Voltage	R_S = 10 kΩ, T_A = 25°C Over Temperature		5	15 20	mV mV
$\Delta V_{OS}/\Delta T$	Average TC of Input Offset Voltage	R_S = 10 kΩ		10		μV/°C
I_{OS}	Input Offset Current	T_j = 25°C, (Notes 4, 5) $T_j \leq$ 70°C		25	200 4	pA nA
I_B	Input Bias Current	T_j = 25°C, (Notes 4, 5) $T_j \leq$ 70°C		50	400 8	pA nA
R_{IN}	Input Resistance	T_j = 25°C		10^{12}		Ω
A_{VOL}	Large Signal Voltage Gain	V_S = ±15V, T_A = 25°C V_O = ±10V, R_L = 2 kΩ Over Temperature	25 15	100		V/mV V/mV
V_O	Output Voltage Swing	V_S = ±15V, R_L = 10 kΩ	±12	±13.5		V
V_{CM}	Input Common-Mode Voltage Range	V_S = ±15V	±11	+15 −12		V V
CMRR	Common-Mode Rejection Ratio	$R_S \leq$ 10 kΩ	70	100		dB
PSRR	Supply Voltage Rejection Ratio	(Note 6)	70	100		dB
I_S	Supply Current			3.6	5.6	mA

AC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	TL082C			Units
			Min	Typ	Max	
	Amplifier to Amplifier Coupling	T_A = 25°C, f = 1Hz- 20 kHz (Input Referred)		−120		dB
SR	Slew Rate	V_S = ±15V, T_A = 25°C	8	13		V/μs
GBW	Gain Bandwidth Product	V_S = ±15V, T_A = 25°C		4		MHz
e_n	Equivalent Input Noise Voltage	T_A = 25°C, R_S = 100Ω, f = 1000 Hz		25		nV/√Hz
i_n	Equivalent Input Noise Current	T_j = 25°C, f = 1000 Hz		0.01		pA/√Hz

Note 1: For operating at elevated temperature, the device must be derated based on a thermal resistance of 115°C/W junction to ambient for the N package.

Note 2: Unless otherwise specified the absolute maximum negative input voltage is equal to the negative power supply voltage.

Note 3: The power dissipation limit, however, cannot be exceeded.

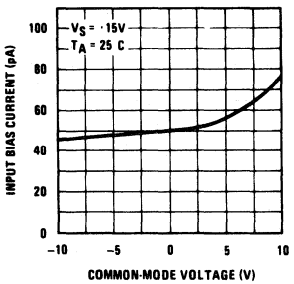
Note 4: These specifications apply for V_S = ±15V and 0°C ≤ T_A ≤ +70°C. V_{OS}, I_B and I_{OS} are measured at V_{CM} = 0.

Note 5: The input bias currents are junction leakage currents which approximately double for every 10°C increase in the junction temperature, T_j. Due to the limited production test time, the input bias currents measured are correlated to junction temperature. In normal operation the junction temperature rises above the ambient temperature as a result of internal power dissipation, P_D. $T_j = T_A + \theta_{jA} P_D$ where θ_{jA} is the thermal resistance from junction to ambient. Use of a heat sink is recommended if input bias current is to be kept to a minimum.

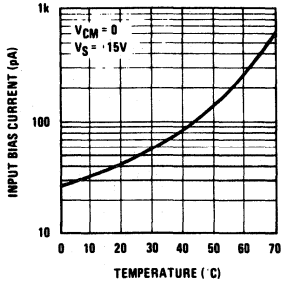
Note 6: Supply voltage rejection ratio is measured for both supply magnitudes increasing or decreasing simultaneously in accordance with common practice. V_S = ±6V to ±15V.

Typical Performance Characteristics

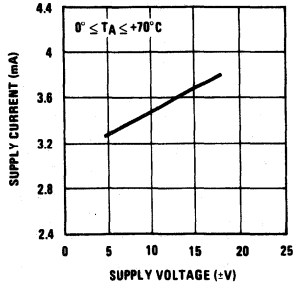
Input Bias Current



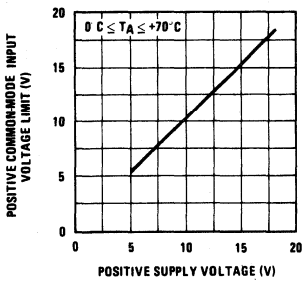
Input Bias Current



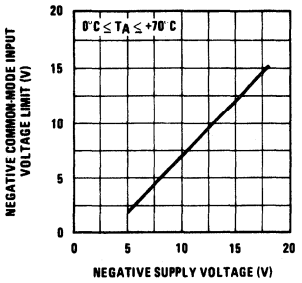
Supply Current



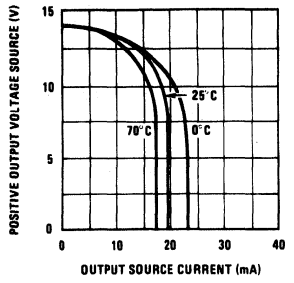
Positive Common-Mode Input Voltage Limit



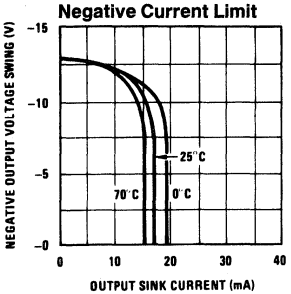
Negative Common-Mode Input Voltage Limit



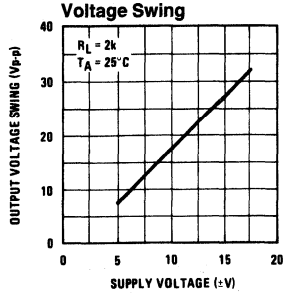
Positive Current Limit



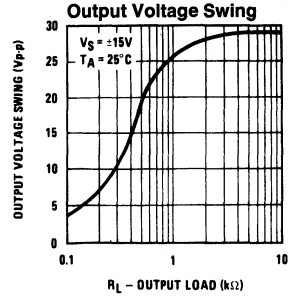
Negative Current Limit



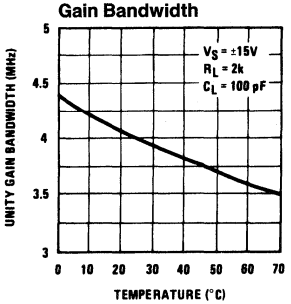
Voltage Swing



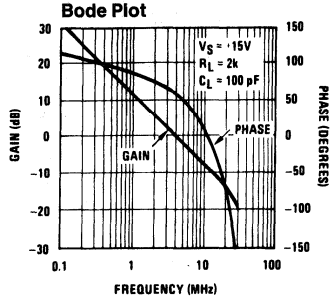
Output Voltage Swing



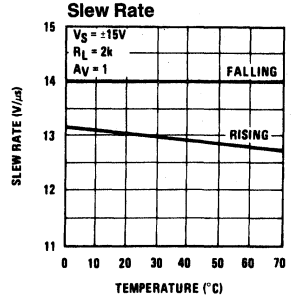
Gain Bandwidth



Bode Plot



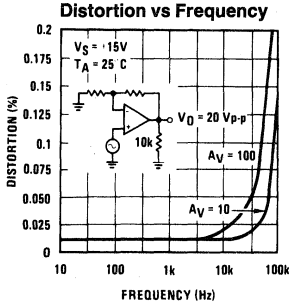
Slew Rate



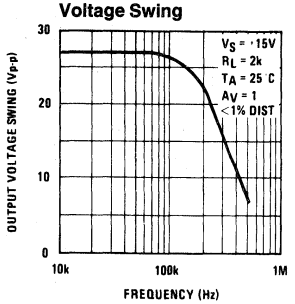
TL/H/8357–4

Typical Performance Characteristics (Continued)

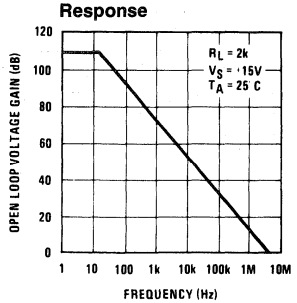
Distortion vs Frequency



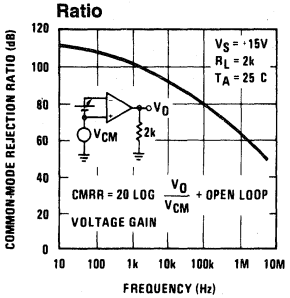
Undistorted Output Voltage Swing



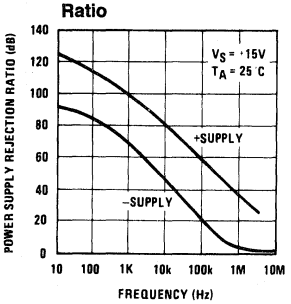
Open Loop Frequency Response



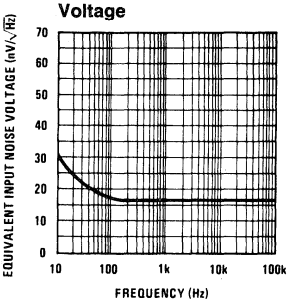
Common-Mode Rejection Ratio



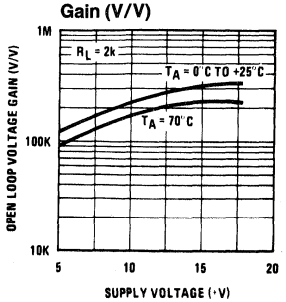
Power Supply Rejection Ratio



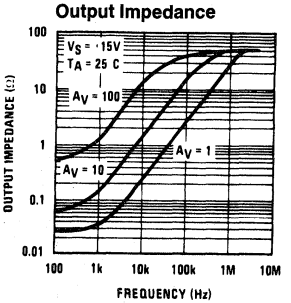
Equivalent Input Noise Voltage



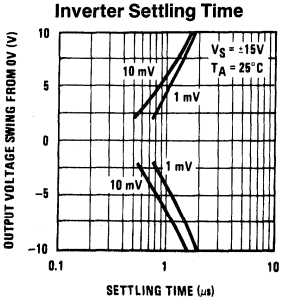
Open Loop Voltage Gain (V/V)



Output Impedance



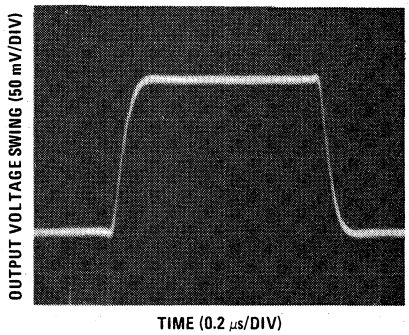
Inverter Settling Time



TL/H/8357–5

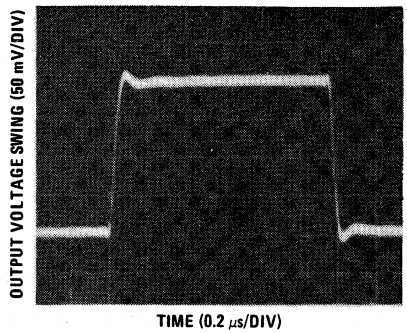
Pulse Response

Small Signal Inverting



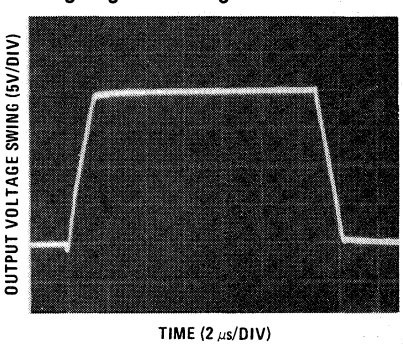
TL/H/8357–6

Small Signal Non-Inverting



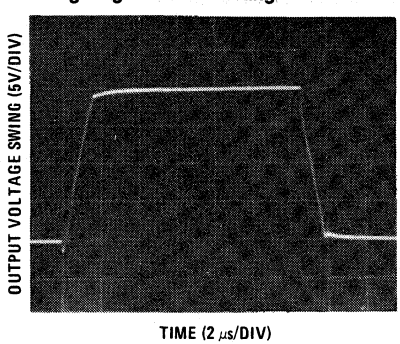
TL/H/8357–7

Large Signal Inverting



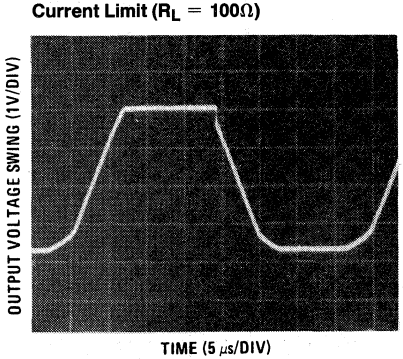
TL/H/8357–8

Large Signal Non-Inverting



TL/H/8357–9

Current Limit (R_L = 100Ω)



TL/H/8357–10

Application Hints

These devices are op amps with an internally trimmed input offset voltage and JFET input devices (BI-FET II). These JFETs have large reverse breakdown voltages from gate to source and drain eliminating the need for clamps across the inputs. Therefore, large differential input voltages can easily be accommodated without a large increase in input current. The maximum differential input voltage is independent of the supply voltages. However, neither of the input voltages should be allowed to exceed the negative supply as this will cause large currents to flow which can result in a destroyed unit.

Exceeding the negative common-mode limit on either input will cause a reversal of the phase to the output and force the amplifier output to the corresponding high or low state. Exceeding the negative common-mode limit on both inputs will force the amplifier output to a high state. In neither case

Application Hints (Continued)

does a latch occur since raising the input back within the common-mode range again puts the input stage and thus the amplifier in a normal operating mode.

Exceeding the positive common-mode limit on a single input will not change the phase of the output; however, if both inputs exceed the limit, the output of the amplifier will be forced to a high state.

The amplifiers will operate with a common-mode input voltage equal to the positive supply; however, the gain bandwidth and slew rate may be decreased in this condition. When the negative common-mode voltage swings to within 3V of the negative supply, an increase in input offset voltage may occur.

Each amplifier is individually biased by a zener reference which allows normal circuit operation on ±6V power supplies. Supply voltages less than these may result in lower gain bandwidth and slew rate.

The amplifiers will drive a 2 kΩ load resistance to ±10V over the full temperature range of 0°C to +70°C. If the amplifier is forced to drive heavier load currents, however, an increase in input offset voltage may occur on the negative voltage swing and finally reach an active current limit on both positive and negative swings.

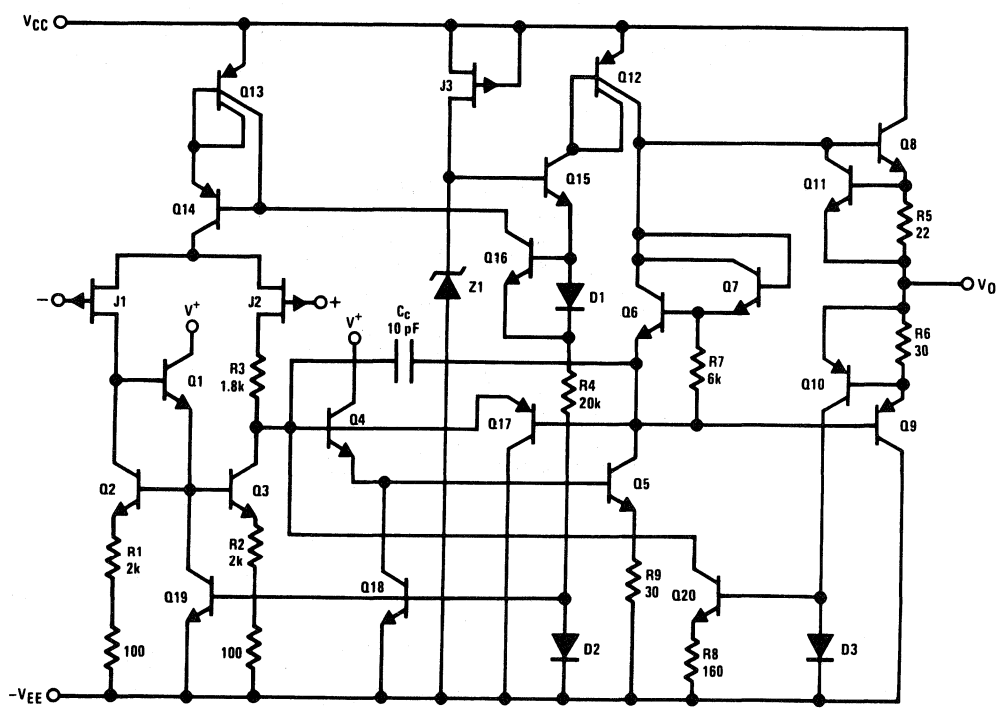
Precautions should be taken to ensure that the power supply for the integrated circuit never becomes reversed in polarity or that the unit is not inadvertently installed backwards in a socket as an unlimited current surge through the resulting forward diode within the IC could cause fusing of the internal conductors and result in a destroyed unit.

Because these amplifiers are JFET rather than MOSFET input op amps they do not require special handling.

As with most amplifiers, care should be taken with lead dress, component placement and supply decoupling in order to ensure stability. For example, resistors from the output to an input should be placed with the body close to the input to minimize "pick-up" and maximize the frequency of the feedback pole by minimizing the capacitance from the input to ground.

A feedback pole is created when the feedback around any amplifier is resistive. The parallel resistance and capacitance from the input of the device (usually the inverting input) to AC ground set the frequency of the pole. In many instances the frequency of this pole is much greater than the expected 3 dB frequency of the closed loop gain and consequently there is negligible effect on stability margin. However, if the feedback pole is less than approximately 6 times the expected 3 dB frequency a lead capacitor should be placed from the output to the input of the op amp. The value of the added capacitor should be such that the RC time constant of this capacitor and the resistance it parallels is greater than or equal to the original feedback pole time constant.

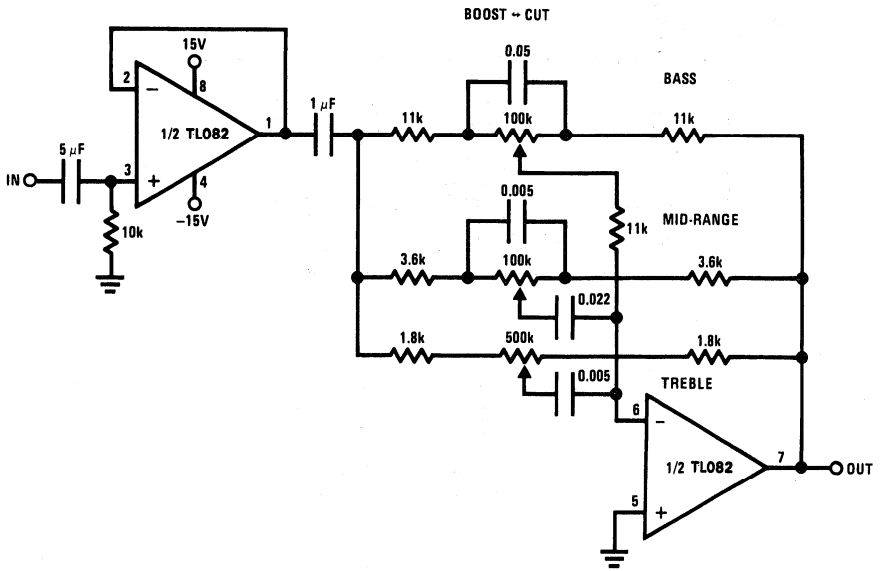
Detailed Schematic



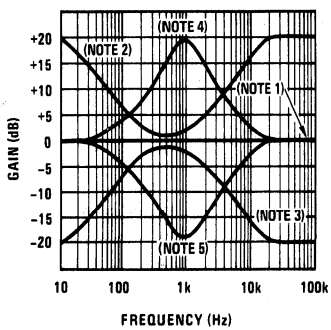
TL/H/8357–11

Typical Applications

Three-Band Active Tone Control



TL/H/8357–12



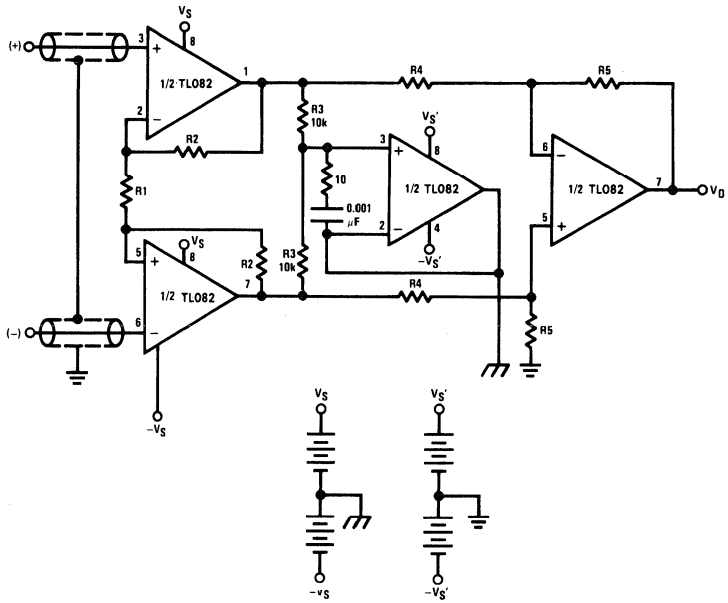
TL/H/8357–13

Note 1: All controls flat.
Note 2: Bass and treble boost, mid flat.
Note 3: Bass and treble cut, mid flat.
Note 4: Mid boost, bass and treble flat.
Note 5: Mid cut, bass and treble flat.

- All potentiometers are linear taper
- Use the LF347 Quad for stereo applications

Typical Applications (Continued)

Improved CMRR Instrumentation Amplifier



TL/H/8357–14

$$A_V = \left(\frac{2R2}{R1} + 1\right)\frac{R5}{R4}$$

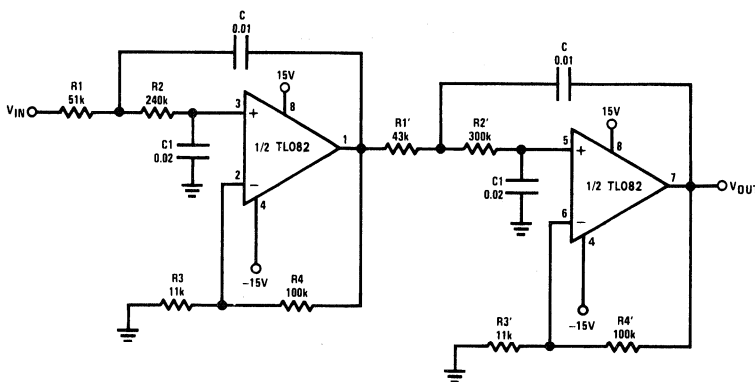
⏥ and ⏚ are separate isolated grounds

Matching of R2's, R4's and R5's control CMRR

With A_{V_T} = 1400, resistor matching = 0.01%: CMRR = 136 dB

- Very high input impedance
- Super high CMRR

Fourth Order Low Pass Butterworth Filter

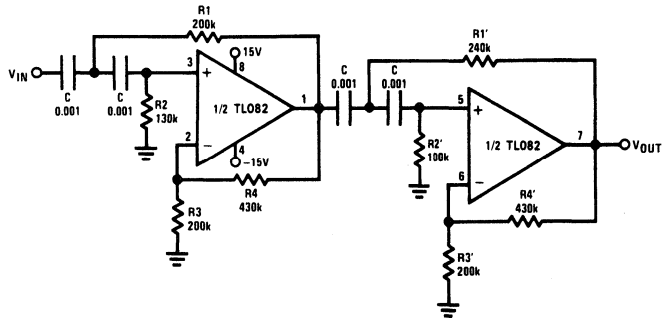


TL/H/8357–15

- Corner frequency (f_c) = $\sqrt{\frac{1}{R1R2CC1}} \cdot \frac{1}{2\pi} = \sqrt{\frac{1}{R1'R2'CC1}} \cdot \frac{1}{2\pi}$
- Passband gain (H_O) = (1 + R4/R3) (1 + R4'/R3')
- First stage Q = 1.31
- Second stage Q = 0.541
- Circuit shown uses nearest 5% tolerance resistor values for a filter with a corner frequency of 100 Hz and a passband gain of 100
- Offset nulling necessary for accurate DC performance

Typical Applications (Continued)

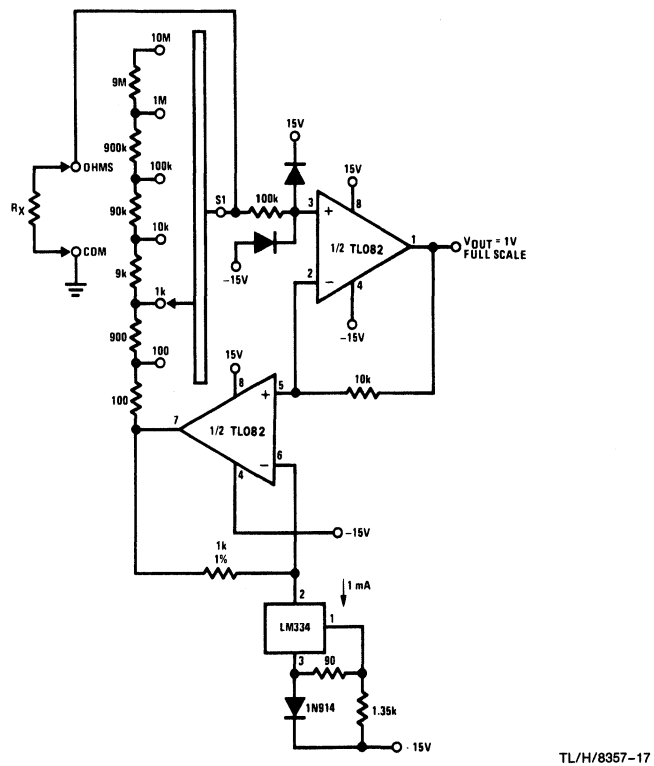
Fourth Order High Pass Butterworth Filter



TL/H/8357–16

- Corner frequency (f_c) = $\sqrt{\frac{1}{R1R2C^2}} \cdot \frac{1}{2\pi} = \sqrt{\frac{1}{R1'R2'C^2}} \cdot \frac{1}{2\pi}$
- Passband gain (H_O) = (1 + R4/R3) (1 + R4'/R3')
- First stage Q = 1.31
- Second stage Q = 0.541
- Circuit shown uses closest 5% tolerance resistor values for a filter with a corner frequency of 1 kHz and a passband gain of 10

Ohms to Volts Converter



TL/H/8357–17

$$V_O = \frac{1V}{R_{LADDER}} \times R_X$$

Where R_{LADDER} is the resistance from switch S1 pole to pin 7 of the TL082CP.

Section 2

Buffers

Section 2 Contents

National Semiconductor

Buffers
Definition of Terms

Bandwidth: That frequency at which the voltage gain is reduced to $1/\sqrt{2}$ times the low frequency value.

Harmonic Distortion: That percentage of harmonic distortion being defined as one-hundred times the ratio of the root-mean-square (rms) sum of the harmonics to the fundamental.

$$\%\ \text{harmonic distortion} = \frac{(V2^2 + V3^2 + V4^2 + \ldots)^{1/2}\,(100\%)}{V1}$$

where V1 is the rms amplitude of the fundamental and V2, V3, V4, . . . are the rms amplitudes of the individual harmonics.

Input Impedance: The ratio of input voltage to input current under the stated conditions for source resistance (R_S) and load resistance (R_L).

Input Offset Voltage: That voltage which must be applied to the input terminal to obtain zero output voltage.

Input Resistance: The ratio of the change in input voltage to the change in input current.

Input Voltage Range: The range of voltages on the input terminal for which the buffer operates within specifications.

Large-Signal Voltage Gain: The ratio of the output voltage swing to the change in input voltage.

Output Impedance: The ratio of change in output voltage to output current under the stated conditions.

Output Resistance: The small signal resistance seen at the output with the output voltage near zero.

Output Voltage Swing: The peak output voltage swing, referred to zero, that can be obtained without clipping.

Offset Voltage Temperature Drift: The average drift rate of offset voltage for a thermal variation from room temperature to the indicated temperature extreme.

Power Supply Rejection: The ratio of the change in input offset voltage to the change in power supply voltages producing it.

Settling Time: The time between the initiation of the input step function and the time when the output voltage has settled to within a specified error band of the final output voltage.

Slew Rate: The internally-limited rate of change in output voltage with a large-amplitude step function applied to the input.

Supply Current: The current required from the power supply to operate the buffer with no load and the output midway between the supplies.

Transient Response: The closed-loop step-function response of the amplifier under small-signal conditions.

Voltage Gain: The ratio of output voltage to input voltage under the stated conditions for source resistance (R_S) and load resistance (R_L).

National Semiconductor

Buffer Selection Guide (Notes 1 and 2)

Device Type	Key Features	Slew Rate (V/μs)	Bandwidth −3 dB (MHz)	Gain (A_V)	Output (V, mA)	Full Power BW (MHz @ V_{PP}, R_L)	Test Conditions
LH0063	FET Input, Very Fast	2400	200	0.93	±13, ±260	40 @ 20, 50	R_L = 50, V_S = ±15V
LH0033	FET Input, High Speed	1500	100	0.98	±9, ±90	24 @ 20, 1k	R_L = 1k, V_S = ±15V
LH4002	Wideband Video Buffer	1250	200	0.97	±2.2, ±44	100 @ 4, 50	R_L = 50, V_S = ±5V
LH2003/2033	Wideband Video Buffer	1200	100	0.9	±11.3, ±113	2 @ 20, 100	R_L = 1k, 50, V_S = ±15
LM6121/6125	High Speed VIP™ Buffer	800	50	0.90	±12, ±240	10.6 @ 12, 50	R_L = 50, V_S = ±15V
LH0002	Medium Speed	200	30	0.97	±10, ±100	3 @ 20, 1k	R_L = 1k, V_S = ±12V
LH4001	Low Cost LH0002	125	25	0.97	±10, ±100	4 @ 10, 100	R_L = 100, V_S = ±12V
LM110, 210, 310	Voltage Follower	30	20	0.9999	±10, ±10	0.5 @ 20, 10k	R_L = 10k, V_S = ±15V

Note 1: Datasheet should be referred to for test conditions and more detailed information.

Note 2: 200°C Temp Range Parts are available. Consult local sales office for information.

National Semiconductor

LH0002 Buffer

General Description

The LH0002 is a general purpose buffer. Its features make it ideal to integrate with operational amplifiers inside a closed loop configuration to increase current output. The symmetrical output portion of the circuit also provides a low output impedance for both the positive and negative slopes of output pulses.

The LH0002 is available in an 8-lead TO-99 can. The LH0002C is available in an 8-lead TO-99, and a 10-pin molded dual-in-line package.

The LH0002 is specified for operation over the −55°C to +125°C military temperature range. The LH0002C is specified for operation over the 0°C to +85°C temperature range.

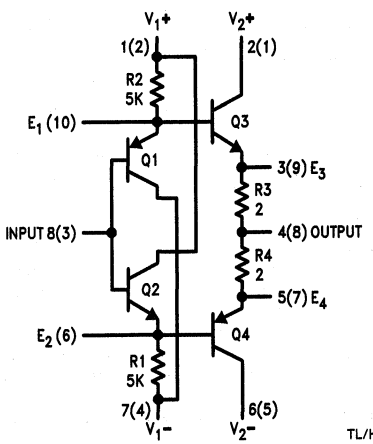
Features

- High input impedance 400 kΩ
- Low output impedance 6Ω
- High power efficiency
- Low harmonic distortion
- DC to 30 MHz bandwidth
- Output voltage swing that approaches supply voltage
- 400 mA pulsed output current
- Slew rate is typically 200 V/μs
- Operation from ±5V to ±20V

Applications

- Line driver
- 30 MHz buffer
- High speed D/A conversion

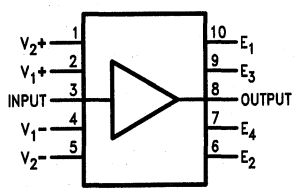
Schematic and Connection Diagrams



TL/H/5560–1

Pin numbers in parentheses denote pin connections for dual-in-line package.

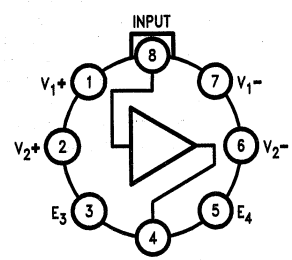
Dual-In-Line Package



TL/H/5560–2

Order Number LH0002CN
See NS Package Number N10A

Metal Can Package



TL/H/5560–3

Order Number LH0002H,
LH0002H-MIL or LH0002CH
LH0002H/883*
See NS Package Number H08D

*Available per SMD #7801301

Absolute Maximum Ratings (Note 3)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications. (Note 2)

Supply Voltage	±22V
Power Dissipation (Note 4)	600 mW
Input Voltage	(Equal to Power Supply Voltage)
Storage Temperature Range	−65°C to +150°C
Junction Temperature	
N Package	+150°C
H Package	+175°C
Steady State Output Current	±100 mA
Pulsed Output Current (50 ms On/1 sec. Off)	±400 mA
Lead Temperature Soldering (10 seconds)	
Metal Can	300°C
Plastic	260°C
ESD Rating (Note 6)	2 kV

Operating Ratings (Note 3)

Temperature Range	
LH0002	−55°C to +125°C
LH0002C	0°C to +85°C
Thermal Resistance (Note 5)	
θ_{JA}, H Package	+125°C/W
θ_{JC}, H Package	+75°C/W
θ_{JA}, N Package	+120°C/W

Electrical Characteristics (Note 1)

Parameter	Conditions	Min	Typ	Max	Units
Voltage Gain	R_S = 10 kΩ, R_L = 1.0 kΩ, V_{IN} = ±10V	0.95	0.97		
Input Impedance	R_S = 200 kΩ, V_{IN} = ±1.0V, R_L = 1.0 kΩ	180	400		kΩ
Output Impedance	V_{IN} = ±1.0V, R_L = 50Ω, R_S = 10 kΩ		6.0	10	Ω
Output Voltage Swing	R_L = 1.0 kΩ, V_{IN} = ±12V	±10	±11		V
Output Voltage Swing	V_S = ±15V, V_{IN} = ±12V, R_S = 50Ω, R_L = 100Ω, T_A = 25°C	±10			V
DC Output Offset Voltage	R_S = 300Ω, R_L = 1.0 kΩ		±10	±30	mV
DC Input Bias Current	R_S = 10 kΩ, R_L = 1.0 kΩ		±6.0	±10	μA
Harmonic Distortion	V_{IN} = 5.0 Vrms, f = 1.0 kHz		0.1		%
Rise Time	R_L = 50Ω, ΔV_{IN} = 100 mV		7.0	12	ns
Positive Supply Current	R_S = 10 kΩ, R_L = 1.0 kΩ		+6.0	+10	mA
Negative Supply Current	R_S = 10 kΩ, R_L = 1.0 kΩ		−6.0	−10	mA

Note 1: Specification applies for T_A = 25°C with +12V on Pins 1 and 2; −12V on Pins 6 and 7 for the metal can package and +12V on Pins 1 and 2; −12V on Pins 4 and 5 for the dual-in-line package, unless otherwise specified. The parameter guarantees for LH0002C apply over the temperature range of 0°C to +85°C, while parameters for the LH0002 are guaranteed over the temperature range −55°C to +125°C unless otherwise specified.

Note 2: Refer to RETS0002X for LH0002 military specifications.

Note 3: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed.

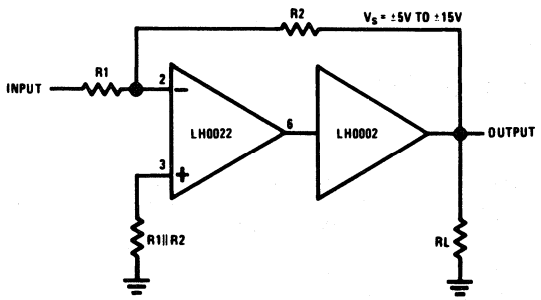
Note 4: The maximum power dissipation is a function of maximum junction temperature (T_JMax), total thermal resistance (θ_{JA}), and ambient temperature (T_A). The maximum allowable power dissipation at any ambient is $P_D = (T_J\text{Max} - T_A)/\theta_{JA}$.

Note 5: For operating at elevated temperatures, the device must be derated based on the thermal resistance θ_{JA} and T_JMax. $T_J = T_A + P_D\theta_{JA}$.

Note 6: Human body model, 1.5 kΩ in series with 100 pF.

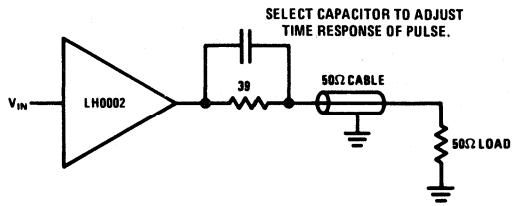
Typical Applications

High Current Operational Amplifier



TL/H/5560–4

Line Driver

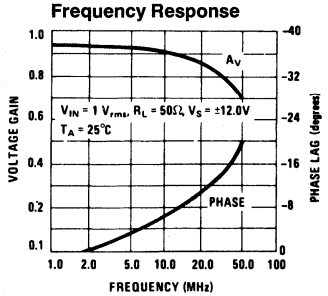


*Previously called NH0002/NH0002C

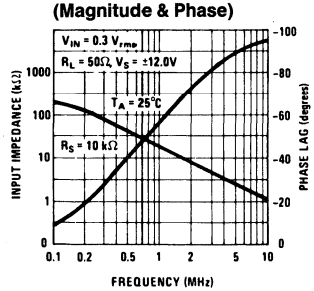
TL/H/5560–5

Typical Performance Characteristics

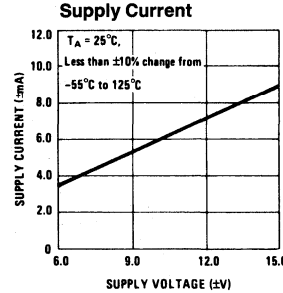
Frequency Response



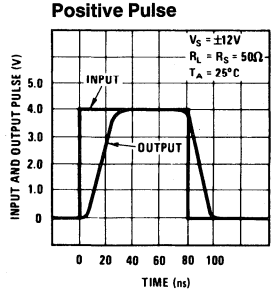
Input Impedance (Magnitude & Phase)



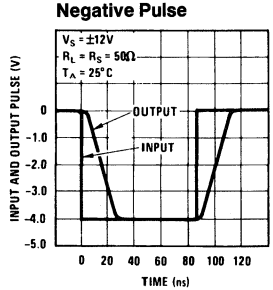
Supply Current



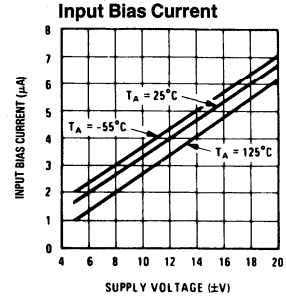
Positive Pulse



Negative Pulse



Input Bias Current



TL/H/5560–7

National Semiconductor

LH0033/LH0063
Fast and Ultra Fast Buffers

General Description

The LH0033 and LH0063 are high speed, FET input, voltage follower/buffers designed to provide high current drive at frequencies from DC to over 100 MHz. The LH0033 will provide ±10 mA into 1 kΩ loads (±100 mA peak) at slew rates of 1500V/μs. The LH0063 will provide ±250 mA into 50Ω loads (±500 mA peak) at slew rates up to 6000V/μs. In addition, both exhibit excellent phase linearity up to 20 MHz.

Both are intended to fulfill a wide range of buffer applications such as high speed line drivers, video impedance transformation, nuclear instrumentation amplifiers, op amp isolation buffers for driving reactive loads and high impedance input buffers for high speed A to Ds and comparators. In addition, the LH0063 can continuously drive 50Ω coaxial cables or be used as a yoke driver for high resolution CRT displays. For additional applications information, see AN-48.

These devices are constructed using specially selected junction FETs and active laser trimming to achieve guaranteed performance specifications. The LH0033 is specified for operation from −55°C to +125°C; the LH0033C and the LH0063C are specified from −25°C to +85°C. The LH0033 is available in either a 1.5W metal TO-8 package or an 8-pin ceramic dual-in-line package. The LH0063 is available in a 5W 8-pin TO-3 package.

Features

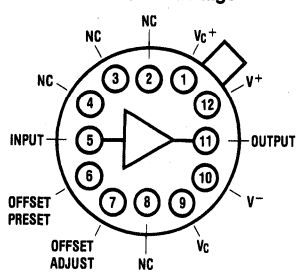
- Ultra fast (LH0063): 6000 V/μs
- Wide range single or dual supply operation
- Wide power bandwidth: DC to 100 MHz
- High output drive: ±10V with 50Ω load
- Low phase non-linearity: 2 degrees
- Fast rise times: 2 ns
- High input resistance: $10^{10}\Omega$

Advantages

- Only 10V supply needed for 5 Vp-p video out
- Speed does not degrade system performance
- Wide data rate range for phase encoded systems

Connection Diagrams

LH0033G
Metal Can Package



TOP VIEW

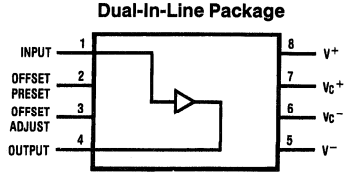
TL/K/5507–1

Case is electrically isolated

Order Number LH0033G, LH0033G-MIL, LH0033CG or LH0033G/883*
See NS Package Number G12B

*Available per SMD #8001401

LH0033J
Dual-In-Line Package

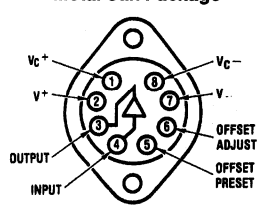


TOP VIEW

TL/K/5507–2

Order Number LH0033J or LH0033CJ
See NS Package Number HY08A

LH0063K
Metal Can Package



TL/K/5507–3

Top View

Case is electrically isolated

Order Number LH0063CK
See NS Package Number K08A

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage ($V^+ - V^-$)	40V
Power Dissipation (See Curves)	
LH0063C	5W
LH0033/LH0033C	2.2W
Junction Temperature	175°C
Input Voltage	$\pm V_S$
Continuous Output Current	
LH0063C	±250 mA
LH0033/LH0033C	±100 mA
Peak Output Current	
LH0063C	±500 mA
LH0033/LH0033C	±250 mA
Lead Temp. (Soldering, 10 seconds)	300°C

Operating Temperature Range

LH0033	−55°C to +125°C
LH0033C and LH0063C	−25°C to +85°C
Storage Temperature Range	−65° to +150°C

ESD rating to be determined.

DC Electrical Characteristics

$V_S = \pm 15V$, $T_{MIN} \leq T_A \leq T_{MAX}$, unless otherwise specified, (Note 1)

Parameter	Conditions	LH0033			LH0033C			Units
		Min	Typ	Max	Min	Typ	Max	
Output Offset Voltage	$R_S = 100\Omega$, $T_J = 25°C$, $V_{IN} = 0V$ (Note 2)		5.0	10		12	20	mV
	$R_S = 100\Omega$			15			25	mV
Average Temperature Coefficient of Offset Voltage	$R_S = 100\Omega$, $V_{IN} = 0V$ (Note 3)		50	100		50	100	μV/°C
Input Bias Current	$V_{IN} = 0V$							
	$T_J = 25°C$ (Note 2)			250			500	pA
	$T_A = 25°C$ (Note 4)			2.5			5.0	nA
	$T_J = T_A = T_{MAX}$			10			20	nA
Voltage Gain	$V_O = \pm 10V$, $R_S = 100\Omega$, $R_L = 1.0k\Omega$	0.97	0.98	1.00	0.96	0.98	1.00	V/V
Input Impedance	$R_L = 1\ k\Omega$	10^{10}	10^{11}		10^{10}	10^{11}		Ω
Output Impedance	$V_{IN} = \pm 1.0V$, $R_L = 1.0k$		6.0	10		6.0	10	Ω
Output Voltage Swing	$V_I = \pm 14V$, $R_L = 1.0k$	±12			±12			V
	$V_I = \pm 10.5V$, $R_L = 100\Omega$, $T_A = 25°C$	±9.0			±9.0			V
Supply Current	$V_{IN} = 0V$ (Note 5)		20	22		21	24	mA
Power Consumption	$V_{IN} = 0V$		600	660		630	720	mW

AC Electrical Characteristics

$T_J = 25°C$, $V_S = \pm 15V$, $R_S = 50\Omega$, $R_L = 1.0\ K\Omega$ (Note 6)

Parameter	Conditions	LH0033			LH0033C			Units
		Min	Typ	Max	Min	Typ	Max	
Slew Rate	$V_{IN} = \pm 10V$	1000	1500		1000	1400		V/μs
Bandwidth	$V_{IN} = 1.0$ Vrms		100			100		MHz
Phase Non-Linearity	BW = 1.0Hz to 20 MHz		2.0			2.0		degrees
Rise Time	$\Delta V_{IN} = 0.5V$		2.9			3.2		ns
Propagation Delay	$\Delta V_{IN} = 0.5V$		1.2			1.5		ns
Harmonic Distortion	f > 1 kHz		<0.1			<0.1		%

Note 1: LH0033 is 100% production tested as specified at 25° C, 125°C, and−55°C. LH0033AC/C are 100% production tested at 25°C only. Specifications at temperature extremes are verified by sample testing, but these limited are not used to calculate outgoing quality level.

Note 2: Specification is at 25°C junction temperature due to requirements of high speed automatic testing. Actual values at operating temperature will exceed the value at $T_J = 25°C$. When supply voltages are ±15V, no-load operating junction temperature may rise 40-60°C above ambient, and more under load conditions. Accordingly, V_{OS} may change one to several mV, and I_B will change significantly during warm-up. Refer to I_B vs temperature graph for expected values.

Note 3: LH0033 is 100% production tested for this parameter. LH0033C is sample tested only. Limits are not used to calculate outgoing quality levels. $\Delta V_{OS}/\Delta T$ is the average value calculated from measurements at 25°C and T_{MAX}.

Note 4: Measured in still air 7 minutes after application of power. Guaranteed through correlated automatic pulse testing.

Note 5: Guaranteed through correlated automatic pulse testing at $T_J = 25°C$.

Note 6: Not 100% production tested; verified by sample testing only. Limits are not used to calculate outgoing quality level.

Note 7: Refer to RETS0033 for the LH0033G military specifications.

DC Electrical Characteristics $V_S = \pm 15V$, $T_{MIN} \leq T_A \leq T_{MAX}$ unless otherwise specified (Note 1)

Parameter	Conditions	LH0063C			Units
		Min	Typ	Max	
Output Offset Voltage	$R_S \leq 100k\Omega$, $T_J = 25°C$, $R_L = 100\Omega$ (Note 2)		10	50	mV
				100	mV
Average Temperature Coefficient of Output Offset Voltage	$R_S \leq 100\ k\Omega$		300		$\mu V/°C$
Input Bias Current	$T_J = 25°C$ (Note 2)		10	30	nA
				100	nA
Voltage Gain	$V_{IN} = \pm 10V$, $R_S \leq 100\ k\Omega$, $R_L = 1\ k\Omega$	0.94	0.96	1.0	V/V
Voltage Gain	$V_{IN} = \pm 10V$, $R_S \leq 100\ k\Omega$, $R_L = 50\Omega$ $T_J = 25°C$	0.91	0.93	0.98	V/V
Input Capacitance	Case Shorted to Output		8.0		pF
Output Impedance	$V_{OUT} = \pm 10V$, $R_S \leq 100\ k\Omega$, $R_L = 50\Omega$		1.0	4.0	Ω
Output Current Swing	$V_{IN} = \pm 10V$, $R_S \leq 100\ k\Omega$	0.2	0.25		A
Output Voltage Swing	$R_L = 50\Omega$	± 10	± 13		V
Output Voltage Swing	$V_S = \pm 5.0V$, $R_L = 50\Omega$, $T_J = 25°C$	5.09	7.0		Vp-p
Supply Current	$T_J = 25°C$, $R_L = \infty$, $V_S = \pm 15V$		50	65	mA
Supply Current	$V_S = \pm 5.0V$		40		mA
Power Consumption	$T_J = 25°C$, $R_L = \infty$, $V_S = \pm 15V$		1.5	1.95	W
Power Consumption	$V_S = \pm 5.0V$		400		mW

AC Electrical Characteristics $T_J = 25°C$, $V_S = \pm 15V$, $R_S = 50\Omega$, $R_L = 50\Omega$ (Note 3)

Parameter	Conditions	LH0063C			Units
		Min	Typ	Max	
Slew Rate	$R_L = 1.0\ k\Omega$, $V_{IN} = \pm 10V$		6000		$V/\mu s$
Slew Rate	$R_L = 50\Omega$, $V_{IN} = \pm 10V$, $T_J = 25°C$	2000	2400		$V/\mu s$
Bandwidth	$V_{IN} = 1.0$ Vrms		200		MHz
Phase Non-Linearity	BW = 1.0 Hz to 20 MHz		2.0		degrees
Rise Time	$\Delta V_{IN} = 0.5V$		1.9		ns
Propagation Delay	$\Delta V_{IN} = 0.5V$		2.1		ns
Harmonic Distortion			<0.1		%

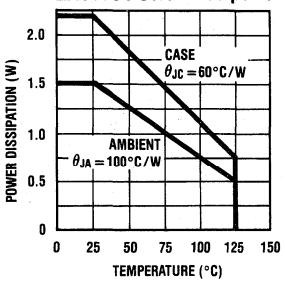
Note 1: LH0063C is 100% production tested at 25°C only. Specifications at temperature extremes are verified by sample testing, but these limits are not used to calculate outgoing quality level.

Note 2: Specification is at 25°C junction temperature due to requirements of high speed automatic testing. Actual values at operating temperature will exceed the value at $T_J = 25°C$. When supply voltages are $\pm 15V$, no-load operating junction temperature may rise 40-60°C above ambient, and more under load conditions. Accordingly, V_{OS} may change one to several mV, and I_B will change significantly during warm-up. Refer to I_B vs temperature graph for expected values.

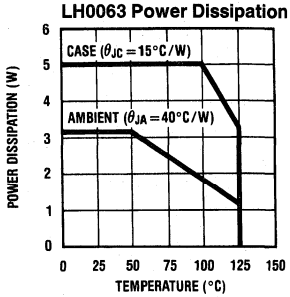
Note 3: Not 100% production tested; verified by sample testing only. Limits are not used to calculate outgoing quality level.

Typical Performance Characteristics

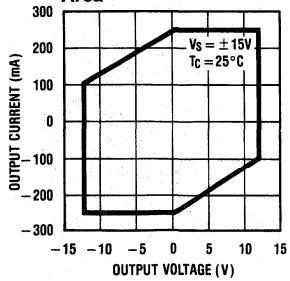
LH0033 Power Dissipation



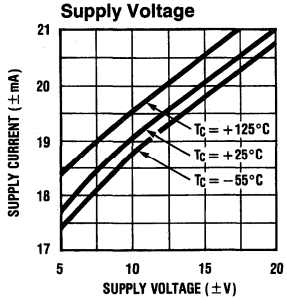
LH0063 Power Dissipation



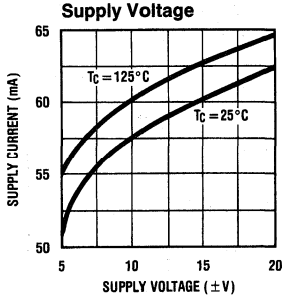
LH0063 DC Safe Operating Area



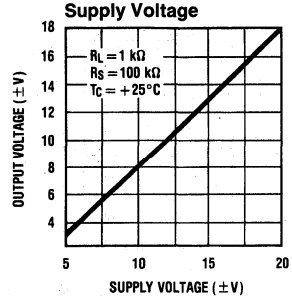
LH0033 Supply Current vs Supply Voltage



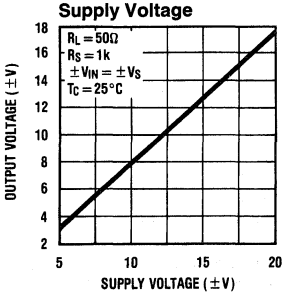
LH0063 Supply Current vs Supply Voltage



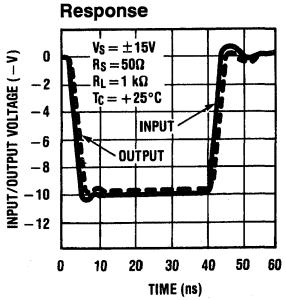
LH0033 Output Voltage vs Supply Voltage



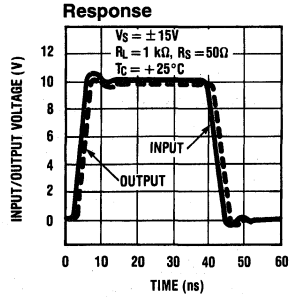
LH0063 Output Voltage vs Supply Voltage



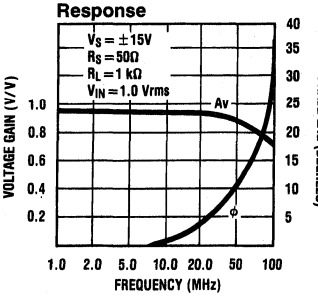
LH0033 Negative Pulse Response



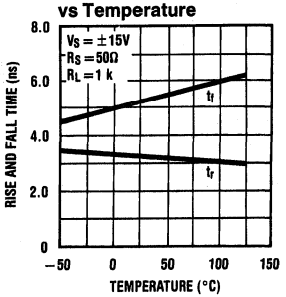
LH0033 Positive Pulse Response



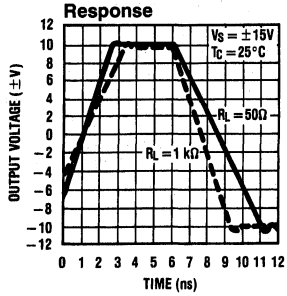
LH0033 Frequency Response



LH0033 Rise and Fall Time vs Temperature



LH0063 Large Signal Pulse Response



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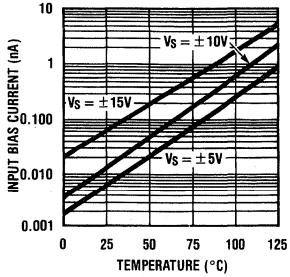
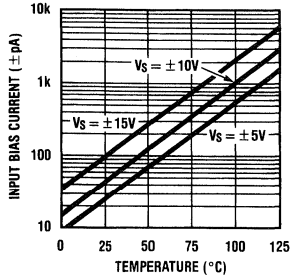
2

Typical Performance Characteristics (Continued)

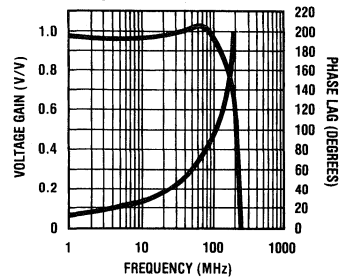
LH0033 Input Bias Current vs Temperature



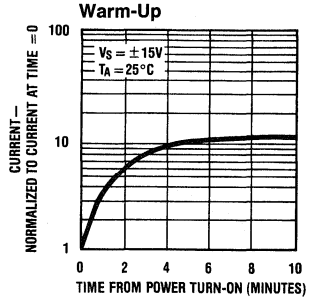
LH0063 Input Current



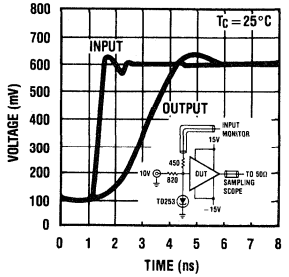
LH0063 Frequency Response



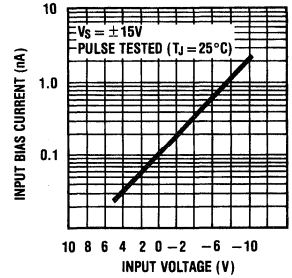
LH0033 Normalized Input Bias Current During Warm-Up



LH0063 Small Signal Rise Time



LH0033 Input Bias Current vs Input Voltage



TL/K/5507–5

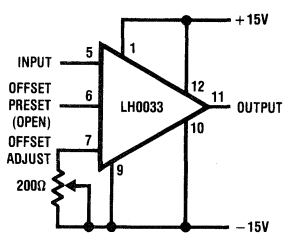
Application Hints

RECOMMENDED LAYOUT PRECAUTIONS

RF/video printed circuit board layout rules should be followed when using the LH0033 and LH0063 since they will provide power gain to frequencies over 100 MHz. Ground planes are recommended and power supplies should be decoupled at each device with low inductance capacitors. In addition, ground plane shielding may be extended to the metal case of the device since it is electrically isolated from internal circuitry. Alternatively the case should be connected to the output to minimize input capacitance.

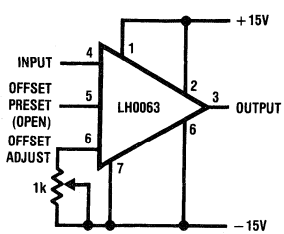
OFFSET VOLTAGE ADJUSTMENT

Both the LH0033's and LH0063's offset voltages have been actively trimmed by laser to meet guaranteed specifications when the offset preset pin is shorted to the offset adjust pin. This pre-calibration allows the devices to be used in most DC or AC applications without individually offset nulling each device. If offset null is desirable, it is simply obtained by leaving the offset preset pin open and connecting a trim pot of 100Ω for the LH0033 or 1 kΩ for the LH0063 between the offset adjust pin and V^-, as illustrated in *Figures 1* and *2*.



TL/K/5507–6

FIGURE 1. Offset Zero Adjust for LH0033 (Pin numbers shown for TO-8)



TL/K/5507–7

FIGURE 2. Offset Zero Adjust for LH0063

Application Hints (Continued)

OPERATION FROM SINGLE OR ASYMMETRICAL POWER SUPPLIES

Both device types may be readily used in applications where symmetrical supplies are unavailable or not desirable. A typical application might be an interface to a MOS shift register where $V^+ = +5V$ and $V^- = -12V$. In this case, an apparent output offset occurs due to the device's voltage gain of less than unity. This additional output offset error may be predicted by:

$$\Delta V_O \cong (1 - A_V)\frac{(V^+ - V^-)}{2} = 0.005(V^+ - V^-)$$

where:

A_V = No load voltage gain, typically 0.99

V^+ = Positive supply voltage

V^- = Negative supply voltage

For the above example, ΔV_O would be $-35mV$. This may be adjusted to zero as described in *Figure 2.* For AC coupled applications, no additional offset occurs if the DC input is properly biased as illustrated in the Typical Applications section.

SHORT CIRCUIT PROTECTION

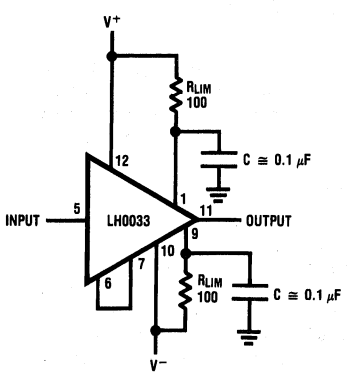
In order to optimize transient response and output swing, output current limit has been omitted from the LH0033 and LH0063. Short circuit protection may be added by inserting appropriate value resistors between V^+ and V_C^+ pins and V^- and V_C^- pins as illustrated in *Figures 3 and 4.* Resistor values may be predicted by:

$$R_{LIM} \cong \frac{V^+}{I_{SC}} = \frac{V^-}{I_{SC}}$$

where:

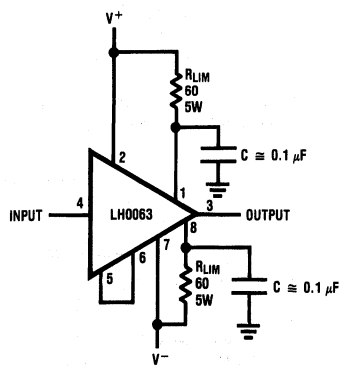
$I_{SC} \leq 100$ mA for LH0033

$I_{SC} \leq 250$ mA for LH0063



TL/K/5507–8

FIGURE 3. LH0033 Using Resistor Current Limiting



TL/K/5507–9

FIGURE 4. LH0063 Using Resistor Current Limiting

Application Hints (Continued)

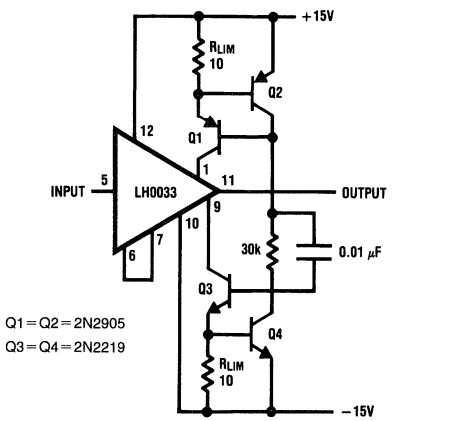
The inclusion of limiting resistors in the collectors of the output transistors reduces output voltage swing. Decoupling V_C^+ and V_C^- pins with capacitors to ground will retain full output swing for transient pulses. Alternate active current limit techniques that retain full DC output swing are shown in *Figures 5* and *6*. In *Figures 5* and *6*, the current sources are saturated during normal operation, thus apply full supply voltage to the V_C pins. Under fault conditions, the voltage decreases as required by the overload.

For *Figure 5:*

$$R_{LIM} = \frac{V_{BE}}{I_{SC}} = \frac{0.6V}{60\ mA} = 10\Omega$$

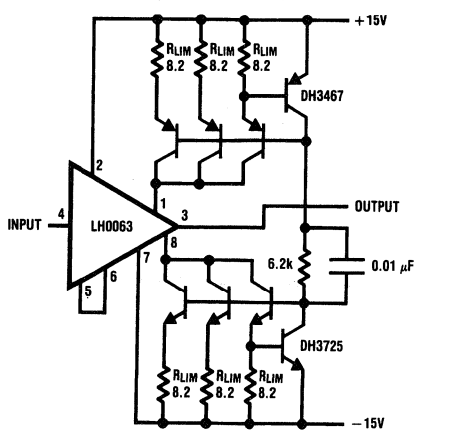
In *Figure 6*, quad transistor arrays are used to minimize can count and:

$$R_{LIM} = \frac{V_{BE}}{1/3(I_{SC})} = \frac{0.6V}{1/3(200\ mA)} = 8.2\Omega$$



TL/K/5507–10

FIGURE 5. LH0033 Current Limiting Using Current Sources



TL/K/5507–11

FIGURE 6. LH0063 Current Limiting Using Current Sources

CAPACITIVE LOADING

Both the LH0033 and LH0063 are designed to drive capacitive loads such as coaxial cables in excess of several thousand picofarads without susceptibility to oscillation. However, peak current resulting from $(C \times dV/dt)$ should be limited below absolute maximum peak current ratings for the devices.

Thus for the LH0033:

$$\left(\frac{\Delta V_{IN}}{\Delta t}\right) \times C_L \leq I_{OUT} \leq \pm 250\ mA$$

and for the LH0063:

$$\left(\frac{\Delta V_{IN}}{\Delta t}\right) \times C_L \leq I_{OUT} \leq \pm 500\ mA$$

In addition, power dissipation resulting from driving capacitive loads plus standby power should be kept below total package power rating:

$P_D pkg. \geq P_{DC} + P_{AC}$

$P_D pkg. \geq (V^+ - V^-) \times I_S + P_{AC}$

$P_{AC} \cong (Vp\text{-}p)^2 \times f \times C_L$

where:

Vp-p = Peak-to-peak output voltage swing

f = Frequency

C_L = Load Capacitance

OPERATION WITHIN AN OP AMP LOOP

Both devices may be used as a current booster or isolation buffer within a closed loop with op amps such as LM6218, LM6361 or LH0032. An isolation resistor of 47Ω should be used between the op amp output and the input of LH0033. The wide bandwidths and high slew rates of the LH0033 and LH0063 assure that the loop has the characteristics of the op amp and that additional rolloff is not required.

HARDWARE

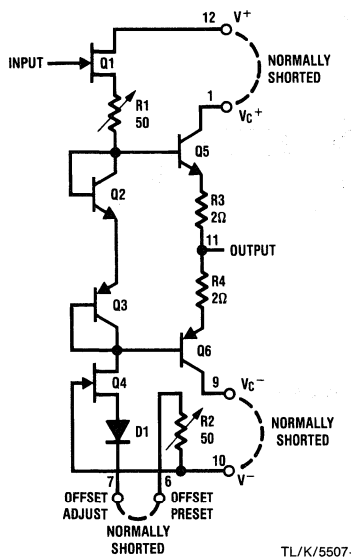
In order to utilize the full drive capabilities of both devices, each should be mounted with a heat sink particularly for extended temperature operation. The cases of both are isolated from the circuit and may be connected to the system chassis.

DESIGN PRECAUTION

Power supply bypassing is necessary to prevent oscillation with both the LH0033 and LH0063 in all circuits. Low inductance ceramic disc capacitors with the shortest practical lead lengths must be connected from each supply lead (within $<1/4$ to $1/2$" of the device package) to a ground plane. Capacitors should be one or two 0.1 μF in parallel for the LH0033; adding a 4.7 μF solid tantalum capacitor will help in troublesome instances. For the LH0063, two 0.1 μF ceramic and one 4.7 μF solid tantalum capacitors in parallel will be necessary on each supply lead.

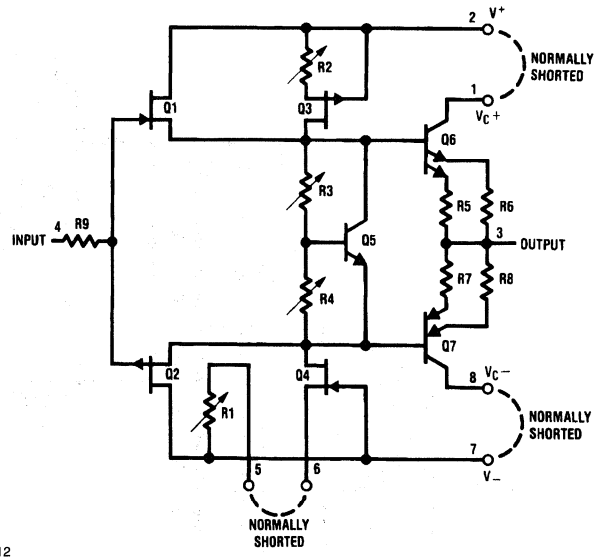
Schematic Diagrams

LH0033/LH0033A



TL/K/5507–12

LH0063

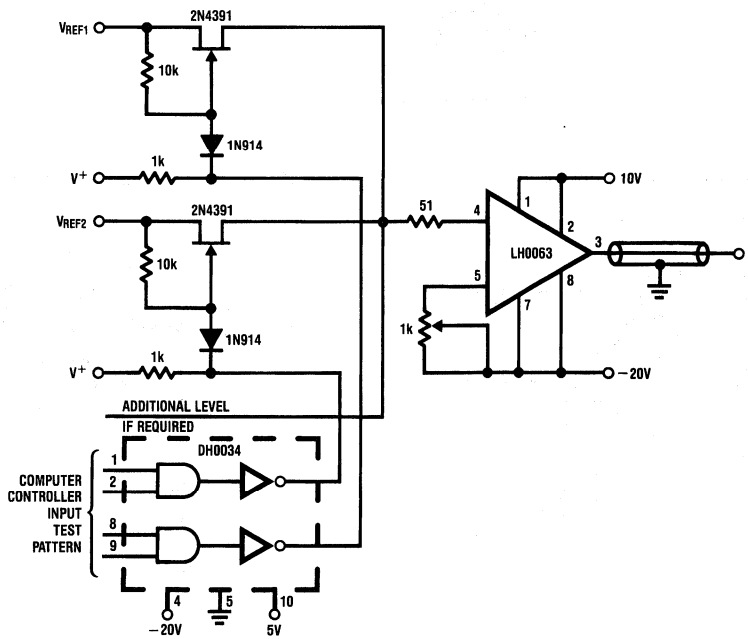


TL/K/5507–13

Pin numbers shown for TO-8 ("G") package.

Typical Applications

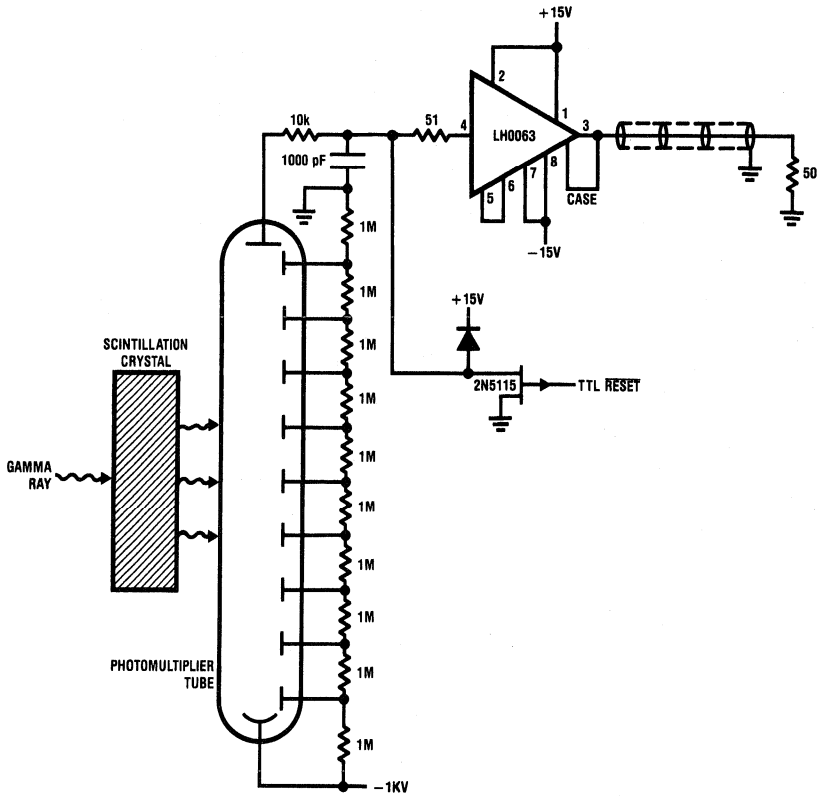
High Speed Automatic Test Equipment
Forcing Function Generator



TL/K/5507–14

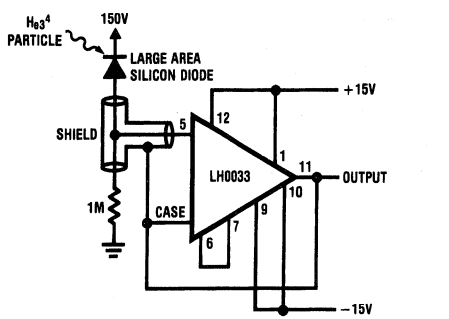
Typical Applications (Continued)

Gamma Ray Pulse Integrator



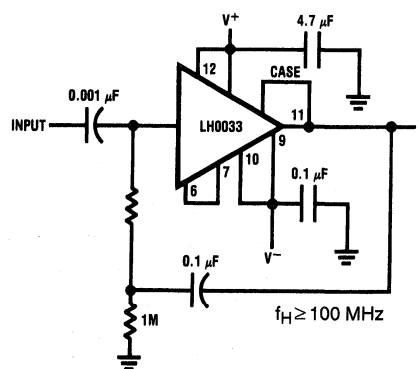
TL/K/5507–15

Nuclear Particle Detector



TL/K/5507–16

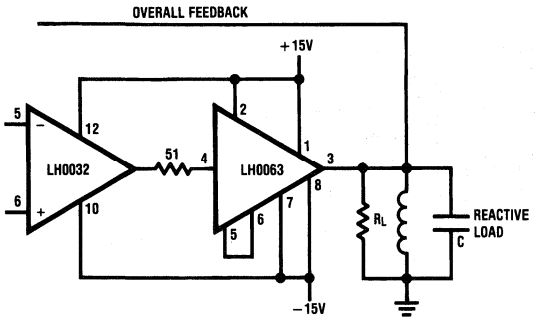
High Input Impedance AC Coupled Amplifier



TL/K/5507–17

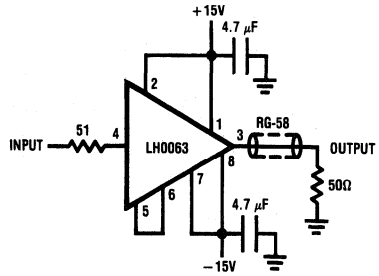
Typical Applications (Continued)

Isolation Buffer



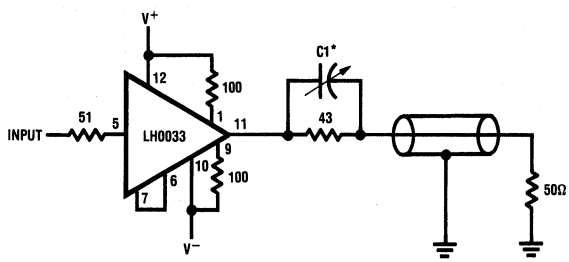
TL/K/5507–18

Coaxial Cable Driver



TL/K/5507–19

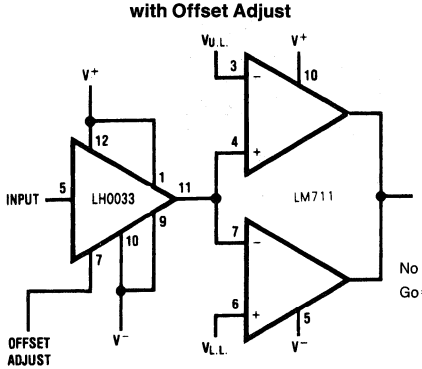
Coaxial Cable Driver



TL/K/5507–20

*Select C1 for optimum pulse response

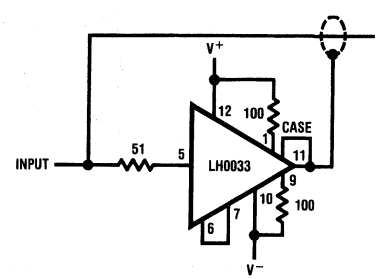
High Input Impedance Comparator with Offset Adjust



No go = logic "1"
Go = logic "0"

TL/K/5507–21

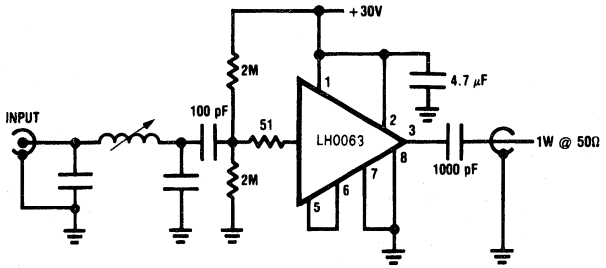
Instrumentation Shield/Line Driver



TL/K/5507–22

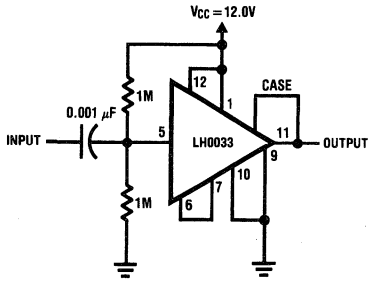
Typical Applications (Continued)

1W CW Final Amplifier



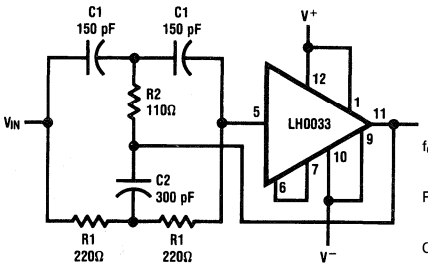
TL/K/5507-23

Single Supply AC Amplifier



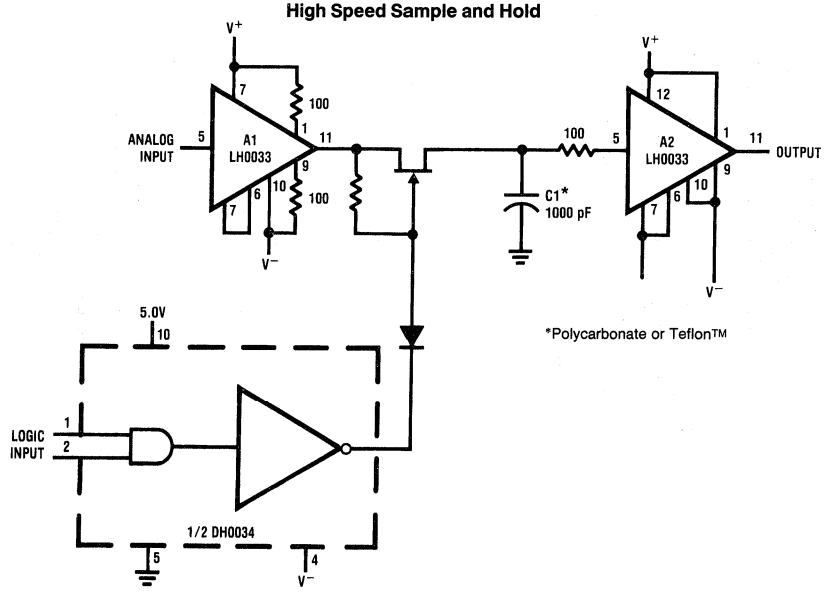
TL/K/5507-24

4.5 MHz Notch Filter



TL/K/5507-25

High Speed Sample and Hold



*Polycarbonate or Teflon™

TL/K/5507-26

National Semiconductor

LH2003/LH2033
100 MHz Video Buffer

General Description

The LH2003/LH2033 is a high speed monolithic open loop buffer designed to provide up to 100 mA drive at frequencies from DC to 100 MHz and slew rates of 1200 V/μs. It is oscillation free driving into capacitive loads and features internal current limiting to protect under overload conditions.

The LH2003/LH2033 is intended for a wide range of buffer applications. Its high speed makes it ideally suited for closed loop buffer applications with wide band op-amps, as well as open loop applications such as driving co-ax cables and twisted pairs.

The following devices are available:

Order Number	Temperature Range	Package
LH2003CN	−25°C to +85°C	Plastic DIP
LH2003CJ	−25°C to +85°C	Ceramic DIP
LH2003J	−55°C to +125°C	Ceramic DIP
LH2003CH	−25°C to +85°C	8-Lead T0-5
LH2003H	−55°C to +125°C	8-Lead T0-5
LH2033CN	−25°C to +85°C	Plastic DIP
LH2033CJ	−25°C to +85°C	Ceramic DIP
LH2033J	−55°C to +125°C	Ceramic DIP

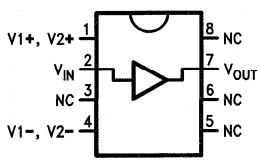
Features

- Differential Gain 0.1%
- Differential Phase 0.1°
- 100 mA continuous output current guaranteed
- Short circuit protected
- Wide bandwidth—100 MHz
- High slew rate—1200 V/μs
- High input impedance—2 MΩ
- Low quiescent current drain
- LH2003N, J—Pin compatible with EL2003
- LH2033—Pin compatible with HA3-5033, HA7-5033, EL2033
- LH2003H—Pin compatible with HA2-5002, EL2003H

Applications

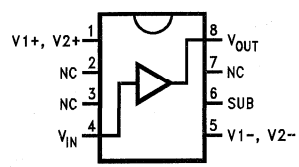
- Co-ax cable driver
- Flash converter driver
- Video DAC buffer
- Op amp booster

Connection Diagrams



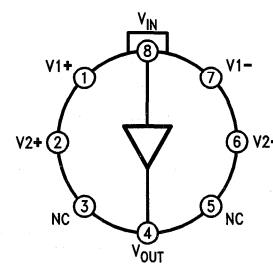
TL/K/10783–1

Order Number LH2003CN, LH2003CJ, and LH2003J
See NS Package Number N08E (LH2003CN)
See NS Package Number J08A (LH2003CJ, LH2003J)



TL/K/10783–2

Order Number LH2033CN, LH2033CJ, and LH2033J
See NS Package Number N08E (LH2033CN)
See NS Package Number J08A (LH2033CJ, LH2033J)



TL/K/10783–3

Top View
Order Number LH2003CH, LH2003H
See NS Package Number H08C

Absolute Maximum Ratings (Note 4)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

V_S	Supply Voltage ($V^+ - V^-$)	±18V or 36V
V_{IN}	Input Voltage (Note 1)	±15V or V_S
I_{IN}	Input Current (Note 1)	±50 mA
P_D	Power Dissipation	(Note 5)
	Output Short Circuit Duration (Note 2)	Continuous
T_{ST}	Storage Temperature	−65°C to +150°C
	Lead Temperature (Soldering, <10 seconds)	+300°C
T_J max	Junction Temperature	
	Metal Can and Ceramic DIP	+175°C
	Plastic DIP	+150°C

Operating Ratings

T_A	Temperature Range:	
	LH2003/2033	−55°C to +125°C
	LH2003C/2033C	−25°C to +85°C
	Thermal Resistance	(Note 6)
θ_{JC},	J Package	40°C/W
θ_{JA},	J Package	125°C/W
θ_{JC},	H Package	55°C/W
θ_{JA},	H Package	190°C/W
θ_{JA},	N Package	95°C/W

DC Electrical Characteristics V_S ±15V R_S = 50Ω (Note 2)

Symbol	Parameter	Conditions		LH2003/LH2033 Min	LH2003/LH2033 Typ	LH2003/LH2033 Max	Units
V_{OS}	Output Offset Voltage	V_{IN} = 0V, R_L = ∞	T_A = 25°C	−40	5	+40	mV
			Over Temp	−50		+50	
I_{IN}	Input Current	V_{IN} = 0V, R_L = ∞	T_A = 25°C	−25	5	+25	μA
			Over Temp	−50		+50	
R_{IN}	Input Resistance	V_{IN} = ±12V, R_L = 100Ω	T_A = 25°C	1	2		MΩ
			Over Temp	0.1			
A_{V1}	Voltage Gain	V_{IN} ±12V, R_L = 1 kΩ	T_A = 25°C	0.98	0.99		V/V
			Over Temp		0.97		
A_{V2}	Voltage Gain	V_{IN} ±6V, R_L = 50Ω	T_A = 25°C	0.83	0.90		V/V
			Over Temp	0.80			
A_{V3}	Voltage Gain	V_{IN} = ±3V, R_L = 50Ω, V_S = ±5V	T_A = 25°C	0.82	0.89		V/V
			Over Temp	0.79			
V_{O1}	Output Voltage Swing	V_{IN} = ±14V, R_L = 1 kΩ	T_A = 25°C	±13	±13.5		V
			Over Temp	±12.5			
V_{O2}	Output Voltage Swing	V_{IN} = ±12V, R_L = 100Ω	T_A = 25°C	±10.5	±11.3		V
			Over Temp	±10			
R_{OUT}	Output Resistance	V_{IN} = ±2V, R_L = 50Ω	T_A = 25°C		7	10	Ω
			Over Temp			12	
I_{OUT}	Output Current (Note 3)	V_{IN} = ±12V, V_{OUT} = ±10V	T_A = 25°C	±105	±230		mA
			Over Temp	±100			
I_S	Supply Current	V_{IN} = 0V, R_L = ∞	T_A = 25°C		10	15	mA
			Over Temp			20	
PSRR	Power Supply Rejection	V_{IN} = 0V, R_L = ∞, V_S = ±4.5V to ±18V	T_A = 25°C	60	80		dB
			Over Temp	50			

Note 1: If V_{IN} exceeds the absolute maximum ratings, or $V_{IN} - V_{OUT}$ exceeds ±7.5V, the input current needs to be limited to maximum 50 mA.

Note 2: Specification applies for V_S = ±15V, R_L = 50Ω unless otherwise specified. "Over Temp." numbers apply over the operating temperature range. Electrical tests are performed with high speed automated test equipment, so that $T_J = T_A$, unless otherwise noted.

Note 3: Input and output voltages are forced to +12V, +10V and −12V, −10V respectively and the output current is measured.

Note 4: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed.

Note 5: The maximum power dissipation is a function of maximum junction temperature (T_J max), total thermal resistance (θ_{JA}), and ambient temperature (T_A). The maximum allowable power dissipation at any ambient temperature is $P_D = (T_J \text{ max} - T_A)/\theta_{JA}$.

Note 6: For operating at elevated temperatures, the device must be derated based on the thermal resistance (θ_{JA}) and T_J max. $T_J = T_A + P_D \theta_{JA}$. An external heatsink will be necessary for the H package to prevent exceeding T_J max in elevated ambients.

AC Electrical Characteristics $V_S = \pm 15V$ $R_S = 50\Omega$ (Note 2)

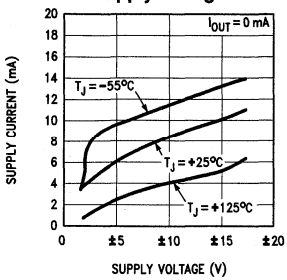
Symbol	Parameter	Conditions	LH2003/LH2033			Units
			Min	Typ	Max	
SR_1	Slew Rate	$V_{IN} = \pm 10V$ $R_L = 1\ k\Omega$ Tested at $V_{OUT} = \pm 5V$	600	1200		V/μs
SR_2	Slew Rate	$V_{IN} = \pm 5V$ $R_L = 50\Omega$ Tested at $V_{OUT} = \pm 2.5V$		400		V/μs
BW	Band Width	$R_L = 50\Omega$ $V_{IN} = 0$ dBm		100		MHz
THD	Distortion	$V_{IN} = 4\ V_{RMS}$, 1 kHz $R_L = 50\Omega$		0.2		%

Note 1: If V_{IN} exceeds the absolute maximum ratings, or $V_{IN} - V_{OUT}$ exceeds $\pm 7.5V$, the input current needs to be limited to maximum 50 mA.

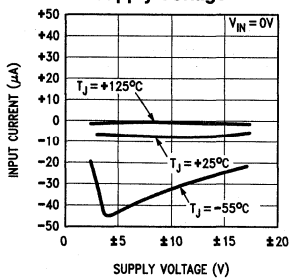
Note 2: Specification applies for $V_S = \pm 15V$, $R_L = 50\Omega$ unless otherwise specified. **Boldface** numbers apply over the operating temperature range. Numbers in standard typeface apply at $T_A = 25°C$. Electrical tests are performed with high speed automated test equipment, so that $T_J = T_A$, unless otherwise noted.

Typical Performance Characteristics (Continued)

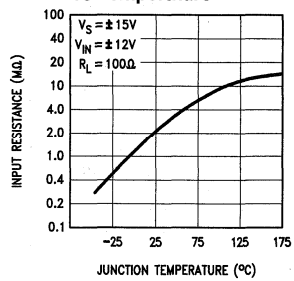
Quiescent Supply Current vs Supply Voltage



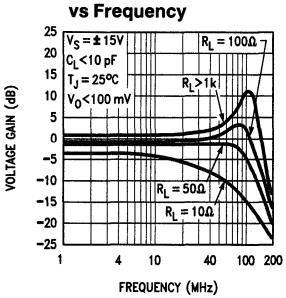
Input Current vs Supply Voltage



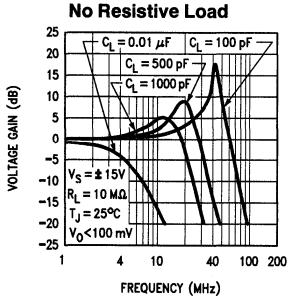
Input Resistance vs Temperature



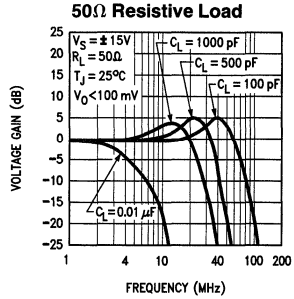
Voltage Gain vs Frequency



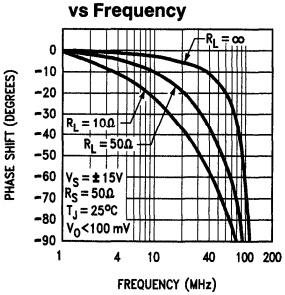
Voltage Gain vs Frequency No Resistive Load



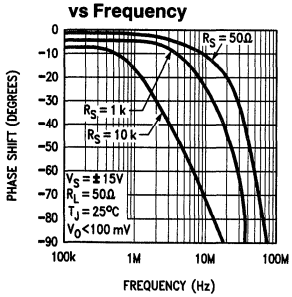
Voltage Gain vs Frequency 50Ω Resistive Load



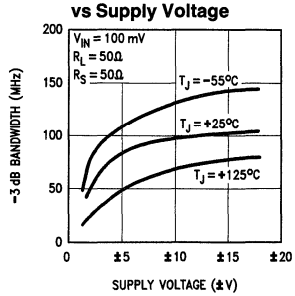
Phase Shift vs Frequency



Phase Shift vs Frequency



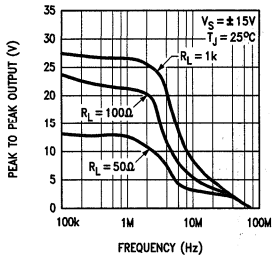
Small Signal Bandwidth vs Supply Voltage



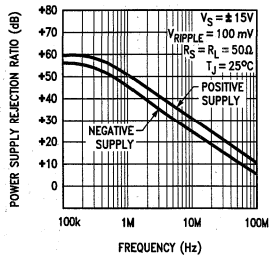
TL/K/10783–5

Typical Performance Characteristics (Continued)

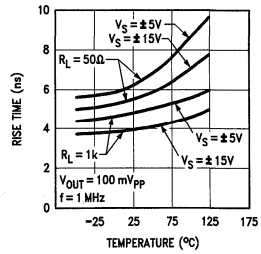
Maximum Undistorted Output Voltage vs Frequency



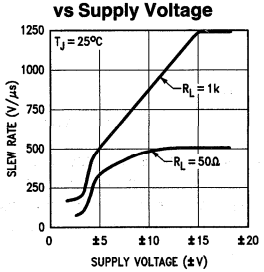
Power Supply Rejection Ratio vs Frequency



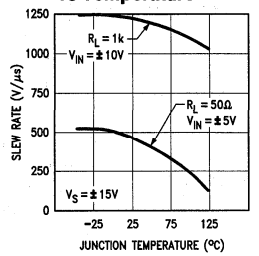
Rise Time vs Temperature



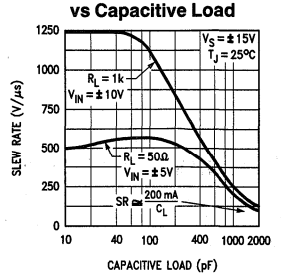
Slew Rate vs Supply Voltage



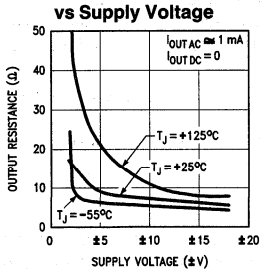
Slew Rate vs Temperature



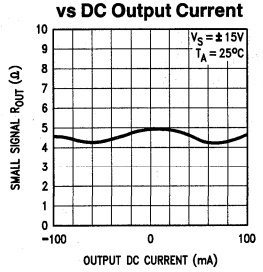
Slew Rate vs Capacitive Load



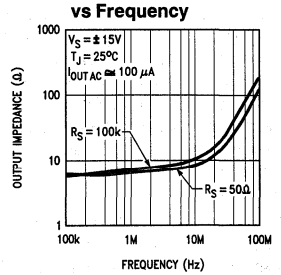
Output Resistance vs Supply Voltage



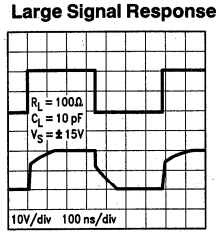
Small Signal Output Resistance vs DC Output Current



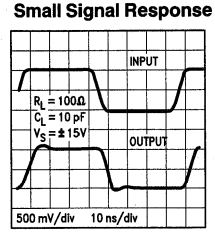
Output Impedance vs Frequency



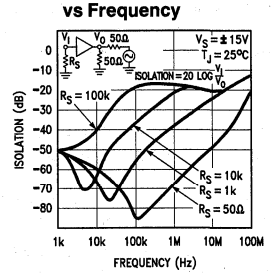
Large Signal Response



Small Signal Response



Reverse Isolation vs Frequency



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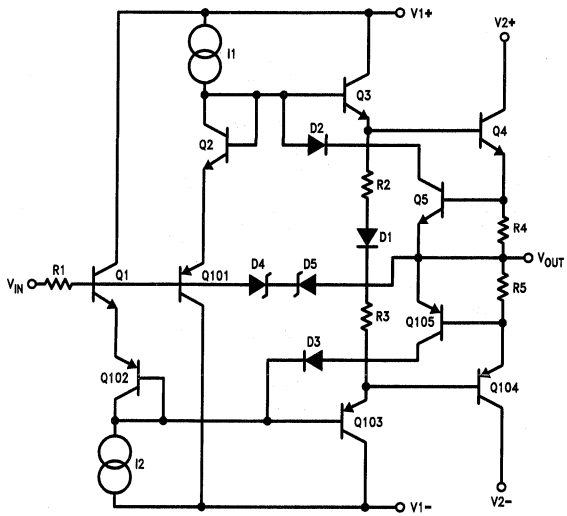
Simplified Schematic



TL/K/10783–7

Applications Information

The LH2003/LH2033 are monolithic open loop buffers with high slew rate and bandwidth. This makes them useful for video frequencies and above.

Supply Voltages

The LH2003/LH2033 can be operated with a difference in voltage supplies of as low as 5V to a maximum of 36V. The supplies do not have to be symmetrical to ground. For optimal performance it is recommended that the power supply pins be decoupled with 0.1 μF capacitors close to the pins (1/4 inch), and additional 10 μF which can be located further away (1 inch). In most cases the LH2003/LH2033 will not oscillate even without bypass capacitors, but the performance (slew rate) will be somewhat degraded, and in addition the supplies tend to ring.

The LH2003H and LH2003CH are in metal can and have the collectors of the output transistors pinned out: they are pin compatible with the EL0002H and EL0002CH. The output stage can therefore be operated from a lower supply voltage and the power dissipation is then reduced. However, when the signal level exceeds the output supply voltages, clipping occurs, and the output transistors also require several μs to come out of saturation.

Input

The input of the LH2003/LH2033 can be approximated with a high resistance in parallel with a small capacitor of several pF. There are clamp diodes from input to output to protect the base emitter junctions of the transistors. These diodes are set to 9.5V and can carry 50 mA.

The input voltages should be not more than 0.5V outside the supply voltages, or the recovery will take several 100 ns. For this reason, if clamps are used, they should be Schottky diodes.

Source impedance usually does not cause problems, but sometimes an inductive source impedance or an unterminated cable can cause instabilities, and in this case a resistance of 100Ω to several 100Ω in series with the input of the buffer may be needed.

Current Limiting

The LH2003/LH2033 have internal current limiting to protect the devices. Recovery time from current limit is about 250 ns. For higher temperatures the limit value is less (see graphs).

If the device is run from ±15V supplies, a long-time short to ground will overstress the device thermally, and in this case heatsinking is required (Aavid, Thermalloy, and others make suitable heatsinks).

Gain

The DC gain of the LH2003/LH2033 can be derived from the unloaded gain and the ratio of output and load resistors:

$$A_V = 0.995 \times RL/(RL + R_{OUT})$$

For high frequency gain see graphs. For low loads peaking occurs, it can be reduced by a snubber, which provides load at high frequencies without loading at low frequencies.

Loads

The LH2003/LH2033 is stable for capacitive loads. However, for small capacitive loads, below 1000 pF, ringing occurs. In this case a suitable snubber (e.g. 1000 pF, 30Ω) will help. For higher capacitive loads care has to be taken not to exceed the current capability of the device:

$$I_{MAX} > I = C_{LOAD} \times dV/dt, \text{ or}$$
$$I_{MAX} > I = V_{PEAK} \times 2 \times 3.14 \times f$$

When driving inductive loads, it may be necessary to use clamp diodes in the output to prevent inductive kickback from damaging the device.

National Semiconductor

LH4001 Wideband Current Buffer

General Description

The LH4001 is a high speed unity gain buffer designed to provide high current drive capability at frequencies from DC to over 25 MHz. It is capable of providing a continuous output current of ±100 mA and a peak of ±200 mA.

The LH4001 is designed to fulfill a wide range of applications such as impedance transformation, high impedance input buffers for A/D converters and comparators, as well as high speed line drivers. It is also suitable for use in current booster applications within an op amp loop. This allows the output current capability of existing op amps to be increased to ±100 mA.

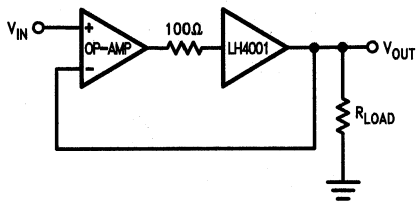
Features

- DC to 25 MHz bandwidth
- 125 V/μs slew rate
- Drives ±10V into 50Ω
- Operates from ±5 to ±20V supplies
- Output swing approaches supply voltage

Applications

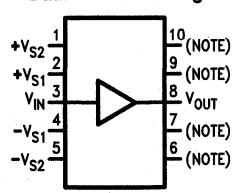
- Boost op amp output
- Buffer amplifiers
- Isolate capacitive loads
- Drive long cables

Typical Applications and Connection Diagram



TL/K/8628–1

Dual-In-Line Package



TL/K/8628–2

Top View

***Note:** Electrically connected internally. No connection should be made to these pins.

Order Number LH4001CN
See NS Package Number N10A

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage, V_S	±22V
Continuous Output Current, I_O	±100 mA
Peak Output Current, $I_{O(peak)}$ (50 ms On/1 Sec Off)	±200 mA
Input Voltage Range, V_{IN}	$\pm V_S$
Power Dissipation	500 mW
Storage Temperature Range, T_{STG}	−65°C to +150°C
Junction Temperature, T_J	150°C
Lead Temp. (Soldering, <10 seconds)	260°C

ESD rating is to be determined.

Operating Ratings

Temperature Range, T_A	0°C to +70°C
Thermal Resistance θ_{JA}	120°C/W

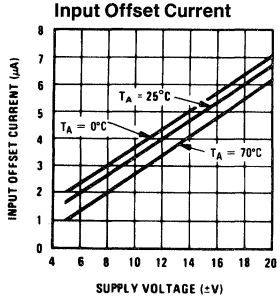
Electrical Characteristics (Note 1)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
A_V	Voltage Gain	R_S = 10 kΩ, R_L = 1 kΩ V_{IN} = ±10V	0.95	0.97	1	V/V
R_{IN}	Input Impedance	R_S = 200 kΩ, R_L = 1 kΩ V_{IN} = ±1.0V	180	400		kΩ
R_{OUT}	Output Impedance	R_S = 10 kΩ, R_L = 50Ω V_{IN} = ±1.0V		6	10	Ω
V_O	Output Swing	V_S = ±15V, R_S = 50Ω R_L = 100Ω, V_{IN} = ±12V	±10	±11		V
I_B	Input Bias Current	R_S = 10 kΩ, R_L = 1 kΩ		±10	±50	μA
t_r	Rise Time	R_L = 100Ω, ΔV_{IN} = 100 mV		7		ns
SR	Slew Rate	V_{IN} = ±5V, R_L = 100Ω		125		V/μs
I_S	Supply Current	R_S = 10 kΩ		±6	±10	mA
V_{OS}	Offset Voltage	R_S = 300Ω, R_L = 1 kΩ		±10	±50	mV

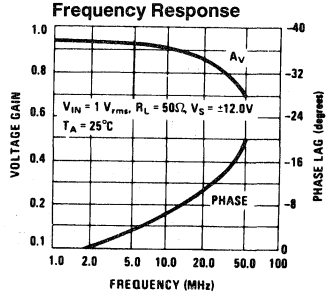
Note 1: Specification applies for T_A = 25°C with +12V on Pins 1 & 2; −12V on Pins 4 & 5 unless otherwise specified.

Typical Performance Characteristics

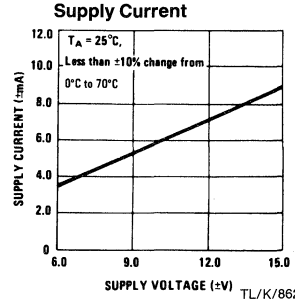
Input Offset Current



Frequency Response

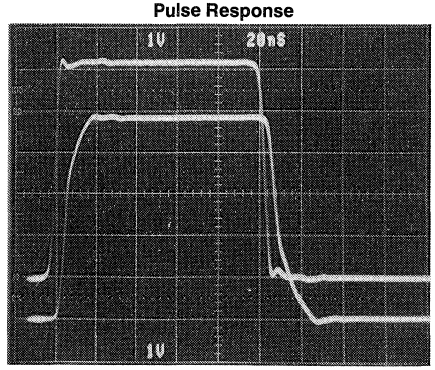


Supply Current



TL/K/8628–3

Pulse Response



TOP TRACE = INPUT

BOTTOM TRACE = OUTPUT

TL/K/8628–10

V_{IN} = ±2.5V, R_S = R_L = 50Ω

Applications Information

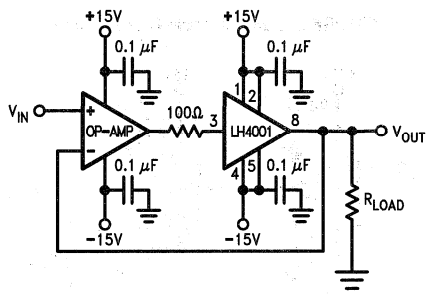
Figure 1 shows a simple implementation of a non-inverting buffer amplifier of unity gain. Popular industry standard operational amplifiers such as LF156, LF351, LF411, LF441, LM11, LM741, etc. can be used in this configuration. Due to the high bandwidth of the LH4001, it is suitable for use with most monolithic op amps.

Figure 2 shows an implementation of an inverting amplifier with output current capability in excess of ±100 mA. The gain of this amplifier is determined by the values of R_F and R_{IN}. The resistor between the non-inverting input and ground is used to minimize the output offset voltage resulting from the input bias current.

Because of its high current drive capability, the LH4001 buffer amplifier is suitable for driving terminated or unterminated co-axial cables, and high current or reactive loads.

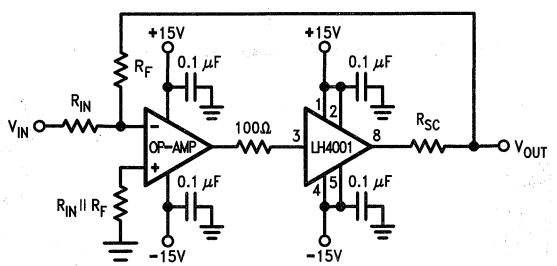
Figure 3 shows a co-axial cable drive circuit. The 43Ω resistor matches the driving source to the cable, however, its inclusion rarely will result in substantial improvement in pulse response into a terminated cable. If the 43Ω resistor is included, the output voltage to the load is about half what it would be without the near end termination.

Figure 4 shows a non-inverting amplifier with gain and output current capability in excess of ±100 mA. It is capable of providing ±10 mA into a 1 kΩ load or ±100 mA into a 100Ω load (±10V swing). *Figures 5* and *6* show two different methods of providing current limit or short circuit protection for the LH4001. In *Figure 6,* the 10Ω resistor limits the output current to approximately 70 mA. This circuit is highly recommended if there is a potential for a short circuit to occur.



TL/K/8628–4

FIGURE 1. Non-Inverting Buffer Amplifier

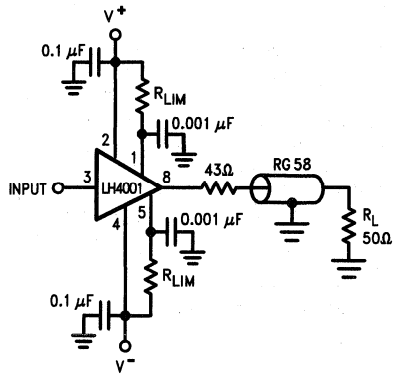


$$\frac{V_{OUT}}{V_{IN}} = -\frac{R_F}{R_{IN}}$$

TL/K/8628–6

FIGURE 2. Inverting Buffer Amplifier with Current Limit

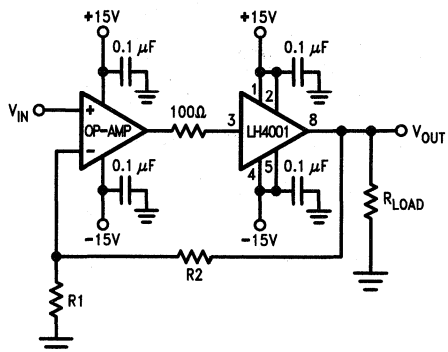
Applications Information (Continued)



$R_{LIM} = 100\Omega$, 1W

TL/K/8628-7

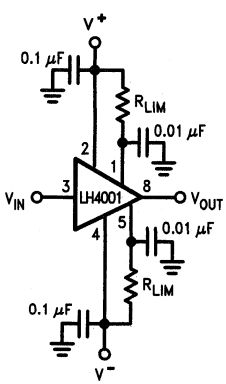
FIGURE 3. Coaxial Cable Drive Circuit



TL/K/8628-5

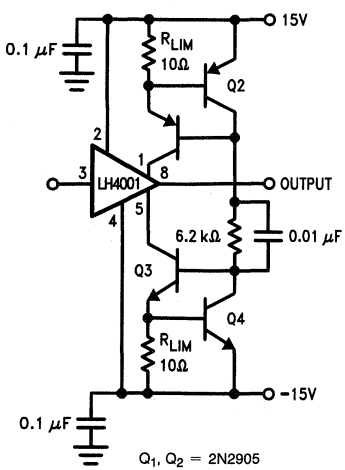
$$V_{OUT} = V_{IN}\left(1 + \frac{R2}{R1}\right)$$

FIGURE 4. Non-Inverting Buffer Amplifier with Gain



TL/K/8628-8

FIGURE 5. LH4001 Using Resistor Current Limiting



Q_1, Q_2 = 2N2905
Q_3, Q_4 = 2N2219

TL/K/8628-9

FIGURE 6. Current Limit Using Current Sources

National Semiconductor

LH4002 Wideband Video Buffer

General Description

The LH4002 is a high speed voltage follower designed to drive video signals from DC up to 200 MHz. At voltage supplies of ±5V, the LH4002 will provide up to 40 mA into 50Ω at slew rates in excess of 1000 V/μs.

The device is intended to fulfill a wide range of high speed applications including video distribution, impedance transformation, and load isolation. It is also suitable for use in current booster applications within an op amp loop. This allows the output current capability of existing op amps to be increased.

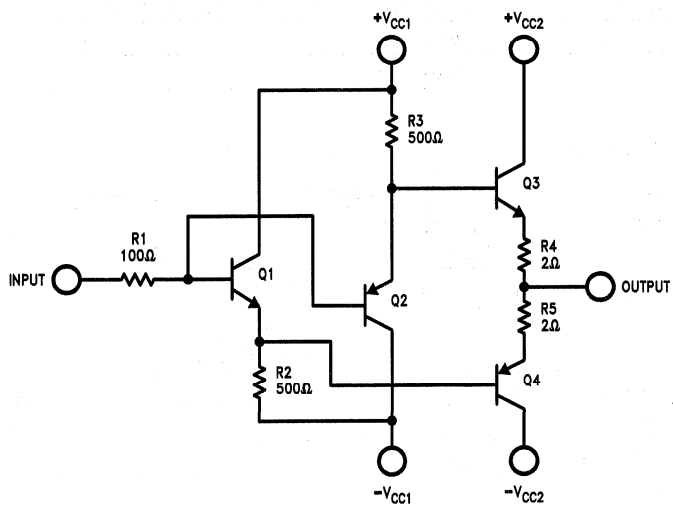
Features

- DC to 200 MHz Bandwidth with V_S = ±5V
- 1250 V/μs Slew Rate into 50Ω
- 150 MHz Bandwidth with V_S = ±5V, R_L = 50Ω and Voltage Swing = 2 V_{P-P}

Applications

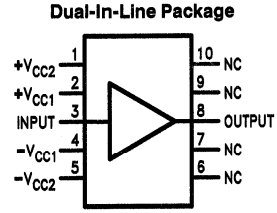
- Wideband Amplifier Buffer
- Wideband Line Driver

Schematic and Connection Diagrams



TL/K/8686-15

Dual-In-Line Package



TL/K/8686-2

Top View

Order Number LH4002CN
See NS Package Number N10A

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage, V_S ±6V
Input Voltage Range, V_{IN} ±V_S
Continuous Output Current, I_O ±60 mA
Storage Temperature Range, T_{STG} −65°C to +150°C
Operating Temperature Range, T_A
LH4002C −25°C to +85°C
Junction Temperature, T_J 150°C
Lead Temperature (Soldering, 10 sec) 300°C
ESD rating is to be determined.

DC Electrical Characteristics V_{CC} = ±5V, $T_{min} \le T_A \le T_{max}$ unless otherwise stated.

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{OS}	Input Offset Voltage	$T_A = T_J = 25°C$ $R_S = 150\Omega$, $R_L = 50\Omega$			20	50	mV
I_B	Input Bias Current	$R_S = 1\ k\Omega$, $R_L = 50\Omega$			100	200	μA
A_V	DC Voltage Gain	$R_S = 10\ k\Omega$, $R_L = 1.0\ k\Omega$, $V_{IN} = \pm 2V$		0.95	0.97		V/V
V_O	Output Voltage Swing	$R_S = 150\Omega$, $V_{IN} = \pm 2.5V$	$R_L = 1\ k\Omega$	±2.2	±2.4		V
			$T_A = 25°C$, $R_L = 50\Omega$	±2.0	±2.2		V
I_S	Supply Current	$R_S = 10\ k\Omega$, $V_{IN} = 0V$, $R_L = 1\ k\Omega$, $T_A = T_J = 25°C$			20	35	mA
R_{OUT}	Output Resistance	$R_S = 10\ k\Omega$, $R_L = 50\Omega$			6	10	Ω
R_{IN}	Input Resistance	$R_S = 10\ k\Omega$, $R_L = 50\Omega$		10	18		kΩ

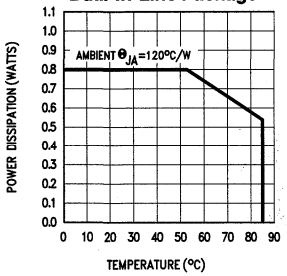
AC Electrical Characteristics V_{CC} = ±5V, T_A = 25°C.

Symbol	Parameter	Conditions		Min	Typ	Max	Units
S_R	Slew Rate	$R_L = 50\Omega$, $R_S = 50\Omega$ $V_{IN} = \pm 2V$		1000	1250		V/μs
f_{3dB}	Bandwidth, −3 dB (Note 2)	$R_S = 50\Omega$ $R_L = 50\Omega$	$V_{OUT} = 4V_{P-P}$		125		MHz
			$V_{OUT} = 2V_{P-P}$	100	150		MHz
			$V_{OUT} = 100\ mV_{P-P}$		200		MHz
	Phase Non-Linearity	BW = 1.0–20 MHz			2.0		degrees
t_r	Rise Time	$\Delta V_{IN} = 0.5V$			3		ns
t_d	Propagation Delay	$\Delta V_{IN} = 0.5V$			1.2		ns
THD	Harmonic Distortion	f = 1 kHz			0.1		%

Note 1: Under normal operating conditions $+V_{CC1}$ and $+V_{CC2}$ should be connected together, and $-V_{CC1}$ and $-V_{CC2}$ should be connected together.
Note 2: Guaranteed by design. This parameter is sample tested.

Typical Performance Characteristics

Maximum Power Dissipation Dual-In-Line Package



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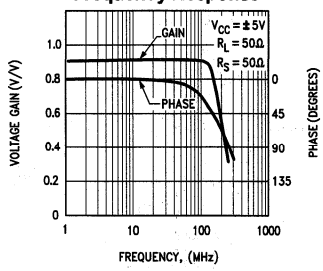
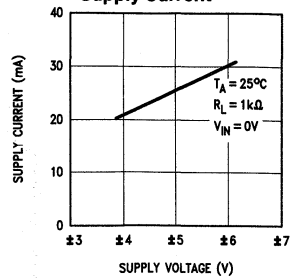
Frequency Response



TL/K/8686-5

Supply Current



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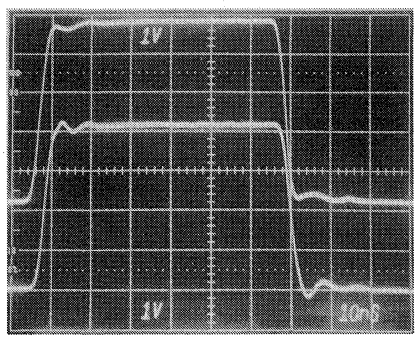
Pulse Response

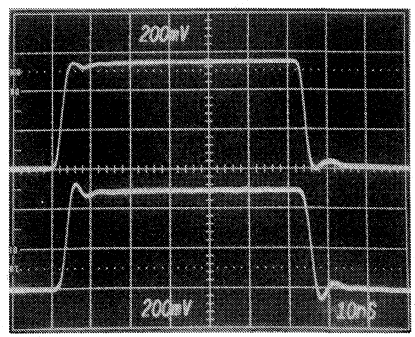


TOP TRACE
= INPUT

BOTTOM TRACE
= OUTPUT

V_S = ±5V
R_L = 50Ω

TL/K/8686-7



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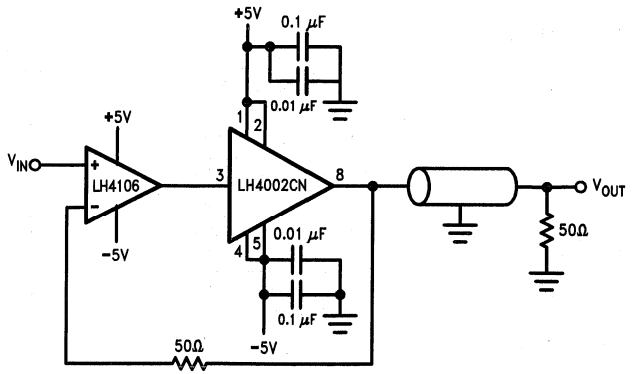
2

Typical Applications



TL/K/8686-11

FIGURE 1. Wideband Unity Gain Amplifier Using LH4002CN

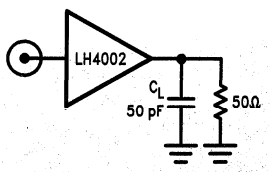


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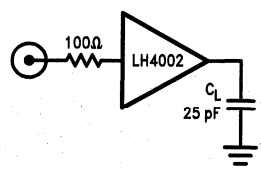
FIGURE 2. Compensation for Capacitive Loads



TL/K/8686-10

FIGURE 3. Compensation for Capacitive Loads

Applications Information

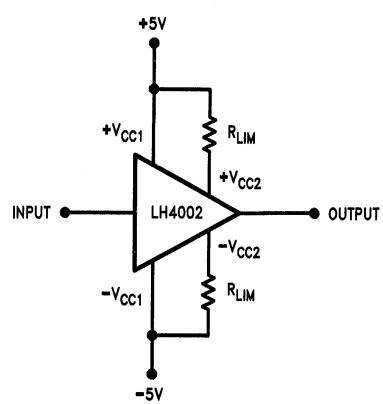
The high speed performance of the LH4002 can only be realized by taking certain precautions in circuit layout and power supply decoupling. Low inductance ceramic chip or disc power supply decoupling capacitors of 0.01 μF in parallel with 0.1 μF should be connected with the shortest practical lead length between device supply leads and a ground plane. Failure to follow these rules can result in oscillations. When driving a capacitive load such as inputs to flash converters, the circuits in *Figure 2* and *3* can be used to minimize the amount of overshoot and ringing at the outputs. *Figure 2* indicates that a 50Ω should be placed in parallel with the load and *Figure 3* recommends that a 100Ω resistor be placed in series with the input to the LH4002.

Short Circuit Protection

In order to optimize transient response and output swing, output current limits have been omitted from the LH4002. Short circuit protection may be added by inserting appropriate value resistors between $+V_{CC1}$ and $+V_{CC2}$ pins and between $-V_{CC1}$ and $-V_{CC2}$ pins as illustrated in *Figure 4*. Resistor values may be predicted by:

$$R_{LIM} = \frac{+V_{CC1}}{I_{SC}} = \frac{-V_{CC1}}{I_{SC}}$$

where $I_{SC} \leq 100$ mA. The inclusion of 50Ω limiting resistors in the collectors of the output transistors limits the short circuit current to approximately 100 mA without reducing the output voltage swing.



TL/K/8686-20

FIGURE 4. LH4002 Using Resistor Current Limiting

National Semiconductor

LM102/LM302 Voltage Followers

General Description

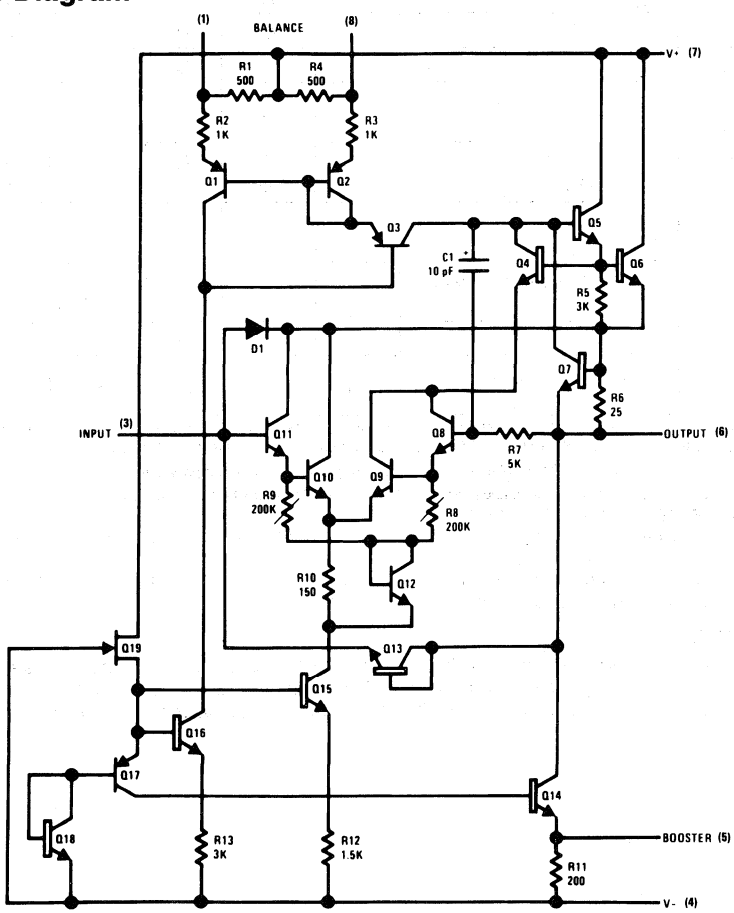
The LM102 series are high-gain operational amplifiers designed specifically for unity-gain voltage follower applications. Built on a single silicon chip, the devices incorporate advanced processing techniques to obtain very low input current and high input impedance. Further, the input transistors are operated at zero collector-base voltage to virtually eliminate high temperature leakage currents. It can therefore be operated in a temperature stabilized component oven to get extremely low input currents and low offset voltage drift.

The LM102, which is designed to operate with supply voltages between ±12V and ±15V, also features low input capacitance as well as excellent small signal and large signal frequency response—all of which minimize high frequency gain error. Because of the low wiring capacitances inherent in monolithic construction, this fast operation can be realized without increasing power consumption.

Features

- Fast slewing — 10V/μs
- Low input current — 10 nA (max)
- High input resistance — 10,000 MΩ
- No external frequency compensation required
- Simple offset balancing with optional 1 kΩ potentiometer
- Plug-in replacement for both the LM101 and LM709 in voltage follower applications

Schematic Diagram



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Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications. (Note 6)

Supply Voltage	±18V
Power Dissipation (Note 1)	500 mW
Input Voltage (Note 2)	±15V
Output Short Circuit Duration (Note 3)	Indefinite
Operating Free Air Temperature Range	
LM102	−55°C to +125°C
LM302	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec.)	300°C

ESD rating to be determined.

Electrical Characteristics (Note 4)

Parameter	Conditions	LM102			LM302			Units
		Min	Typ	Max	Min	Type	Max	
Input Offset Voltage	$T_A = 25°C$		2	5		5	15	mV
Input Bias Current	$T_A = 25°C$		3	10		10	30	nA
Input Resistance	$T_A = 25°C$	10^{10}	10^{12}		10^9	10^{12}		Ω
Input Capacitance				3.0		3.0		pF
Large Signal Voltage Gain	$T_A = 25°C$, V_S ±15V, V_{OUT} = ±10V, R_L = 8 kΩ	0.999	0.9996		0.9985	0.9995	1.0	V/V
Output Resistance	$T_A = 25°C$		0.8	2.5		0.8	2.5	Ω
Supply Current	$T_A = 25°C$		3.5	5.5		3.5	5.5	mA
Input Offset Voltage				7.5			20	mV
Offset Voltage Temperature Drift			6			20		μV/°C
Input Bias Current	$T_A = T_AMAX$ $T_A = T_AMIN$		3 30	10 100		3.0 20	15 50	nA nA
Large Signal Voltage Gain	V_S = ±15V, V_{OUT} = ±10V, R_L = 10 kΩ	0.999						
Output Voltage Swing	V_S = ±15V, R_L = 10 kΩ (Note 5)	±10			±10			V
Supply Current	$T_A = 125°C$		2.6	4.0				mA
Supply Voltage Rejection Ratio	±12V ≤ V_S ≤ ±15V	60			60			dB

Note 1: The maximum junction temperature of the LM102 is 150°C, while that of the LM302 is 85°C. For operating at elevated temperatures, devices in the H08 package must be derated based on a thermal resistance of 150°C/W, junction to ambient, or 20°C/W, junction to case.

Note 2: For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

Note 3: It is necessary to insert a resistor (at least 5k and preferably 10k) in series with the input pin when the amplifier is driven from low impedance sources to prevent damage when the output is shorted and to ensure stability.

Note 4: These specifications apply for ±12V ≤ V_S ≤ ±15V and −55°C ≤ T_A ≤ 125°C for the LM102 and 0°C ≤ T_A ≤ 70°C for the LM302 unless otherwise specified.

Note 5: Increased output swing under load can be obtained by connecting an external resistor between the booster and V^- terminals. See curve.

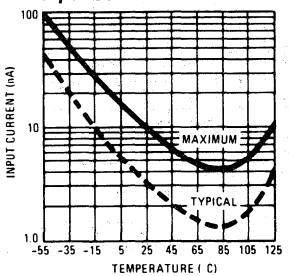
Note 6: Refer to RETS102X for the LM102H military specifications.

APPLICATION HINT

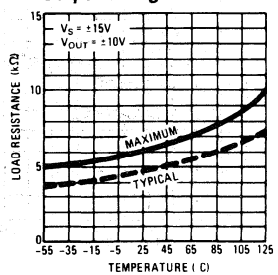
The input must be driven from a source impedance of typically 10 kΩ (5 kΩ Min) to maintain stability. The total source impedance will be reduced at high frequencies if there is stray capacitance at the input pin. In these cases, a 10 kΩ resistor should be inserted in series with the input, physically close to the input pin to minimize the stray capacitance and prevent oscillation.

Guaranteed Performance Characteristics LM102

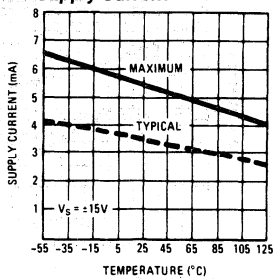
Input Current



Output Swing



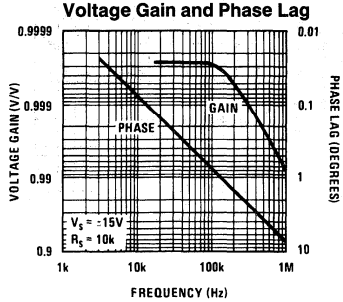
Supply Current



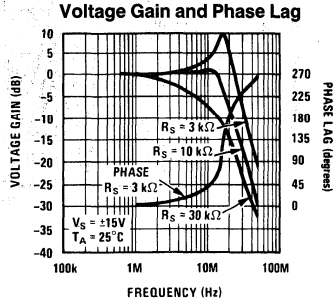
TL/H/7753–7

Typical Performance Characteristics LM102

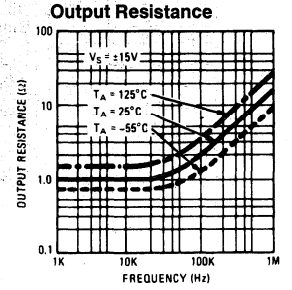
Voltage Gain and Phase Lag



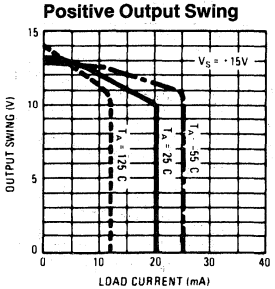
Voltage Gain and Phase Lag



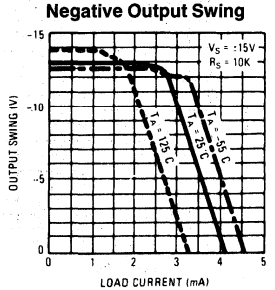
Output Resistance



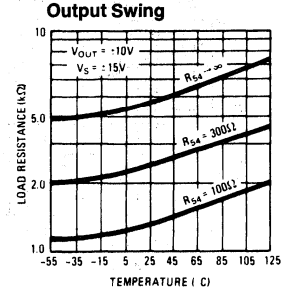
Positive Output Swing



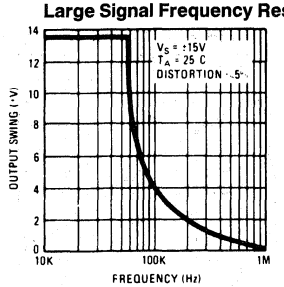
Negative Output Swing



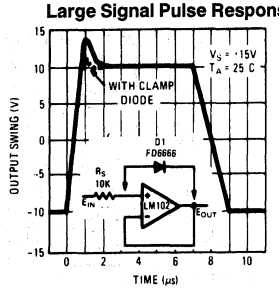
Output Swing



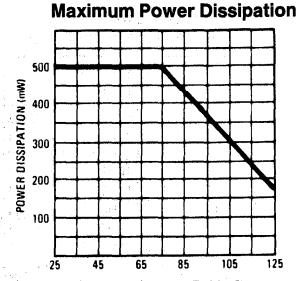
Large Signal Frequency Response



Large Signal Pulse Response



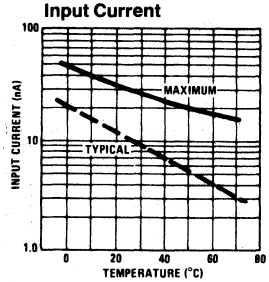
Maximum Power Dissipation



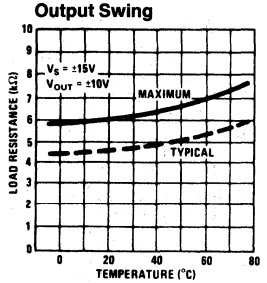
TL/H/7753–8

Guaranteed Performance Characteristics LM302

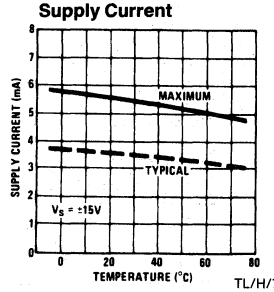
Input Current



Output Swing



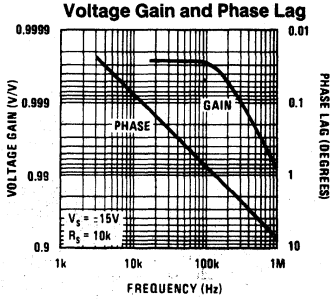
Supply Current



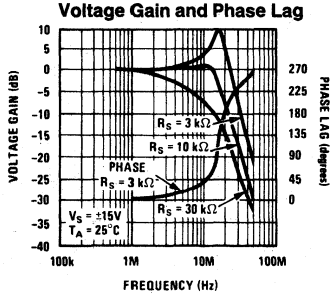
TL/H/7753–9

Typical Performance Characteristics LM302

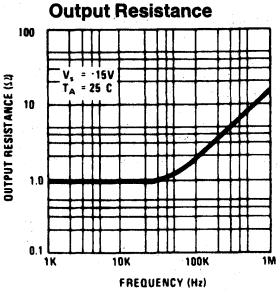
Voltage Gain and Phase Lag



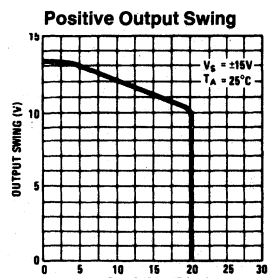
Voltage Gain and Phase Lag



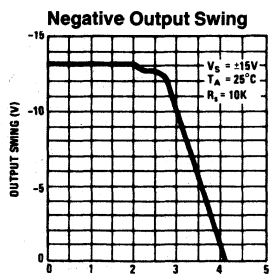
Output Resistance



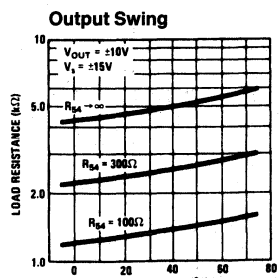
Positive Output Swing



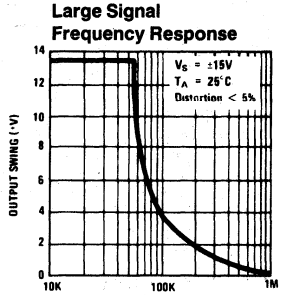
Negative Output Swing



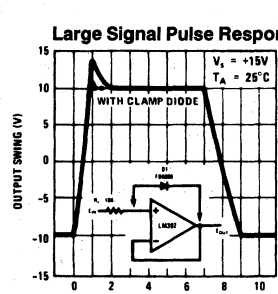
Output Swing



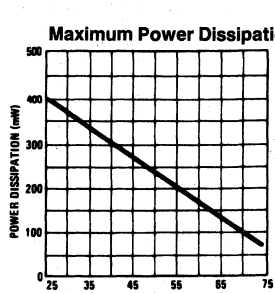
Large Signal Frequency Response



Large Signal Pulse Response



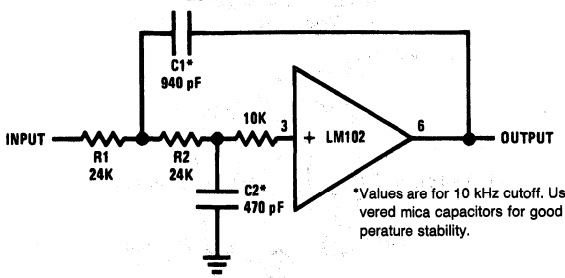
Maximum Power Dissipation



TL/H/7753–10

Typical Applications

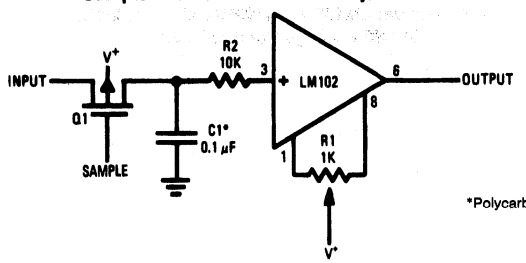
Low Pass Active Filter



*Values are for 10 kHz cutoff. Use silvered mica capacitors for good temperature stability.

TL/H/7753–3

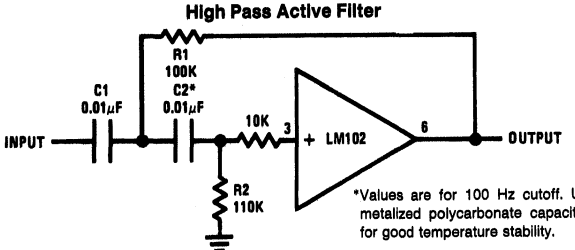
Sample and Hold with Offset Adjustment



*Polycarbonate-dielectric capacitor.

TL/H/7753–4

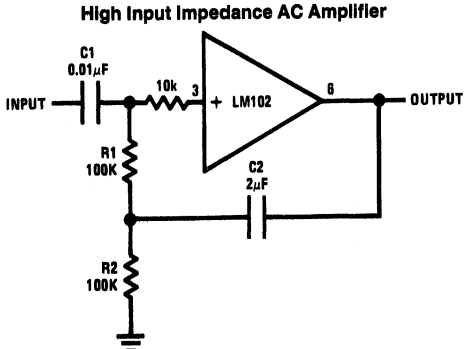
High Pass Active Filter



*Values are for 100 Hz cutoff. Use metalized polycarbonate capacitors for good temperature stability.

TL/H/7753–5

High Input Impedance AC Amplifier



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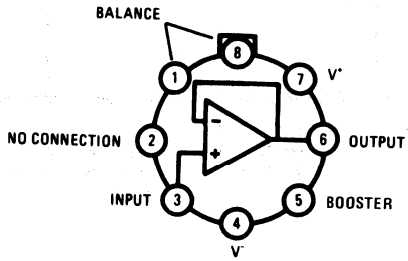
Connection Diagram

Metal Can Package
Top View



TL/H/7753–2

Order Number LM102H, LM102H/883 or LM302H
See NS Package Number H08C

National Semiconductor

LM110/LM210/LM310 Voltage Follower

General Description

The LM110 series are monolithic operational amplifiers internally connected as unity-gain non-inverting amplifiers. They use super-gain transistors in the input stage to get low bias current without sacrificing speed. Directly interchangeable with 101, 741 and 709 in voltage follower applications, these devices have internal frequency compensation and provision for offset balancing.

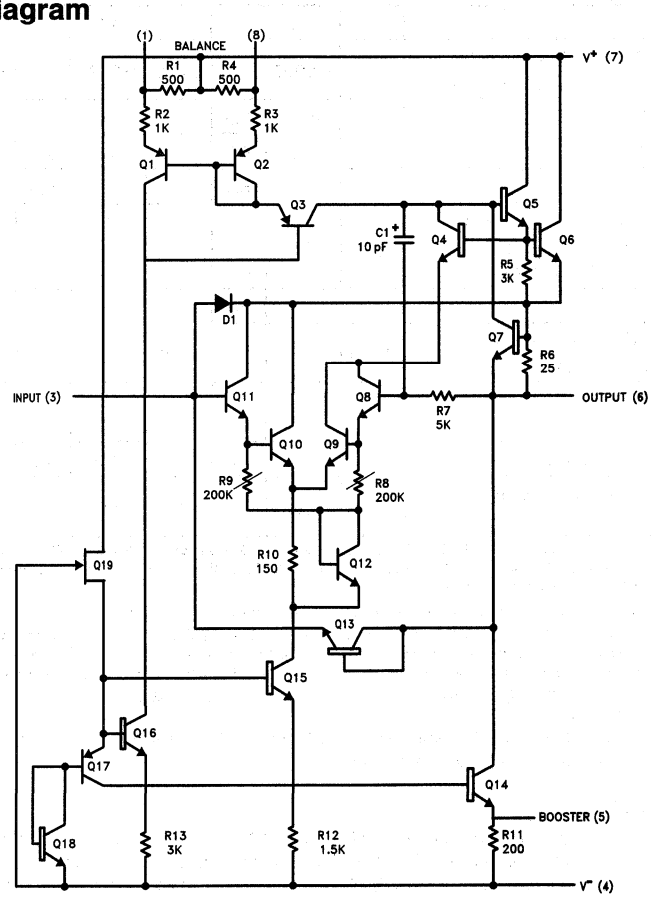
The LM110 series are useful in fast sample and hold circuits, active filters, or as general-purpose buffers. Further, the frequency response is sufficiently better than standard IC amplifiers that the followers can be included in the feedback loop without introducing instability. They are plug-in replacements for the LM102 series voltage followers, offering lower offset voltage, drift, bias current and noise in addition to higher speed and wider operating voltage range.

The LM110 is specified over a temperature range $-55°C \leq T_A \leq +125°C$, the LM210 from $-25°C \leq T_A \leq +85°C$ and the LM310 from $0°C \leq T_A \leq +70°C$.

Features

■ Input current	10 nA max over temperature
■ Small signal bandwidth	20 MHz
■ Slew rate	30 V/μs
■ Supply voltage range	±5V to ±18V

Schematic Diagram



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Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications. (Note 6)

Supply Voltage	±18V
Power Dissipation (Note 1)	500 mW
Input Voltage (Note 2)	±15V
Output Short Circuit Duration (Note 3)	Indefinite
Operating Temperature Range	
LM110	−55°C to +125°C
LM210	−25°C to +85°C
LM310	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec.)	260°C
Soldering Information	
Dual-In-Line Package	
Soldering (10 sec.)	260°C
Small Outline Package	
Vapor Phase (60 sec.)	215°C
Infrared (15 sec.)	220°C

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

ESD rating to be determined.

Electrical Characteristics (Note 4)

Parameter	Conditions	LM110			LM210			LM310			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	$T_A = 25°C$		1.5	4.0		1.5	4.0		2.5	7.5	mV
Input Bias Current	$T_A = 25°C$		1.0	3.0		1.0	3.0		2.0	7.0	nA
Input Resistance	$T_A = 25°C$	10^{10}	10^{12}		10^{10}	10^{12}		10^{10}	10^{12}		Ω
Input Capacitance			1.5			1.5			1.5		pF
Large Signal Voltage Gain	$T_A = 25°C$, $V_S = ±15V$ $V_{OUT} = ±10V$, $R_L = 8\ k\Omega$	0.999	0.9999		0.999	0.9999		0.999	0.9999		V/V
Output Resistance	$T_A = 25°C$		0.75	2.5		0.75	2.5		0.75	2.5	Ω
Supply Current	$T_A = 25°C$		3.9	5.5		3.9	5.5		3.9	5.5	mA
Input Offset Voltage				6.0			6.0			10	mV
Offset Voltage Temperature Drift	$-55°C \le T_A \le +85°C$ $+85 \le T_A \le 125°C$ $0°C \le T_A \le +70°C$		6 12			6			 10		μV/°C μV/°C μV/°C
Input Bias Current				10			10			10	nA
Large Signal Voltage Gain	$V_S = ±15V$, $V_{OUT} = ±10V$ $R_L = 10\ k\Omega$	0.999			0.999			0.999			V/V
Output Voltage Swing (Note 5)	$V_S = ±15V$, $R_L = 10\ k\Omega$	±10			±10			±10			V
Supply Current	$T_A = 125°C$		2.0	4.0		2.0	4.0				mA
Supply Voltage Rejection Ratio	$±5V \le V_S \le ±18V$	70	80		70	80		70	80		dB

Note 1: The maximum junction temperature of the LM110 is 150°C, of the LM210 is 100°C, and of the LM310 is 85°C. For operating at elevated temperatures, devices in the HO8 package must be derated based on a thermal resistance of 165°C/W, junction to ambient, or 22°C/W, junction to case. The thermal resistance of the dual-in-line package is 100°C/W, junction to ambient.

Note 2: For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

Note 3: Continuous short circuit for the LM110 and LM210 is allowed for case temperatures to 125°C and ambient temperatures to 70°C, and for the LM310, 70°C case temperature or 55°C ambient temperature. It is necessary to insert a resistor greater than 2 kΩ in series with the input when the amplifier is driven from low impedance sources to prevent damage when the output is shorted. R_S = 5k min, 10k typical is recommended for dynamic stability in all applications.

Note 4: These specifications apply for $±5V \le V_S \le ±18V$ and $-55°C \le T_A$ 125°C for the LM110, $-25°C \le T_A \le 85°C$ for the LM210, and $0°C \le T_A \le 70°C$ for the LM310 unless otherwise specified.

Note 5: Increased output swing under load can be obtained by connecting an external resistor between the booster and V^- terminals. See curve.

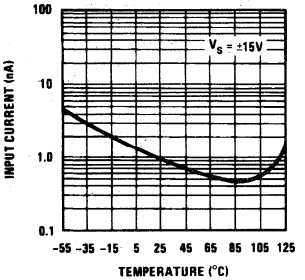
Note 6: Refer to RETS110X for LM110H, LM110J military specifications.

Application Hint

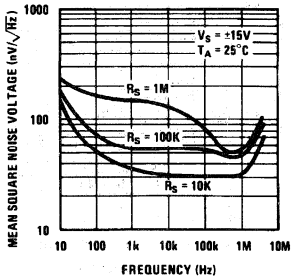
The input must be driven from a source impedance of typically 10 kΩ (5 kΩ min.) to maintain stability. The total source impedance will be reduced at high frequencies if there is stray capacitance at the input pin. In these cases, a 10 kΩ resistor should be inserted in series with the input, physically close to the input pin to minimize the stray capacitance and prevent oscillation.

Typical Performance Characteristics (LM110/LM210)

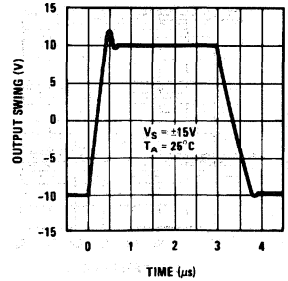
Input Current



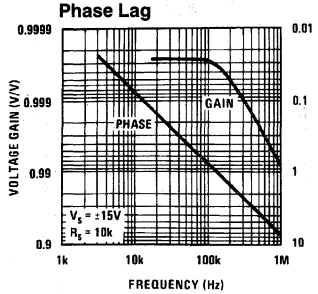
Output Noise Voltage



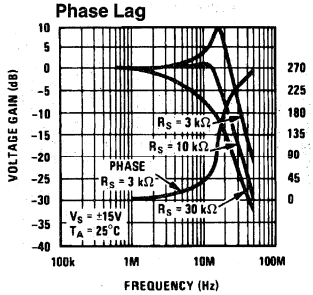
Large Signal Pulse Response



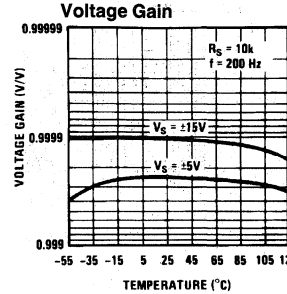
Voltage Gain and Phase Lag



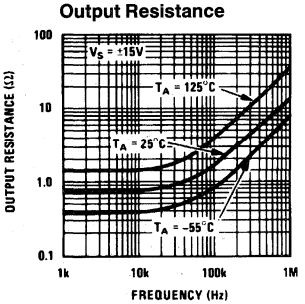
Voltage Gain and Phase Lag



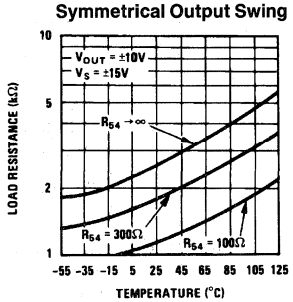
Voltage Gain



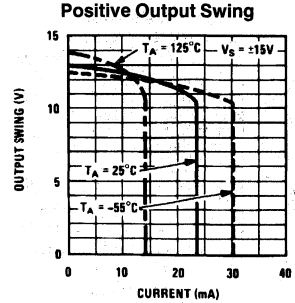
Output Resistance



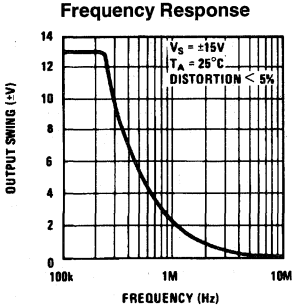
Symmetrical Output Swing



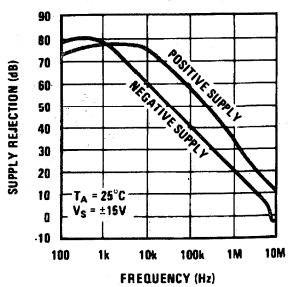
Positive Output Swing



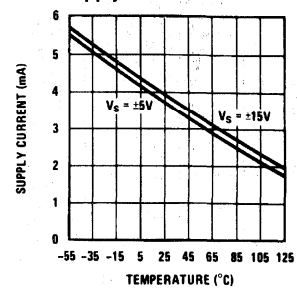
Large Signal Frequency Response



Power Supply Rejection



Supply Current



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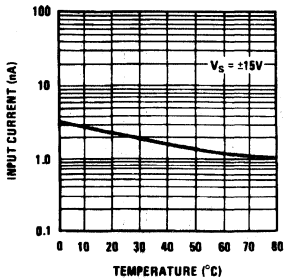
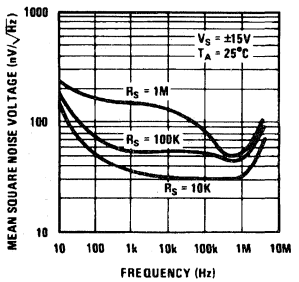
Typical Performance Characteristics (LM310)

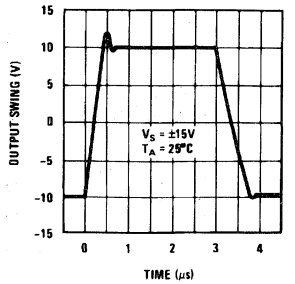
Input Current



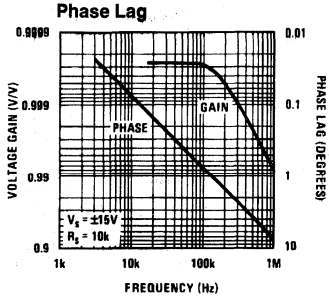
Output Noise Voltage



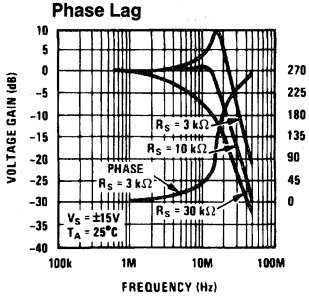
Large Signal Pulse Response



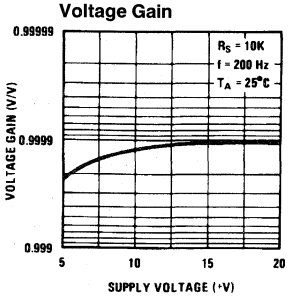
Voltage Gain and Phase Lag



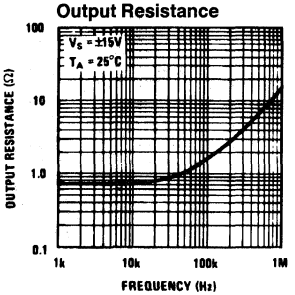
Voltage Gain and Phase Lag



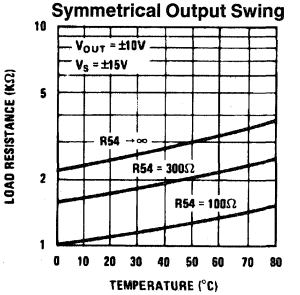
Voltage Gain



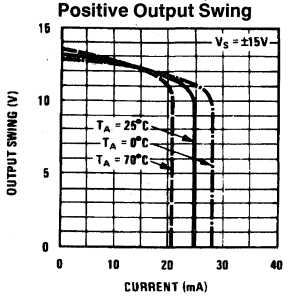
Output Resistance



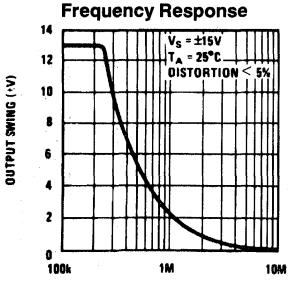
Symmetrical Output Swing



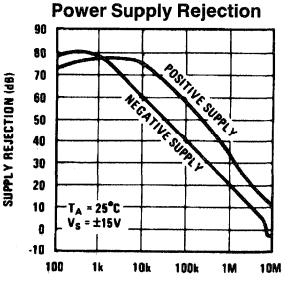
Positive Output Swing



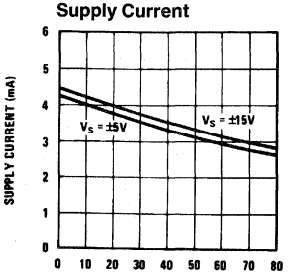
Large Signal Frequency Response



Power Supply Rejection



Supply Current



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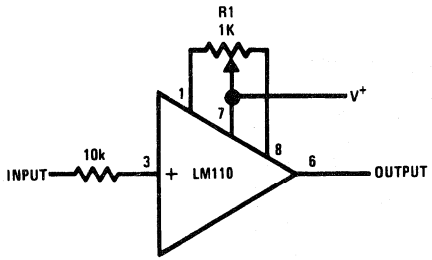
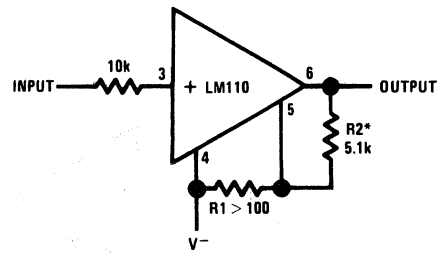
Auxiliary Circuits

Offset Balancing Circuit



TL/H/7761–2

Increasing Negative Swing Under Load

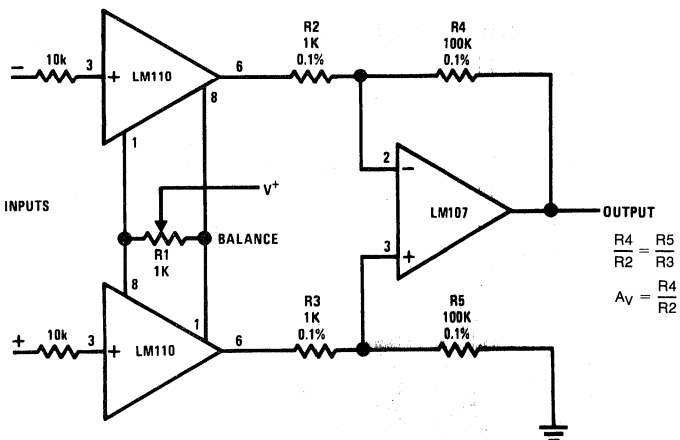


TL/H/7761–3

*May be added to reduce internal dissipation

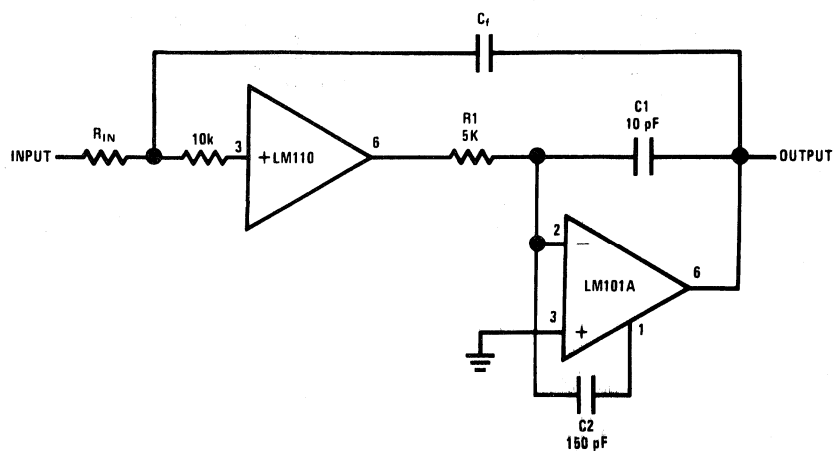
Typical Applications

Differential Input Instrumentation Amplifier



TL/H/7761–4

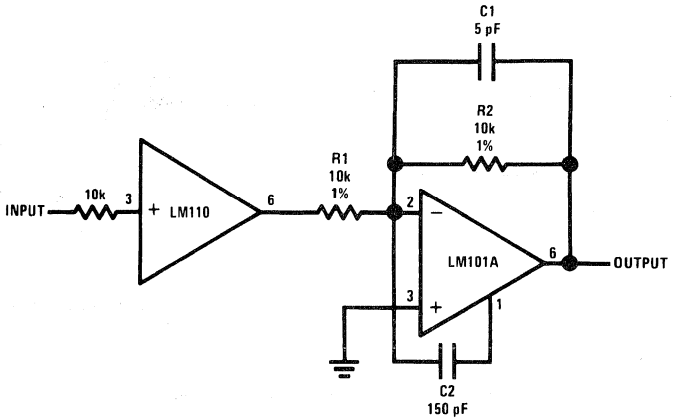
Fast Integrator with Low Input Current



TL/H/7761–5

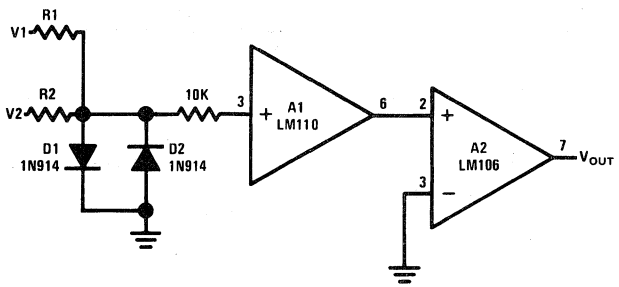
Typical Applications (Continued)

Fast Inverting Amplifier with High Input Impedance



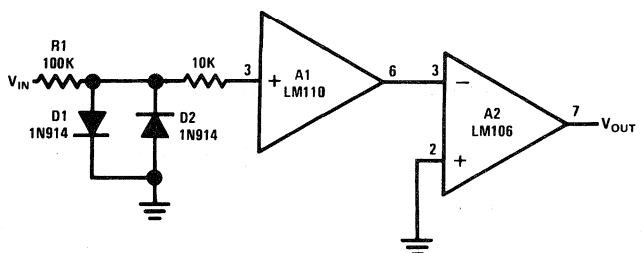
TL/H/7761–6

Comparator for Signals of Opposite Polarity



TL/H/7761–7

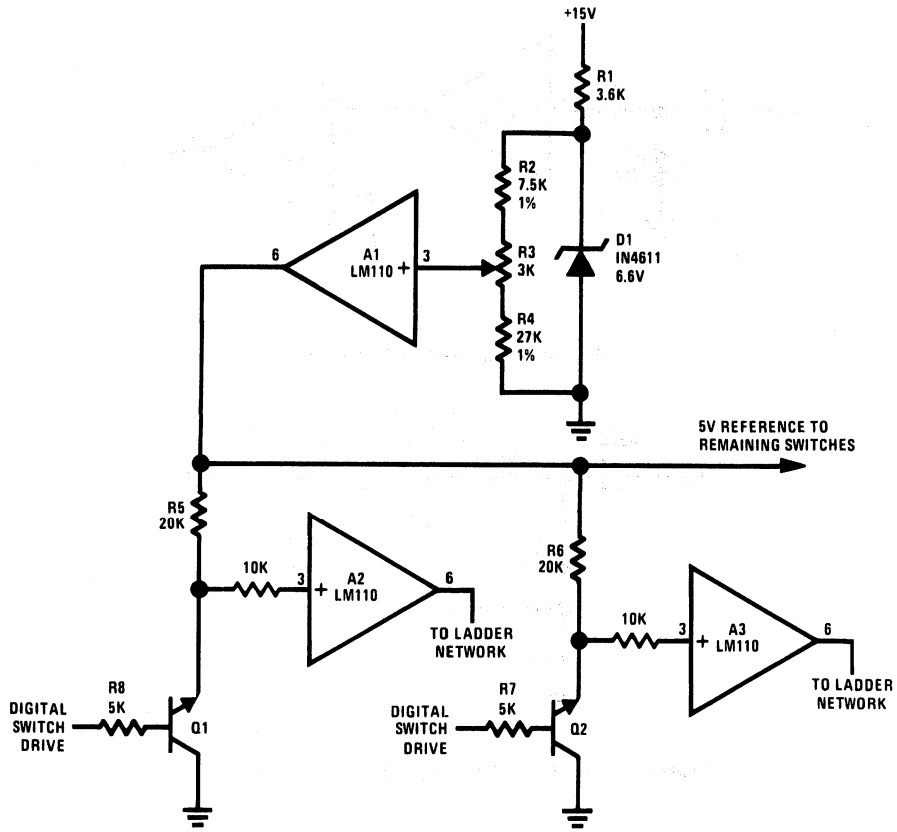
Zero Crossing Detector



TL/H/7761–9

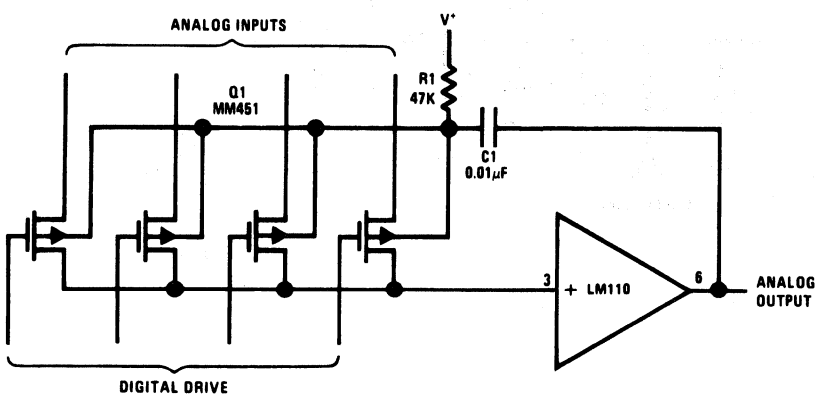
Typical Applications (Continued)

Driver for A/D Ladder Network



TL/H/7761–8

Buffer for Analog Switch*

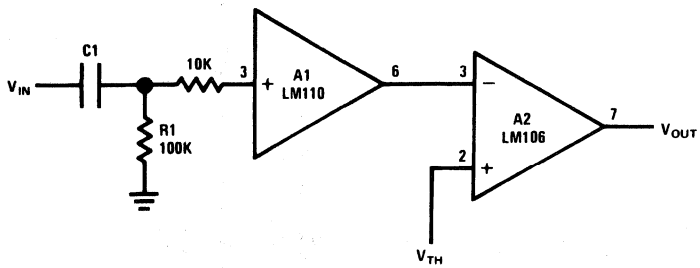


TL/H/7761–10

*Switch substrates are boot-strapped to reduce output capacitance of switch.

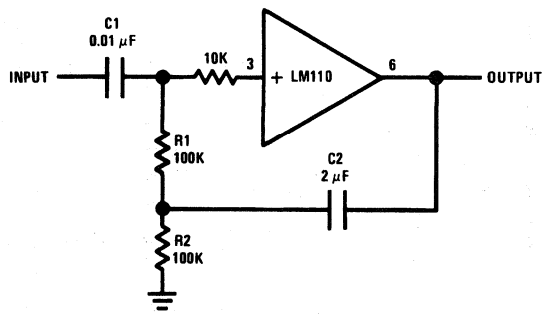
Typical Applications (Continued)

Comparator for AC Coupled Signals



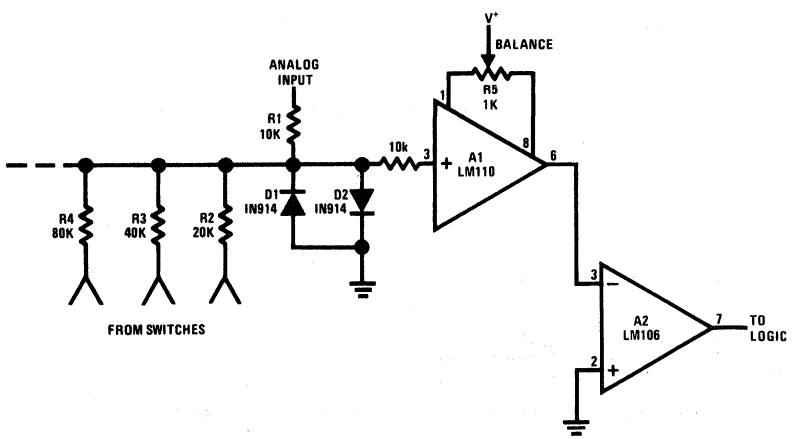
TL/H/7761–11

High Input Impedance AC Amplifier



TL/H/7761–12

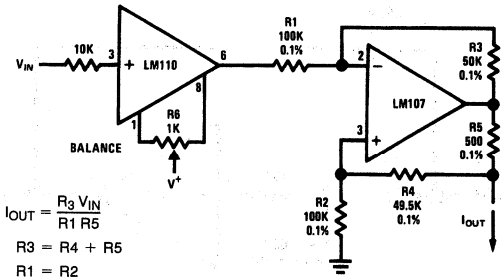
Comparator for A/D Converter Using a Binary-Weighted Network



TL/H/7761–13

Typical Applications (Continued)

Bilateral Current Source



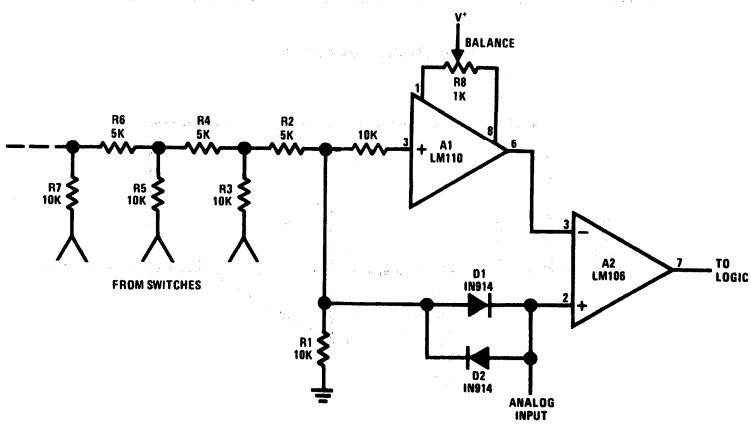
$$I_{OUT} = \frac{R_3 V_{IN}}{R1\ R5}$$

$R3 = R4 + R5$

$R1 = R2$

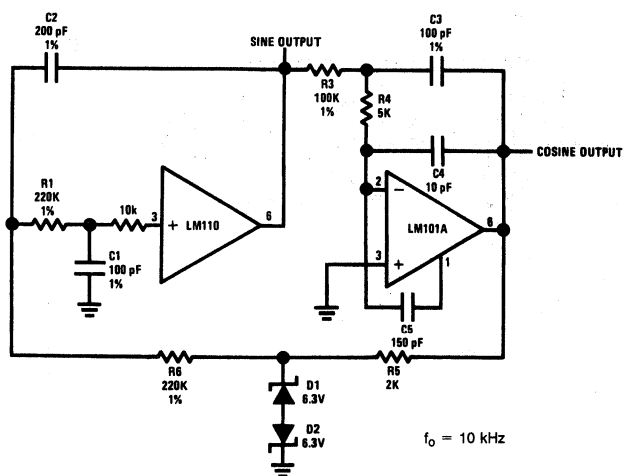
TL/H/7761–14

Comparator for A/D Converter Using a Ladder Network



TL/H/7761–15

Sine Wave Oscillator

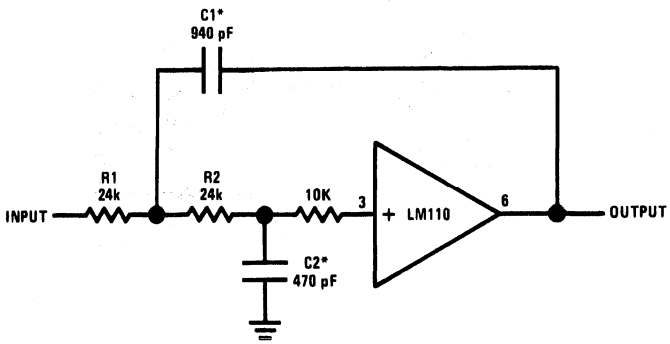


f_O = 10 kHz

TL/H/7761–16

Typical Applications (Continued)

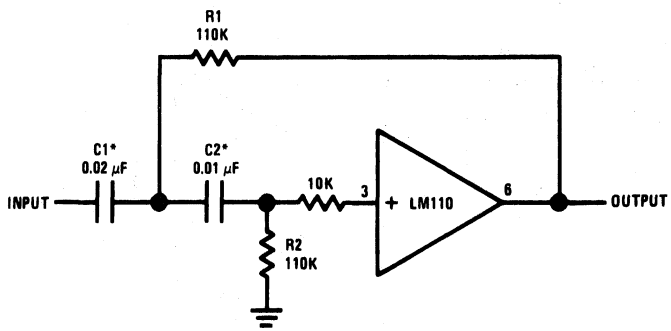
Low Pass Active Filter



TL/H/7761–18

*Values are for 10 kHz cutoff. Use silvered mica capacitors for good temperature stability.

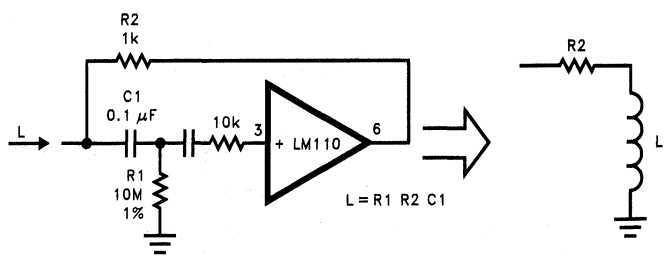
High Pass Active Filter



TL/H/7761–19

*Values are for 100 Hz cutoff. Use metalized polycarbonate capacitors for good temperature stability.

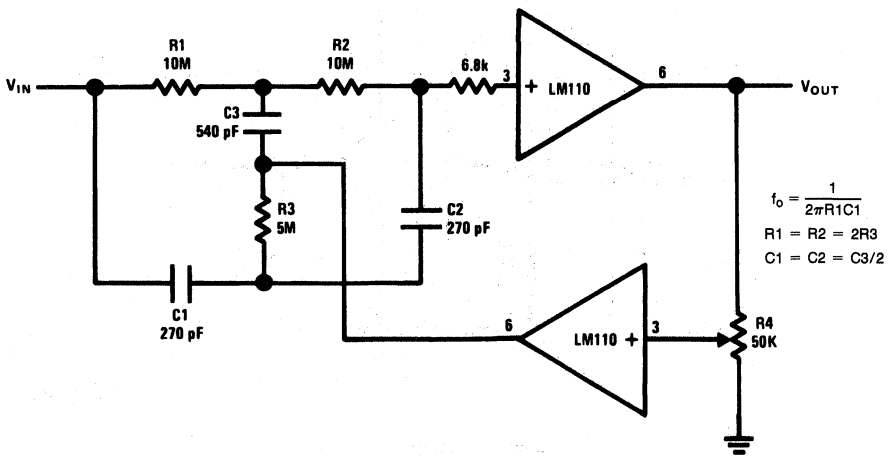
Simulated Inductor



TL/H/7761–21

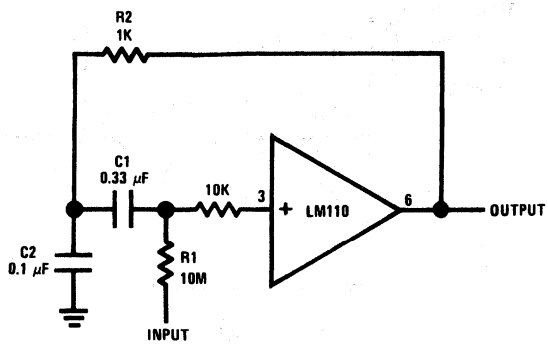
Typical Applications (Continued)

Adjustable Q Notch Filter



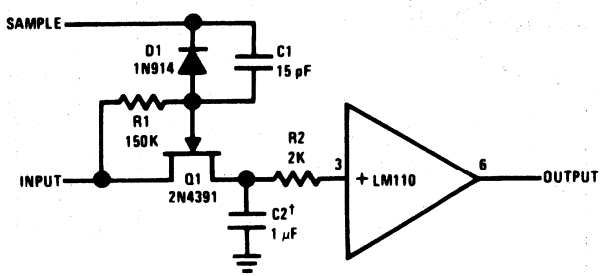
TL/H/7761–22

Bandpass Filter



TL/H/7761–23

Sample and Hold

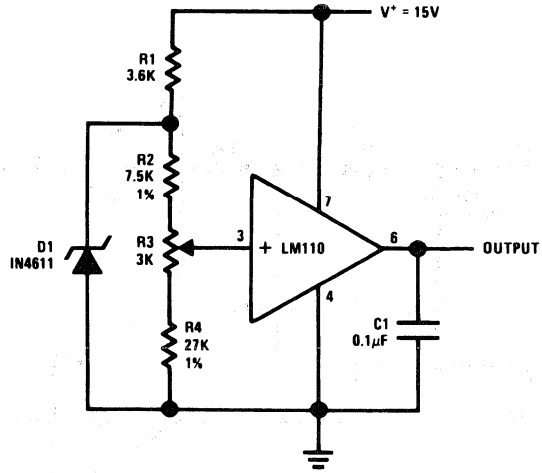


TL/H/7761–24

†Use capacitor with polycarbonate teflon or polythylene dietetric

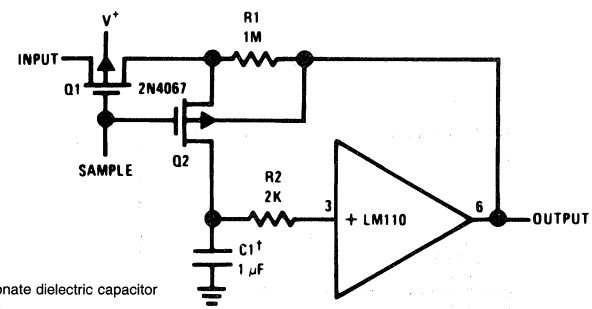
Typical Applications (Continued)

Buffered Reference Source



TL/H/7761–25

Low Drift Sample and Hold*



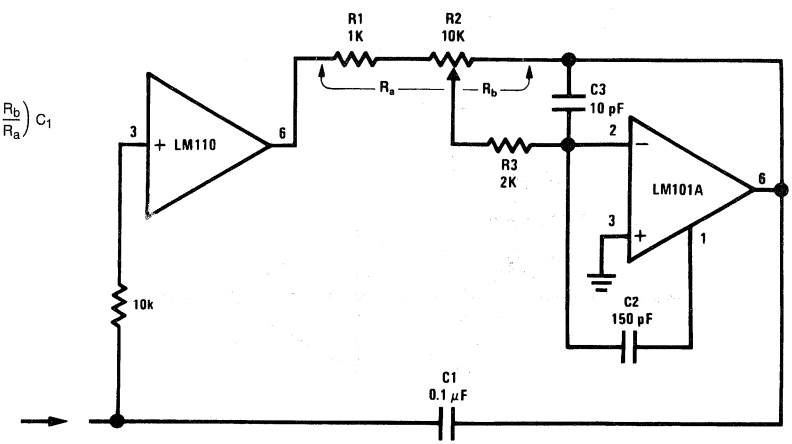
†Teflon polyethylene or polycarbonate dielectric capacitor

*Worst case drift less than 3 mV/sec

TL/H/7761–26

Variable Capacitance Multiplier

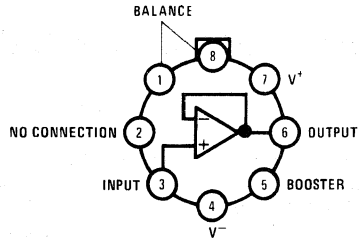
$$C = \left(1 + \frac{R_b}{R_a}\right) C_1$$



TL/H/7761–27

Connection Diagrams

Metal Can Package



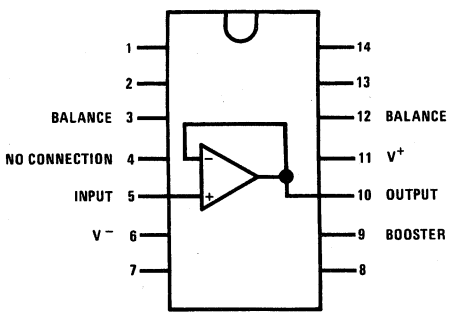
TL/H/7761–30

Package is connected to Pin 4 (V^-)

Top View

Order Number LM110H, LM210H or LM310H
LM110H/883*
See NS Package Number H08C

Dual-In-Line Package

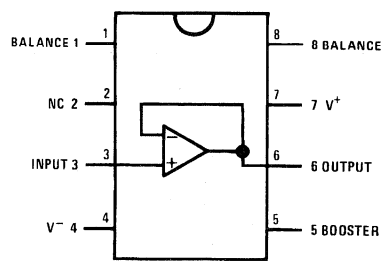


TL/H/7761–31

Top View

Order Number LM110J, LM210J,
LM310J or LM110J/883*
See NS Package Number J14A

Dual-In-Line Package



TL/H/7761–32

Top View

Order Number LM310M, LM310N or LM110J-8/883*
See NS Package Number J08A, M08A or N08E

*Available per SMD# 5962-8760601

National Semiconductor

LM6121/LM6221/LM6321 High Speed Buffer

General Description

These high speed unity gain buffers slew at 800 V/μs and have a small signal bandwidth of 50 MHz while driving a 50Ω load. They can drive ±300 mA peak and do not oscillate while driving large capacitive loads. The LM6121 family are monolithic ICs which offer performance similar to the LH0002 with the additional features of current limit and thermal shutdown.

These buffers are built with National's VIP™ (Vertically Integrated PNP) process which provides fast PNP transistors that are true complements to the already fast NPN devices. This advanced junction-isolated process delivers high speed performance without the need for complex and expensive dielectric isolation.

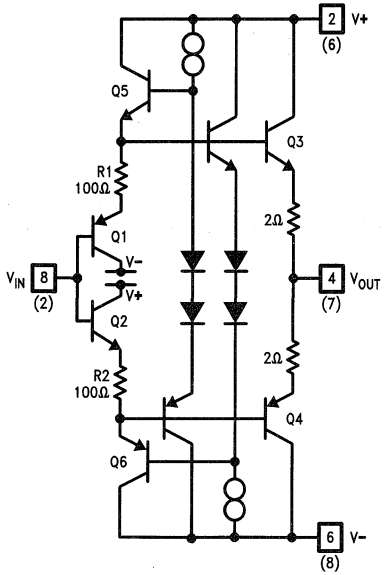
Features

- High slew rate — 800 V/μs
- Wide bandwidth — 50 MHz
- Slew rate and bandwidth 100% tested
- Peak output current — ±300 mA
- High input impedance — 5 MΩ
- LH0002H pin compatible
- No oscillations with capacitive loads
- 5V to ±15V operation guaranteed
- Current and thermal limiting
- Fully specified to drive 50Ω lines

Applications

- Line Driving
- Radar
- Sonar

Simplified Schematic

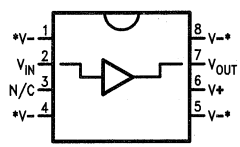


TL/H/9223–1

Numbers in ( ) are for 8-pin N DIP.

Connection Diagrams

Plastic DIP

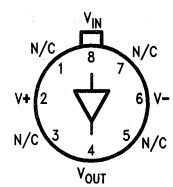


TL/H/9223–2

*Heat-sinking pins. See Application section on heat sinking requirements.

Order Number LM6221N or LM6321N See NS Package Number N08E

Metal Can



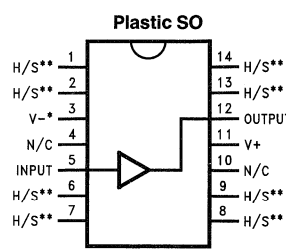
TL/H/9223–3

Top View

Note: Pin 6 connected to case.

Order Number LM6121H, LM6221H or LM6121H/883 See NS Package Number H08C

Plastic SO



TL/H/9223–7

*Pin 3 must be connected to the negative supply.

**Heat-sinking pins. See Application section on heat-sinking requirements. These pins are at V^- potential.

Order Number LM6321M See NS Package Number M14A

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	36V (±18)
Input to Output Voltage (Note 2)	±7V
Input Voltage	±Vsupply
Output Short-Circuit to GND (Note 3)	Continuous
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	260°C
Power Dissipation	(Note 10)
ESD Tolerance (Note 8)	±2000V
Junction Temperature ($T_{J(max)}$)	150°C

Operating Ratings

Operating Temperature Range	
LM6121, LM6121H/883	−55°C to +125°C
LM6221	−40°C to +85°C
LM6321	0°C to +70°C
Operating Supply Range	4.75 to ±16V
Thermal Resistance (θ_{JA}), (Note 4)	
H Package	150°C/W
N Package	47°C/W
M Package	69°C/W
Thermal Resistance (θ_{JC}), H Package	17°C/W

DC Electrical Characteristics

The following specifications apply for Supply Voltage = ±15V, V_{CM} = 0, $R_L \geq 100\ k\Omega$ and $R_S = 50\Omega$ unless otherwise noted. **Boldface** limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX}; all other limits $T_A = T_J = 25°C$.

Symbol	Parameter	Conditions	Typ	LM6121 Limit (Notes 5, 9)	LM6221 Limit (Note 5)	LM6321 Limit (Note 5)	Units
A_{V1}	Voltage Gain 1	$R_L = 1\ k\Omega$, $V_{IN} = \pm 10V$	0.990	0.980 **0.970**	0.980 **0.950**	0.970 **0.950**	V/V Min
A_{V2}	Voltage Gain 2	$R_L = 50\Omega$, $V_{IN} = \pm 10V$	0.900	0.860 **0.800**	0.860 **0.820**	0.850 **0.820**	
A_{V3}	Voltage Gain 3 (Note 6)	$R_L = 50\Omega$, $V^+ = 5V$ $V_{IN} = 2\ V_{pp}$ **(1.5 V_{pp})**	0.840	0.780 **0.750**	0.780 **0.700**	0.750 **0.700**	
V_{OS}	Offset Voltage	$R_L = 1\ k\Omega$	15	30 **50**	30 **60**	50 **100**	mV Max
I_B	Input Bias Current	$R_L = 1\ k\Omega$, $R_S = 10\ k\Omega$	1	4 **7**	4 **7**	5 **7**	μA Max
R_{IN}	Input Resistance	$R_L = 50\Omega$	5				MΩ
C_{IN}	Input Capacitance		3.5				pF
R_O	Output Resistance	$I_{OUT} = \pm 10$ mA	3	5 **10**	5 **10**	5 **6**	Ω Max
I_{S1}	Supply Current 1	$R_L = \infty$	15	18 **20**	18 **20**	20 **22**	mA Max
I_{S2}	Supply Current 2	$R_L = \infty$, $V^+ = 5V$	14	16 **18**	16 **18**	18 **20**	
V_{O1}	Output Swing 1	$R_L = 1k$	13.5	13.3 **13**	13.3 **13**	13.2 **13**	±V Min
V_{O2}	Output Swing 2	$R_L = 100\Omega$	12.7	11.5 **10**	11.5 **10**	11 **10**	
V_{O3}	Output Swing 3	$R_L = 50\Omega$	12	11 **9**	11 **9**	10 **9**	
V_{O4}	Output Swing 4	$R_L = 50\Omega$, $V^+ = 5V$ (Note 6)	1.8	1.6 **1.3**	1.6 **1.4**	1.6 **1.5**	V_{PP} Min
PSSR	Power Supply Rejection Ratio	$V^{\pm} = \pm 5V$ to $\pm 15V$	70	60 **55**	60 **50**	60 **50**	dB Min

AC Electrical Characteristics

The following specifications apply for Supply Voltage = ±15V, V_{CM} = 0, $R_L \geq 100\ k\Omega$ and $R_S = 50\Omega$ unless otherwise noted. **Boldface** limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX}; all other limits $T_A = T_J = 25°C$.

Symbol	Parameter	Conditions	Typ	LM6121 Limit (Note 5)	LM6221 Limit (Note 5)	LM6321 Limit (Note 5)	Units
SR_1	Slew Rate 1	$V_{IN} = \pm 11V$, $R_L = 1\ k\Omega$	1200	550	550	550	V/μs Min
SR_2	Slew Rate 2	$V_{IN} = \pm 11V$, $R_L = 50\Omega$ (Note 7)	800	550	550	550	
SR_3	Slew Rate 3	$V_{IN} = 2\ V_{PP}$, $R_L = 50\Omega$ $V^+ = 5V$ (Note 6)	50	550	550	550	
BW	−3 dB Bandwidth	$V_{IN} = \pm 100\ mV_{PP}$, $R_L = 50\Omega$ $C_L \leq 10\ pF$	50	30	30	30	MHz Min
t_r, t_f	Rise Time Fall Time	$R_L = 50\Omega$, $C_L \leq 10\ pF$ $V_O = 100\ mV_{PP}$	7.0				ns
t_{pd}	Propagation Delay Time	$R_L = 50\Omega$, $C_L \leq 10\ pF$ $V_O = 100\ mV_{PP}$	4.0				ns
O_S	Overshoot	$R_L = 50\Omega$, $C_L \leq 10\ pF$ $V_O = 100\ mV_{PP}$	10				%

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its rated operating conditions.

Note 2: During current limit or thermal limit, the input current will increase if the input to output differential voltage exceeds 8V. For input to output differential voltages in excess of 8V the input current should be limited to ±20 mA.

Note 3: The LM6121 series buffers contain current limit and thermal shutdown to protect against fault conditions.

Note 4: The thermal resistance θ_{JA} of the device in the N package is measured when soldered directly to a printed circuit board, and the heat-sinking pins (pins 1, 4, 5 and 8) are connected to 2 square inches of 2 oz. copper. When installed in a socket, the thermal resistance θ_{JA} of the N package is 84°C/W. The thermal resistance θ_{JA} of the device in the M package is measured when soldered directly to a printed circuit board, and the heat-sinking pins (pins 1, 2, 6, 7, 8, 9, 13, 14) are connected to 1 square inch of 2 oz. copper.

Note 5: Limits are guaranteed by testing or correlation.

Note 6: The input is biased to 2.5V and V_{IN} swings V_{pp} about this value. The input swing is 2 V_{pp} at all temperatures except for the A_V3 test at −55°C where it is reduced to 1.5 V_{pp}.

Note 7: Slew rate is measured with a ±11V input pulse and 50Ω source impedance at 25°C. Since voltage gain is typically 0.9 driving a 50Ω load, the output swing will be approximately ±10V. Slew rate is calculated for transitions between ±5V levels on both rising and falling edges. A high speed measurement is done to minimize device heating. For slew rate versus junction temperature see typical performance curves. The input pulse amplitude should be reduced to ±10V for measurements at temperature extremes. For accurate measurements, the input slew rate should be at least 1700 V/μs.

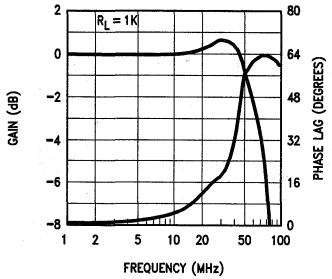
Note 8: The test circuit consists of the human body model of 120 pF in series with 1500Ω.

Note 9: A military RETS specification is available on request. At the time of printing, the LM6121H/883 RETS spec complied with the **Boldface** limits in this column. The LM6121H/883 may also be procured as Standard Military Drawing specification #5962-9081201MXA.

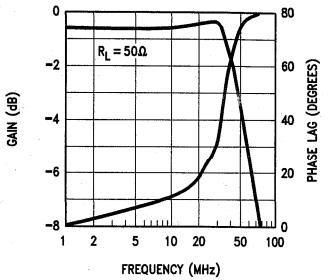
Note 10: The maximum power dissipation is a function of $T_{J(max)}$, θ_{JA}, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(max)} - T_A)/\theta_{JA}$.

Typical Performance Characteristics T_J = 25°C, unless otherwise specified

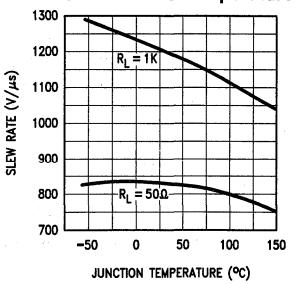
Frequency Response



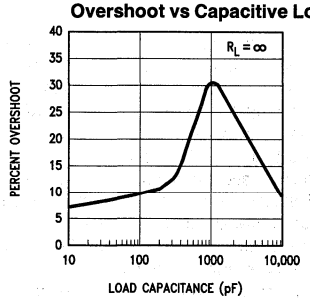
Frequency Response



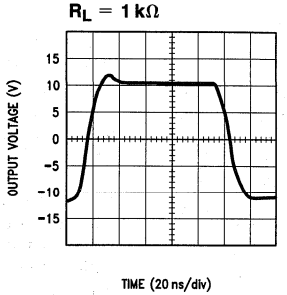
Slew Rate vs Temperature



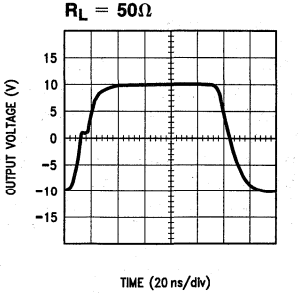
Overshoot vs Capacitive Load



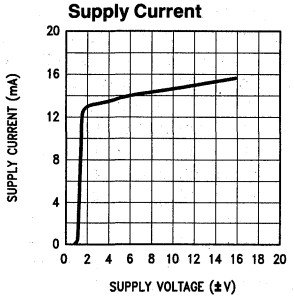
Large Signal Response
R_L = 1 kΩ



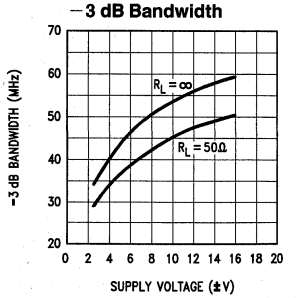
Large Signal Response
R_L = 50Ω



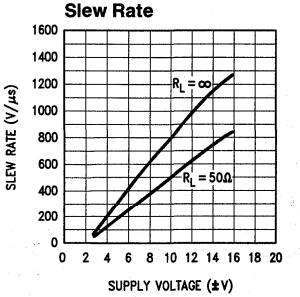
Supply Current



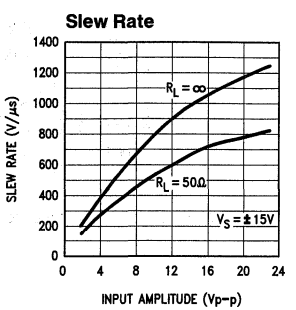
−3 dB Bandwidth



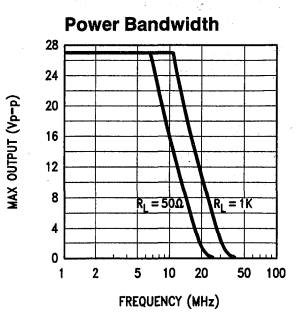
Slew Rate



Slew Rate



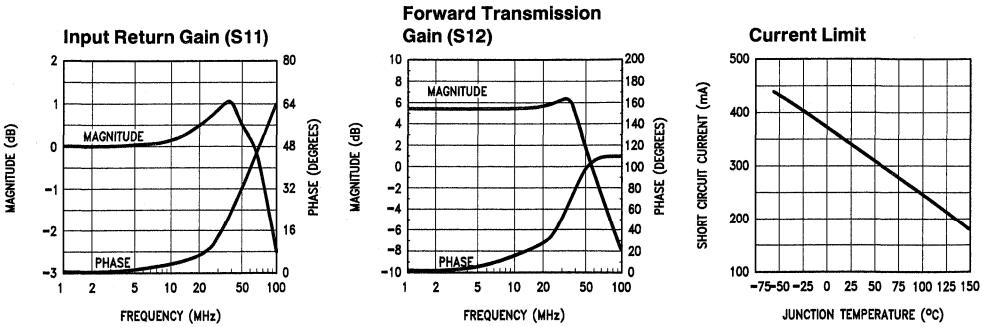
Power Bandwidth



TL/H/9223–4

2

Typical Performance Characteristics T_J = 25°C, unless otherwise specified (Continued)



TL/H/9223–5

Application Hints

POWER SUPPLY DECOUPLING

The method of supply bypassing is not critical for stability of the LM6121 series buffers. However, their high current output combined with high slew rate can result in significant voltage transients on the power supply lines if much inductance is present. For example, a slew rate of 900 V/μs into a 50Ω load produces a di/dt of 18 A/μs. Multiplying this by a wiring inductance of 50 nH (which corresponds to approximately 1½" of 22 gauge wire) result in a 0.9V transient. To minimize this problem use high quality decoupling very close to the device. Suggested values are a 0.1 μF ceramic in parallel with one or two 2.2 μF tantalums. A ground plane is recommended.

LOAD IMPEDANCE

The LM6121 is stable to any load when driven by a 50Ω source. As shown in the *Overshoot vs Capacitive Load* graph, worst case is a purely capacitive load of about 1000 pF. Shunting the load capacitance with a resistor will reduce overshoot.

SOURCE INDUCTANCE

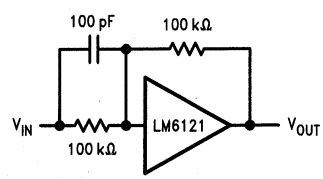
Like any high frequency buffer, the LM6121 can oscillate at high values of source inductance. The worst case condition occurs at a purely capacitive load of 50 pF where up to 100 nH of source inductance can be tolerated. With a 50Ω load, this goes up to 200 nH. This sensitivity may be reduced at the expense of a slight reduction in bandwidth by adding a resistor in series with the buffer input. A 100Ω resistor will ensure stability with source inductances up to 400 nH with any load.

OVERVOLTAGE PROTECTION

The LM6121 may be severely damaged or destroyed if the Absolute Maximum Rating of 7V between input and output pins is exceeded.

If the buffer's input-to-output differential voltage is allowed to exceed 7V, a base-emitter junction will be in reverse-breakdown, and will be in series with a forward-biased base-emitter junction. Referring to the LM6121 simplified schematic, the transistors involved are Q1 and Q3 for positive inputs, and Q2 and Q4 for negative inputs. If any current is allowed to flow through these junctions, localized heating of the reverse-biased junction will occur, potentially causing damage. The effect of the damage is typically increased offset voltage, increased bias current, and/or degraded AC performance. Furthermore, this will defeat the short-circuit and over-temperature protection circuitry. Exceeding ±7V input with a shorted output will destroy the device.

The device is best protected by the insertion of the parallel combination of a 100 kΩ resistor (R1) and a small capacitor (C1) in series with the buffer input, and a 100 kΩ resistor (R2) from input to output of the buffer (see *Figure 1*). This network normally has no effect on the buffer output. However, if the buffer's current limit or shutdown is activated, and the output has a ground-referred load of significantly less than 100 kΩ, a large input-to-output voltage may be present. R1 and R2 then form a voltage divider, keeping the input-output differential below the 7V Maximum Rating for input voltages up to 14V. This protection network should be sufficient to protect the LM6121 from the output of nearly any op amp which is operated on supply voltages of ±15V or lower.



TL/H/9223–6

FIGURE 1. LM6121 with Overvoltage Protection

Application Hints

HEATSINK REQUIREMENTS

A heatsink may be required with the LM6321 depending on the maximum power dissipation and maximum ambient temperature of the application. Under all possible operating conditions, the junction temperature must be within the range specified under Absolute Maximum Ratings.

To determine if a heatsink is required, the maximum power dissipated by the buffer, P(max), must be calculated. The formula for calculating the maximum allowable power dissipation in any application is $P_D = (T_J(max) - T_A)/\theta_{JA}$. For the simple case of a buffer driving a resistive load as in *Figure 2*, the maximum DC power dissipation occurs when the output is at half the supply. Assuming equal supplies, the formula is $P_D = I_S (2V^+) + V^{+2}/2\ R_L$.

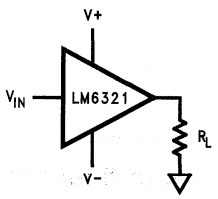


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FIGURE 2

The next parameter which must be calculated is the maximum allowable temperature rise, $T_R(max)$. This is calculated by using the formula:

$$T_R(max) = T_J(max) - T_A(max)$$

where: $T_J(max)$ is the maximum allowable junction temperature

$T_A(max)$ is the maximum ambient temperature

Using the calculated values for $T_R(max)$ and P(max), the required value for junction-to-ambient thermal resistance, $\theta_{(J-A)}$, can now be found:

$$\theta_{(J-A)} = T_R(max)/P(max)$$

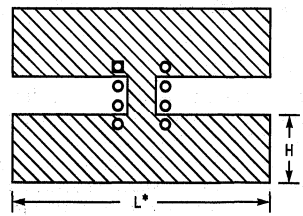
The heatsink for the LM6321 is made using the PC board copper. The heat is conducted from the die, through the lead frame (inside the part), and out the pins which are soldered to the PC board. The pins used for heat conduction are:

TABLE I

Part	Package	Pins
LM6321N	8-Pin DIP	1, 4, 5, 8
LM6321M	14-Pin SO	1, 2, 3, 6, 7, 8, 9, 13, 14

Figure 3 shows copper patterns which may be used to dissipate heat from the LM6321.

8-Pin DIP



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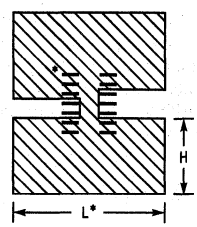
14-Pin SO



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*For best results, use L = 2H

FIGURE 3. Copper Heatsink Patterns

Table II shows some values of junction-to-ambient thermal resistance (θ_{J-A}) for values of L and W for 2 oz. copper:

TABLE II

Package	L (in.)	H (in.)	θ_{J-A} (°C/W)
8-Pin DIP	2	0.5	47
14-Pin SO	1	0.5	69
	2	1	57

National Semiconductor

LM6125/LM6225/LM6325 High Speed Buffer

General Description

The LM6125 family of high speed unity gain buffers slew at 800 V/μs and have a small signal bandwidth of 50 MHz while driving a 50Ω load. These buffers drive ±300 mA peak and do not oscillate while driving large capacitive loads. The LM6125 contains unique features not found in power buffers; these include current limit, thermal shutdown, electronic shutdown, and an error flag that warns of fault conditions.

These buffers are built with National's VIP™ (Vertically Integrated PNP) process which provides fast PNP transistors that are true complements to the already fast NPN devices. This advanced junction-isolated process delivers high speed performance without the need for complex and expensive dielectric isolation.

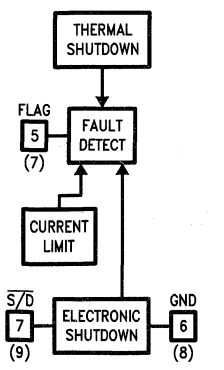
Features

- High slew rate 800 V/μs
- High output current ±300 mA
- Stable with large capacitive loads
- Current and thermal limiting
- Electronic shutdown
- 5V to ±15V operation guaranteed
- Fully specified to drive 50Ω lines

Applications

- Line Driving
- Radar
- Sonar

Simplified Schematic and Block Diagram



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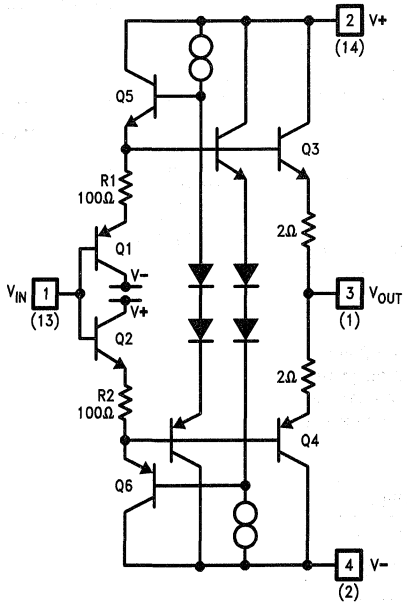

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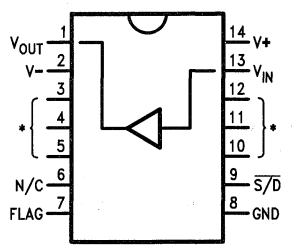
Numbers in ( ) are for 14-pin N DIP.

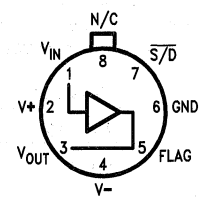
Pin Configurations



TL/H/9222-3

*Heat sinking pins.
Internally connected to V−.

Order Number LM6225N or LM6325N
See NS Package Number N14A



TL/H/9222-4

Top View
Note: Pin 4 connected to case

Order Number LM6125H or LM6125H/883*
See NS Package Number H08C

*Available per 5962-9081501

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	36V (±18V)
Input to Output Voltage (Note 2)	±7V
Input Voltage	±Vsupply
Output Short-Circuit to GND (Note 3)	Continuous
Flag Output Voltage	GND ≤ Vflag ≤ +Vsupply
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	260°C
ESD Tolerance (Note 9)	±1500V
θ_{JA} (Note 4)	
H Package	150°C/W
N Package	40°C/W
Maximum Junction Temperature (T_J)	150°C
Operating Temperature Range	
LM6125	−55°C to +125°C
LM6225	−40°C to +85°C
LM6325	0°C to +70°C
Operating Supply Voltage Range	4.75V to ±16V

DC Electrical Characteristics

The following specifications apply for Supply Voltage = ±15V, V_{CM} = 0, $R_L \geq 100\ k\Omega$ and $R_S = 50\Omega$ unless otherwise noted. **Boldface** limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX}; all other limits $T_A = T_J = 25°C$.

Symbol	Parameter	Conditions	Typ	LM6125 Limit (Notes 5, 10)	LM6225 Limit (Note 5)	LM6325 Limit (Note 5)	Units
A_{V1}	Voltage Gain 1	$R_L = 1k\Omega$, $V_{IN} = \pm 10V$	0.990	0.980 **0.970**	0.980 **0.950**	0.970 **0.950**	V/V Min
A_{V2}	Voltage Gain 2	$R_L = 50\Omega$, $V_{IN} = \pm 10V$	0.900	0.860 **0.800**	0.860 **0.820**	0.850 **0.820**	
A_{V3}	Voltage Gain 3 (Note 6)	$R_L = 50\Omega$, $V^+ = 5V$ $V_{IN} = 2\ V_{PP}$ **(1.5 V_{PP})**	0.840	0.780 **0.750**	0.780 **0.700**	0.750 **0.700**	
V_{OS}	Offset Voltage	$R_L = 1\ k\Omega$	15	30 **50**	30 **60**	50 **100**	mV Max
I_B	Input Bias Current	$R_L = 1\ k\Omega$, $R_S = 10\ k\Omega$	1	4 **7**	4 **7**	5 **7**	μA Max
R_{IN}	Input Resistance	$R_L = 50\Omega$	5				MΩ
C_{IN}	Input Capacitance		3.5				pF
R_O	Output Resistance	$I_{OUT} = \pm 10$ mA	3	5 **10**	5 **10**	5 **6**	Ω Max
I_{S1}	Supply Current 1	$R_L = \infty$	15	18 **20**	18 **20**	20 **22**	mA Max
I_{S2}	Supply Current 2	$R_L = \infty$, $V^+ = 5V$	14	16 **18**	16 **18**	18 **20**	
$I_{S/D}$	Supply Current in Shutdown	$R_L = \infty$, $V^{\pm} = \pm 15V$	1.1	1.5 **2.0**	1.5 **2.0**	1.5 **2.0**	
V_{O1}	Output Swing 1	$R_L = 1\ k\Omega$	13.5	13.3 **13**	13.3 **13**	13.2 **13**	±V Min
V_{O2}	Output Swing 2	$R_L = 100\Omega$	12.7	11.5 **10**	11.5 **10**	11 **10**	
V_{O3}	Output Swing 3	$R_L = 50\Omega$	12	11 **9**	11 **9**	10 **9**	
V_{O4}	Output Swing 4	$R_L = 50\Omega$	1.8	1.6 **1.3**	1.6 **1.4**	1.6 **1.5**	V_{PP} Min
PSRR	Power Supply Rejection Ratio	$V^+ = 5V$ (Note 6)	70	60 **55**	60 **50**	60 **50**	dB Min
V_{OL}	Flag Pin Output Low Voltage	$V^{\pm} = \pm 5V$ to $\pm 15V$ $V_{S/D} = 0V$		300 **400**	300 **400**	340 **400**	mV Max
I_{OH}	Flag Pin Output High Current	V_{OH} Flag Pin = 15V (Note 7)	0.01	10 **20**	10 **20**	10 **20**	μA Max

DC Electrical Characteristics (Continued)

The following specifications apply for Supply Voltage = ±15V, V_{CM} = 0, $R_L \geq 100\ k\Omega$ and $R_S = 50\Omega$ unless otherwise noted. **Boldface** limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX}; all other limits $T_A = T_J = 25°C$.

Symbol	Parameter	Conditions	Typ	LM6125 Limit (Notes 5, 10)	LM6225 Limit (Note 5)	LM6325 Limit (Note 5)	Units
V_{TH}	Shutdown Threshold		1.4				V
V_{IH}	Shutdown Pin Trip Point High			2.0 **2.0**	2.0 **2.0**	2.0 **2.0**	V Min
V_{IL}	Shutdown Pin Trip Point Low			0.8 **0.8**	0.8 **0.8**	0.8 **0.8**	V Max
I_{IL}	Shutdown Pin Input Low Current	$V_{S/D}$ = 0V	−0.07	−10 **−20**	−10 **−20**	−10 **−20**	μA Max
I_{IH}	Shutdown Pin Input High Current	$V_{S/D}$ = 5V	−0.05	−10 **−20**	−10 **−20**	−10 **−20**	μA Max
I_O	Bi-State Output Current	Shutdown Pin = 0V V_{OUT} = +5V or −5V	1	50 **2000**	50 **100**	100 **200**	μA

AC Electrical Characteristics

The following specifications apply for Supply Voltage = ±15V, V_{CM} = 0, $R_L \geq 100\ k\Omega$ and $R_S = 50\Omega$ unless otherwise noted. **Boldface** limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX}; all other limits $T_A = T_J = 25°C$.

Symbol	Parameter	Conditions	Typ	LM6125 Limit (Note 5)	LM6225 Limit (Note 5)	LM6325 Limit (Note 5)	Units
SR_1	Slew Rate 1	V_{IN} = ±11V, R_L = 1 kΩ	1200				
SR_2	Slew Rate 2	V_{IN} = ±11V, R_L = 50Ω (Note 8)	800	550	550	550	V/μs Min
SR_3	Slew Rate 3	V_{IN} = 2 V_{PP}, R_L = 50Ω V^+ = 5V (Note 6)	50				
BW	−3 dB Bandwidth	V_{IN} = 100 mV_{PP} R_L = 50Ω, $C_L \leq$ 10 pF	50	30	30	30	MHz Min
t_r, t_f	Rise Time Fall Time	R_L = 50Ω, $C_L \leq$ 10 pF V_O = 100 mV_{PP}	8.0				ns
t_{PD}	Propagation Delay Time	R_L = 50Ω, $C_L \leq$ 10 pF V_O = 100 mV_{PP}	4.0				ns
O_S	Overshoot	R_L = 50Ω, $C_L \leq$ 10 pF V_O = 100 mV_{PP}	10				%
V_{FT}	V_{IN}, V_{OUT} Feedthrough in Shutdown	Shutdown Pin = 0V V_{IN} = 4 V_{PP}, 1 MHz R_L = 50Ω	−50				dB
C_{OUT}	Output Capacitance in Shutdown	Shutdown Pin = 0V	30				pF
t_{SD}	Shutdown Response Time		700				ns

Electrical Characteristics (Continued)

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its rated operating conditions.

Note 2: During current limit, thermal limit, or electronic shutdown the input current will increase if the input to output differential voltage exceeds 8V. See Overvoltage Protection in Application Hints.

Note 3: The LM6125 series buffers contain current limit and thermal shutdown to protect against fault conditions.

Note 4: For operation at elevated temperature, these devices must be derated based on a thermal resistance of θ_{JA} and T_J max, $T_J = T_A + \theta_{JA} P_D$. θ_{JC} for the LM6125H and LM6225H is 17°C/W. The thermal impedance θ_{JA} of the device in the N package is 40°C/W when soldered directly to a printed circuit board, and the heat-sinking pins (pins 3, 4, 5, 10, 11, and 12) are connected to 2 square inches of 2 oz. copper. When installed in a socket, the thermal impedance θ_{JA} of the N package is 60°C/W.

Note 5: Limits are guaranteed by testing or correlation.

Note 6: The input is biased to +2.5V, and V_{IN} swings V_{PP} about this value. The input swing is 2 V_{PP} at all temperatures except for the A_V3 test at −55°C where it is reduced to 1.5 V_{PP}.

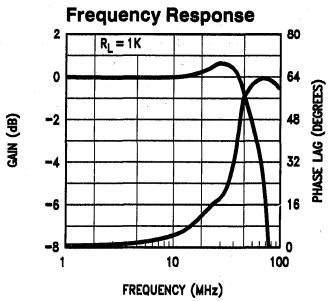
Note 7: The Error Flag is set (low) during current limit or thermal fault detection in addition to being set by the Shutdown pin. It is an open-collector output which requires an external pullup resistor.

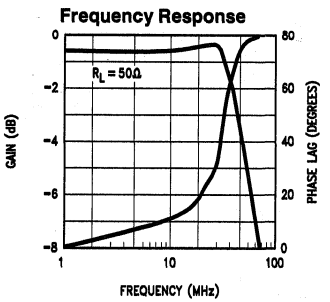
Note 8: Slew rate is measured with a ±11V input pulse and 50Ω source impedance at 25°C. Since voltage gain is typically 0.9 driving a 50Ω load, the output swing will be approximately ±10V. Slew rate is calculated for transitions between ±5V levels on both rising and falling edges. A high speed measurement is done to minimize device heating. For slew rate versus junction temperature see typical performance curves. The input pulse amplitude should be reduced to ±10V for measurements at temperature extremes. For accurate measurements, the input slew rate should be at least 1700 V/μs.

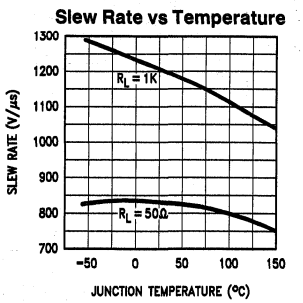
Note 9: The test circuit consists of the human body model of 120 pF in series with 1500Ω.

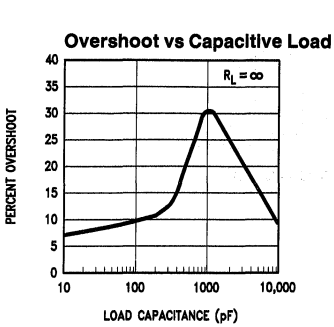
Note 10: A military RETS specification is available on request. At the time of printing, the LM6125H/883 RETS spec complied with the **Boldface** limits in this column. The LM6125H/883 may also be procured as Standard Military Drawing specification #5962-9081501MXX.

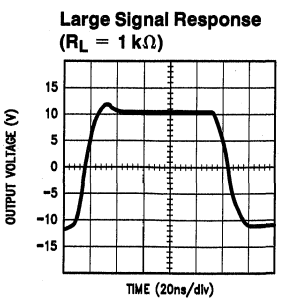
Typical Performance Characteristics T_A = 25°C, V_S = ±15V, unless otherwise specified

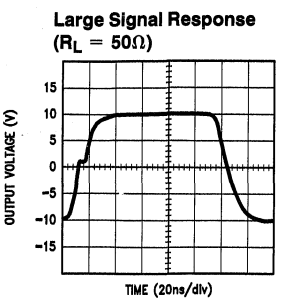








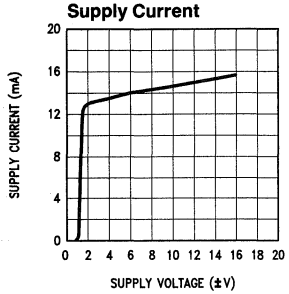




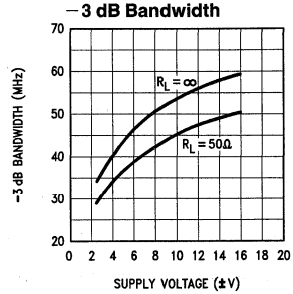
TL/H/9222-5

Typical Performance Characteristics $T_A = 25°C$, $V_S = \pm 15V$, unless otherwise specified (Continued)

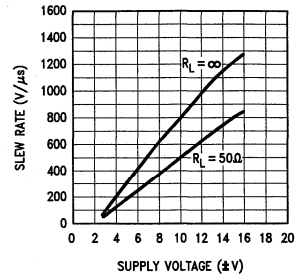
Supply Current



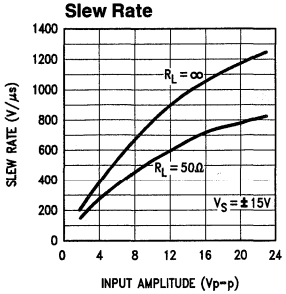
−3 dB Bandwidth



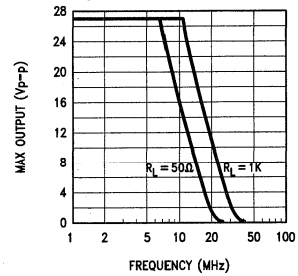
Slew Rate



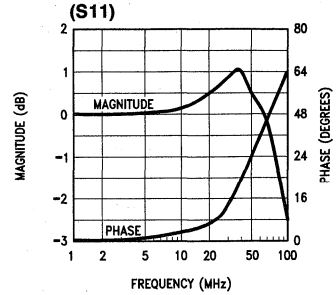
Slew Rate



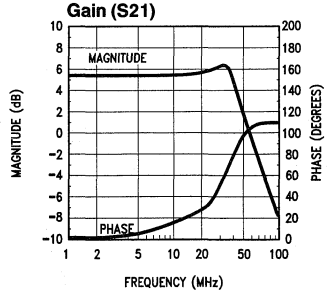
Power Bandwidth



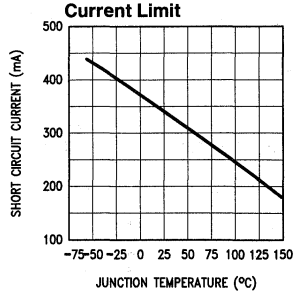
Input Return Gain (S11)



Forward Transmission Gain (S21)



Current Limit



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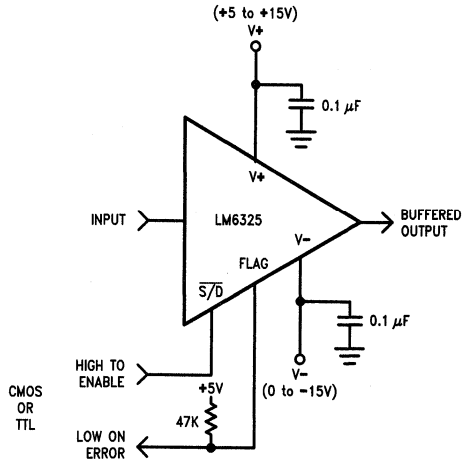
Typical Connection Diagram



TL/H/9222–6

Application Hints

POWER SUPPLY DECOUPLING

The method of supply bypassing is not critical for stability of the LM6125 series buffers. However, their high current output combined with high slew rate can result in significant voltage transients on the power supply lines if much inductance is present. For example, a slew rate of 900 V/μs into a 50Ω load produces a di/dt of 18 A/μs. Multiplying this by a wiring inductance of 50 nH results in a 0.9V transient. To minimize this problem use high quality decoupling very close to the device. Suggested values are a 0.1 μF ceramic in parallel with one or two 2.2 μF tantalums. A ground plane is recommended.

LOAD IMPEDANCE

The LM6125 is stable into any load when driven by a 50Ω source. As shown in the *Overshoot vs Capacitive Load* graph, worst case is a purely capacitive load of about 1000 pF. Shunting the load capacitance with a resistor will reduce overshoot.

SOURCE INDUCTANCE

Like any high-frequency buffer, the LM6125 can oscillate at high values of source inductance. The worst case condition occurs at a purely capacitive load of 50 pF where up to 100 nH of source inductance can be tolerated. With a 50Ω load, this goes up to 200 nH. This sensitivity may be reduced at the expense of a slight reduction in bandwidth by adding a resistor in series with the buffer input. A 100Ω resistor will ensure stability with source inductances up to 400 nH with any load.

ERROR FLAG LOGIC

The Error Flag pin is an open-collector output which requires an external pull-up resistor. Flag voltage is HIGH during operation, and is LOW during a fault condition. A fault condition occurs if either the internal current limit or the thermal shutdown is activated, or the shutdown (S/D) pin is driven low by external logic. Flag voltage returns to its HIGH state when normal operation resumes.

If the S/D pin is not to be used, it should be connected to V^+.

OVERVOLTAGE PROTECTION

The LM6125 may be severely damaged or destroyed if the Absolute Maximum Rating of 7V between input and output pins is exceeded.

If the buffer's input-to-output differential voltage is allowed to exceed 7V, a base-emitter junction will be in reverse-breakdown, and will be in series with a forward-biased base-emitter junction. Referring to the LM6125 simplified schematic, the transistors involved are Q1 and Q3 for positive inputs, and Q2 and Q4 for negative inputs. If any current is allowed to flow through these junctions, localized heating of the reverse-biased junction will occur, potentially causing damage. The effect of the damage is typically increased offset voltage, increased bias current, and/or degraded AC performance. The damage is cumulative, and may eventually result in complete device failure.

The device is best protected by the insertion of the parallel combination of a 100 kΩ resistor (R1) and a small capacitor (C1) in series with the buffer input, and a 100 kΩ resistor (R2) from input to output of the buffer (see *Figure 1*). This network normally has no effect on the buffer output. However, if the buffer's current limit or shutdown is activated, and the output has a ground-referred load of significantly less than 100 kΩ, a large input-to-output voltage may be present. R1 and R2 then form a voltage divider, keeping the input-output differential below the 7V Maximum Rating for input voltages up to 14V. This protection network should be sufficient to protect the LM6125 from the output of nearly any op amp which is operated on supply voltages of ±15V or lower.

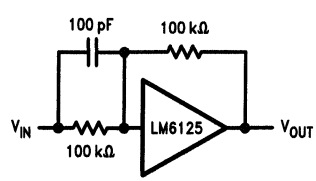


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FIGURE 1. LM6125 with Overvoltage Protection

Section 3

Voltage Comparators

Section 3 Contents

National Semiconductor

Voltage Comparators Definition of Terms

Input Bias Current: The average of the two input currents.

Input Offset Current: The absolute value of the difference between the two input currents for which the output will be driven higher than or lower than specified voltages.

Input Offset Voltage: The absolute value of the voltage between the input terminals required to make the output voltage greater than or less than specified voltages.

Input Voltage Range: The range of voltage on the input terminals (common-mode) over which the offset specifications apply.

Logic Threshold Voltage: The voltage at the output of the comparator at which the loading logic circuitry changes its digital state.

Negative Output Level: The negative DC output voltage with the comparator saturated by a differential input equal to or greater than a specified voltage.

Output Leakage Current: The current into the output terminal with the output voltage within a given range and the input drive equal to or greater than a given value.

Output Resistance: The resistance seen looking into the output terminal with the DC output level at the logic threshold voltage.

Output Sink Current: The maximum negative current that can be delivered by the comparator.

Positive Output Level: The high output voltage level with a given load and the input drive equal to or greater than a specified value.

Power Consumption: The power required to operate the comparator with no output load. The power will vary with signal level, but is specified as a maximum for the entire range of input signal conditions.

Response Time: The interval between the application of an input step function and the time when the output crosses the logic threshold voltage. The input step drives the comparator from some initial, saturated input voltage to an input level just barely in excess of that required to bring the output from saturation to the logic threshold voltage. This excess is referred to as the voltage overdrive.

Saturation Voltage: The low-output voltage level with the input drive equal to or greater than a specified value.

Strobe Current: The current out of the strobe terminal when it is at the zero logic level.

Strobe Output Level: The DC output voltage, independent of input conditions, with the voltage on the strobe terminal equal to or less than the specified low state.

Strobe "ON" Voltage: The maximum voltage on either strobe terminal required to force the output to the specified high state independent of the input voltage.

Strobe "OFF" Voltage: The minimum voltage on the strobe terminal that will guarantee that it does not interfere with the operation of the comparator.

Strobe Release Time: The time required for the output to rise to the logic threshold voltage after the strobe terminal has been driven from zero to the one logic level.

Supply Current: The current required from the positive or negative supply to operate the comparator with no output load. The power will vary with input voltage, but is specified as a maximum for the entire range of input voltage conditions.

Voltage Gain: The ratio of the change in output voltage to the change in voltage between the input terminals producing it.

National Semiconductor

Voltage Comparators Selection Guide

	Response Time (Typ) ns	V_{OS} mV(Max)	I_S mA(Max)	I_B nA(Max)	Comments
T_A = 25°C (Notes 1 and 2)					
LM6685	2.6	1.9	23	9,000	Single, Very High Speed ECL Output
LM6687	2.6	1.9	38	9,000	Dual, Very High Speed ECL Output
LM360	14	5	32	20,000	High Speed, Complementary Outputs
LM361	14	5	20	30,000	High Speed w/Strobes
LM306	28	5	10	25,000	High Speed, High Drive
LM319	80	8	12.5	1000	High Speed Dual
LF311	200	10	7.5	0.15	FET Input
LM311	200	7.5	7.5	250	General Purpose Single
LH2311	200	7.5	7.5	250	Dual LM311
LP311	1200	7.5	0.3	100	Low Power Single
LM339	1300	5	2.5	250	General Purpose Quad
LM392	1300	10	1	400	One Comparator Plus One Op Amp
LM393	1300	5	2.5	250	General Purpose Dual
LM2901	1300	7	2.5	250	Automotive Quad
LM612	1500	5	0.250	35	Super-Block™ Dual Comparator + Reference
LM613	1500	5	1	35	Super-Block™ Dual Comparator + Dual Op Amp + Reference
LM615	1500	5	0.600	35	Super-Block™ Quad Comparator + Reference
LM2903	1500	7	2.5	250	Automotive Dual
LP365	4000	6	0.275	75	Programmable Quad
LP339	8000	5	0.1	25	Low Power Quad

Note 1: Datasheet should be referred to for test conditions and more detailed information.

Note 2: This selection guide should be used to select for Response Time required. Industrial and Military Temperature Range types are available. The DC specs are for the lowest Commercial Grade available.

National Semiconductor

LF111/LF211/LF311 Voltage Comparators

General Description

The LF111, LF211 and LF311 are FET input voltage comparators that virtually eliminate input current errors. Designed to operate over a 5.0V to ±15V range the LF111 can be used in the most critical applications.

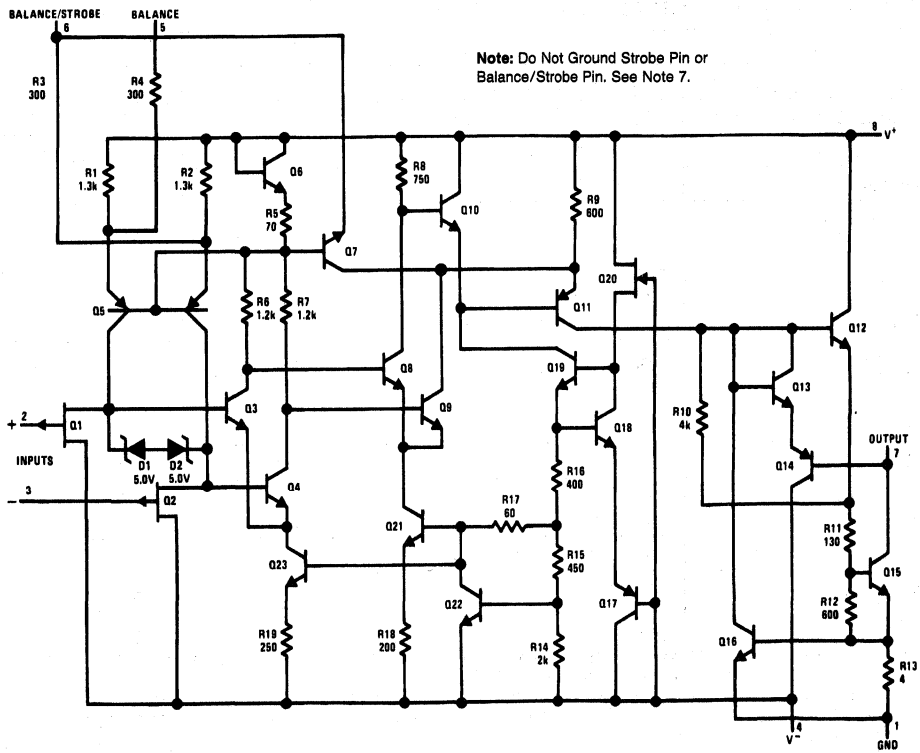
The extremely low input currents of the LF111 allows the use of a simple comparator in applications usually requiring input current buffering. Leakage testing, long time delay circuits, charge measurements, and high source impedance voltage comparisons are easily done.

Further, the LF111 can be used in place of the LM111 eliminating errors due to input currents. See the "application hints" of the LM311 for application help.

Features

- Eliminates input current errors
- Interchangeable with LM111
- No need for input current buffering

Schematic Diagram



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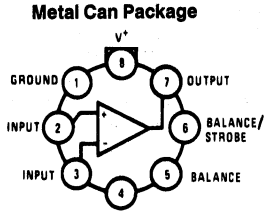
Connection Diagram

Metal Can Package



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Top View
Order Number LF111H, LF111H-MIL, LF211H or LF311H
See NS Package Number H08C

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

(Note 8)

	LF111/LF211	LF311
Total Supply Voltage (V_{84})	36V	36V
Output to Negative Supply Voltage (V_{74})	50V	40V
Ground to Negative Supply Voltage (V_{14})	30V	30V
Differential Input Voltage	±30V	±30V
Input Voltage (Note 1)	±15V	±15V
Power Dissipation (Note 2)	500 mW	500 mW
Output Short Circuit Duration	10 seconds	10 seconds

	LF111/LF211	LF311
Operating Temp. Range		
LF111	−55°C to +125°C	
LF211	−25°C to +85°C	
LF311		0°C to +70°C
Storage Temp. Range	−65°C to +150°C	−65°C to +150°C
Lead Temp. (Soldering, 10 seconds)	260°C	260°C

ESD rating to be determined.

Electrical Characteristics (LF111/LF211) (Note 3)

Parameter	Conditions	Min	Typ	Max	Units
Input Offset Voltage (Note 4)	$T_A = 25°C$, $R_S \leq 50k$		0.7	4.0	mV
Input Offset Current (Note 4)	$T_A = 25°C$, $V_{CM} = 0$ (Note 6)		5.0	25	pA
Input Bias Current	$T_A = 25°C$, $V_{CM} = 0$ (Note 6)		20	50	pA
Voltage Gain	$T_A = 25°C$	40	200		V/mV
Response Time (Note 5)	$T_A = 25°C$		200		ns
Saturation Voltage	$V_{IN} \leq -5.0$ mV, $I_{OUT} = 50$ mA, $T_A = 25°C$		0.75	1.5	V
Strobe On Current	$T_A = 25°C$		3.0		mA
Output Leakage Current	$V_{IN} \leq 5.0$ mV, $V_{OUT} = 35V$, $T_A = 25°C$		0.2	10	nA
Input Offset Voltage (Note 4)	$R_S \leq 50k$			6.0	mV
Input Offset Current (Note 4)	$V_S = \pm 15V$, $V_{CM} = 0$ (Note 6)		2.0	3.0	nA
Input Bias Current	$V_S = \pm 15V$, $V_{CM} = 0$ (Note 6)		5.0	7.0	nA
Input Voltage Range		−13.5	±14	13.0	V
Saturation Voltage	$V^+ \geq 4.5V$, $V^- = 0$ $V_{IN} \leq -6.0$ mV, $I_{OUT} \leq 8.0$ mA		0.23	0.4	V
Output Leakage Current	$V_{IN} \geq 5.0$ mV, $V_{OUT} = 35V$		0.1	0.5	μA
Positive Supply Current	$T_A = 25°C$		5.1	6.0	mA
Negative Supply Current	$T_A = 25°C$		4.1	5.0	mA

Note 1: This rating applies for ±15V supplies. The positive input voltage limit is 30V above the negative supply. The negative input voltage limit is equal to the negative supply voltage or 30V below the positive supply, whichever is less.

Note 2: The maximum junction temperature of the LF111 is +150°C, the LF211 is +110°C and the LF311 is +85°C. For operating at elevated temperatures, devices in the H08 package must be derated based on a thermal resistance of +65°C/W junction to ambient (in 400 linear feet/min air flow), +165°C/W junction to ambient (in static air), or +20°C/W junction to case.

Note 3: These specifications apply for $V_S = \pm 15V$, and the Ground pin at ground, and $-55°C \leq T_A \leq +125°C$ for the LF111, unless otherwise stated. With the LF211, however, all temperature specifications are limited to $-25°C \leq T_A \leq \pm 85°C$ and for the LF311 $0°C \leq T_A \leq +70°C$. The offset voltage, offset current and bias current specifications apply for any supply voltage from a single 5.0V supply up to ±15V supplies.

Note 4: The offset voltages and offset currents given are the maximum values required to drive the output within a volt of either supply with a 1.0 mA load. Thus, these parameters define an error band and take into account the worst case effects of voltage gain and input impedance.

Note 5: The response time specified (see definitions) is for a 100 mV input step with 5.0 mV overdrive.

Note 6: For input voltages greater than 15V above the negative supply the bias and offset currents will increase—see typical performance curves.

Note 7: This specification gives the current that must be drawn from the strobe pin to ensure the output is properly disabled. Do not short the strobe pin to ground; it should be current driven at 3 to 5 mA.

Note 8: Refer to RETSF111X for LF111H military specifications.

Electrical Characteristics (LF311) (Note 3)

Parameter	Conditions	Min	Typ	Max	Units
Input Offset Voltage (Note 4)	$T_A = 25°C$, $R_S \leq 50k$		2.0	10	mV
Input Offset Current (Note 4)	$T_A = 25°C$, $V_{CM} = 0$ (Note 6)		5.0	75	pA
Input Bias Current	$T_A = 25°C$, $V_{CM} = 0$ (Note 6)		25	150	pA
Voltage Gain	$T_A = 25°C$		200		V/mV
Response Time (Note 5)	$T_A = 25°C$		200		ns
Saturation Voltage	$V_{IN} \leq -10$ mV, $I_{OUT} = 50$ mA, $T_A = 25°C$		0.75	1.5	V
Strobe On Current	$T_A = 25°C$		3.0		mA
Output Leakage Current	$V_{IN} \geq 10$mV, $V_{OUT} = 35V$, $T_A = 25°C$		0.2	10	nA
Input Offset Voltage (Note 4)	$R_S \leq 50k$			15	mV
Input Offset Current (Note 4)	$V_S = \pm 15V$, $V_{CM} = 0$ (Note 6)		1.0		nA
Input Bias Current	$V_S = 15V$, $V_{CM} = 0$ (Note 6)		3.0		nA
Input Voltage Range			+14 −13.5		V V
Saturation Voltage	$V^+ \geq 4.5V$, $V^- = 0$ $V_{IN} \leq -10$ mV, $I_{OUT} \leq 8.0$ mA		0.23	0.4	V
Positive Supply Current	$T_A = 25°C$		5.1	7.5	mA
Negative Supply Current	$T_A = 25°C$		4.1	5.0	mA

Note 1: This rating applies for ±15V supplies. The positive input voltage limit is 30V above the negative supply. The negative input voltage limit is equal to the negative supply voltage or 30V below the positive supply, whichever is less.

Note 2: The maximum junction temperature of the LF111 is +150°C, the LF211 is +110°C and the LF311 is +85°C. For operating at elevated temperatures, devices in the H08 package must be derated based on a thermal resistance of +165°C/W, junction to ambient, or +20°C/W, junction to case.

Note 3: These specifications apply for $V_S = \pm 15V$ and $-55°C \leq T_A \leq +125°C$ for the LF111, unless otherwise stated. With the LF211, however, all temperature specifications are limited to $-25°C \leq T_A \leq +85°C$ and for the LF311 $0°C \leq T_A \leq +70°C$. The offset voltage, offset current and bias current specifications apply for any supply voltage from a single 5.0 mV supply up to ±15V supplies.

Note 4: The offset voltages and offset currents given are the maximum values required to drive the output within a volt of either supply with a 1.0 mA load. Thus, these parameters define an error band and take into account the worst case effects of voltage gain and input impedance.

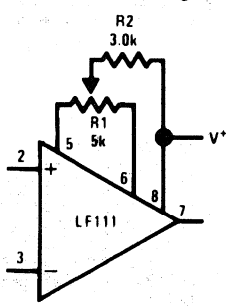
Note 5: The response time specified (see definitions) is for a 100 mV input step with 5.0 mV overdrive.

Note 6: For input voltages greater than 15V above the negative supply the bias and offset currents will increase—see typical performance curves.

Note 7: This specification gives the current that must be drawn from the strobe pin to ensure the output is properly disabled. Do not short the strobe pin to ground; it should be current driven at 3 to 5 mA.

Auxiliary Circuits

Offset Balancing



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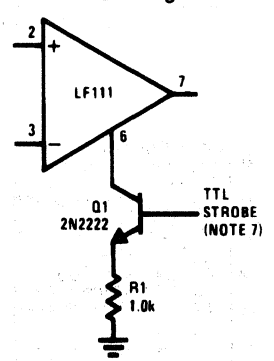
Strobing



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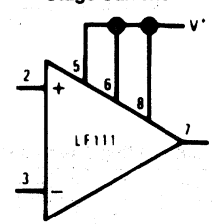
Note: Do Not Ground Strobe Pin.

Increasing Input Stage Current*



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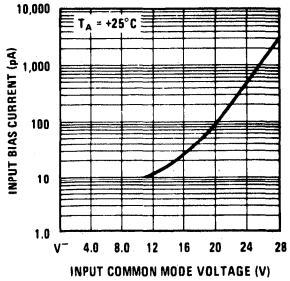
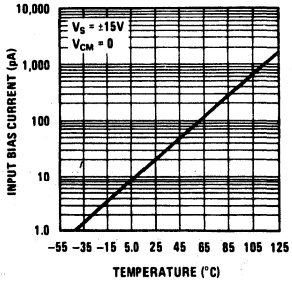
*Increases typical common mode slew from 7.0V/μs to 18V/μs

Typical Performance Characteristics

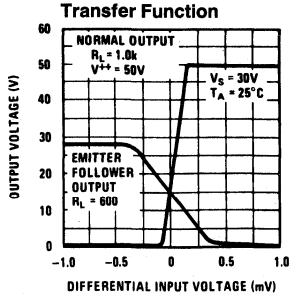
Input Bias Current vs Common Mode



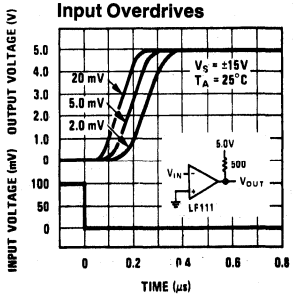
Input Bias Current vs Temperature



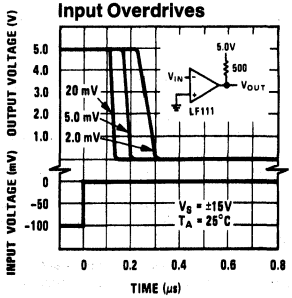
Transfer Function



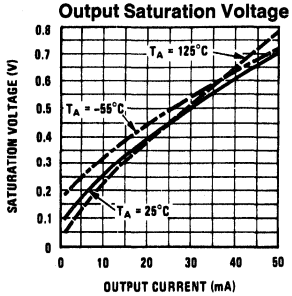
Response Time for Various Input Overdrives



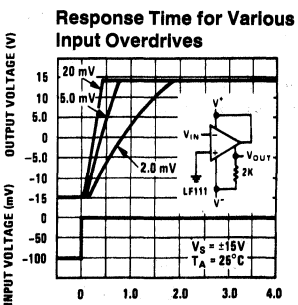
Response Time for Various Input Overdrives



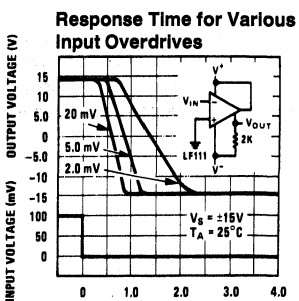
Output Saturation Voltage



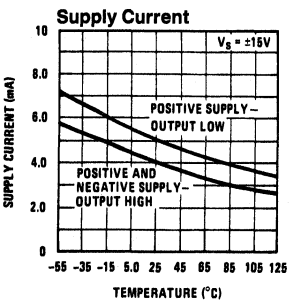
Response Time for Various Input Overdrives



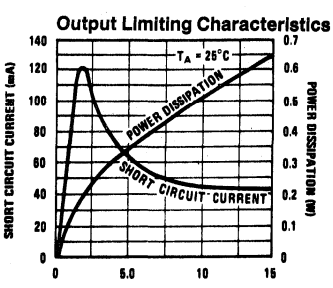
Response Time for Various Input Overdrives



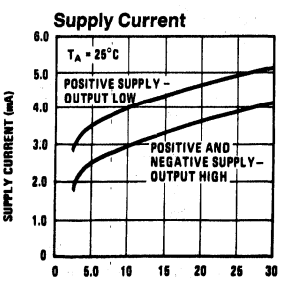
Supply Current



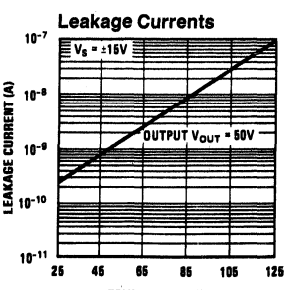
Output Limiting Characteristics



Supply Current



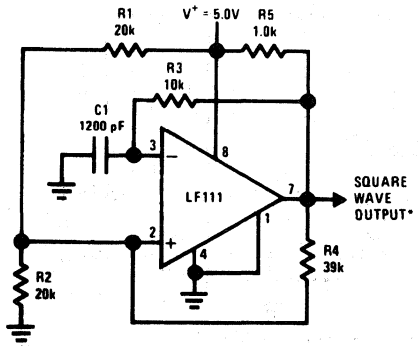
Leakage Currents



TL/H/5703–4

Typical Applications

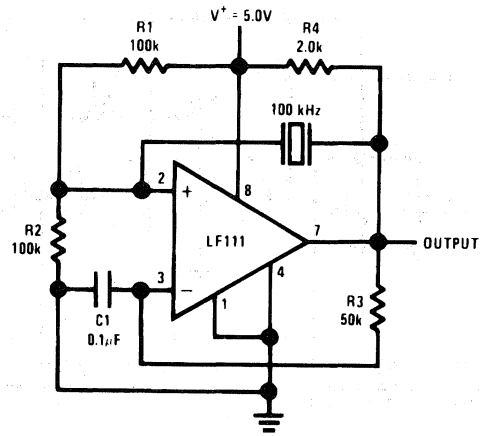
100 kHz Free Running Multivibrator



TL/H/5703–7

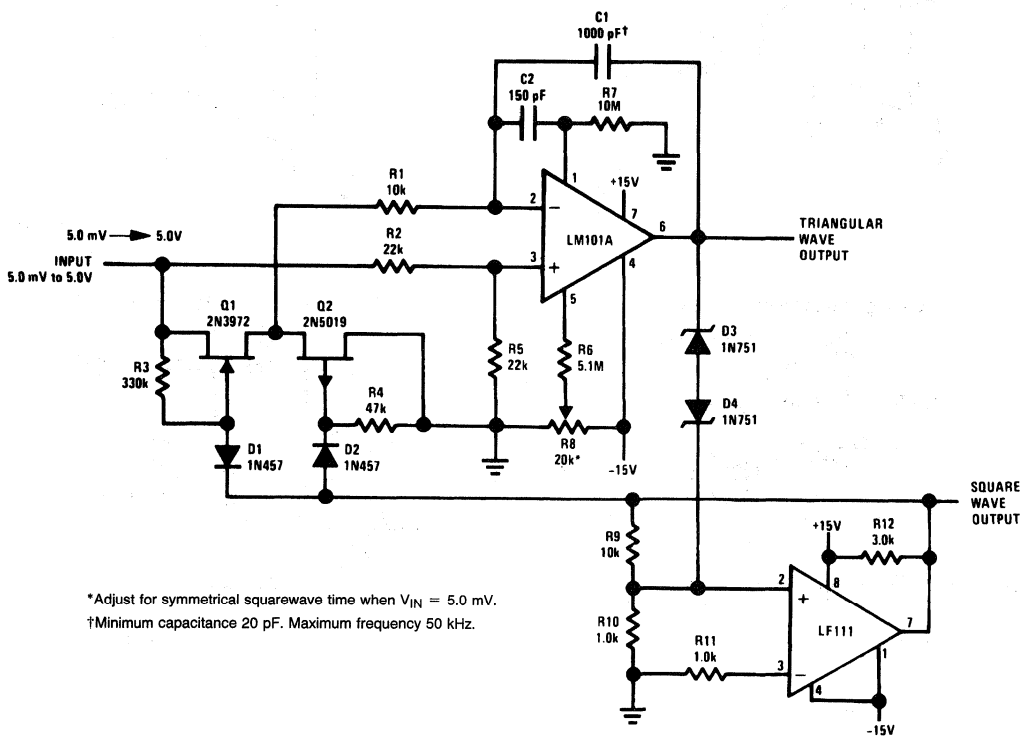
*TTL or DTL fanout of two.

Crystal Oscillator



TL/H/5703–3

10 Hz to 10 kHz Voltage Controlled Oscillator



*Adjust for symmetrical squarewave time when V_{IN} = 5.0 mV.

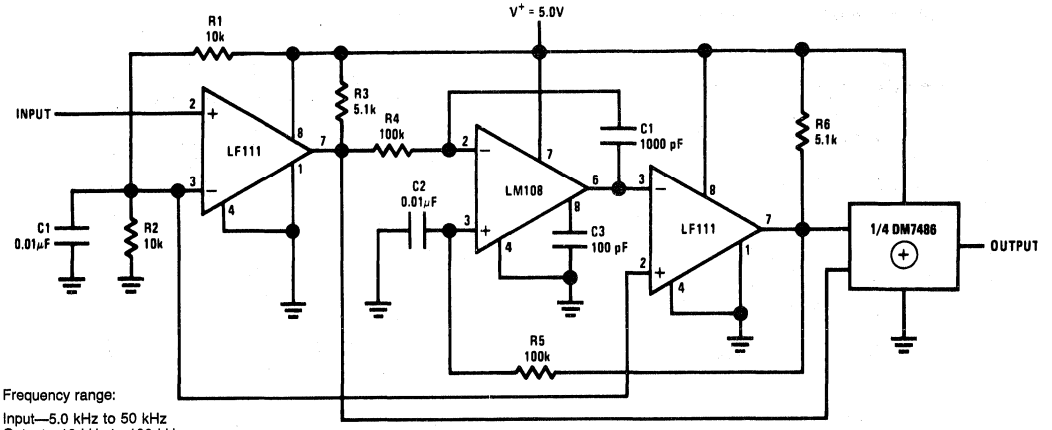
†Minimum capacitance 20 pF. Maximum frequency 50 kHz.

TL/H/5703–5

3

Typical Applications (Continued)

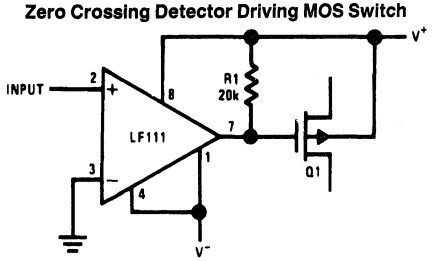
Frequency Doubler



Frequency range:
Input—5.0 kHz to 50 kHz
Output—10 kHz to 100 kHz

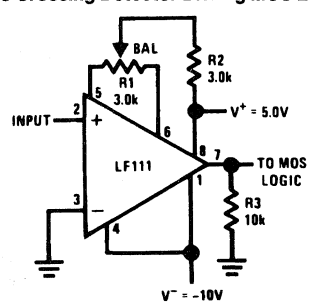
TL/H/5703–8

Zero Crossing Detector Driving MOS Switch



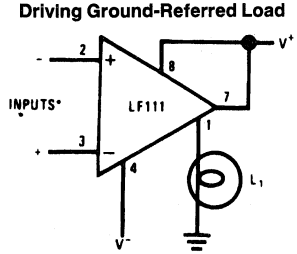
TL/H/5703–9

Zero Crossing Detector Driving MOS Logic



TL/H/5703–10

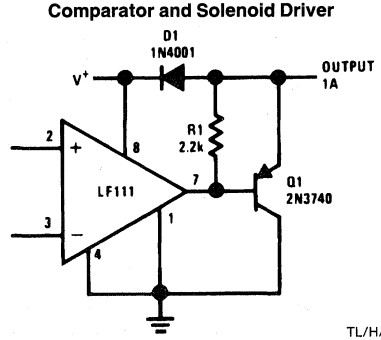
Driving Ground-Referred Load



TL/H/5703–11

*Input polarity is reversed when using pin 1 as output.

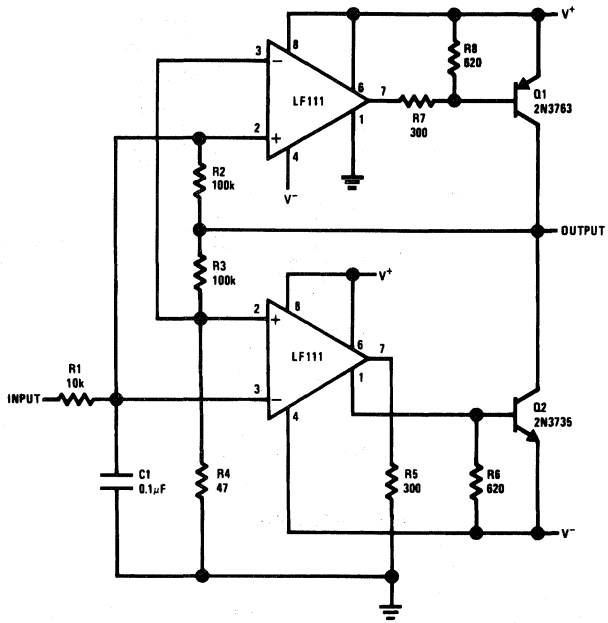
Comparator and Solenoid Driver



TL/H/5703–12

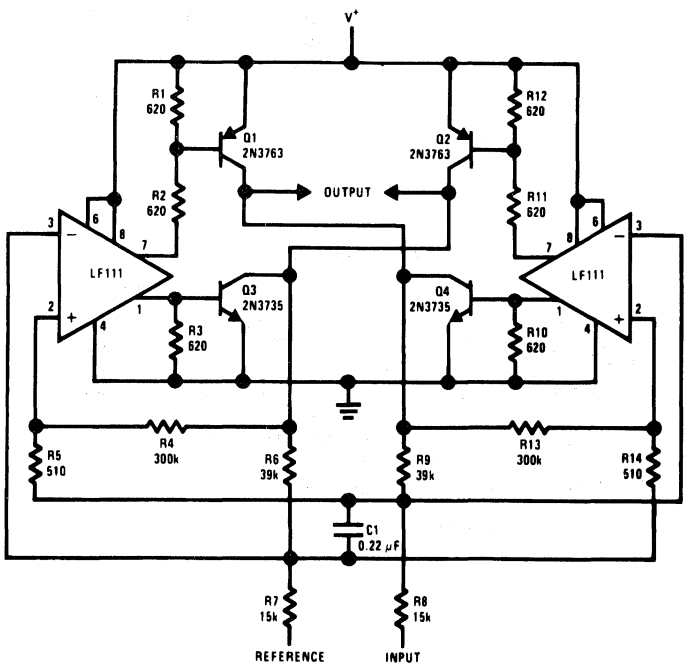
Typical Applications (Continued)

Switching Power Amplifier



TL/H/5703–16

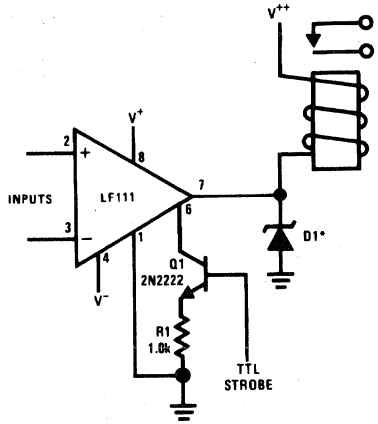
Switching Power Amplifier



TL/H/5703–17

Typical Applications (Continued)

Relay Driver with Strobe

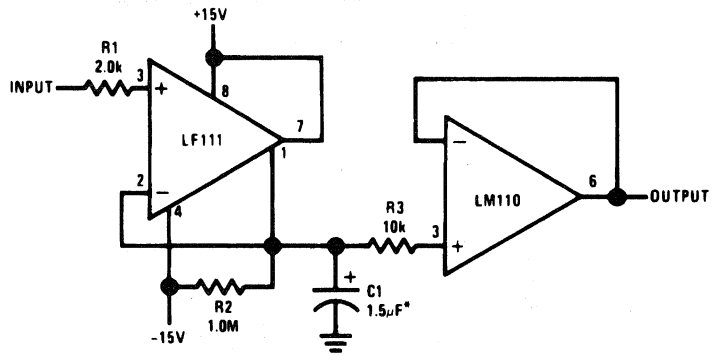


*Absorbs inductive kickback of relay and protects IC from severe voltage transients on V^{++} line.

TL/H/5703–18

Note: Do Not Ground Strobe Pin.

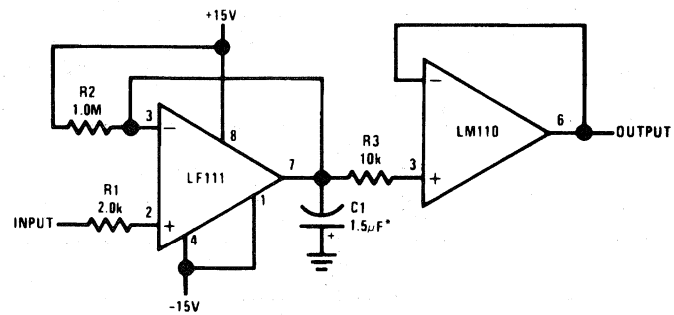
Positive Peak Detector



*Solid tantalum

TL/H/5703–19

Negative Peak Detector

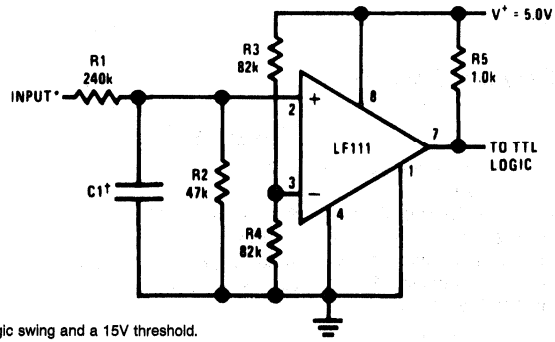


*Solid tantalum

TL/H/5703–20

Typical Applications (Continued)

TTL Interface with High Level Logic

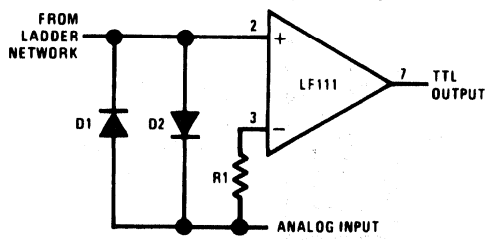


*Values shown are for a 0 to 30V logic swing and a 15V threshold.

†May be added to control speed and reduce susceptibility to noise spikes

TL/H/5703–21

Using Clamp Diodes to Improve Response



TL/H/5703–6

National Semiconductor

LH2111/LH2311
Dual Voltage Comparators

General Description

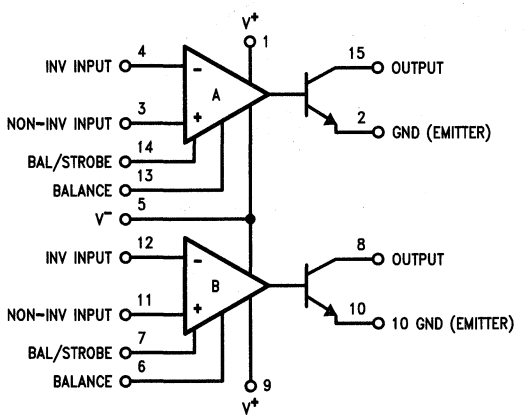
The LH2111 series of dual voltage comparators are two LM111 type comparators in a single hermetic package. Featuring all the same performance characteristics of the single, these duals offer in addition closer thermal tracking, lower weight, reduced insertion cost and smaller size than two singles. For additional information see the LM111 data sheet and National's Linear Application Handbook.

The LH2111 is specified for operation over the −55°C to +125°C military temperature range. The LH2311 is specified for operation over the 0°C to 70°C temperature range.

Features

■ Wide operating supply range	±15V to a single +5V
■ Low input currents	6 nA
■ High sensitivity	10 μV
■ Wide differential input range	±30V
■ High output drive	50 mA, 50V

Connection Diagram



TL/K/10116–1

Order Number LH2111D, LH2111D/883 or LH2311D
See NS Package Number D16C

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Total Supply Voltage ($V^+ - V^-$)	36V
Output to Negative Supply Voltage ($V_{OUT} - V^-$)	50V
Ground to Negative Supply Voltage (GND $- V^-$)	30V
Differential Input Voltage	±30V
Input Voltage (Note 1)	±15V
Power Dissipation (Note 2)	500 mW
Output Short Circuit Duration	10 sec
Operating Temperature Range LH2111	−55°C to +125°C
LH2311	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec)	300°C

Electrical Characteristics Each Side (Note 3)

Parameter	Conditions	Limits		Units
		LH2111	LH2311	
Input Offset Voltage (Note 4)	$T_A = 25°C$, $R_S \leq 50k$	3.0	7.5	mV Max
Input Offset Current (Note 4)	$T_A = 25°C$	10	50	nA Max
Input Bias Current	$T_A = 25°C$	100	250	nA Max
Voltage Gain	$T_A = 25°C$	200	200	V/mV Typ
Response Time (Note 5)	$T_A = 25°C$	200	200	ns Typ
Saturation Voltage	$V_{IN} \leq -5$ mV, $I_{OUT} = 50$ mA $T_A = 25°C$	1.5	1.5	V Max
Strobe On Current	$T_A = 25°C$	3.0	3.0	mA Typ
Output Leakage Current	$V_{IN} \geq 5$ mV, $V_{OUT} = 35V$ $T_A = 25°C$	10	50	nA Max
Input Offset Voltage (Note 4)	$R_S \leq 50k$	4.0	10	mV Max
Input Offset Current (Note 4)		20	70	nA Max
Input Bias Current		150	300	nA Max
Input Voltage Range		±14	±14	V Typ
Saturation Voltage	$V^+ \geq 4.5V$, $V^- = 0$ $V_{IN} \leq -5$ mV, $I_{SINK} \leq 8$ mA	0.4	0.4	V Max
Positive Supply Current	$T_A = 25°C$	6.0	7.5	mA Max
Negative Supply Current	$T_A = 25°C$	5.0	5.0	mA Max

Note 1: This rating applies for ±15V supplies. The positive input voltage limit is 30V above the negative supply. The negative input voltage limit is equal to the negative supply voltage or 30V below the positive supply, whichever is less.

Note 2: The maximum junction temperature is 150°C. For operating at elevated temperatures, devices in the flat package, the derating is based on a thermal resistance of 185°C/W when mounted on a $^1/_{16}$-inch-thick epoxy glass board with 0.03-inch-wide, 2 ounce copper conductor. The thermal resistance of the dual-in-line package is 100°C/W, junction to ambient.

Note 3: These specifications apply for $V_S = \pm 15V$ and $-55°C \leq T_A \leq 125°C$ for the LH2111, and $0°C \leq T_A \leq 70°C$ for the LH2311, unless otherwise stated. The offset voltage, offset current and bias current specifications apply for any supply voltage from a single 5V supply up to ±15V supplies. For the LH2311, $V_{IN} = \pm 10$ mV.

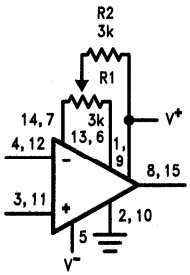
Note 4: The offset voltages and offset currents given are the maximum values required to drive the output within a volt of either supply with a 1 mA load. Thus, these parameters define an error band and take into account the worst case effects of voltage gain and input impedance.

Note 5: The response time specified is for a 100 mV input step with 5 mV overdrive.

Note 6: RETS2111X for the LH2111D and LH2111F military specifications.

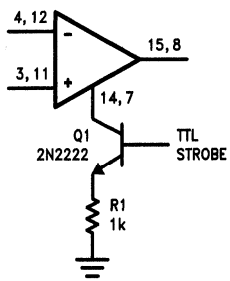
Auxiliary Circuits

Offset Balancing



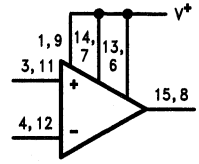
TL/K/10116–2

Strobing



TL/K/10116–3

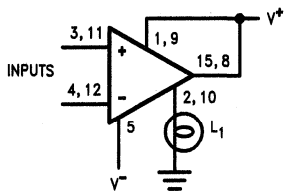
Increasing Input Stage Current*



TL/K/10116–4

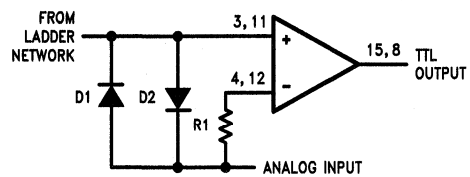
*Increases typical common mode slew from 7.0 V/μs to 18 V/μs

Driving Ground-Referred Load



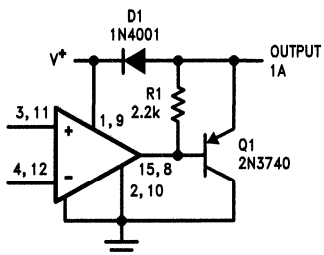
TL/K/10116–5

Using Clamp Diodes to Improve Responses



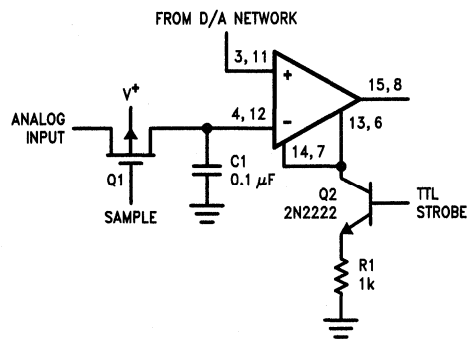
TL/K/10116–6

Comparator and Solenoid Driver



TL/K/10116–7

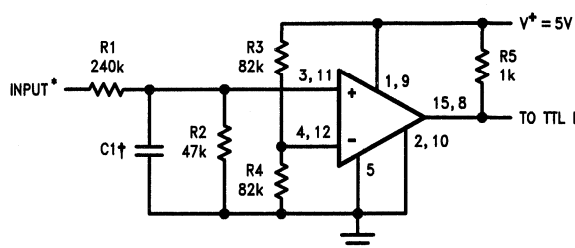
Strobing off Both Input* and Output Stages



TL/K/10116–8

*Typical input current is 50 pA with inputs strobed off

TTL Interface with High Level Logic



*Values shown are for a 0V to 30V logic swing and a 15V threshold.

†May be added to control speed and reduce susceptibility to noise spikes.

TL/K/10116–9

National Semiconductor

LM106/LM306 Voltage Comparator

General Description

The LM106 series are high-speed voltage comparators designed to accurately detect low-level analog signals and drive a digital load. They are equivalent to an LM710, combined with a two input NAND gate and an output buffer. The circuits can drive RTL, DTL or TTL integrated circuits directly. Furthermore, their outputs can switch voltages up to 24V at currents as high as 10 mA.

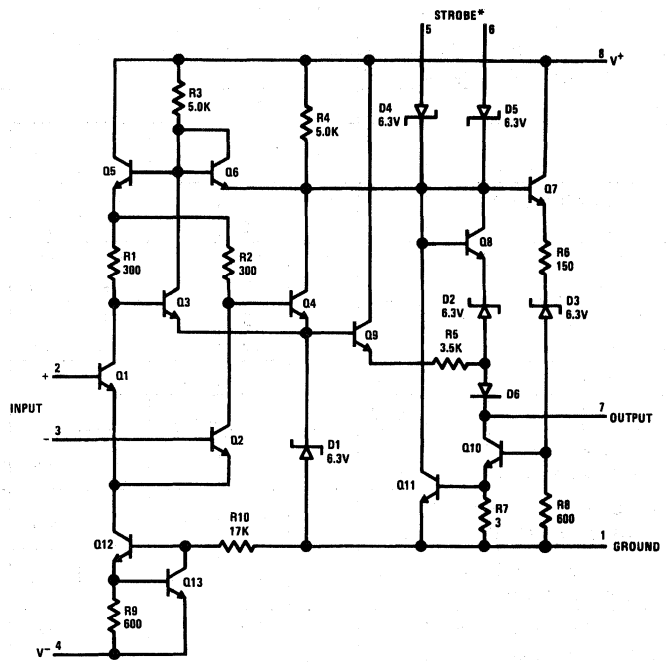
The devices have short-circuit protection which limits the inrush current when it is used to drive incandescent lamps, in addition to preventing damage from accidental shorts to the positive supply. The speed is equivalent to that of an LM710. However, they are even faster where buffers and additional logic circuitry can be eliminated by the increased flexibility of the LM106 series. They can also be operated from any negative supply voltage between −3V and −12V with little effect on performance.

The LM106 is specified for operation over the −55°C to +125°C military temperature range. The LM306 is specified for operation over 0°C to +70°C temperature range.

Features

- Improved accuracy
- Fan-out of 10 with DTL or TTL
- Added logic or strobe capability
- Useful as a relay or lamp driver
- Plug-in replacement for the LM710
- 40 ns maximum response time

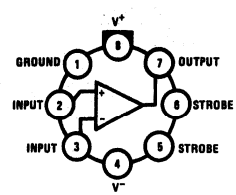
Schematic and Connection Diagrams



TL/H/7756–1

*Grounding either strobe forces the output to −0.5V (typ.). To disable strobe function, connect strobes to V+ or leave open.

Metal Can



TL/H/7756–2

Top View

Note: Pin 4 connected to case.

Order Number LM106H, LM106H/883† or LM306H
See NS Package Number H08A

†Available per SMD# 8003701

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications. (Note 6)

Positive Supply Voltage	15V
Negative Supply Voltage	−15V
Output Voltage	24V
Output to Negative Supply Voltage	30V
Differential Input Voltage	±5V
Input Voltage	±7V

Power Dissipation (Note 1)	600 mW
Output Short Circuit Duration	10 seconds
Operating Temperature Range	T_{MIN} T_{MAX}
LM106	−55°C to +125°C
LM306	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec.)	300°C

ESD rating to be determined.

Electrical Characteristics (Note 2)

Parameter	Conditions	LM106			LM306			Units
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	(Note 3)		0.5	2.0		1.6	5.0	mV
Input Offset Current	(Note 3)		0.7	3.0		1.8	5.0	μA
Input Bias Current			10	20		16	25	μA
Response Time	R_L = 390Ω to 5V C_L = 15 pF, (Note 4)		28	40		28	40	ns
Saturation Voltage	$V_{IN} \leq -5$ mV, I_{OUT} = 100 mA $V_{IN} \leq -7$ mV, I_{OUT} = 100 mA		1.0	1.5		0.8	2.0	V V
Output Leakage Current	$V_{IN} \geq 5$ mV, 8V ≤ V_{OUT} ≤ 24V $V_{IN} \geq 7$ mV, 8V ≤ V_{OUT} ≤ 24V		0.02	1.0		0.02	2.0	μA μA
THE FOLLOWING SPECIFICATIONS APPLY FOR $T_{MIN} \leq T_A \leq T_{MAX}$ (Note 5)								
Input Offset Voltage	(Note 3)			3.0			6.5	mV
Average Temperature Coefficient of Input Offset Voltage			3.0	10		5	20	μV/°C
Input Offset Current	$T_L \leq T_A \leq 25°C$, (Note 3) $25°C \leq T_A \leq T_H$		1.8 0.25	7.0 3.0		2.4	7.5 5.0	μA μA
Average Temperature Coefficient of Input Offset Current	$25°C \leq T_A \leq T_H$ $T_L \leq T_A \leq 25°C$		5.0 15	25 75		15 24	50 100	nA/°C nA/°C
Input Bias Current	$T_L \leq T_A \leq 25°C$ $25°C \leq T_A \leq T_H$			45 20		25	40 25	μA μA
Input Voltage Range	$-7V \geq V^- \geq -12V$	±5.0			±5.0			V
Differential Input Voltage Range		±5.0			±5.0			V
Saturation Voltage	$V_{IN} \leq -5$ mV, I_{OUT} = 50 mA $V_{IN} \leq -8$ mV For LM306			1.0			1.0	V
Saturation Voltage	$V_{IN} \leq -5$ mV, I_{OUT} = 16 mA $V_{IN} \leq -8$ mV For LM306			0.4			0.4	V
Positive Output Level	$V_{IN} \geq 5$ mV, $I_{OUT} = -400\mu A$ $V_{IN} \geq 8$ mV For LM306	2.5		5.5	2.5		5.5	V
Output Leakage Current	$V_{IN} \geq 5$ mV, 8V ≤ V_{OUT} ≤ 24V $V_{IN} \geq 8$ mV For LM306 $T_L \leq T_A \leq 25°C$ $25°C < T_A \leq T_H$			1.0 100			2.0 100	μA μA
Strobe Current	V_{STROBE} = 0.4V		−1.7	−3.2		−1.7	−3.2	mA

Electrical Characteristics (Note 2) (Continued)

Parameter	Conditions	LM106			LM306			Units
		Min	Typ	Max	Min	Typ	Max	
Strobe "ON" Voltage		0.9	1.4		0.9	1.4		V
Strobe "OFF" Voltage	$I_{SINK} \leq 16$ mA		1.4	2.2		1.4	2.2	V
Positive Supply Current	$V_{IN} = -5$ mV $V_{IN} = -8$ mV for LM306		5.5	10		5.5	10	mA
Negative Supply Current			−1.5	−3.6		−1.5	−3.6	mA

Note 1: The maximum junction temperature of LM106 is 150°C, LM306 is 85°C. For operating at elevated temperatures, devices must be derated based on a thermal resistance of 170°C/W, junction to ambient, or 23°C/W, junction to case.

Note 2: These specifications apply for $-3V \geq V^- \geq -12V$, $V^+ = 12V$ and $T_A = 25°C$ unless otherwise specified. All currents into device pins are considered positive.

Note 3: The offset voltages and offset currents given are the maximum values required to drive the output down to 0.5V or up to 4.4V (0.5V or up to 4.8V for the LM306). Thus, these parameters actually define an error band and take into account the worst-case effects of voltage gain, specified supply voltage variations, and common mode voltage variations.

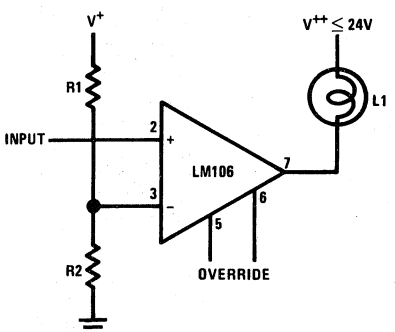
Note 4: The response time specified (see definitions) is for a 100 mV input step with 5 mV overdrive.

Note 5: All currents into device pins are considered positive.

Note 6: Refer to RETS106X for LM106 military specifications.

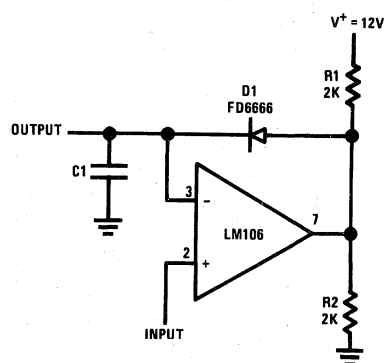
Typical Applications

Level Detector and Lamp Driver



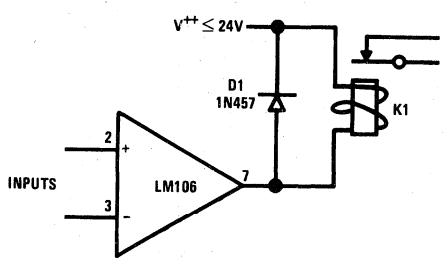
TL/H/7756–4

Fast Response Peak Detector



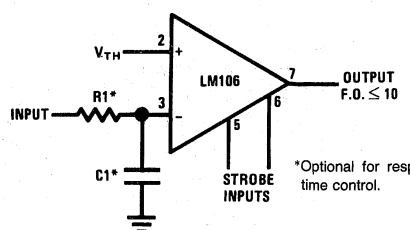
TL/H/7756–5

Relay Driver



TL/H/7756–6

Adjustable Threshold Line Receiver

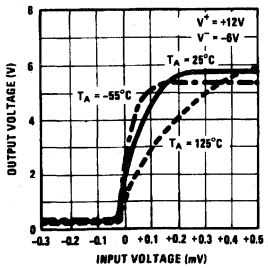


*Optional for response time control.

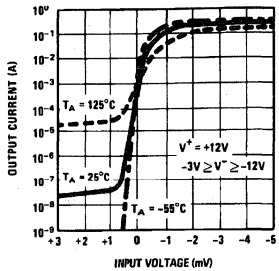
TL/H/7756–7

Typical Performance Characteristics

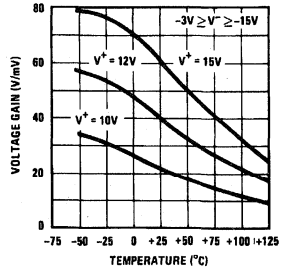
Transfer Function



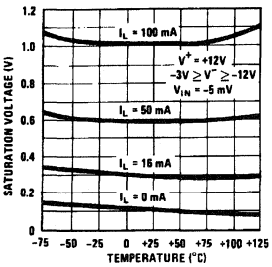
Transconductance



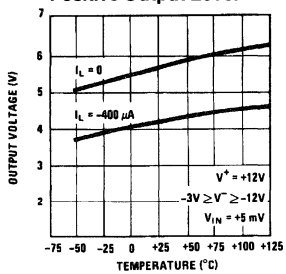
Voltage Gain



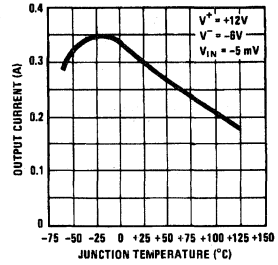
Saturation Voltage



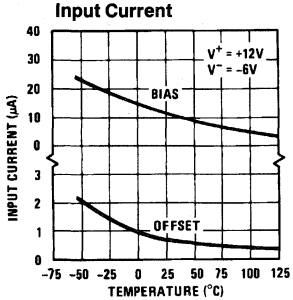
Positive Output Level



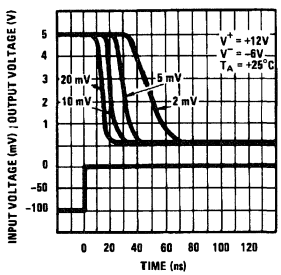
Short Circuit Output Current



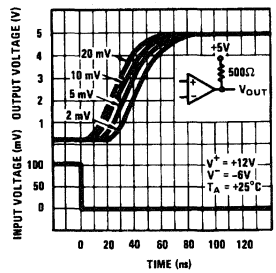
Input Current



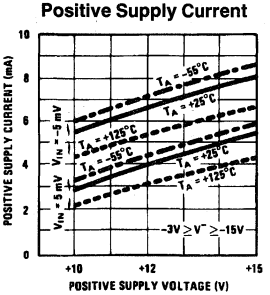
Response Time for Various Input Overdrives



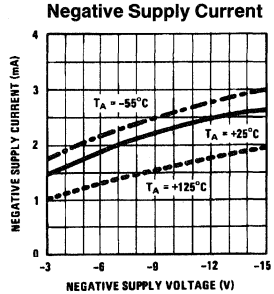
Response Time for Various Input Overdrives



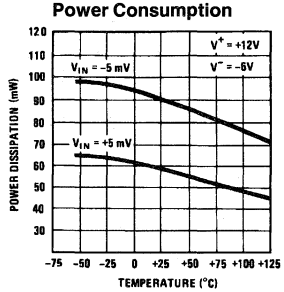
Positive Supply Current



Negative Supply Current



Power Consumption



TL/H/7756–8

National Semiconductor

LM111/LM211/LM311 Voltage Comparator

General Description

The LM111, LM211 and LM311 are voltage comparators that have input currents nearly a thousand times lower than devices like the LM106 or LM710. They are also designed to operate over a wider range of supply voltages: from standard ±15V op amp supplies down to the single 5V supply used for IC logic. Their output is compatible with RTL, DTL and TTL as well as MOS circuits. Further, they can drive lamps or relays, switching voltages up to 50V at currents as high as 50 mA.

Both the inputs and the outputs of the LM111, LM211 or the LM311 can be isolated from system ground, and the output can drive loads referred to ground, the positive supply or the negative supply. Offset balancing and strobe capability are provided and outputs can be wire OR'ed. Although slower than the LM106 and LM710 (200 ns response time vs 40 ns) the devices are also much less prone to spurious oscillations. The LM111 has the same pin configuration as the LM106 and LM710.

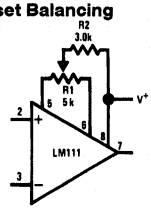
The LM211 is identical to the LM111, except that its performance is specified over a −25°C to +85°C temperature range instead of −55°C to +125°C. The LM311 has a temperature range of 0°C to +70°C.

Features

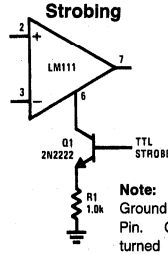
- Operates from single 5V supply
- Input current: 150 nA max. over temperature
- Offset current: 20 nA max. over temperature
- Differential input voltage range: ±30V
- Power consumption: 135 mW at ±15V

Typical Applications**

Offset Balancing



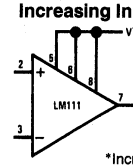
Strobing



Note: Do Not Ground Strobe Pin. Output is turned off when current is pulled from Strobe Pin.

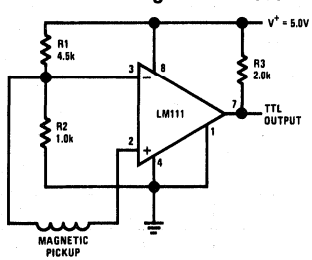
Note: Pin connections shown on schematic diagram and typical applications are for H08 metal can package.

Increasing Input Stage Current*

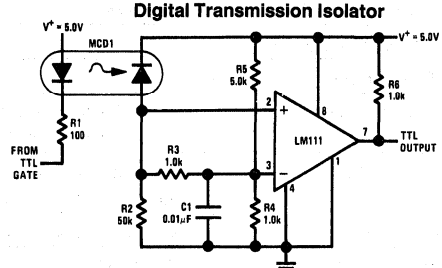


*Increases typical common mode slew from 7.0V/μs to 18V/μs.

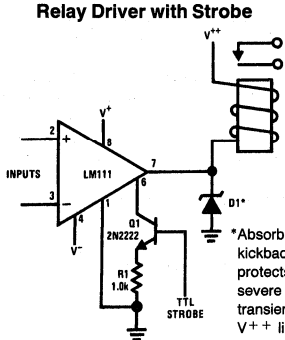
Detector for Magnetic Transducer



Digital Transmission Isolator



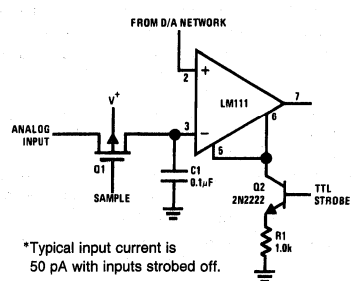
Relay Driver with Strobe



*Absorbs inductive kickback of relay and protects IC from severe voltage transients on V++ line.

Note: Do Not Ground Strobe Pin.

Strobing off Both Input* and Output Stages



*Typical input current is 50 pA with inputs strobed off.

Note: Do Not Ground Strobe Pin.

TL/H/5704–1

Absolute Maximum Ratings for the LM111/LM211

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications. (Note 7)

Total Supply Voltage (V_{84})	36V
Output to Negative Supply Voltage (V_{74})	50V
Ground to Negative Supply Voltage (V_{14})	30V
Differential Input Voltage	±30V
Input Voltage (Note 1)	±15V
Power Dissipation (Note 2)	500 mW
Output Short Circuit Duration	10 sec
Operating Temperature Range LM111	−55°C to 125°C
LM211	−25°C to 85°C
Storage Temperature Range	−65°C to 150°C
Lead Temperature (Soldering, 10 sec)	260°C
Voltage at Strobe Pin	V+ −5V

Soldering Information
- Dual-In-Line Package
  - Soldering (10 seconds) ..... 260°C
- Small Outline Package
  - Vapor Phase (60 seconds) ..... 215°C
  - Infrared (15 seconds) ..... 220°C

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

ESD Rating (Note 8) 300V

Electrical Characteristics for the LM111 and LM211 (Note 3)

Parameter	Conditions	Min	Typ	Max	Units
Input Offset Voltage (Note 4)	$T_A = 25°C$, $R_S \leq 50k$		0.7	3.0	mV
Input Offset Current (Note 4)	$T_A = 25°C$		4.0	10	nA
Input Bias Current	$T_A = 25°C$		60	100	nA
Voltage Gain	$T_A = 25°C$	40	200		V/mV
Response Time (Note 5)	$T_A = 25°C$		200		ns
Saturation Voltage	$V_{IN} \leq -5$ mV, $I_{OUT} = 50$ mA $T_A = 25°C$		0.75	1.5	V
Strobe ON Current (Note 6)	$T_A = 25°C$	2.0	3.0	5.0	mA
Output Leakage Current	$V_{IN} \geq 5$ mV, $V_{OUT} = 35V$ $T_A = 25°C$, $I_{STROBE} = 3$ mA		0.2	10	nA
Input Offset Voltage (Note 4)	$R_S \leq 50$ k			4.0	mV
Input Offset Current (Note 4)				20	nA
Input Bias Current				150	nA
Input Voltage Range	$V^+ = 15V$, $V^- = -15V$, Pin 7 Pull-Up May Go To 5V	−14.5	13.8,-14.7	13.0	V
Saturation Voltage	$V^+ \geq 4.5V$, $V^- = 0$ $V_{IN} \leq -6$ mV, $I_{OUT} \leq 8$ mA		0.23	0.4	V
Output Leakage Current	$V_{IN} \geq 5$ mV, $V_{OUT} = 35V$		0.1	0.5	μA
Positive Supply Current	$T_A = 25°C$		5.1	6.0	mA
Negative Supply Current	$T_A = 25°C$		4.1	5.0	mA

Note 1: This rating applies for ±15 supplies. The positive input voltage limit is 30V above the negative supply. The negative input voltage limit is equal to the negative supply voltage or 30V below the positive supply, whichever is less.

Note 2: The maximum junction temperature of the LM111 is 150°C, while that of the LM211 is 110°C. For operating at elevated temperatures, devices in the H08 package must be derated based on a thermal resistance of 165°C/W, junction to ambient, or 20°C/W, junction to case. The thermal resistance of the dual-in-line package is 110°C/W, junction to ambient.

Note 3: These specifications apply for $V_S = \pm 15V$ and Ground pin at ground, and $-55°C \leq T_A \leq +125°C$, unless otherwise stated. With the LM211, however, all temperature specifications are limited to $-25°C \leq T_A \leq +85°C$. The offset voltage, offset current and bias current specifications apply for any supply voltage from a single 5V supply up to ±15V supplies.

Note 4: The offset voltages and offset currents given are the maximum values required to drive the output within a volt of either supply with a 1 mA load. Thus, these parameters define an error band and take into account the worst-case effects of voltage gain and input impedance.

Note 5: The response time specified (see definitions) is for a 100 mV input step with 5 mV overdrive.

Note 6: This specification gives the range of current which must be drawn from the strobe pin to ensure the output is properly disabled. Do not short the strobe pin to ground; it should be current driven at 3 to 5 mA.

Note 7: Refer to RETS111X for the LM111H, LM111J and LM111J-8 military specifications.

Note 8: Human body model, 1.5 kΩ in series with 100 pF.

Absolute Maximum Ratings for the LM311

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Total Supply Voltage (V_{84})	36V
Output to Negative Supply Voltage V_{74})	40V
Ground to Negative Supply Voltage V_{14})	30V
Differential Input Voltage	±30V
Input Voltage (Note 1)	±15V
Power Dissipation (Note 2)	500 mW
ESD Rating (Note 7)	300V
Output Short Circuit Duration	10 sec
Operating Temperature Range	0° to 70°C
Storage Temperature Range	−65°C to 150°C
Lead Temperature (soldering, 10 sec)	260°C
Voltage at Strobe Pin	$V^+ - 5V$

Soldering Information
- Dual-In-Line Package
  - Soldering (10 seconds) ..... 260°C
- Small Outline Package
  - Vapor Phase (60 seconds) ..... 215°C
  - Infrared (15 seconds) ..... 220°C

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

Electrical Characteristics for the LM311 (Note 3)

Parameter	Conditions	Min	Typ	Max	Units
Input Offset Voltage (Note 4)	$T_A = 25°C$, $R_S \leq 50k$		2.0	7.5	mV
Input Offset Current (Note 4)	$T_A = 25°C$		6.0	50	nA
Input Bias Current	$T_A = 25°C$		100	250	nA
Voltage Gain	$T_A = 25°C$	40	200		V/mV
Response Time (Note 5)	$T_A = 25°C$		200		ns
Saturation Voltage	$V_{IN} \leq -10$ mV, $I_{OUT} = 50$ mA $T_A = 25°C$		0.75	1.5	V
Strobe ON Current	$T_A = 25°C$	1.5	3.0		mA
Output Leakage Current	$V_{IN} \geq 10$ mV, $V_{OUT} = 35V$ $T_A = 25°C$, $I_{STROBE} = 3$ mA $V^- = V_{GRND} = -5V$		0.2	50	nA
Input Offset Voltage (Note 4)	$R_S \leq 50K$			10	mV
Input Offset Current (Note 4)				70	nA
Input Bias Current				300	nA
Input Voltage Range		−14.5	13.8, −14.7	13.0	V
Saturation Voltage	$V^+ \geq 4.5V$, $V^- = 0$ $V_{IN} \leq -10$ mV, $I_{OUT} \leq 8$ mA		0.23	0.4	V
Positive Supply Current	$T_A = 25°C$		5.1	7.5	mA
Negative Supply Current	$T_A = 25°C$		4.1	5.0	mA

Note 1: This rating applies for ±15V supplies. The positive input voltage limit is 30V above the negative supply. The negative input voltage limit is equal to the negative supply voltage or 30V below the positive supply, whichever is less.

Note 2: The maximum junction temperature of the LM311 is 110°C. For operating at elevated temperature, devices in the H08 package must be derated based on a thermal resistance of 165°C/W, junction to ambient, or 20°C/W, junction to case. The thermal resistance of the dual-in-line package is 100°C/W, junction to ambient.

Note 3: These specifications apply for $V_S = \pm 15V$ and the Ground pin at ground, and $0°C < T_A < +70°C$, unless otherwise specified. The offset voltage, offset current and bias current specifications apply for any supply voltage from a single 5V supply up to ±15V supplies.

Note 4: The offset voltages and offset currents given are the maximum values required to drive the output within a volt of either supply with 1 mA load. Thus, these parameters define an error band and take into account the worst-case effects of voltage gain and input impedance.

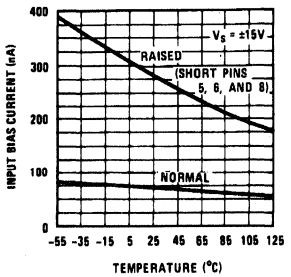
Note 5: The response time specified (see definitions) is for a 100 mV input step with 5 mV overdrive.

Note 6: This specification gives the range of current which must be drawn from the strobe pin to ensure the output is properly disabled. Do not short the strobe pin to ground; it should be current driven at 3 to 5 mA.

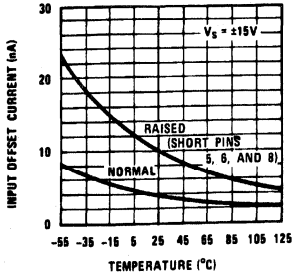
Note 7: Human body model, 1.5 kΩ in series with 100 pF.

LM111/LM211 Typical Performance Characteristics

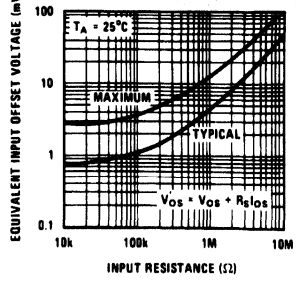
Input Bias Current



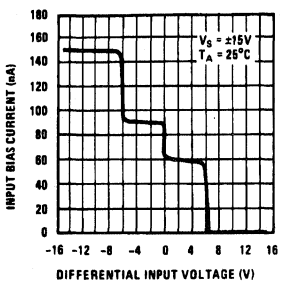
Input Offset Current



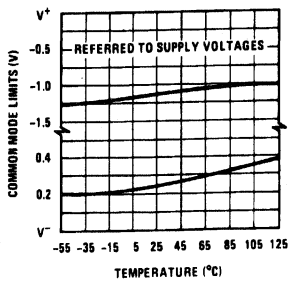
Offset Error



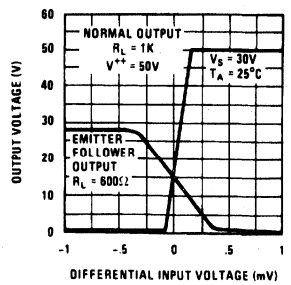
Input Characteristics



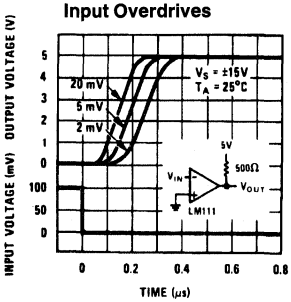
Common Mode Limits



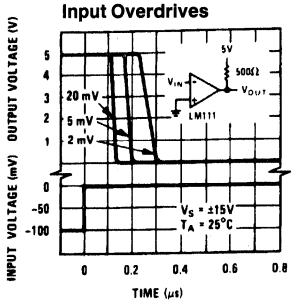
Transfer Function



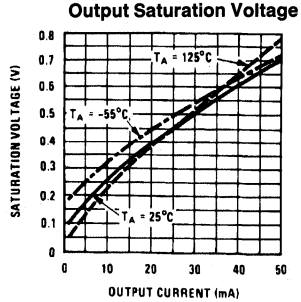
Response Time for Various Input Overdrives



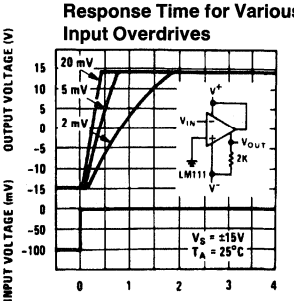
Response Time for Various Input Overdrives



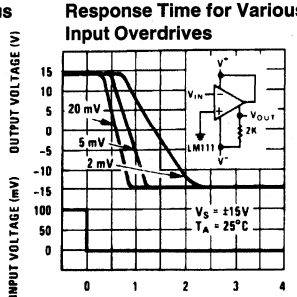
Output Saturation Voltage



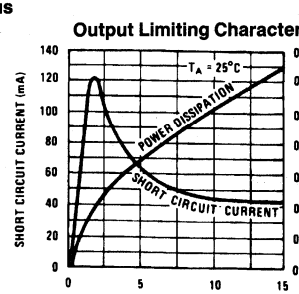
Response Time for Various Input Overdrives



Response Time for Various Input Overdrives

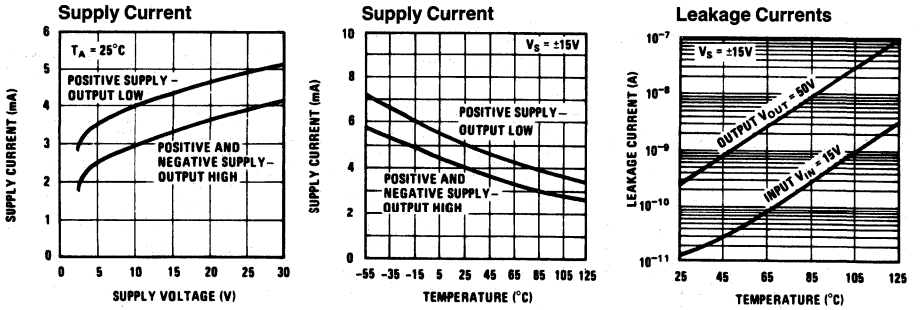


Output Limiting Characteristics



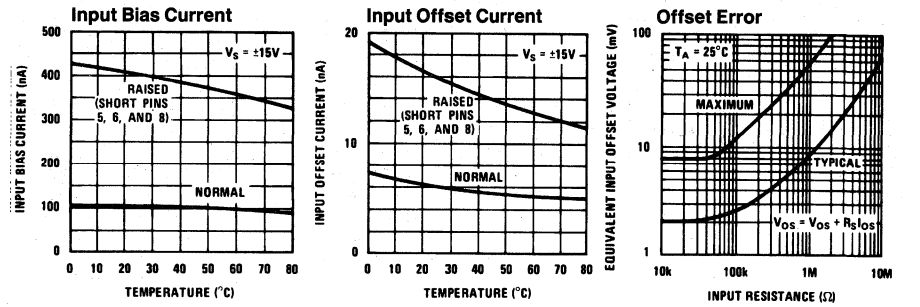
TL/H/5704–2

LM111/LM211 Typical Performance Characteristics (Continued)

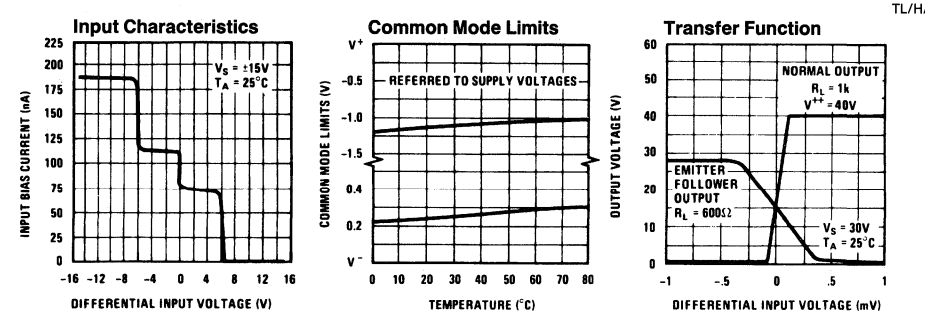


TL/H/5704–3

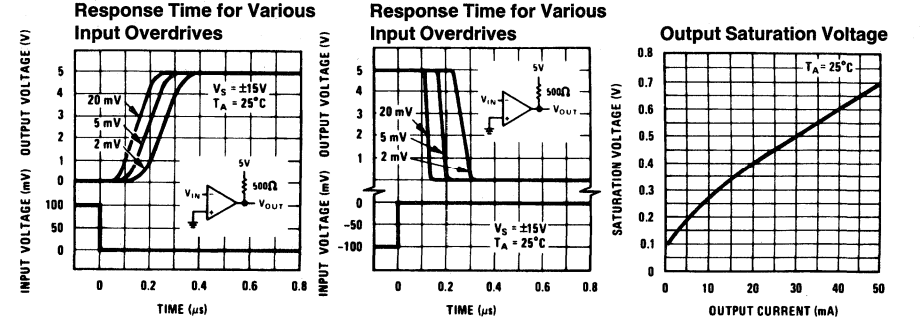
LM311 Typical Performance Characteristics



TL/H/5704–8

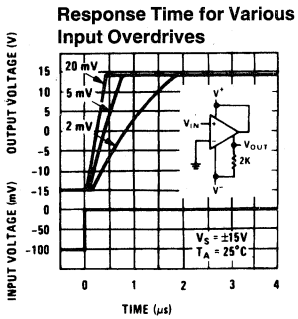


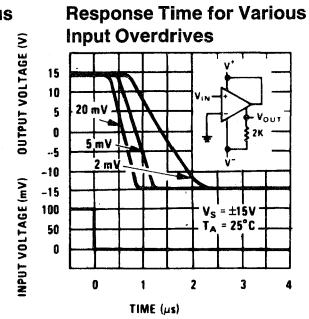
TL/H/5704–9

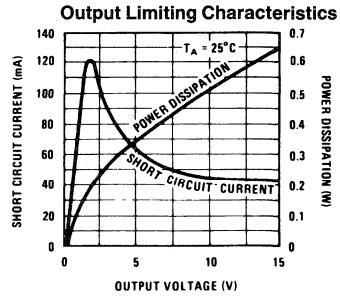


TL/H/5704–10

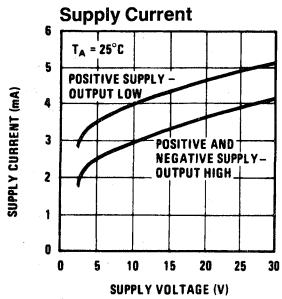
LM311 Typical Performance Characteristics (Continued)

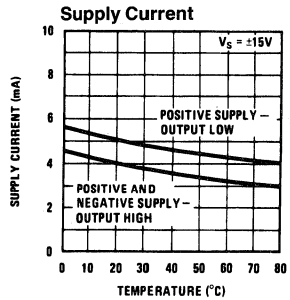


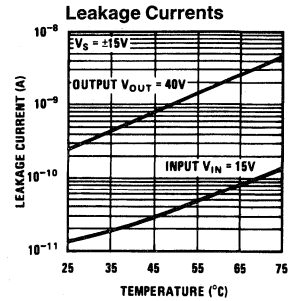




TL/H/5704–11







TL/H/5704–12

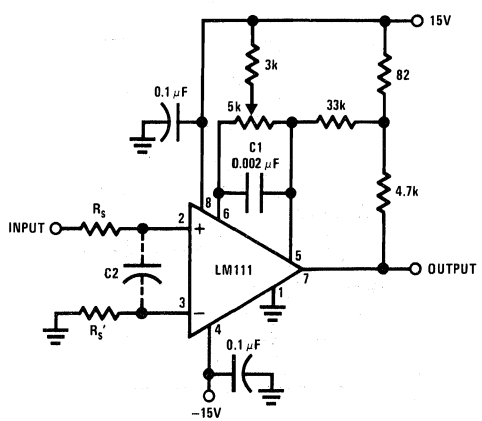
Application Hints

CIRCUIT TECHNIQUES FOR AVOIDING OSCILLATIONS IN COMPARATOR APPLICATIONS

When a high-speed comparator such as the LM111 is used with fast input signals and low source impedances, the output response will normally be fast and stable, assuming that the power supplies have been bypassed (with 0.1 μF disc capacitors), and that the output signal is routed well away from the inputs (pins 2 and 3) and also away from pins 5 and 6.

However, when the input signal is a voltage ramp or a slow sine wave, or if the signal source impedance is high (1 kΩ to 100 kΩ), the comparator may burst into oscillation near the crossing-point. This is due to the high gain and wide bandwidth of comparators like the LM111. To avoid oscillation or instability in such a usage, several precautions are recommended, as shown in *Figure 1* below.

1. The trim pins (pins 5 and 6) act as unwanted auxiliary inputs. If these pins are not connected to a trim-pot, they should be shorted together. If they are connected to a trim-pot, a 0.01 μF capacitor C1 between pins 5 and 6 will minimize the susceptibility to AC coupling. A smaller capacitor is used if pin 5 is used for positive feedback as in *Figure 1*.
2. Certain sources will produce a cleaner comparator output waveform if a 100 pF to 1000 pF capacitor C2 is connected directly across the input pins.
3. When the signal source is applied through a resistive network, R_S, it is usually advantageous to choose an R_S' of substantially the same value, both for DC and for dynamic (AC) considerations. Carbon, tin-oxide, and metal-film resistors have all been used successfully in comparator input circuitry. Inductive wirewound resistors are not suitable.
4. When comparator circuits use input resistors (eg. summing resistors), their value and placement are particularly important. In all cases the body of the resistor should be close to the device or socket. In other words there should be very little lead length or printed-circuit foil run between comparator and resistor to radiate or pick up signals. The same applies to capacitors, pots, etc. For example, if $R_S = 10$ kΩ, as little as 5 inches of lead between the resistors and the input pins can result in oscillations that are very hard to damp. Twisting these input leads tightly is the only (second best) alternative to placing resistors close to the comparator.
5. Since feedback to almost any pin of a comparator can result in oscillation, the printed-circuit layout should be engineered thoughtfully. Preferably there should be a groundplane under the LM111 circuitry, for example, one side of a double-layer circuit card. Ground foil (or, positive supply or negative supply foil) should extend between the output and the inputs, to act as a guard. The foil connections for the inputs should be as small and compact as possible, and should be essentially surrounded by ground foil on all sides, to guard against capacitive coupling from any high-level signals (such as the output). If pins 5 and 6 are not used, they should be shorted together. If they are connected to a trim-pot, the trim-pot should be located, at most, a few inches away from the LM111, and the 0.01 μF capacitor should be installed. If this capacitor cannot be used, a shielding printed-circuit foil may be advisable between pins 6 and 7. The power supply bypass capacitors should be located within a couple inches of the LM111. (Some other comparators require the power-supply bypass to be located immediately adjacent to the comparator.)



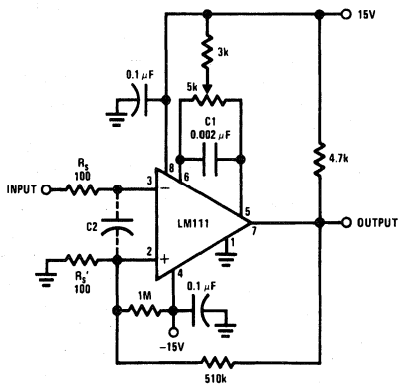
TL/H/5704–29

Pin connections shown are for LM111H in the H08 hermetic package

FIGURE 1. Improved Positive Feedback

Application Hints (Continued)

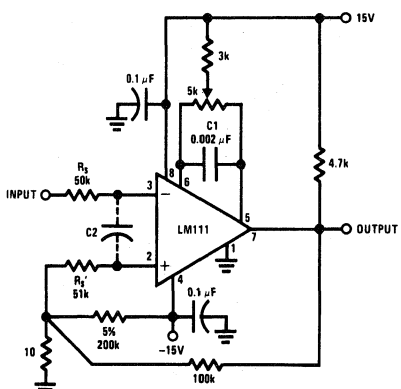
6. It is a standard procedure to use hysteresis (positive feedback) around a comparator, to prevent oscillation, and to avoid excessive noise on the output because the comparator is a good amplifier for its own noise. In the circuit of *Figure 2*, the feedback from the output to the positive input will cause about 3 mV of hysteresis. However, if R_S is larger than 100Ω, such as 50 kΩ, it would not be reasonable to simply increase the value of the positive feedback resistor above 510 kΩ. the circuit of *Figure 3* could be used, but it is rather awkward. See the notes in paragraph 7 below.
7. When both inputs of the LM111 are connected to active signals, or if a high-impedance signal is driving the positive input of the LM111 so that positive feedback would be disruptive, the circuit of *Figure 1* is ideal. The positive feedback is to pin 5 (one of the offset adjustment pins). It is sufficient to cause 1 to 2 mV hysteresis and sharp transitions with input triangle waves from a few Hz to hundreds of kHz. The positive-feedback signal across the 82Ω resistor swings 240 mV below the positive supply. This signal is centered around the nominal voltage at pin 5, so this feedback does not add to the V_{OS} of the comparator. As much as 8 mV of V_{OS} can be trimmed out, using the 5 kΩ pot and 3 kΩ resistor as shown.
8. These application notes apply specifically to the LM111, LM211, LM311, and LF111 families of comparators, and are applicable to all high-speed comparators in general, (with the exception that not all comparators have trim pins).



TL/H/5704–30

Pin connections shown are for LM111H in the H08 hermetic package

FIGURE 2. Conventional Positive Feedback

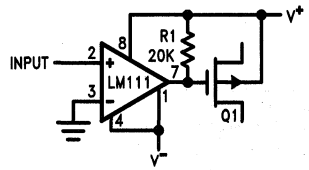


TL/H/5704–31

FIGURE 3. Positive Feedback with High Source Resistance

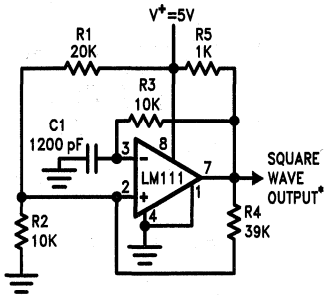
Typical Applications (Continued) (Pin numbers refer to H08 package)

Zero Crossing Detector Driving MOS Switch



TL/H/5704–13

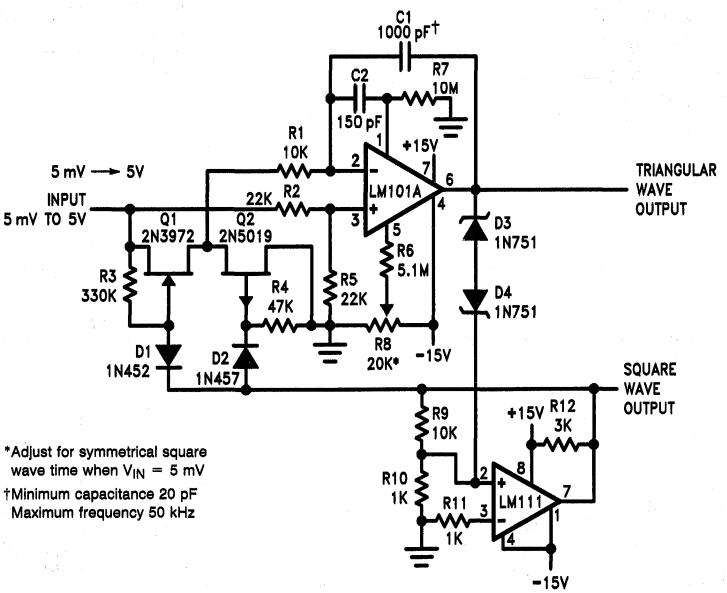
100 kHz Free Running Multivibrator



*TTL or DTL fanout of two

TL/H/5704–14

10 Hz to 10 kHz Voltage Controlled Oscillator

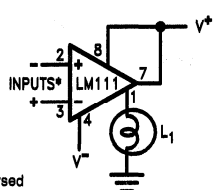


*Adjust for symmetrical square wave time when V_{IN} = 5 mV

†Minimum capacitance 20 pF
Maximum frequency 50 kHz

TL/H/5704–15

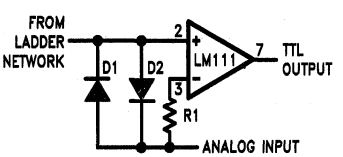
Driving Ground-Referred Load



*Input polarity is reversed when using pin 1 as output.

TL/H/5704–16

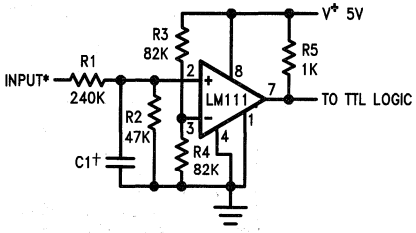
Using Clamp Diodes to Improve Response



TL/H/5704–17

Typical Applications (Continued) (Pin numbers refer to H08 package)

TTL Interface with High Level Logic

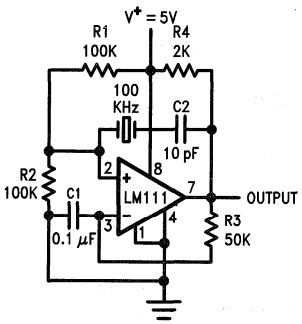


*Values shown are for a 0 to 30V logic swing and a 15V threshold.

†May be added to control speed and reduce susceptibility to noise spikes.

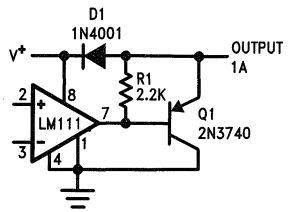
TL/H/5704–18

Crystal Oscillator



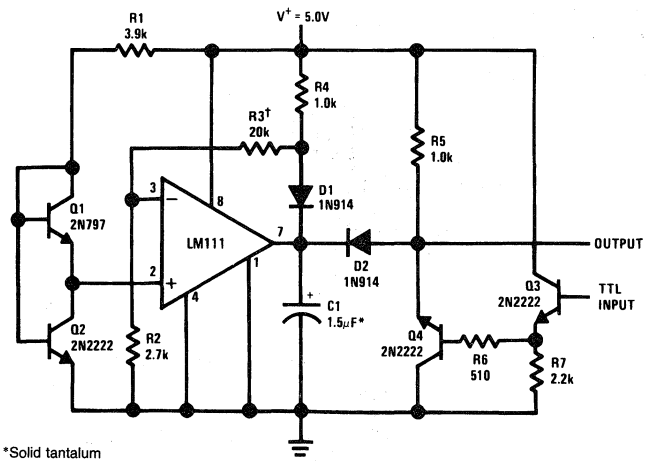
TL/H/5704–19

Comparator and Solenoid Driver



TL/H/5704–20

Precision Squarer

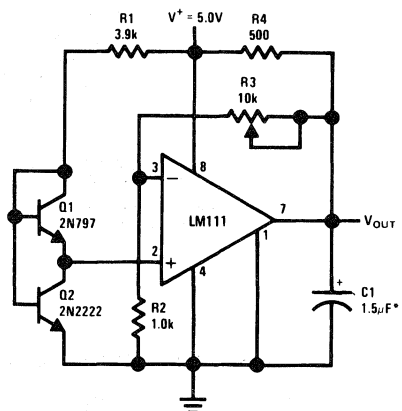


*Solid tantalum

†Adjust to set clamp level

TL/H/5704–21

Low Voltage Adjustable Reference Supply

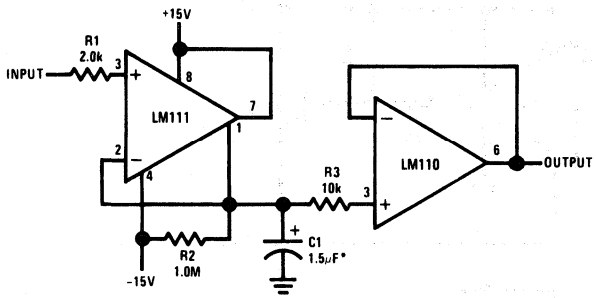


*Solid tantalum

TL/H/5704–22

Typical Applications (Continued) (Pin numbers refer to H08 package)

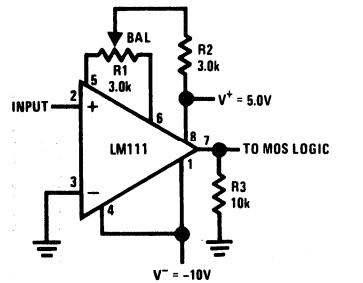
Positive Peak Detector



*Solid tantalum

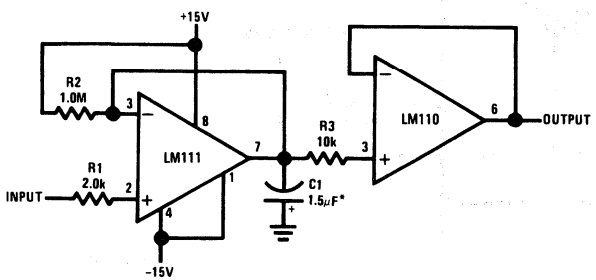
TL/H/5704-23

Zero Crossing Detector Driving MOS Logic



TL/H/5704-24

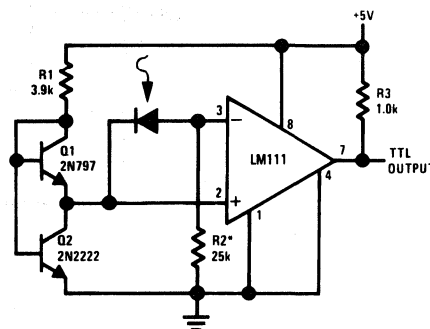
Negative Peak Detector



*Solid tantalum

TL/H/5704-25

Precision Photodiode Comparator

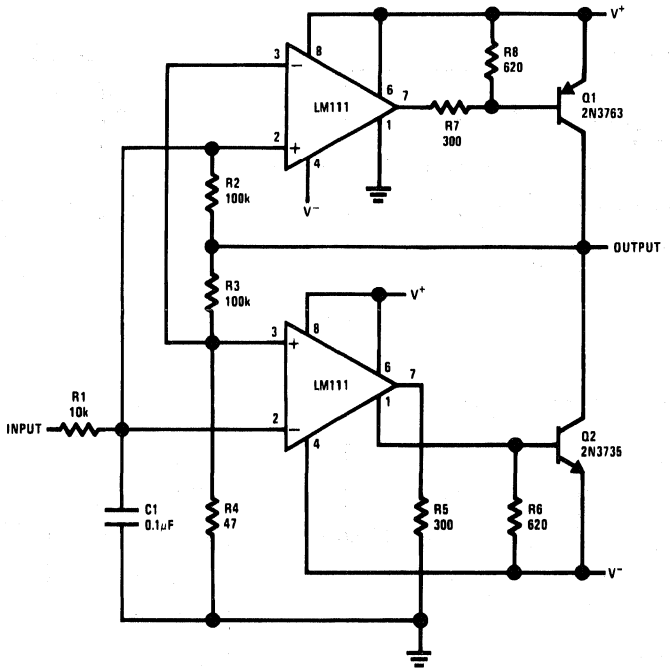


TL/H/5704-26

*R2 sets the comparison level. At comparison, the photodiode has less than 5 mV across it, decreasing leakages by an order of magnitude.

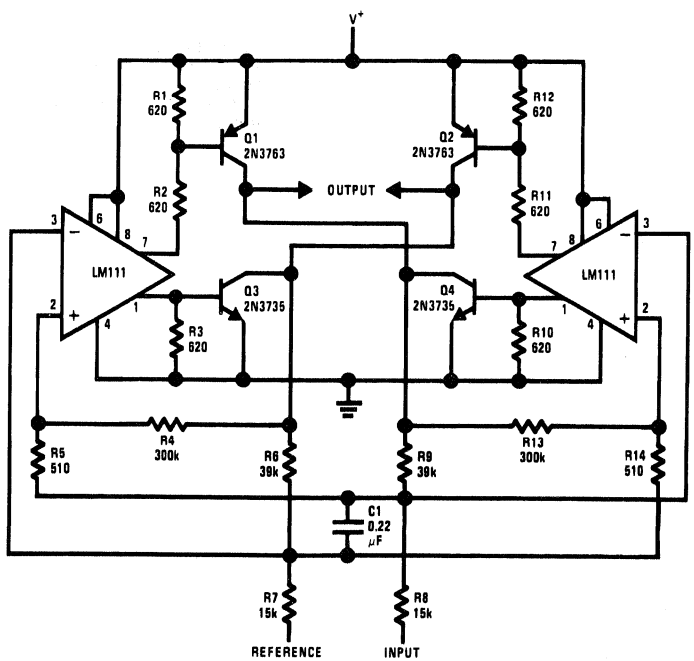
Typical Applications (Continued) (Pin numbers refer to H08 package)

Switching Power Amplifier



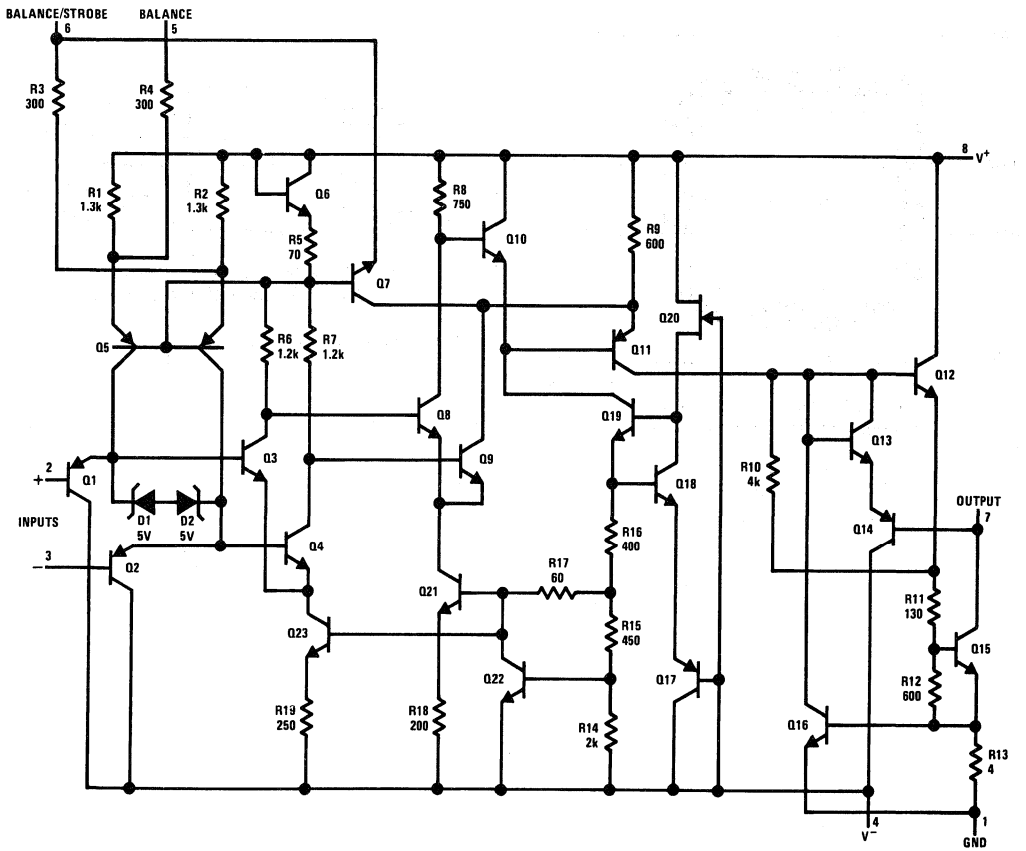
TL/H/5704-27

Switching Power Amplifier



TL/H/5704-28

Schematic Diagram**

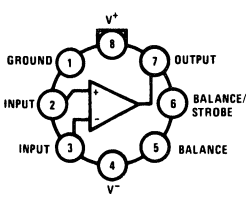


TL/H/5704–5

**Pin connections shown on schematic diagram are for H08 package.

Connection Diagrams*

Metal Can Package



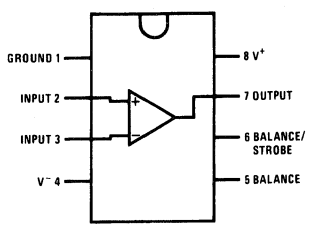
TL/H/5704–6

Top View

Note: Pin 4 connected to case

Order Number LM111H, LM111H/883*, LM211H or LM311H
See NS Package Number H08C

Dual-In-Line Package

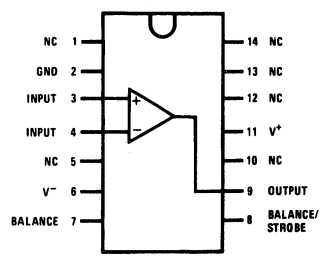


TL/H/5704–34

Top View

Order Number LM111J-8, LM111J-8/883*, LM211J-8, LM211M, LM311J-8, LM311M or LM311N
See NS Package Number J08A, M08A or N08E

Dual-In-Line Package



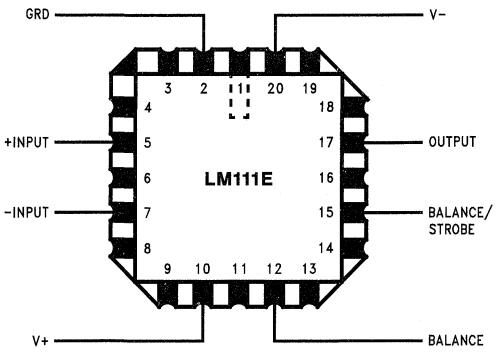
TL/H/5704–35

Top View

Order Number LM111J, LM111J/883*, LM211J, LM311J or LM311N-14
See NS Package Number J14A or N14A

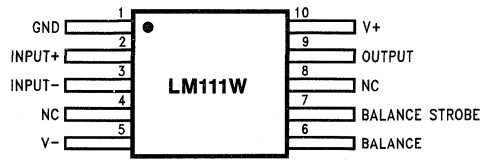
*Also available per JM38510/10304

Connection Diagrams (Continued)



TL/H/5704–32

Order Number LM111E/883
See NS Package Number E20A



TL/H/5704–33

Order Number LM111W/883*
See NS Package Number W10A

*Also available per JM38510/10304

National Semiconductor

LM119/LM219/LM319
High Speed Dual Comparator

General Description

The LM119 series are precision high speed dual comparators fabricated on a single monolithic chip. They are designed to operate over a wide range of supply voltages down to a single 5V logic supply and ground. Further, they have higher gain and lower input currents than devices like the LM710. The uncommitted collector of the output stage makes the LM119 compatible with RTL, DTL and TTL as well as capable of driving lamps and relays at currents up to 25 mA.

The LM319A offers improved precision over the standard LM319, with tighter tolerances on offset voltage, offset current, and voltage gain.

Features

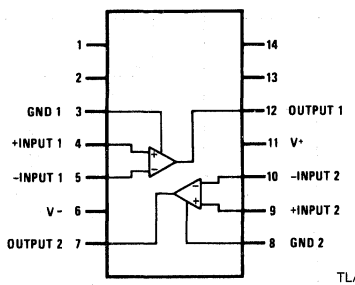
- Two independent comparators
- Operates from a single 5V supply
- Typically 80 ns response time at ±15V
- Minimum fan-out of 2 each side
- Maximum input current of 1 μA over temperature
- Inputs and outputs can be isolated from system ground
- High common mode slew rate

Although designed primarily for applications requiring operation from digital logic supplies, the LM119 series are fully specified for power supplies up to ±15V. It features faster response than the LM111 at the expense of higher power dissipation. However, the high speed, wide operating voltage range and low package count make the LM119 much more versatile than older devices like the LM711.

The LM119 is specified from −55°C to +125°C, the LM219 is specified from −25°C to +85°C, and the LM319A and LM319 are specified from 0°C to +70°C.

Connection Diagrams

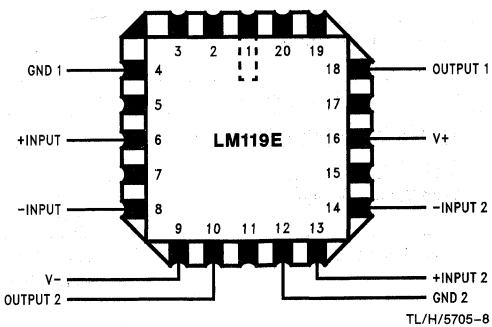
Dual-In-Line-Package



TL/H/5705–4

Top View

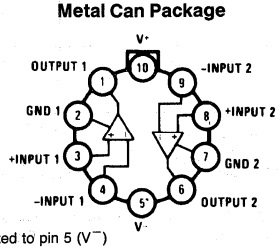
Order Number LM119J, LM119J/883*, LM219J, LM319J, LM319AM, LM319M, LM319AN or LM319N
See NS Package Number J14A, M14A or N14A



TL/H/5705–8

Order Number LM119E/883
See NS Package Number E20A

Metal Can Package

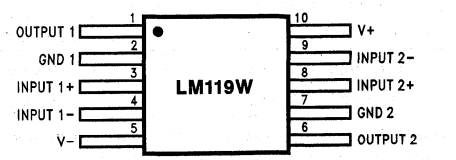


Case is connected to pin 5 (V⁻)

TL/H/5705–7

Top View

Order Number LM119H, LM119H/883*, or LM319H
See NS Package Number H10C



TL/H/5705–9

Order Number LM119W/883
See NS Package Number W10A

*Also available per SMD# 8601401 or JM38510/10306

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications. (Note 7)

Total Supply Voltage	36V
Output to Negative Supply Voltage	36V
Ground to Negative Supply Voltage	25V
Ground to Positive Supply Voltage	18V
Differential Input Voltage	±5V
Input Voltage (Note 1)	±15V
ESD rating (1.5 kΩ in series with 100 pF)	800V
Power Dissipation (Note 2)	500 mW
Output Short Circuit Duration	10 sec
Storage Temperature Range	−65°C to 150°C
Lead Temperature (Soldering, 10 sec.)	260°C
Soldering Information	
Dual-In-Line Package	
Soldering (10 seconds)	260°C
Small Outline Package	
Vapor Phase (60 seconds)	215°C
Infrared (15 seconds)	220°C

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

Operating Temperature Range

LM119	−55°C to 125°C
LM219	−25°C to 85°C

Electrical Characteristics (Note 3)

Parameter	Conditions	LM119/LM219			Units
		Min	Typ	Max	
Input Offset Voltage (Note 4)	$T_A = 25°C$, $R_S \leq 5k$		0.7	4.0	mV
Input Offset Current (Note 4)	$T_A = 25°C$		30	75	nA
Input Bias Current	$T_A = 25°C$		150	500	nA
Voltage Gain	$T_A = 25°C$ (Note 6)	10	40		V/mV
Response Time (Note 5)	$T_A = 25°C$, $V_S = \pm 15V$		80		ns
Saturation Voltage	$V_{IN} \leq -5$ mV, $I_{OUT} = 25$ mA $T_A = 25°C$		0.75	1.5	V
Output Leakage Current	$V_{IN} \geq 5$ mV, $V_{OUT} = 35V$ $T_A = 25°C$		0.2	2	μA
Input Offset Voltage (Note 4)	$R_S \leq 5k$			7	mV
Input Offset Current (Note 4)				100	nA
Input Bias Current				1000	nA
Input Voltage Range	$V_S = \pm 15V$ $V^+ = 5V$, $V^- = 0$	−12 1	±13	+12 3	V V
Saturation Voltage	$V^+ \geq 4.5V$, $V^- = 0$ $V_{IN} \leq -6$ mV, $I_{SINK} \leq 3.2$ mA $T_A \geq 0°C$ $T_A \leq 0°C$		0.23	0.4 0.6	V V
Output Leakage Current	$V_{IN} \geq 5$ mV, $V_{OUT} = 35V$, $V^- = V_{GND} = 0V$		1	10	μA
Differential Input Voltage				±5	V
Positive Supply Current	$T_A = 25°C$, $V^+ = 5V$, $V^- = 0$		4.3		mA
Positive Supply Current	$T_A = 25°C$, $V_S = \pm 15V$		8	11.5	mA
Negative Supply Current	$T_A = 25°C$, $V_S = \pm 15V$		3	4.5	mA

Note 1: For supply voltages less than ±15V the absolute maximum input voltage is equal to the supply voltage.

Note 2: The maximum junction temperature of the LM119 is 150°C, while that of the LM219 is 110°C. For operating at elevated temperatures, devices in the H10 package must be derated based on a thermal resistance of 160°C/W, junction to ambient, or 19°C/W, junction to case. The thermal resistance of the J14 and N14 packages is 100°C/W, junction to ambient.

Note 3: These specifications apply for $V_S = \pm 15V$, and the Ground pin at ground, and $-55°C \leq T_A \leq +125°C$, unless otherwise stated. With the LM219, however, all temperature specifications are limited to $-25°C \leq T_A \leq +85°C$. The offset voltage, offset current and bias current specifications apply for any supply voltage from a single 5V supply up to ±15V supplies. Do not operate the device with more than 16V from ground to V_S.

Note 4: The offset voltages and offset currents given are the maximum values required to drive the output within a volt of either supply with a 1 mA load. Thus, these parameters define an error band and take into account the worst case effects of voltage gain and input impedance.

Note 5: The response time specified (see definitions) is for a 100 mV input step with 5 mV overdrive.

Note 6: Output is pulled up to 15V through a 1.4 kΩ resistor.

Note 7: Refer to RETS119X for LM119H/883 and LM119J/883 specifications.

Absolute Maximum Ratings LM319A/319

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Total Supply Voltage	36V
Output to Negative Supply Voltage	36V
Ground to Negative Supply Voltage	25V
Ground to Positive Supply Voltage	18V
Differential Input Voltage	±5V
Input Voltage (Note 1)	±15V
Power Dissipation (Note 2)	500 mW
Output Short Circuit Duration	10 sec
ESD rating (1.5 kΩ in series with 100 pF)	800V
Storage Temperature Range	−65°C to 150°C
Lead Temperature (Soldering, 10 sec.)	260°C
Soldering Information	
Dual-In-Line Package	
Soldering (10 sec.)	260°C
Small Outline Package	
Vapor Phase (60 sec.)	215°C
Infrared (15 sec.)	220°C

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

Operating Temperature Range

LM319A, LM319	0°C to 70°C

Electrical Characteristics (Note 3)

Parameter	Conditions	LM319A			LM319			Units
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage (Note 4)	$T_A = 25°C$, $R_S \leq 5k$		0.5	1.0		2.0	8.0	mV
Input Offset Current (Note 4)	$T_A = 25°C$		20	40		80	200	nA
Input Bias Current	$T_A = 25°C$		150	500		250	1000	nA
Voltage Gain	$T_A = 25°C$ (Note 6)	20	40		8	40		V/mV
Response Time (Note 5)	$T_A = 25°C$, $V_S = \pm 15V$		80			80		ns
Saturation Voltage	$V_{IN} \leq -10$ mV, $I_{OUT} = 25$ mA $T_A = 25°C$		0.75	1.5		0.75	1.5	V
Output Leakage Current	$V_{IN} \geq 10$ mV, $V_{OUT} = 35V$, $V^- = V_{GND} = 0V$, $T_A = 25°C$		0.2	10		0.2	10	μA
Input Offset Voltage (Note 4)	$R_S \leq 5k$			10			10	mV
Input Offset Current (Note 4)				300			300	nA
Input Bias Current				1000			1200	nA
Input Voltage Range	$V_S = \pm 15V$ $V^+ = 5V$, $V^- = 0$	 1	±13	 3	 1	±13	 3	V V
Saturation Voltage	$V^+ \geq 4.5V$, $V^- = 0$ $V_{IN} \leq -10$ mV, $I_{SINK} \leq 3.2$ mA		0.3	0.4		0.3	0.4	V
Differential Input Voltage				±5			±5	V
Positive Supply Current	$T_A = 25°C$, $V^+ = 5V$, $V^- = 0$		4.3			4.3		mA
Positive Supply Current	$T_A = 25°C$, $V_S = \pm 15V$		8	12.5		8	12.5	mA
Negative Supply Current	$T_A = 25°C$, $V_S = \pm 15V$		3	5		3	5	mA

Note 1: For supply voltages less than ±15 the absolute maximum input voltage is equal to the supply voltage.

Note 2: The maximum junction temperature of the LM319A and LM319 is 85°C. For operating at elevated temperatures, devices in the H10 package must be derated based on a thermal resistance of 160°C/W, junction to ambient, or 19°C/W, junction to case. The thermal resistance of the N14 and J14 package is 100°C/W, junction to ambient. The thermal resistance of the M14 package is 115°C/W, junction to ambient.

Note 3: These specifications apply for $V_S = \pm 15V$, and $0°C \leq T_A \leq 70°C$, unless otherwise stated. The offset voltage, offset current and bias current specifications apply for any supply voltage from a single 5V supply up to ±15V supplies. Do not operate the device with more than 16V from ground to V_S.

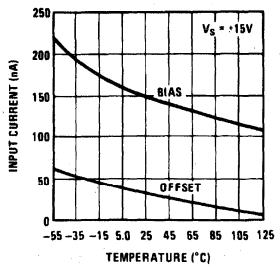
Note 4: The offset voltages and offset currents given are the maximum values required to drive the output within a volt of either supply with a 1 mA load. Thus, these parameters define an error band and take into account the worst case effects of voltage gain and input impedance.

Note 5: The response time specified is for a 100 mV input step with 5 mV overdrive.

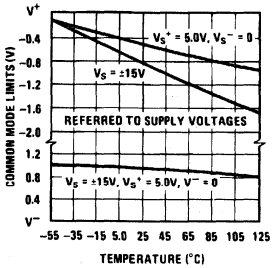
Note 6: Output is pulled up to 15V through a 1.4 kΩ resistor.

Typical Performance Characteristics LM119A/LM119/LM219

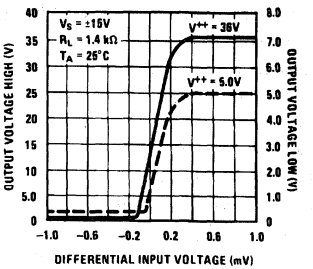
Input Currents



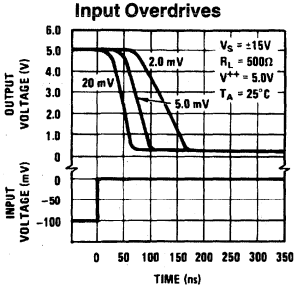
Common Mode Limits



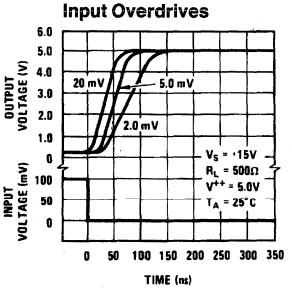
Transfer Function



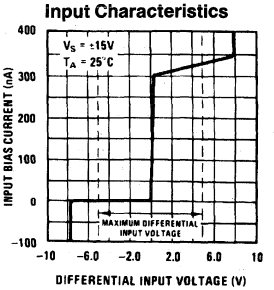
Response Time for Various Input Overdrives



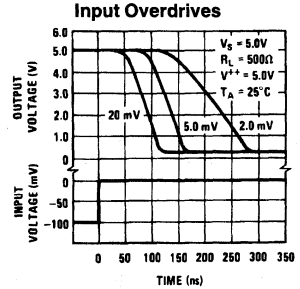
Response Time for Various Input Overdrives



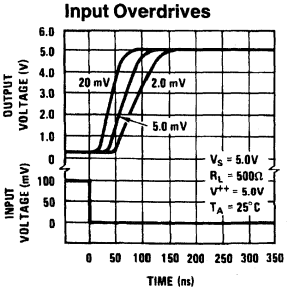
Input Characteristics



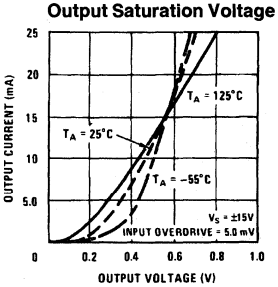
Response Time for Various Input Overdrives



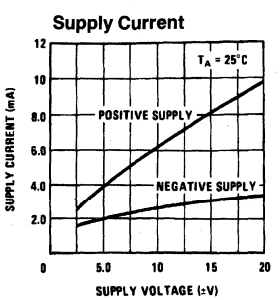
Response Time for Various Input Overdrives



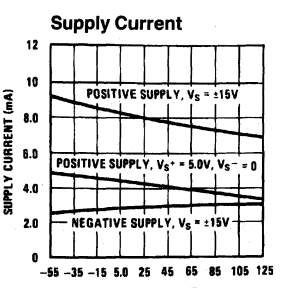
Output Saturation Voltage



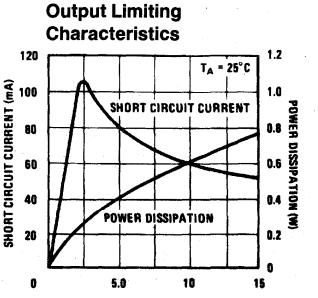
Supply Current



Supply Current



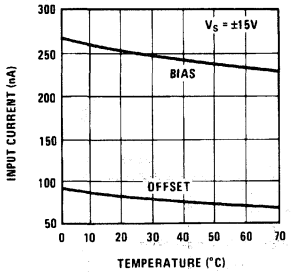
Output Limiting Characteristics



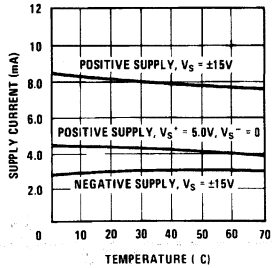
TL/H/5705–2

Typical Performance Characteristics LM319A, LM319

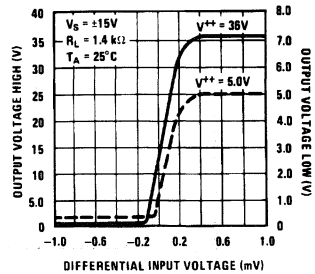
Input Currents



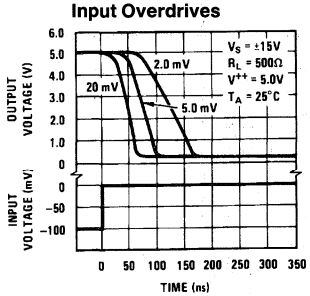
Supply Currents



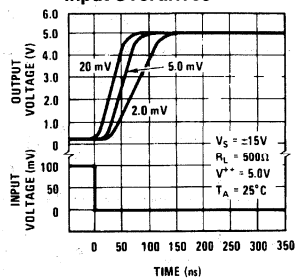
Transfer Function



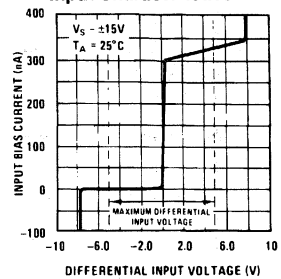
Response Time for Various Input Overdrives



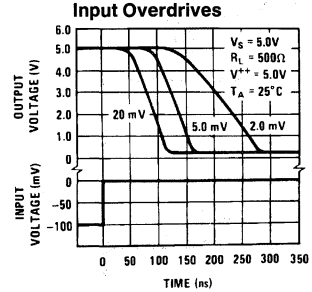
Response Time for Various Input Overdrives



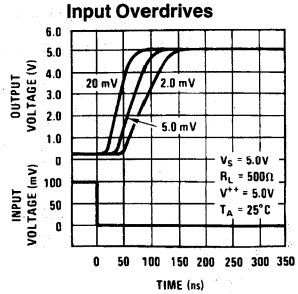
Input Characteristics



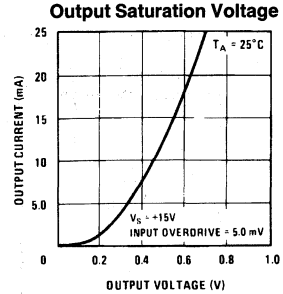
Response Time for Various Input Overdrives



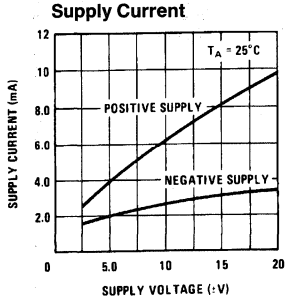
Response Time for Various Input Overdrives



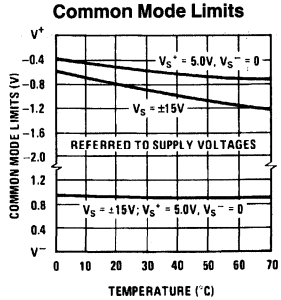
Output Saturation Voltage



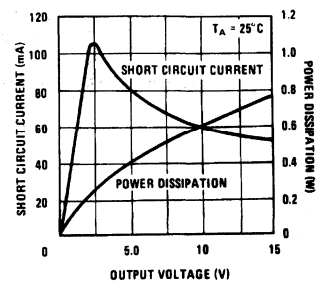
Supply Current



Common Mode Limits



Output Limiting Characteristics



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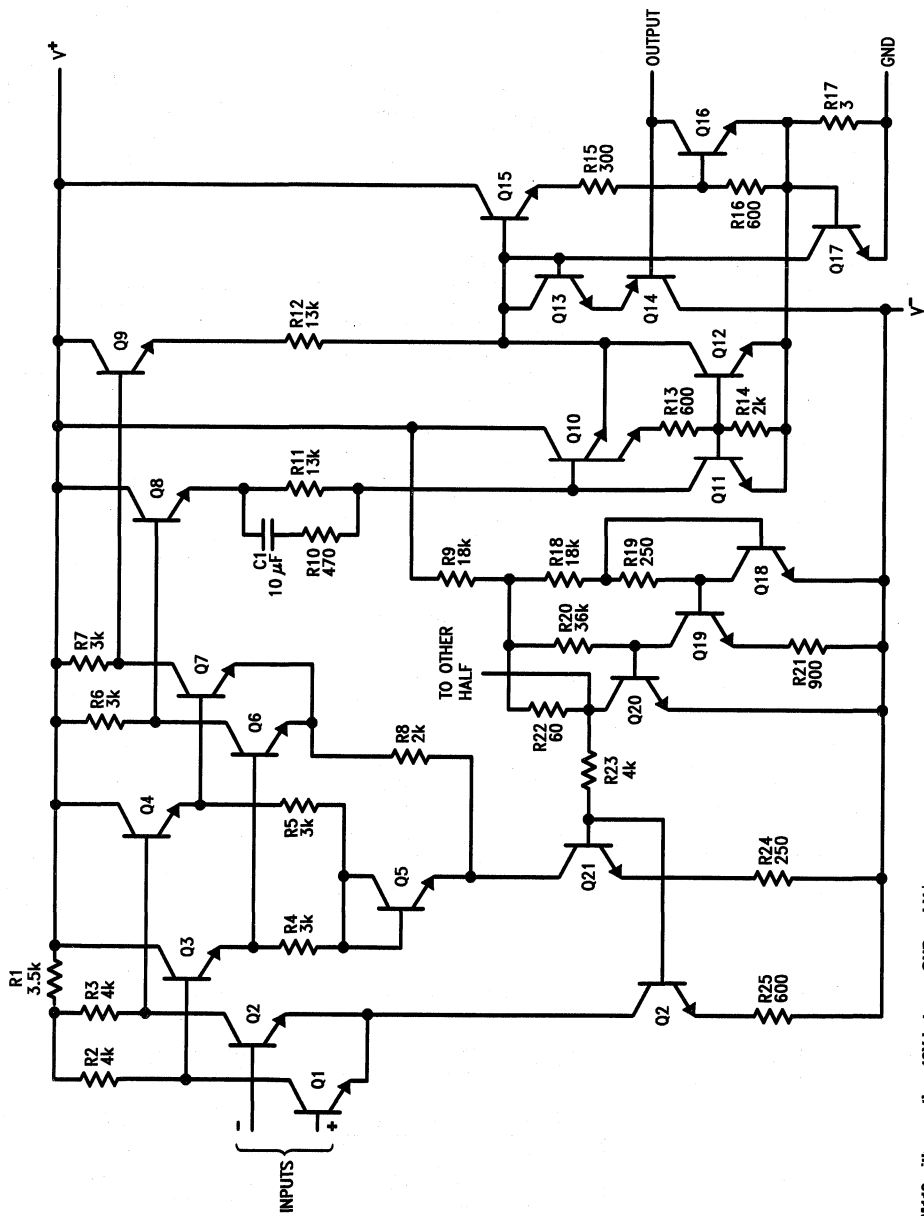
Schematic Diagram

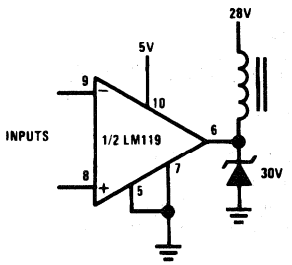


TL/H/5705–1

*Do not operate the LM119 with more than 16V between GND and V+.

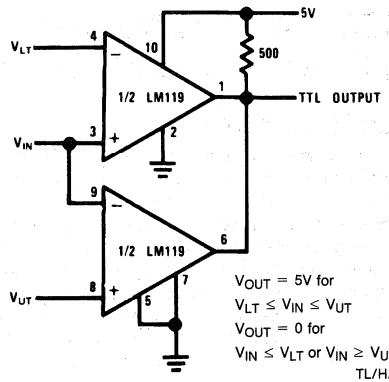
Typical Applications*

Relay Driver



TL/H/5705–5

Window Detector



V_{OUT} = 5V for
$V_{LT} \leq V_{IN} \leq V_{UT}$
V_{OUT} = 0 for
$V_{IN} \leq V_{LT}$ or $V_{IN} \geq V_{UT}$

TL/H/5705–6

*Pin numbers are for metal can package.

National Semiconductor

LM139/LM239/LM339/LM2901/LM3302
Low Power Low Offset Voltage Quad Comparators

General Description

The LM139 series consists of four independent precision voltage comparators with an offset voltage specification as low as 2 mV max for all four comparators. These were designed specifically to operate from a single power supply over a wide range of voltages. Operation from split power supplies is also possible and the low power supply current drain is independent of the magnitude of the power supply voltage. These comparators also have a unique characteristic in that the input common-mode voltage range includes ground, even though operated from a single power supply voltage.

Application areas include limit comparators, simple analog to digital converters; pulse, squarewave and time delay generators; wide range VCO; MOS clock timers; multivibrators and high voltage digital logic gates. The LM139 series was designed to directly interface with TTL and CMOS. When operated from both plus and minus power supplies, they will directly interface with MOS logic— where the low power drain of the LM339 is a distinct advantage over standard comparators.

Advantages

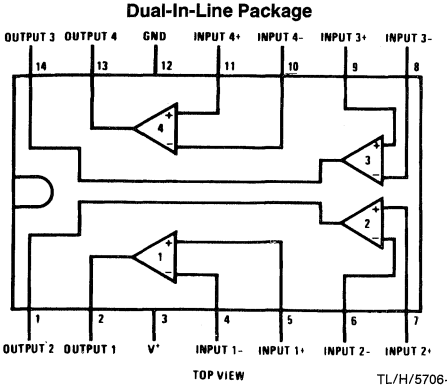
- High precision comparators
- Reduced V_{OS} drift over temperature
- Eliminates need for dual supplies
- Allows sensing near GND
- Compatible with all forms of logic
- Power drain suitable for battery operation

Features

- Wide supply voltage range
  LM139 series, 2 V_{DC} to 36 V_{DC} or ±1 V_{DC} to ±18 V_{DC}
  LM139A series, LM2901 2 V_{DC} to 28 V_{DC}
  LM3302 or ±1 V_{DC} to ±14 V_{DC}
- Very low supply current drain (0.8 mA) — independent of supply voltage
- Low input biasing current 25 nA
- Low input offset current ±5 nA
  and offset voltage ±3 mV
- Input common-mode voltage range includes GND
- Differential input voltage range equal to the power supply voltage
- Low output saturation voltage 250 mV at 4 mA
- Output voltage compatible with TTL, DTL, ECL, MOS and CMOS logic systems

Connection Diagrams

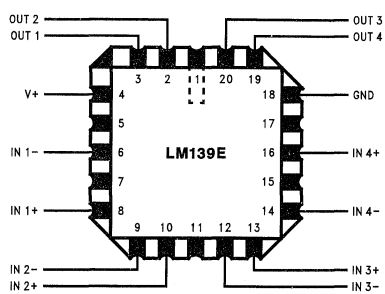
Dual-In-Line Package



TOP VIEW TL/H/5706-2

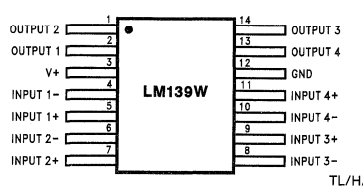
Order Number LM139J, LM139J/883*, LM139AJ, LM139AJ/883, LM239J, LM239AJ, LM339J, LM339AJ or LM2901J**
See NS Package Number J14A
Order Number LM339AM, LM339M or LM2901M
See NS Package Number M14A
Order Number LM339N, LM339AN, LM2901N or LM3302N
See NS Package Number N14A

*Available per JM38510/11201
**Available per SMD# 5962-8873901



TL/H/5706-26

Order Number LM139AE/883 or LM139E/883
See NS Package Number E20A



TL/H/5706-27

Order Number LM139AW/883 or LM139W/883*
See NS Package Number W14B

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications. (Note 10)

	LM139/LM239/LM339 LM139A/LM239A/LM339A LM2901	LM3302
Supply Voltage, V^+	36 V_{DC} or ±18 V_{DC}	28 V_{DC} or ±14 V_{DC}
Differential Input Voltage (Note 8)	36 V_{DC}	28 V_{DC}
Input Voltage	−0.3 V_{DC} to +36 V_{DC}	−0.3 V_{DC} to +28 V_{DC}
Input Current ($V_{IN} < -0.3$ V_{DC}), (Note 3)	50 mA	50 mA
Power Dissipation (Note 1)		
Molded DIP	1050 mW	1050 mW
Cavity DIP	1190 mW	
Small Outline Package	760 mW	
Output Short-Circuit to GND, (Note 2)	Continuous	Continuous
Storage Temperature Range	−65°C to +150°C	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	260°C	260°C

	LM139/LM239/LM339 LM139A/LM239A/LM339A LM2901	LM3302
Operating Temperature Range		−40°C to +85°C
LM339/LM339A	0°C to +70°C	
LM239/LM239A	−25°C to +85°C	
LM2901	−40°C to +85°C	
LM139/LM139A	−55°C to +125°C	
Soldering Information		
Dual-In-Line Package		
Soldering (10 seconds)	260°C	260°C
Small Outline Package		
Vapor Phase (60 seconds)	215°C	215°C
Infrared (15 seconds)	220°C	220°C

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

ESD rating (1.5 kΩ in series with 100 pF)	600V	600V

Electrical Characteristics ($V^+ = 5$ V_{DC}, $T_A = 25°C$, unless otherwise stated)

Parameter	Conditions	LM139A			LM239A, LM339A			LM139			LM239, LM339			LM2901			LM3302			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	(Note 9)		1.0	2.0		1.0	2.0		2.0	5.0		2.0	5.0		2.0	7.0		3	20	mV_{DC}
Input Bias Current	$I_{IN(+)}$ or $I_{IN(-)}$ with Output in Linear Range, (Note 5), $V_{CM} = 0V$		25	100		25	250		25	100		25	250		25	250		25	500	nA_{DC}
Input Offset Current	$I_{IN(+)} - I_{IN(-)}$, $V_{CM} = 0V$		3.0	25		5.0	50		3.0	25		5.0	50		5	50		3	100	nA_{DC}
Input Common-Mode Voltage Range	$V^+ = 30$ V_{DC} (LM3302, $V^+ = 28$ V_{DC}) (Note 6)	0		$V^+ - 1.5$	0		$V^+ - 1.5$	0		$V^+ - 1.5$	0		$V^+ - 1.5$	0		$V^+ - 1.5$	0		$V^+ - 1.5$	V_{DC}
Supply Current	$R_L = \infty$ on all Comparators, $R_L = \infty$, $V^+ = 36V$, (LM3302, $V^+ = 28$ V_{DC})		0.8 1.0	2.0 2.5		0.8 1.0	2.0 2.5		0.8 1.0	2.0 2.5		0.8 1.0	2.0 2.5		0.8 1.0	2.0 2.5		0.8 1.0	2.0 2.5	mA_{DC} mA_{DC}
Voltage Gain	$R_L \geq 15$ kΩ, $V^+ = 15$ V_{DC} $V_o = 1$ V_{DC} to 11 V_{DC}	50	200		50	200		50	200		50	200		25	100		2	30		V/mV
Large Signal Response Time	V_{IN} = TTL Logic Swing, $V_{REF} = 1.4$ V_{DC}, $V_{RL} = 5$ V_{DC}, $R_L = 5.1$ kΩ,		300			300			300			300			300			300		ns
Response Time	$V_{RL} = 5$ V_{DC}, $R_L = 5.1$ kΩ, (Note 7)		1.3			1.3			1.3			1.3			1.3			1.3		μs
Output Sink Current	$V_{IN(-)} = 1$ V_{DC}, $V_{IN(+)} = 0$, $V_O \leq 1.5$ V_{DC}	6.0	16		6.0	16		6.0	16		6.0	16		6.0	16		6.0	16		mA_{DC}

Electrical Characteristics ($V^+ = 5\ V_{DC}$, $T_A = 25°C$, unless otherwise stated) (Continued)

Parameter	Conditions	LM139A			LM239A, LM339A			LM139			LM239, LM339			LM2901			LM3302			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Saturation Voltage	$V_{IN(-)} = 1\ V_{DC}$, $V_{IN(+)} = 0$, $I_{SINK} \leq 4$ mA		250	400		250	400		250	400		250	400		250	400		250	500	mV_{DC}
Output Leakage Current	$V_{IN(+)} = 1\ V_{DC}$, $V_{IN(-)} = 0$, $V_O = 5\ V_{DC}$		0.1			0.1			0.1			0.1			0.1			0.1		nA_{DC}

Electrical Characteristics ($V^+ = 5.0\ V_{DC}$, Note 4)

Parameter	Conditions	LM139A			LM239A, LM339A			LM139			LM239, LM339			LM2901			LM3302			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	(Note 9)			4.0			4.0			9.0			9.0		9	15			40	mV_{DC}
Input Offset Current	$I_{IN(+)} - I_{IN(-)}$, $V_{CM} = 0V$			100			150			100			150		50	200			300	nA_{DC}
Input Bias Current	$I_{IN(+)}$ or $I_{IN(-)}$ with Output in Linear Range, $V_{CM} = 0V$ (Note 5)			300			400			300			400		200	500			1000	nA_{DC}
Input Common-Mode Voltage Range	$V^+ = 30\ V_{DC}$ (LM3302, $V^+ = 28\ V_{DC}$) (Note 6)	0		$V^+ - 2.0$	0		$V^+ - 2.0$	0		$V^+ - 2.0$			$V^+ - 2.0$	0		$V^+ - 2.0$	0		$V^+ - 2.0$	V_{DC}
Saturation Voltage	$V_{IN(-)} = 1\ V_{DC}$, $V_{IN(+)} = 0$, $I_{SINK} \leq 4$ mA			700			700			700			700		400	700			700	mV_{DC}
Output Leakage Current	$V_{IN(+)} = 1\ V_{DC}$, $V_{IN(-)} = 0$, $V_O = 30\ V_{DC}$, (LM3302, $V_O = 28\ V_{DC}$)			1.0			1.0			1.0			1.0			1.0			1.0	μA_{DC}
Differential Input Voltage	Keep all V_{IN}'s $\geq 0\ V_{DC}$ (or V^-, if used), (Note 8)			36			36			36			36			36			28	V_{DC}

Note 1: For operating at high temperatures, the LM339/LM339A, LM2901, LM3302 must be derated based on a 125°C maximum junction temperature and a thermal resistance of 95°C/W which applies for the device soldered in a printed circuit board, operating in a still air ambient. The LM239 and LM139 must be derated based on a 150°C maximum junction temperature. The low bias dissipation and the "ON-OFF" characteristic of the outputs keeps the chip dissipation very small ($P_D \leq 100$ mW), provided the output transistors are allowed to saturate.

Note 2: Short circuits from the output to V^+ can cause excessive heating and eventual destruction. When considering short circuits to ground, the maximum output current is approximately 20 mA independent of the magnitude of V^+.

Note 3: This input current will only exist when the voltage at any of the input leads is driven negative. It is due to the collector-base junction of the input PNP transistors becoming forward biased and thereby acting as input diode clamps. In addition to this diode action, there is also lateral NPN parasitic transistor action on the IC chip. This transistor action can cause the output voltages of the comparators to go to the V^+ voltage level (or to ground for a large overdrive) for the time duration that an input is driven negative. This is not destructive and normal output states will re-establish when the input voltage, which was negative, again returns to a value greater than $-0.3\ V_{DC}$ (at 25°)C.

Note 4: These specifications are limited to $-55°C \leq T_A \leq +125°C$, for the LM139/LM139A. With the LM239/LM239A, all temperature specifications are limited to $-25°C \leq T_A \leq +85°C$, the LM339/LM339A temperature specifications are limited to $0°C \leq T_A \leq +70°C$, and the LM2901, LM3302 temperature range is $-40°C \leq T_A \leq +85°C$.

Note 5: The direction of the input current is out of the IC due to the PNP input stage. This current is essentially constant, independent of the state of the output so no loading change exists on the reference or input lines.

Note 6: The input common-mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3V. The upper end of the common-mode voltage range is $V^+ - 1.5V$ at 25°C, but either or both inputs can go to $+30\ V_{DC}$ without damage (25V for LM3302), independent of the magnitude of V^+.

Note 7: The response time specified is a 100 mV input step with 5 mV overdrive. For larger overdrive signals 300 ns can be obtained, see typical performance characteristics section.

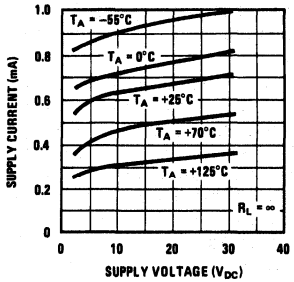
Note 8: Positive excursions of input voltage may exceed the power supply level. As long as the other voltage remains within the common-mode range, the comparator will provide a proper output state. The low input voltage state must not be less than $-0.3\ V_{DC}$ (or $0.3\ V_{DC}$ below the magnitude of the negative power supply, if used) (at 25°C).

Note 9: At output switch point, $V_O \cong 1.4\ V_{DC}$, $R_S = 0\Omega$ with V^+ from $5\ V_{DC}$ to $30\ V_{DC}$; and over the full input common-mode range ($0\ V_{DC}$ to $V^+ - 1.5\ V_{DC}$), at 25°C. For LM3302, V^+ from $5\ V_{DC}$ to $28\ V_{DC}$.

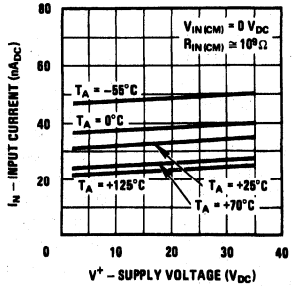
Note 10: Refer to RETS139AX for LM139A military specifications and to RETS139X for LM139 military specifications.

Typical Performance Characteristics LM139/LM239/LM339, LM139A/LM239A/LM339A, LM3302

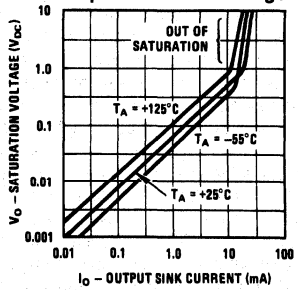
Supply Current



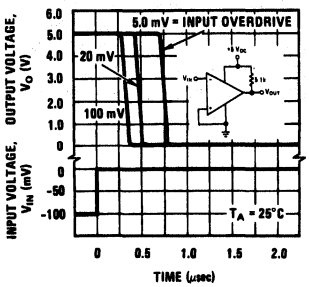
Input Current



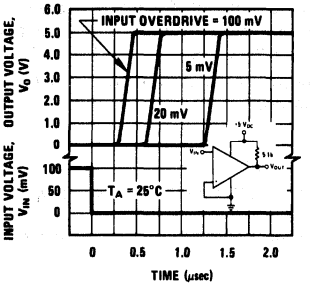
Output Saturation Voltage



Response Time for Various Input Overdrives—Negative Transition



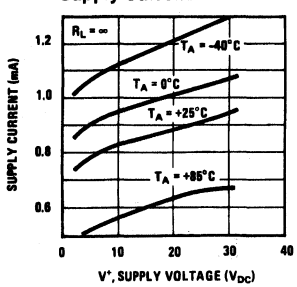
Response Time for Various Input Overdrives—Positive Transition



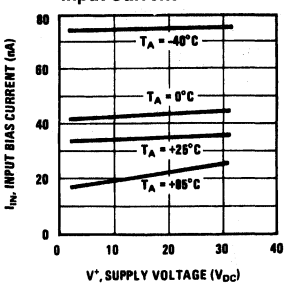
TL/H/5706–6

Typical Performance Characteristics LM2901

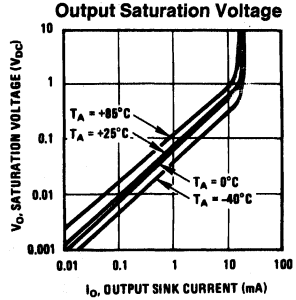
Supply Current



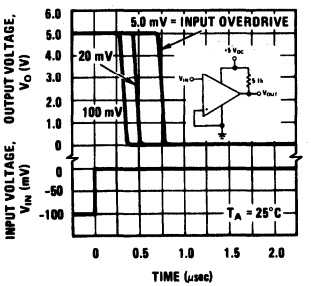
Input Current



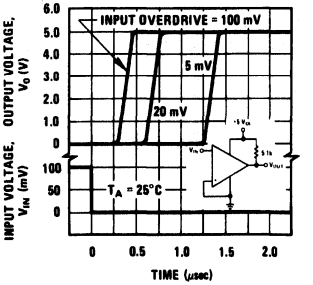
Output Saturation Voltage



Response Time for Various Input Overdrives-Negative Transition



Response Time for Various Input Overdrives-Positive Transition



TL/H/5706–7

Application Hints

The LM139 series are high gain, wide bandwidth devices which, like most comparators, can easily oscillate if the output lead is inadvertently allowed to capacitively couple to the inputs via stray capacitance. This shows up only during the output voltage transition intervals as the comparator changes states. Power supply bypassing is not required to solve this problem. Standard PC board layout is helpful as it reduces stray input-output coupling. Reducing this input resistors to $< 10\ k\Omega$ reduces the feedback signal levels and finally, adding even a small amount (1 to 10 mV) of positive feedback (hysteresis) causes such a rapid transition that oscillations due to stray feedback are not possible. Simply socketing the IC and attaching resistors to the pins will cause input-output oscillations during the small transition intervals unless hysteresis is used. If the input signal is a pulse waveform, with relatively fast rise and fall times, hysteresis is not required.

All pins of any unused comparators should be grounded.

The bias network of the LM139 series establishes a drain current which is independent of the magnitude of the power supply voltage over the range of from 2 V_{DC} to 30 V_{DC}.

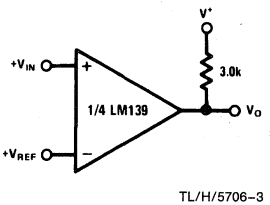
It is usually unnecessary to use a bypass capacitor across the power supply line.

The differential input voltage may be larger than V^+ without damaging the device. Protection should be provided to prevent the input voltages from going negative more than -0.3 V_{DC} (at 25°C). An input clamp diode can be used as shown in the applications section.

The output of the LM139 series is the uncommitted collector of a grounded-emitter NPN output transistor. Many collectors can be tied together to provide an output OR'ing function. An output pull-up resistor can be connected to any available power supply voltage within the permitted supply voltage range and there is no restriction on this voltage due to the magnitude of the voltage which is applied to the V^+ terminal of the LM139A package. The output can also be used as a simple SPST switch to ground (when a pull-up resistor is not used). The amount of current which the output device can sink is limited by the drive available (which is independent of V^+) and the β of this device. When the maximum current limit is reached (approximately 16 mA), the output transistor will come out of saturation and the output voltage will rise very rapidly. The output saturation voltage is limited by the approximately 60Ω R_{SAT} of the output transistor. The low offset voltage of the output transistor (1 mV) allows the output to clamp essentially to ground level for small load currents.

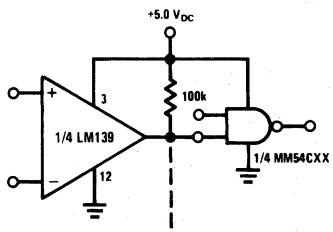
Typical Applications ($V^+ = 5.0\ V_{DC}$)

Basic Comparator



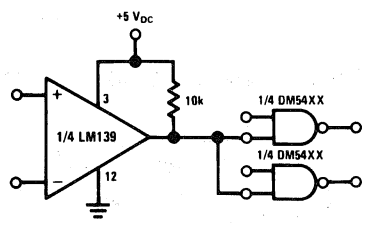
TL/H/5706–3

Driving CMOS



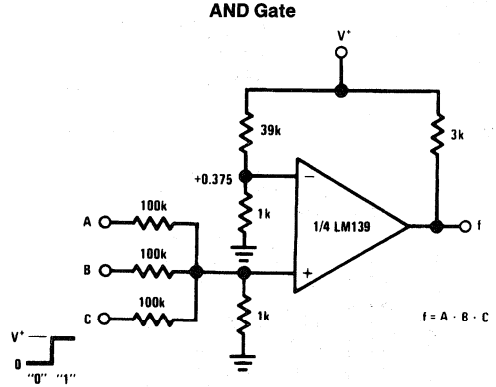
TL/H/5706–4

Driving TTL



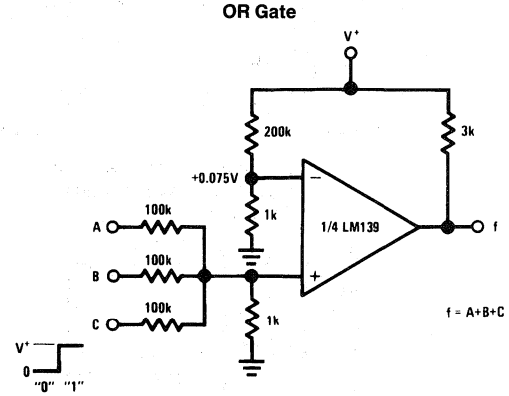
TL/H/5706–5

AND Gate



TL/H/5706–8

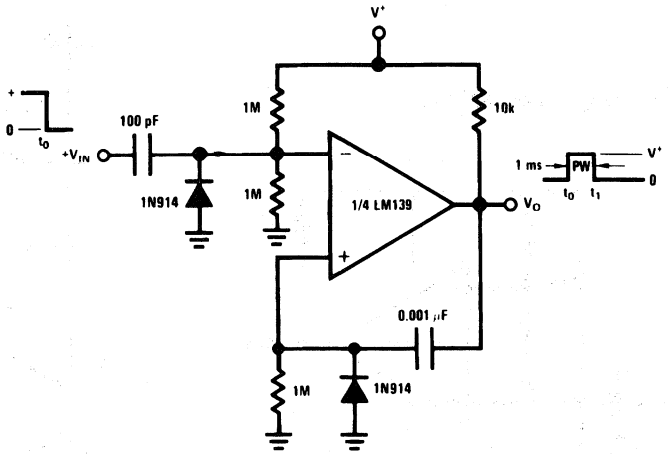
OR Gate



TL/H/5706–9

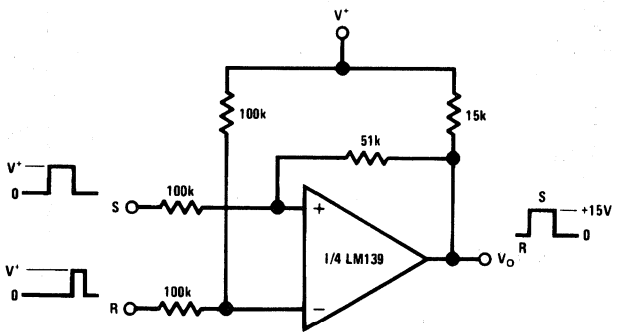
Typical Applications ($V^+ = 15\ V_{DC}$) (Continued)

One-Shot Multivibrator



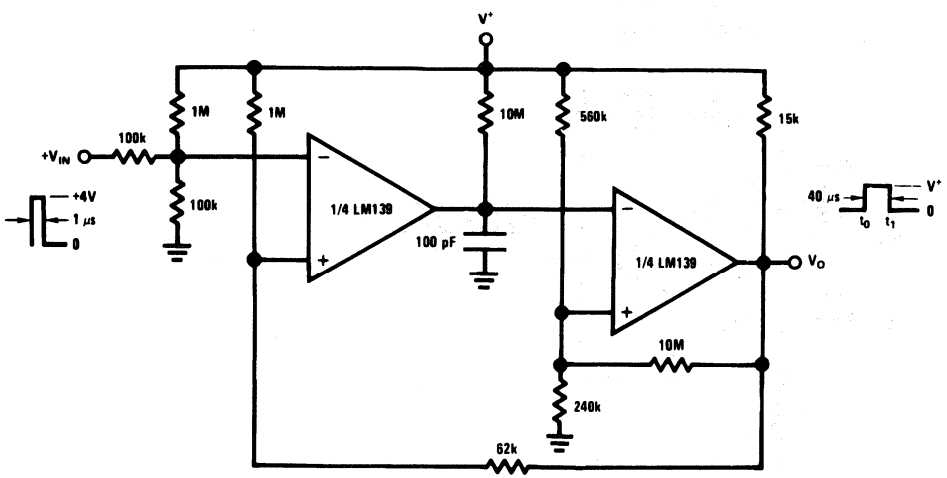
TL/H/5706–10

Bi-Stable Multivibrator



TL/H/5706–11

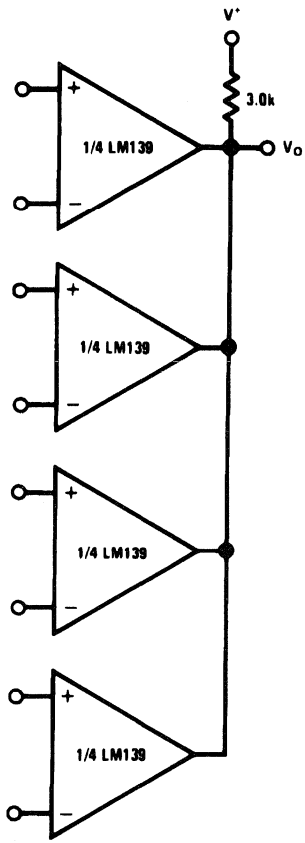
One-Shot Multivibrator with Input Lock Out



TL/H/5706–12

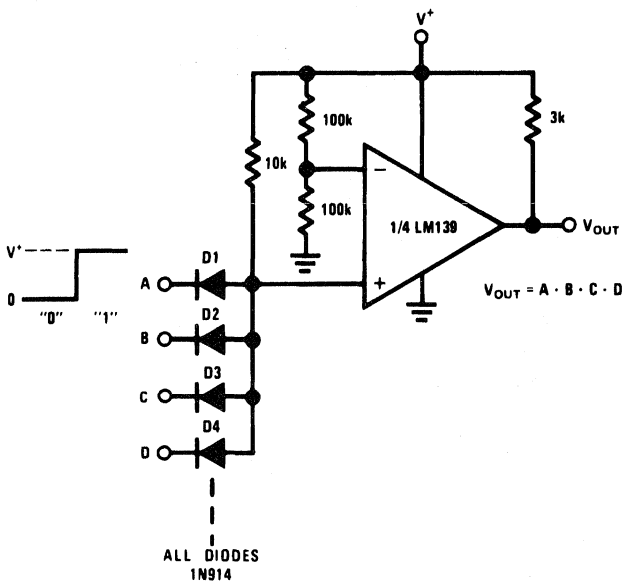
Typical Applications ($V^+ = 15\ V_{DC}$) (Continued)

ORing the Outputs



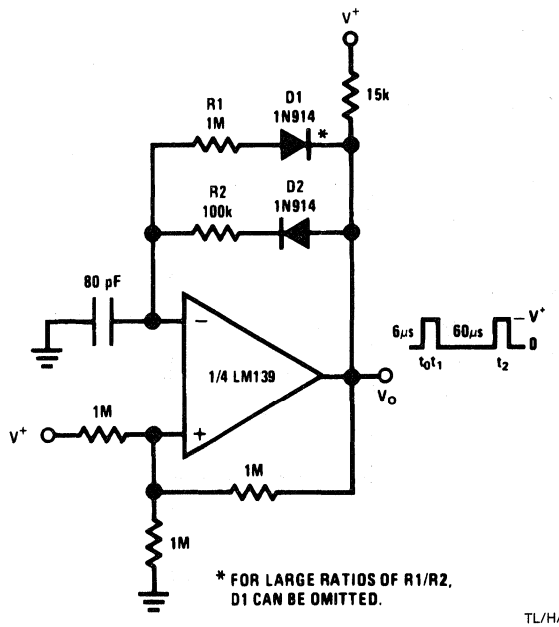
TL/H/5706–15

Large Fan-In AND Gate



TL/H/5706–13

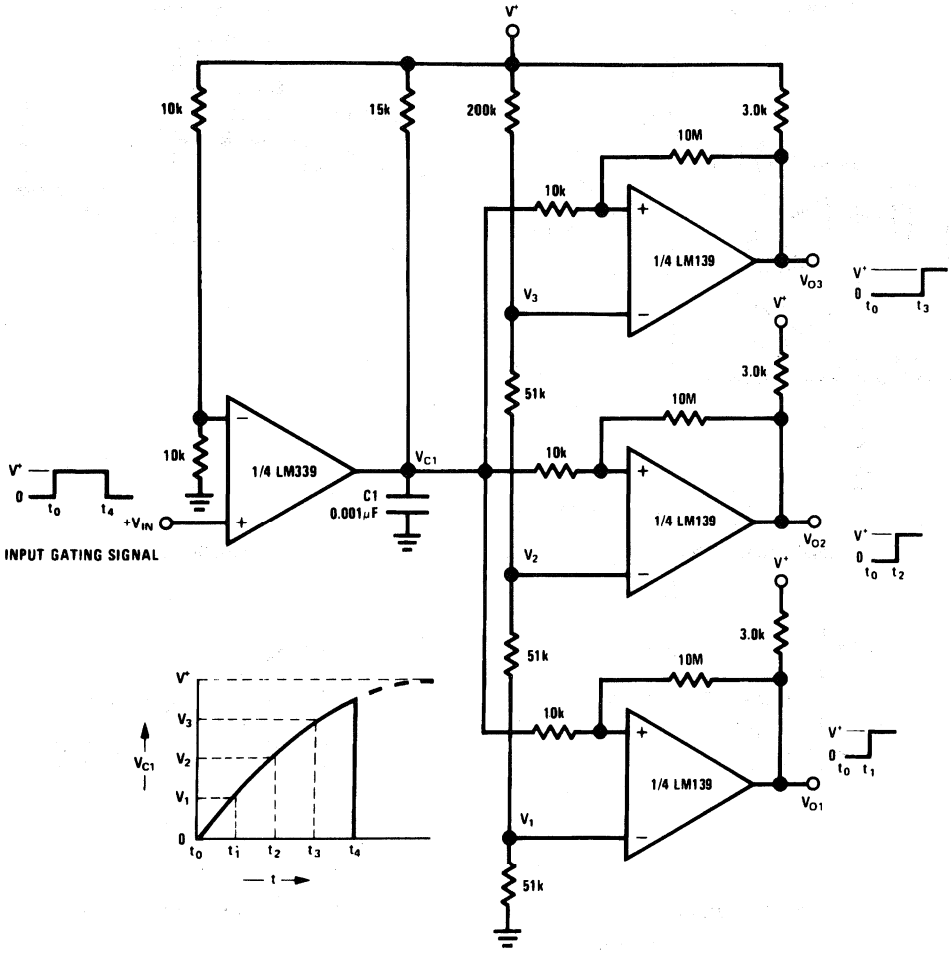
Pulse Generator



TL/H/5706–17

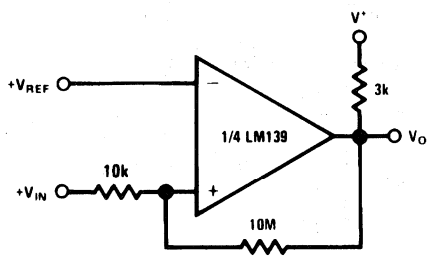
Typical Applications ($V^+ = 15\ V_{DC}$) (Continued)

Time Delay Generator



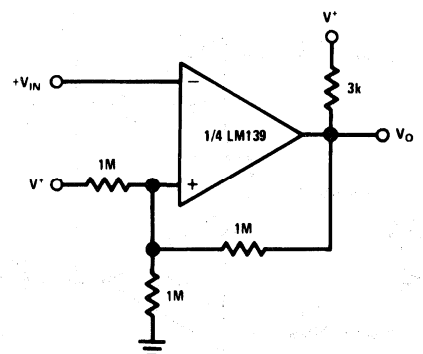
TL/H/5706–14

Non-Inverting Comparator with Hysteresis



TL/H/5706–18

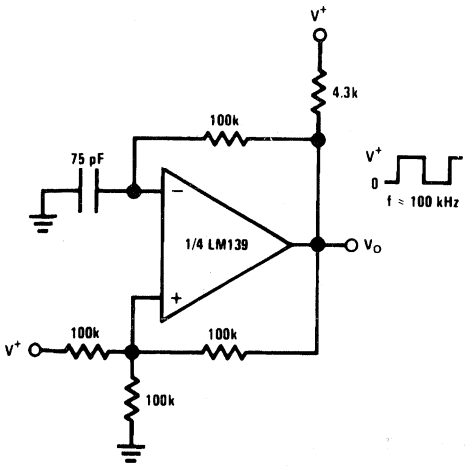
Inverting Comparator with Hysteresis



TL/H/5706–19

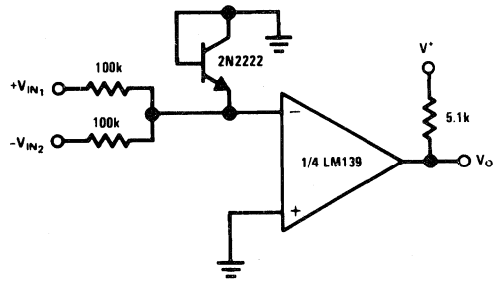
Typical Applications ($V^+ = 15\ V_{DC}$) (Continued)

Squarewave Oscillator



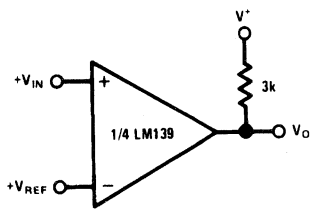
TL/H/5706–16

Comparing Input Voltages of Opposite Polarity



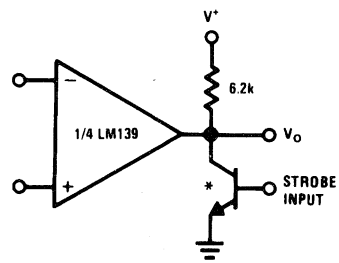
TL/H/5706–20

Basic Comparator



TL/H/5706–21

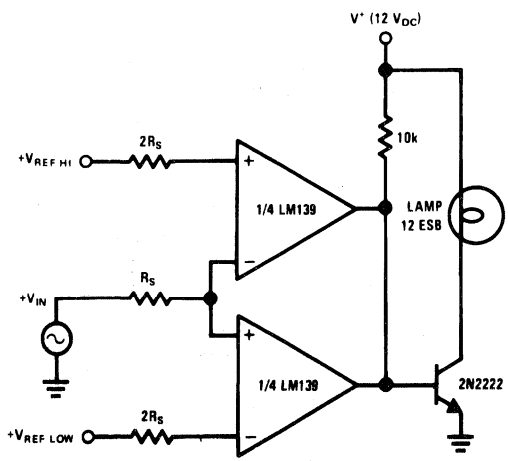
Output Strobing



TL/H/5706–22

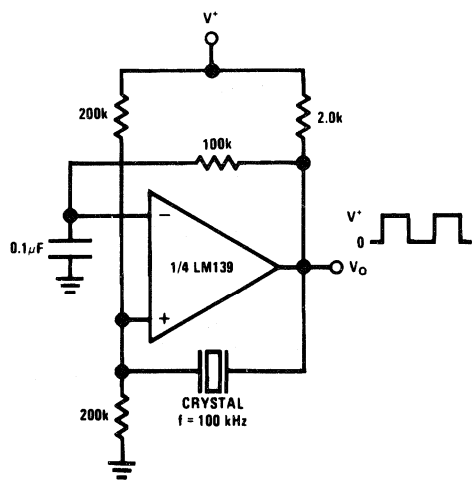
*Or open-collector logic gate without pull-up resistor

Limit Comparator



TL/H/5706–24

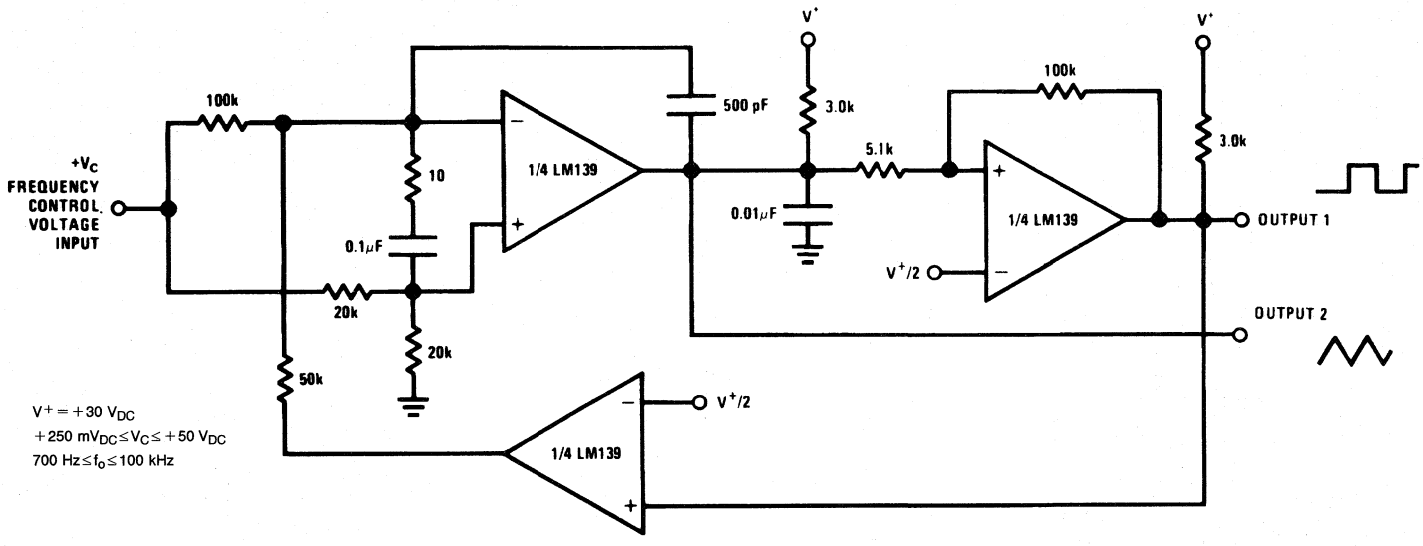
Crystal Controlled Oscillator



TL/H/5706–25

Typical Applications ($V^+ = 15\ V_{DC}$) (Continued)

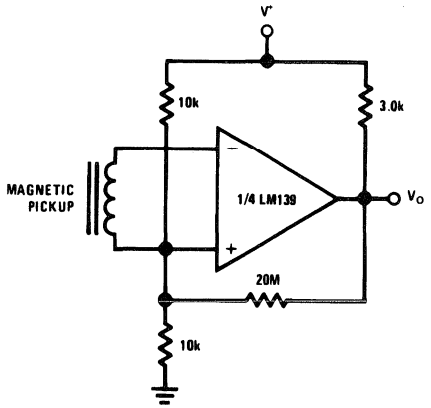
Two-Decade High-Frequency VCO



TL/H/5706–23

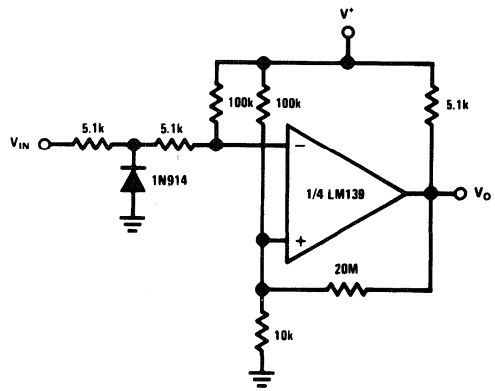
Typical Applications ($V^+ = 5\ V_{DC}$) (Continued)

Transducer Amplifier



TL/H/5706–28

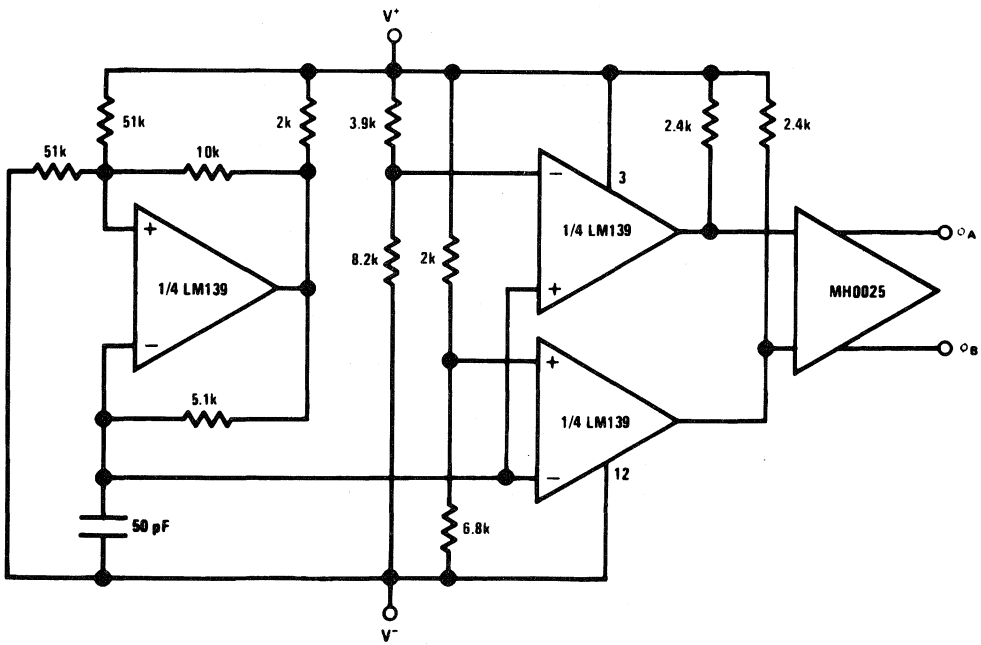
Zero Crossing Detector (Single Power Supply)



TL/H/5706–30

Split-Supply Applications ($V^+ = +15\ V_{DC}$ and $V^- = -15\ V_{DC}$)

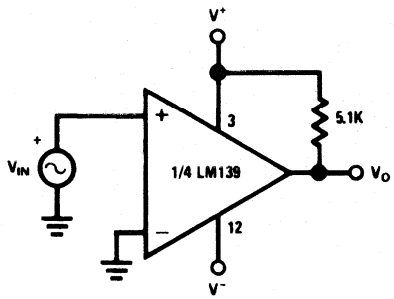
MOS Clock Driver



TL/H/5706–31

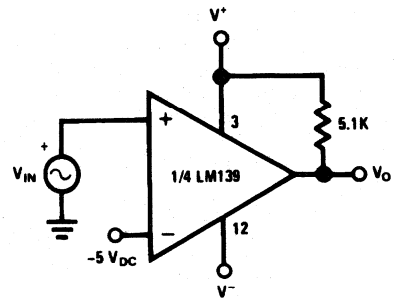
Split-Supply Applications ($V^+ = +15\ V_{DC}$ and $V^- = -15\ V_{DC}$) (Continued)

Zero Crossing Detector



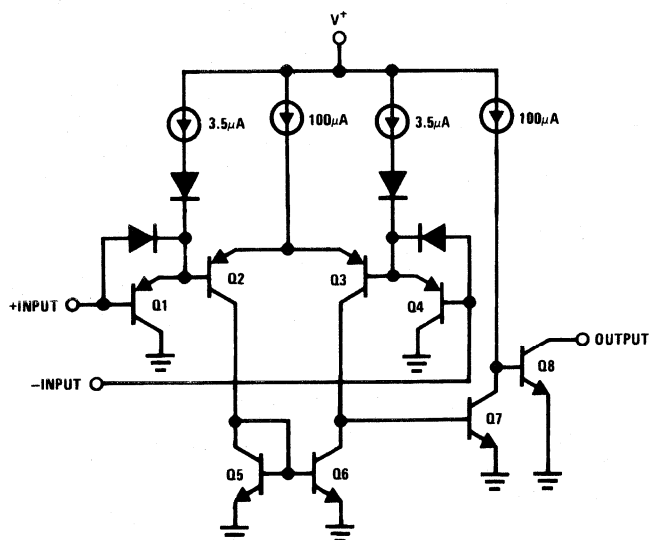
TL/H/5706–32

Comparator With a Negative Reference



TL/H/5706–33

Schematic Diagram



TL/H/5706–1

National Semiconductor

LM160/LM360 High Speed Differential Comparator

General Description

The LM160/LM360 is a very high speed differential input, complementary TTL output voltage comparator with improved characteristics over the μA760/μA760C, for which it is a pin-for-pin replacement. The device has been optimized for greater speed, input impedance and fan-out, and lower input offset voltage. Typically delay varies only 3 ns for overdrive variations of 5 mV to 400 mV.

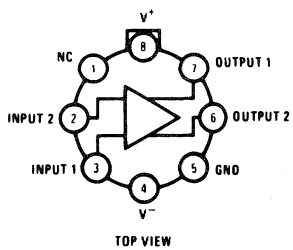
Complementary outputs having minimum skew are provided. Applications involve high speed analog to digital convertors and zero-crossing detectors in disk file systems.

Features

- Guaranteed high speed — 20 ns max
- Tight delay matching on both outputs
- Complementary TTL outputs
- High input impedance
- Low speed variation with overdrive variation
- Fan-out of 4
- Low input offset voltage
- Series 74 TTL compatible

Connection Diagrams

Metal Can Package

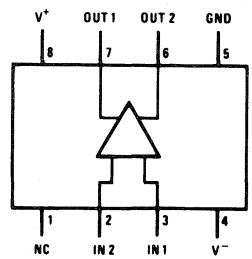


TOP VIEW

TL/H/5707–4

Order Number LM160H, LM160H/883* or LM360H
See NS Package Number H08C

Dual-In-Line Package

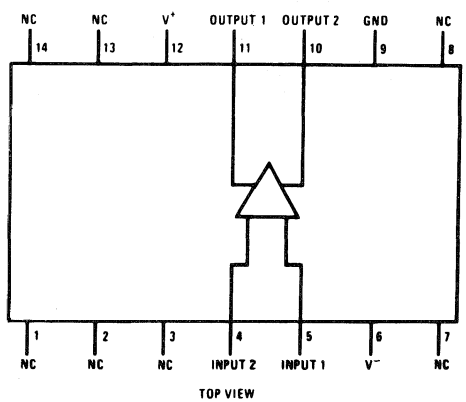


TOP VIEW

TL/H/5707–5

Order Number LM160J, LM160J/883*, LM360J, LM360M or LM360N
See NS Package Number J08A, M08A or N08E

Dual-In-Package



TOP VIEW

TL/H/5707–6

Order Number LM160J-14, LM160J-14/883*, LM360J-14 or LM360N-14
See NS Package Number J14A or N14A

*Also available in SMD# 5962-8767401

Absolute Maximum Ratings (Note 5)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

(Note 7)

Positive Supply Voltage	+8V
Negative Supply Voltage	−8V
Peak Output Current	20 mA
Differential Input Voltage	±5V
Input Voltage	$V^+ \geq V_{IN} \geq V^-$
ESD Tolerance (Note 8)	1600V

Operating Temperature Range	
LM160	−55°C to +125°C
LM360	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec.)	260°C
Soldering Information	
Dual-In-Line Package	
Soldering (10 seconds)	260°C
Small Outline Package	
Vapor Phase (60 seconds)	215°C
Infrared (15 seconds)	220°C

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

Electrical Characteristics ($T_{MIN} \leq T_A \leq T_{MAX}$)

Parameter	Conditions	Min	Typ	Max	Units
Operating Conditions					
Supply Voltage V_{CC}^+		4.5	5	6.5	V
Supply Voltage V_{CC}^-		−4.5	−5	−6.5	V
Input Offset Voltage	$R_S \leq 200\Omega$		2	5	mV
Input Offset Current			0.5	3	μA
Input Bias Current			5	20	μA
Output Resistance (Either Output)	$V_{OUT} = V_{OH}$		100		Ω
Response Time	$T_A = 25°C$, $V_S = \pm 5V$ (Notes 1, 6)		13	25	ns
	$T_A = 25°C$, $V_S = \pm 5V$ (Notes 2, 6)		12	20	ns
	$T_A = 25°C$, $V_S = \pm 5V$ (Notes 3, 6)		14		ns
Response Time Difference between Outputs					
(t_{pd} of $+V_{IN1}$) − (t_{pd} of $-V_{IN2}$)	$T_A = 25°C$ (Notes 1, 6)		2		ns
(t_{pd} of $+V_{IN2}$) − (t_{pd} of $-V_{IN\,1}$)	$T_A = 25°C$ (Notes 1, 6)		2		ns
(t_{pd} of $+V_{IN1}$) − (t_{pd} of $+V_{IN2}$)	$T_A = 25°C$ (Notes 1, 6)		2		ns
(t_{pd} of $-V_{IN1}$) − (t_{pd} of $-V_{IN2}$)	$T_A = 25°C$ (Notes 1, 6)		2		ns
Input Resistance	f = 1 MHz		17		kΩ
Input Capacitance	f = 1 MHz		3		pF
Average Temperature Coefficient of Input Offset Voltage	$R_S = 50\Omega$		8		μV/°C
Average Temperature Coefficient of Input Offset Current			7		nA/°C
Common Mode Input Voltage Range	$V_S = \pm 6.5V$	±4	±4.5		V
Differential Input Voltage Range		±5			V
Output High Voltage (Either Output)	$I_{OUT} = -320\ \mu A$, $V_S = \pm 4.5V$	2.4	3		V
Output Low Voltage (Either Output)	$I_{SINK} = 6.4$ mA		0.25	0.4	V
Positive Supply Current	$V_S = \pm 6.5V$		18	32	mA
Negative Supply Current	$V_S = \pm 6.5V$		−9	−16	mA

Note 1: Response time measured from the 50% point of a 30 mVp-p 10 MHz sinusoidal input to the 50% point of the output.

Note 2: Response time measured from the 50% point of a 2 Vp-p 10 MHz sinusoidal input to the 50% point of the output.

Note 3: Response time measured from the start of a 100 mV input step with 5 mV overdrive to the time when the output crosses the logic threshold.

Note 4: Typical thermal impedances are as follows:

Cavity DIP (J):	θ_{jA}	135°C/W	Header (H)	θ_{jA}	165°C/W	(Still Air)
Molded DIP (N):	θ_{jA}	130°C/W			67°C/W	(400 LF/min Air Flow)
				θ_{jC}	25°C/W	

Note 5: The device may be damaged if used beyond the maximum ratings.

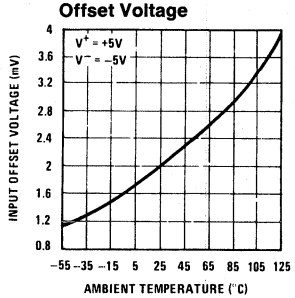
Note 6: Measurements are made in AC Test Circuit, Fanout = 1

Note 7: Refer to RETS 160X for LM160H, LM160J-14 and LM160J military specifications.

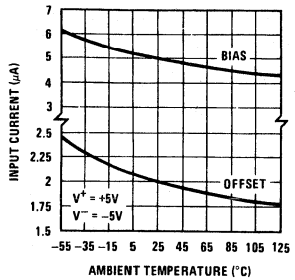
Note 8: Human body model, 1.5 kΩ in series with 100 pF.

Typical Performance Characteristics

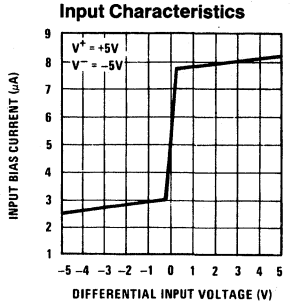
Offset Voltage



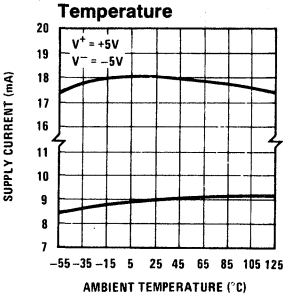
Input Currents vs Ambient Temperature



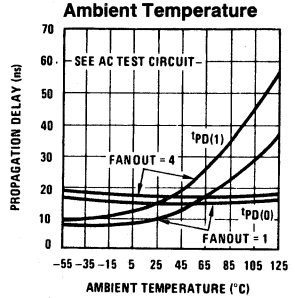
Input Characteristics



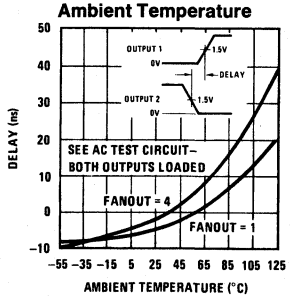
Supply Current vs Ambient Temperature



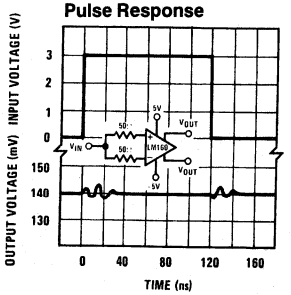
Propagation Delay vs Ambient Temperature



Delay of Output 1 With Respect to Output 2 vs Ambient Temperature

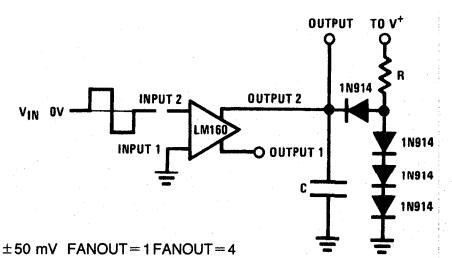


Common-Mode Pulse Response



TL/H/5707–2

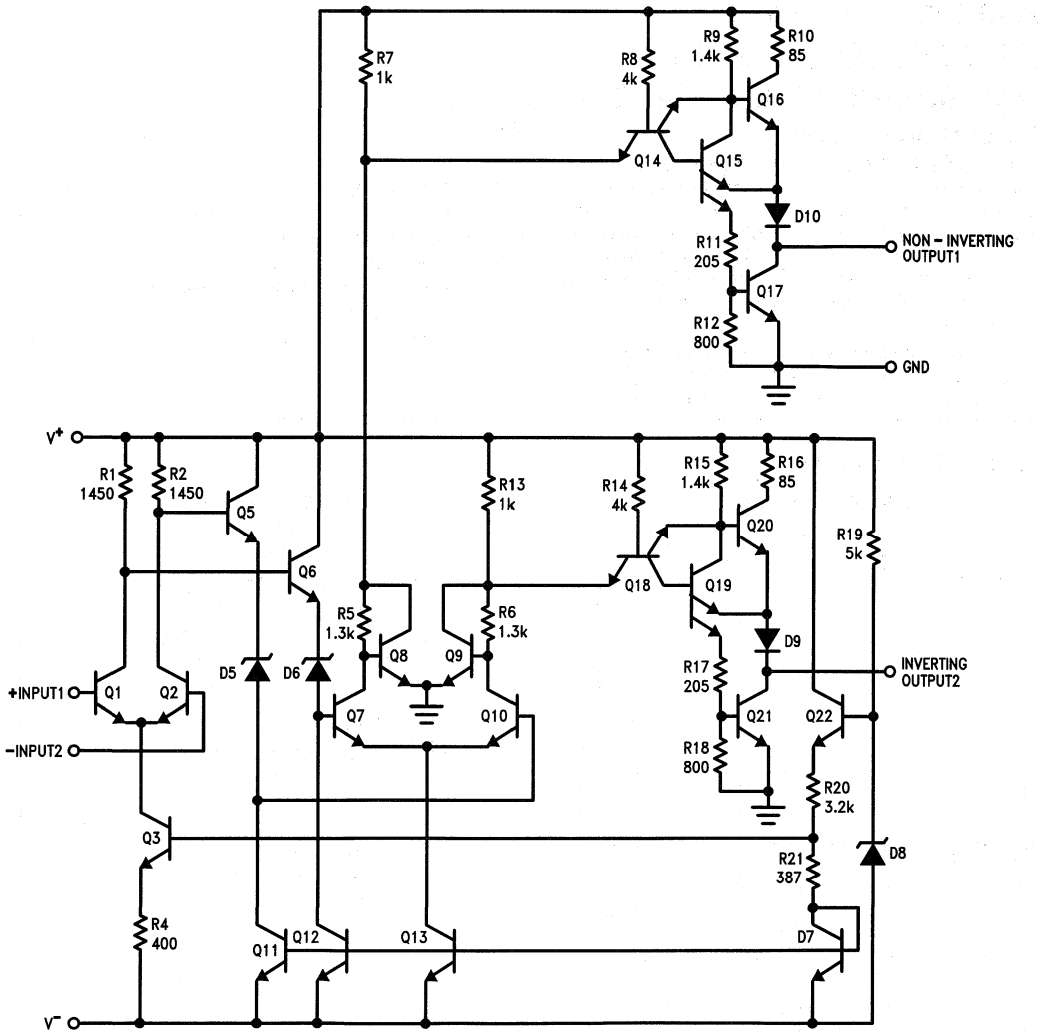
AC Test Circuit



V_{IN} = ±50 mV FANOUT = 1 FANOUT = 4
V^+ = +5V R = 2.4k R = 630Ω
V^- = −5V C = 15 pF C = 30 pF

TL/H/5707–3

Schematic Diagram



TL/H/5707–1

National Semiconductor

LM161/LM261/LM361
High Speed Differential Comparators

General Description

The LM161/LM261/LM361 is a very high speed differential input, complementary TTL output voltage comparator with improved characteristics over the SE529/NE529 for which it is a pin-for-pin replacement. The device has been optimized for greater speed performance and lower input offset voltage. Typically delay varies only 3 ns for over-drive variations of 5 mV to 500 mV. It may be operated from op amp supplies (±15V).

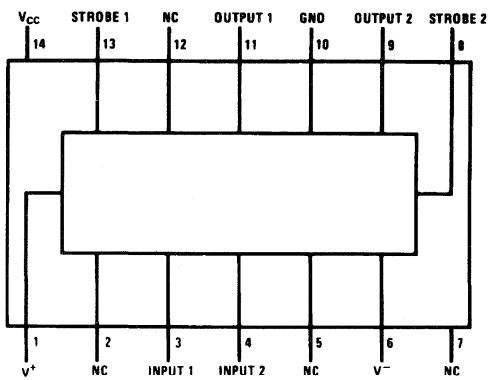
Complementary outputs having maximum skew are provided. Applications involve high speed analog to digital converters and zero-crossing detectors in disk file systems.

Features

- Independent strobes
- Guaranteed high speed — 20 ns max
- Tight delay matching on both outputs
- Complementary TTL outputs
- Operates from op amp supplies — ±15V
- Low speed variation with overdrive variation
- Low input offset voltage
- Versatile supply voltage range

Connection Diagrams

Dual-In-Line Package

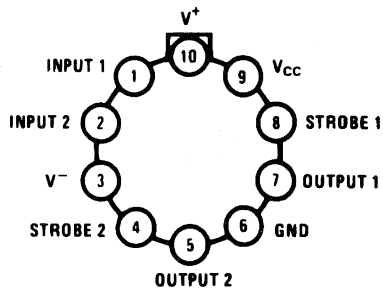


TL/H/5708–2

Top View
Order Number LM161J, LM161J/883*, LM361J, LM361M or LM361N
See NS Package Number J14A, M14A or N14A

*Also available per SMD #5962-8757203

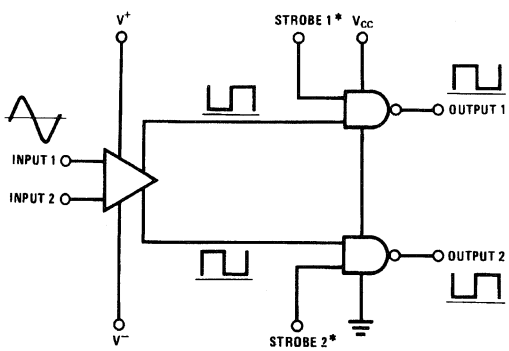
Metal Can Package



TL/H/5708–3

Order Number LM161H, LM161H/883*, LM261H or LM361H
See NS Package Number H10C

Logic Diagram



*Output is low when current is drawn from strobe pin.

TL/H/5708–4

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications. (Note 4)

Positive Supply Voltage, V^+	+16V
Negative Supply Voltage, V^-	−16V
Gate Supply Voltage, V_{CC}	+7V
Output Voltage	+7V
Differential Input Voltage	±5V
Input Common Mode Voltage	±6V
Power Dissipation	600 mW
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	T_{MIN} T_{MAX}
LM161	−55°C to +125°C
LM261	−25°C to +85°C
LM361	0°C to +70°C
Lead Temp. (Soldering, 10 seconds)	260°C
For Any Device Lead Below V^-	0.3V

Operating Conditions

	Min	Typ	Max
Supply Voltage V^+			
LM161/LM261	5V		15V
LM361	5V		15V
Supply Voltage V^-			
LM161/LM261	−6V		−15V
LM361	−6V		−15V
Supply Voltage V_{CC}			
LM161/LM261	4.5V	5V	5.5V
LM361	4.75V	5V	5.25V
ESD Tolerance (Note 5)			1600V
Soldering Information			
Dual-In-Line Package			
Soldering (10 seconds)			260°C
Small Outline Package			
Vapor Phase (60 seconds)			215°C
Infrared (15 seconds)			220°C

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

Electrical Characteristics ($V^+ = +10V$, $V_{CC} = +5V$, $V^- = -10V$, $T_{MIN} \le T_A \le T_{MAX}$, unless noted)

Parameter	Conditions	Limits						Units
		LM161/LM261			LM361			
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage			1	3		1	5	mV
Input Bias Current	$T_A = 25°C$		5	20		10	30	μA μA
Input Offset Current	$T_A = 25°C$		2	3		2	5	μA μA
Voltage Gain	$T_A = 25°C$		3			3		V/mV
Input Resistance	$T_A = 25°C$, f = 1 kHz		20			20		kΩ
Logical "1" Output Voltage	$V_{CC} = 4.75V$, $I_{SOURCE} = -0.5$ mA	2.4	3.3		2.4	3.3		V
Logical "0" Output Voltage	$V_{CC} = 4.75V$, $I_{SINK} = 6.4$ mA			0.4			0.4	V
Strobe Input "1" Current (Output Enabled)	$V_{CC} = 5.25V$, $V_{STROBE} = 2.4V$			200			200	μA
Strobe Input "0" Current (Output Disabled)	$V_{CC} = 5.25V$, $V_{STROBE} = 0.4V$			−1.6			−1.6	mA
Strobe Input "0" Voltage	$V_{CC} = 4.75V$			0.8			0.8	V
Strobe Input "1" Voltage	$V_{CC} = 4.75V$	2			2			V
Output Short Circuit Current	$V_{CC} = 5.25V$, $V_{OUT} = 0V$	−18		−55	−18		−55	mA

Electrical Characteristics (Continued)

($V^+ = +10V$, $V_{CC} = +5V$, $V^- = -10V$, $T_{MIN} \le T_A \le T_{MAX}$, unless noted)

Parameter	Conditions	Limits						Units
		LM161/LM261			LM361			
		Min	Typ	Max	Min	Typ	Max	
Supply Current I^+	$V^+ = 10V$, $V^- = -10V$, $V_{CC} = 5.25V$, $-55°C \le T_A \le 125°C$			4.5				mA
Supply Current I^+	$V^+ = 10V$, $V^- = -10V$, $V_{CC} = 5.25V$, $0°C \le T_A \le 70°C$						5	mA
Supply Current I^-	$V^+ = 10V$, $V^- = -10V$, $V_{CC} = 5.25V$, $-55°C \le T_A \le 125°C$			10				mA
Supply Current I^-	$V^+ = 10V$, $V^- = -10V$, $V_{CC} = 5.25V$, $0°C \le T_A \le 70°C$						10	mA
Supply Current I_{CC}	$V^+ = 10V$, $V^- = -10V$, $V_{CC} = 5.25V$, $-55°C \le T_A \le 125°C$			18				mA
Supply Current I_{CC}	$V^+ = 10V$, $V^- = -10V$, $V_{CC} = 5.25V$, $0°C \le T_A \le 70°C$						20	mA
Transient Response	V_{IN} = 50 mV overdrive (Note 3)							
Propagation Delay Time ($t_{pd(0)}$)	$T_A = 25°C$		14	20		14	20	ns
Propagation Delay Time ($t_{pd(1)}$)	$T_A = 25°C$		14	20		14	20	ns
Delay Between Output A and B	$T_A = 25°C$		2	5		2	5	ns
Strobe Delay Time ($t_{pd(0)}$)	$T_A = 25°C$		8			8		ns
Strobe Delay Time ($t_{pd(1)}$)	$T_A = 25°C$		8			8		ns

Note 1: The device may be damaged by use beyond the maximum ratings.

Note 2: Typical thermal impedances are as follows:

	H Package	J Package	N Package
θ_{jA}	165°C/W (Still Air) 67°C/W (400 LF/Min Air Flow)	112°C/W	105°C/W
θ_{jC}	25°C/W		

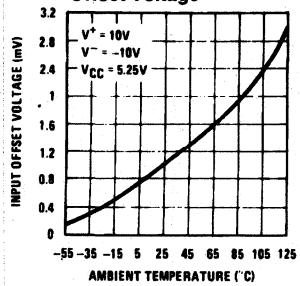
Note 3: Measurements using AC Test circuit, Fanout = 1. The devices are faster at low supply voltages.

Note 4: Refer to RETS161X for LM161H and LM161J military specifications.

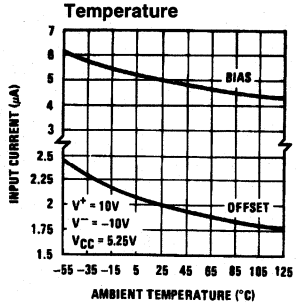
Note 5: Human body model, 1.5 kΩ in series with 100 pF.

Typical Performance Characteristics

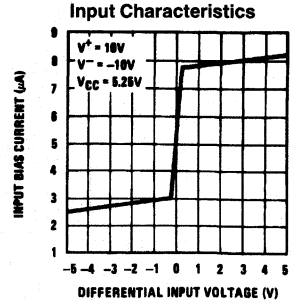
Offset Voltage



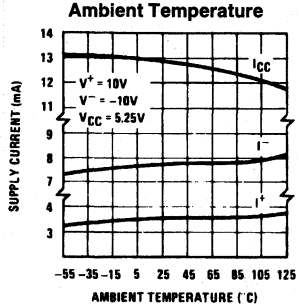
Input Currents vs Ambient Temperature



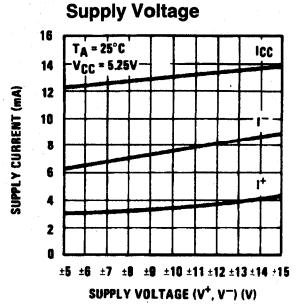
Input Characteristics



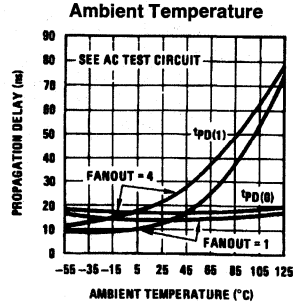
Supply Current vs Ambient Temperature



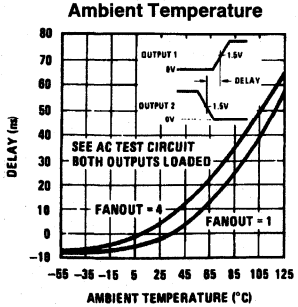
Supply Current vs Supply Voltage



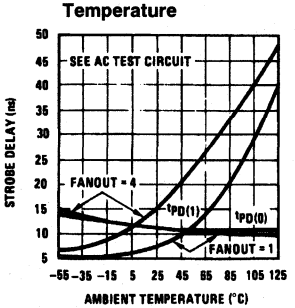
Propagation Delay vs Ambient Temperature



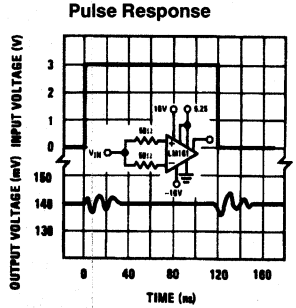
Delay of Output 1 With Respect to Output 2 vs Ambient Temperature



Strobe Delay vs Ambient Temperature

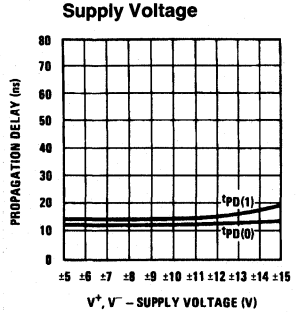


Common-Mode Pulse Response



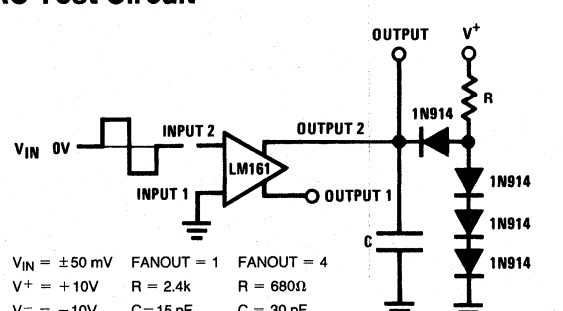
TL/H/5708–5

Propagation Delay vs Supply Voltage



TL/H/5708–7

AC Test Circuit

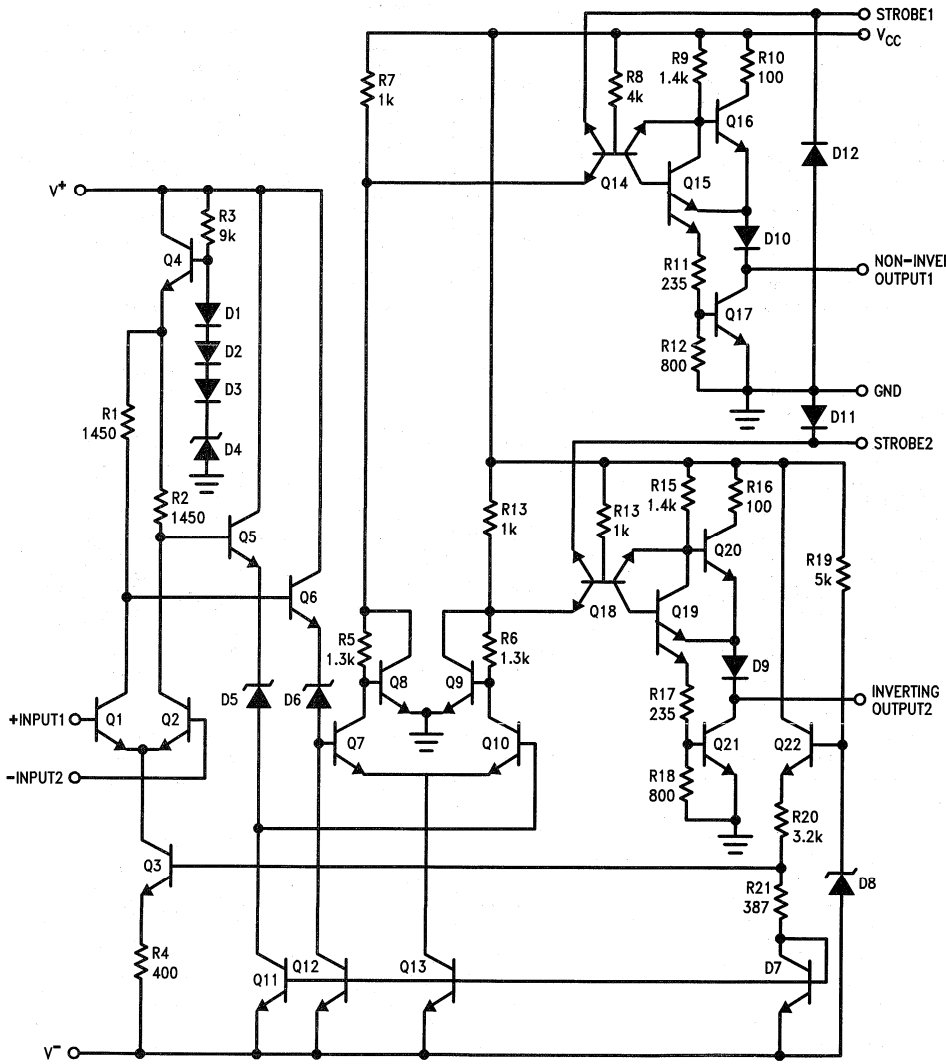


V_{IN} = ±50 mV	FANOUT = 1	FANOUT = 4
V+ = +10V	R = 2.4k	R = 680Ω
V− = −10V	C = 15 pF	C = 30 pF
V_{CC} = 5.25V		

TL/H/5708–6

Schematic Diagram

LM161



TL/H/5708–1

R10, R16: 85
R11, R17: 205

National Semiconductor

LM193/LM293/LM393, LM2903
Low Power Low Offset Voltage Dual Comparators

General Description

The LM193 series consists of two independent precision voltage comparators with an offset voltage specification as low as 2.0 mV max for two comparators which were designed specifically to operate from a single power supply over a wide range of voltages. Operation from split power supplies is also possible and the low power supply current drain is independent of the magnitude of the power supply voltage. These comparators also have a unique characteristic in that the input common-mode voltage range includes ground, even though operated from a single power supply voltage.

Application areas include limit comparators, simple analog to digital converters; pulse, squarewave and time delay generators; wide range VCO; MOS clock timers; multivibrators and high voltage digital logic gates. The LM193 series was designed to directly interface with TTL and CMOS. When operated from both plus and minus power supplies, the LM193 series will directly interface with MOS logic where their low power drain is a distinct advantage over standard comparators.

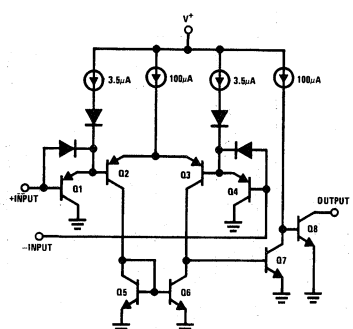
Advantages

- High precision comparators
- Reduced V_{OS} drift over temperature
- Eliminates need for dual supplies
- Allows sensing near ground
- Compatible with all forms of logic
- Power drain suitable for battery operation

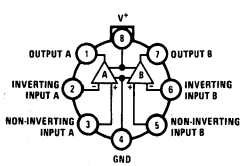
Features

- Wide supply
  - Voltage range: 2.0 V_{DC} to 36 V_{DC}
  - single or dual supplies: ±1.0 V_{DC} to ±18 V_{DC}
- Very low supply current drain (0.4 mA) — independent of supply voltage
- Low input biasing current: 25 nA
- Low input offset current: ±5 nA
  and maximum offset voltage: ±3 mV
- Input common-mode voltage range includes ground
- Differential input voltage range equal to the power supply voltage
- Low output saturation voltage, 250 mV at 4 mA
- Output voltage compatible with TTL, DTL, ECL, MOS and CMOS logic systems

Schematic and Connection Diagrams

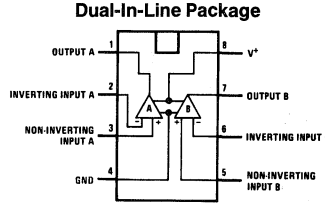


Metal Can Package



Order Number LM193H, LH193H/883*, LM193AH, LM193AH/883, LM293H, LM293AH, LM393H or LM393AH
See NS Package Number H08C

Dual-In-Line Package



TL/H/5709–1

Order Number LM193J/883*, LM193AJ/883, LM393J, LM393AJ, LM393M, LM2903M, LM393N, LM2903J or LM2903N
See NS Package Number J08A, M08A or N08E

*Also available per JM38510/11202

3

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.
(Note 10)

Supply Voltage, V^+	36 V_{DC} or ±18 V_{DC}
Differential Input Voltage (Note 8)	36 V_{DC}
Input Voltage	−0.3 V_{DC} to +36 V_{DC}
Input Current ($V_{IN} < -0.3\ V_{DC}$) (Note 3)	50 mA
Power Dissipation (Note 1)	
Molded DIP	780 mW
Metal Can	660 mW
Small Outline Package	510 mW
Output Short-Circuit to Ground (Note 2)	Continuous

Operating Temperature Range	
LM393/LM393A	0°C to +70°C
LM293/LM293A	−25°C to +85°C
LM193/LM193A	−55°C to +125°C
LM2903	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	+260°C
Soldering Information	
Dual-In-Line Package	
Soldering (10 seconds)	260°C
Small Outline Package	
Vapor Phase (60 seconds)	215°C
Infrared (15 seconds)	220°C

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

ESD rating (1.5 kΩ in series with 100 pF) 1300V

Electrical Characteristics ($V^+ = 5\ V_{DC}$, T_A = 25°C, unless otherwise stated)

Parameter	Conditions	LM193A			LM293A, LM393A			LM193			LM293, LM393			LM2903			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	(Note 9)		±1.0	±2.0		±1.0	±2.0		±1.0	±5.0		±1.0	±5.0		±2.0	±7.0	mV_{DC}
Input Bias Current	$I_{IN}(+)$ or $I_{IN}(-)$ with Output In Linear Range, V_{CM} = 0V (Note 5)		25	100		25	250		25	100		25	250		25	250	nA_{DC}
Input Offset Current	$I_{IN}(+) - I_{IN}(-)$ V_{CM} = 0V		±3.0	±25		±5.0	±50		±3.0	±25		±5.0	±50		±5.0	±50	nA_{DC}
Input Common Mode Voltage Range	V^+ = 30 V_{DC} (Note 6)	0		$V^+ - 1.5$	0		$V^+ - 1.5$	0		$V^+ - 1.5$	0		$V^+ - 1.5$	0		$V^+ - 1.5$	V_{DC}
Supply Current	$R_L = \infty$ on All Comparators, $R_L = \infty$ on All Amps, $V^+ = 36\ V_{DC}$		0.4 1	1 2.5		0.4 1	1 2.5		0.4 1	1 2.5		0.4 1	1 2.5		0.4 1	1.0 2.5	mA_{DC} mA_{DC}
Voltage Gain	$R_L \geq 15\ k\Omega$, $V^+ = 15\ V_{DC}$ V_O = 1 V_{DC} to 11 V_{DC}	50	200		50	200		50	200		50	200		25	100		V/mV
Large Signal Response Time	V_{IN} = TTL Logic Swing, $V_{REF} = 1.4\ V_{DC}$ $V_{RL} = 5\ V_{DC}$, $R_L = 5.1\ k\Omega$		300			300			300			300			300		ns
Response Time	$V_{RL} = 5\ V_{DC}$, $R_L = 5.1\ k\Omega$ (Note 7)		1.3			1.3			1.3			1.3			1.5		μs
Output Sink Current	$V_{IN}(-) = 1\ V_{DC}$, $V_{IN}(+) = 0$, $V_O \leq 1.5\ V_{DC}$	6.0	16		6.0	16		6.0	16		6.0	16		6.0	16		mA_{DC}
Saturation Voltage	$V_{IN}(-) = 1\ V_{DC}$, $V_{IN}(+) = 0$, $I_{SINK} \leq 4\ mA$		250	400		250	400		250	400		250	400		250	400	mV_{DC}
Output Leakage Current	$V_{IN}(-) = 0$, $V_{IN}(+) = 1\ V_{DC}$, $V_O = 5\ V_{DC}$		0.1			0.1			0.1			0.1			0.1		nA_{DC}

Electrical Characteristics ($V^+ = 5\ V_{DC}$) (Note 4)

Parameter	Conditions	LM193A			LM293A, LM393A			LM193			LM293, LM393			LM2903			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	(Note 9)			±4.0			±4.0			±9			±9		±9	±15	mV_{DC}
Input Offset Current	$I_{IN(+)} - I_{IN(-)}$, $V_{CM} = 0V$			±100			±150			±100			±150		±50	±200	nA_{DC}
Input Bias Current	$I_{IN(+)}$ or $I_{IN(-)}$ with Output in Linear Range, $V_{CM} = 0V$ (Note 5)			300			400			300			400		200	500	nA_{DC}
Input Common Mode Voltage Range	$V^+ = 30\ V_{DC}$ (Note 6)	0		$V^+ - 2.0$	0		$V^+ - 2.0$	0		$V^+ - 2.0$	0		$V^+ - 2.0$	0		$V^+ - 2.0$	V_{DC}
Saturation Voltage	$V_{IN(-)} = 1\ V_{DC}$, $V_{IN(+)} = 0$, $I_{SINK} \leq 4$ mA,			700			700			700			700		400	700	mV_{DC}
Output Leakage Current	$V_{IN(-)} = 0$, $V_{IN(+)} = 1\ V_{DC}$, $V_O = 30\ V_{DC}$			1.0			1.0			1.0			1.0			1.0	μA_{DC}
Differential Input Voltage	Keep All V_{IN}'s $\geq 0\ V_{DC}$ (or V^-, if Used), (Note 8)			36			36			36			36			36	V_{DC}

Note 1: For operating at high temperatures, the LM393/LM393A and LM2903 must be derated based on a 125°C maximum junction temperature and a thermal resistance of 170°C/W which applies for the device soldered in a printed circuit board, operating in a still air ambient. The LM193/LM193A/LM293/LM293A must be derated based on a 150°C maximum junction temperature. The low bias dissipation and the "ON-OFF" characteristic of the outputs keeps the chip dissipation very small ($P_D \leq 100$ mW), provided the output transistors are allowed to saturate.

Note 2: Short circuits from the output to V^+ can cause excessive heating and eventual destruction. When considering short circuits to ground, the maximum output current is approximately 20 mA independent of the magnitude of V^+.

Note 3: This input current will only exist when the voltage at any of the input leads is driven negative. It is due to the collector-base junction of the input PNP transistors becoming forward biased and thereby acting as input diode clamps. In addition to this diode action, there is also lateral NPN parasitic transistor action on the IC chip. This transistor action can cause the output voltages of the comparators to go to the V^+ voltage level (or to ground for a large overdrive) for the time duration that an input is driven negative. This is not destructive and normal output states will re-establish when the input voltage, which was negative, again returns to a value greater than $-0.3\ V_{DC}$.

Note 4: These specifications are limited to $-55°C \leq T_A \leq +125°C$, for the LM193/LM193A, With the LM293/LM293A all temperature specifications are limited to $-25°C \leq T_A \leq +85°C$ and the LM393/LM393A temperature specifications are limited to $0°C \leq T_A \leq +70°C$. The LM2903 is limited to $-40°C \leq T_A \leq +85°C$.

Note 5: The direction of the input current is out of the IC due to the PNP input stage. This current is essentially constant, independent of the state of the output so no loading change exists on the reference or input lines.

Note 6: The input common-mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3V. The upper end of the common-mode voltage range is $V^+ - 1.5V$ at 25°C, but either or both inputs can go to $36\ V_{DC}$ without damage, independent of the magnitude of V^+.

Note 7: The response time specified is for a 100 mV input step with 5 mV overdrive. For larger overdrive signals 300 ns can be obtained, see typical performance characteristics section.

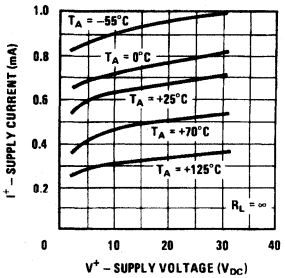
Note 8: Positive excursions of input voltage may exceed the power supply level. As long as the other voltage remains within the common-mode range, the comparator will provide a proper output state. The low input voltage state must not be less than $-0.3\ V_{DC}$ (or $0.3\ V_{DC}$ below the magnitude of the negative power supply, if used).

Note 9: At output switch point, $V_O \cong 1.4\ V_{DC}$, $R_S = 0\Omega$ with V^+ from $5\ V_{DC}$ to $30\ V_{DC}$; and over the full input common-mode range ($0\ V_{DC}$ to $V^+ - 1.5\ V_{DC}$), at 25°C.

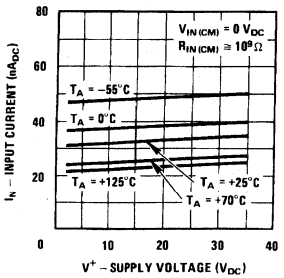
Note 10: Refer to RETS193AX for LM193AH military specifications and to RETS193X for LM193H military specifications.

Typical Performance Characteristics LM193/LM293/LM393, LM193A/LM293A/LM393A

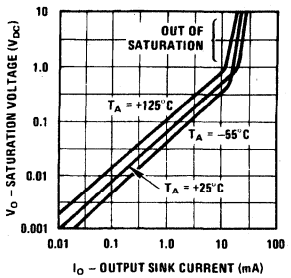
Supply Current



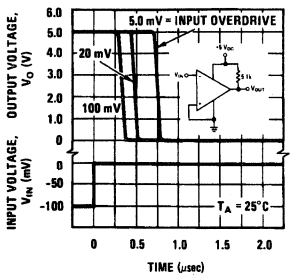
Input Current



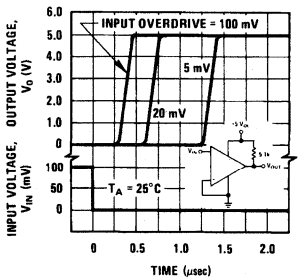
Output Saturation Voltage



Response Time for Various Input Overdrives—Negative Transition



Response Time for Various Input Overdrives—Positive Transition



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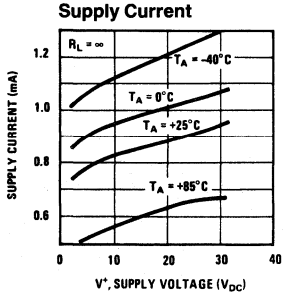
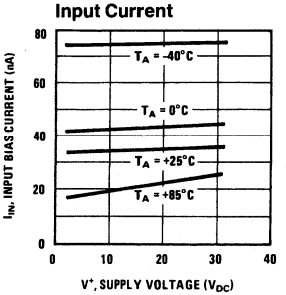
Typical Performance Characteristics LM2903

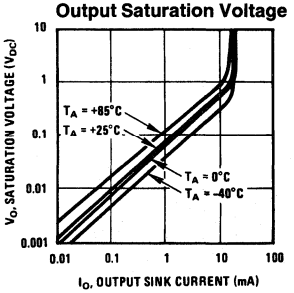
Supply Current



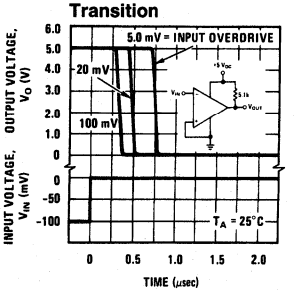
Input Current



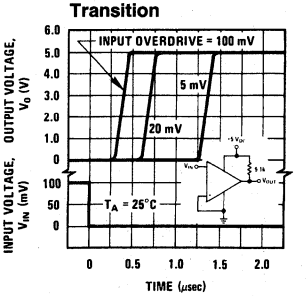
Output Saturation Voltage



Response Time for Various Input Overdrives—Negative Transition



Response Time for Various Input Overdrives—Positive Transition



TL/H/5709–4

Application Hints

The LM193 series are high gain, wide bandwidth devices which, like most comparators, can easily oscillate if the output lead is inadvertently allowed to capacitively couple to the inputs via stray capacitance. This shows up only during the output voltage transition intervals as the comparator change states. Power supply bypassing is not required to solve this problem. Standard PC board layout is helpful as it reduces stray input-output coupling. Reducing the input resistors to $< 10\ k\Omega$ reduces the feedback signal levels and finally, adding even a small amount (1.0 to 10 mV) of positive feedback (hysteresis) causes such a rapid transition that oscillations due to stray feedback are not possible. Simply socketing the IC and attaching resistors to the pins will cause input-output oscillations during the small transition intervals unless hysteresis is used. If the input signal is a pulse waveform, with relatively fast rise and fall times, hysteresis is not required.

All pins of any unused comparators should be grounded.

The bias network of the LM193 series establishes a drain current which is independent of the magnitude of the power supply voltage over the range of from 2.0 V_{DC} to 30 V_{DC}.

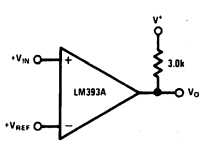
It is usually unnecessary to use a bypass capacitor across the power supply line.

The differential input voltage may be larger than V^+ without damaging the device (see Note 8). Protection should be provided to prevent the input voltages from going negative more than $-0.3\ V_{DC}$ (at 25°C). An input clamp diode can be used as shown in the applications section.

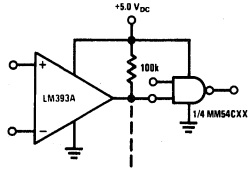
The output of the LM193 series is the uncommitted collector of a grounded-emitter NPN output transistor. Many collectors can be tied together to provide an output OR'ing function. An output pull-up resistor can be connected to any available power supply voltage within the permitted supply voltage range and there is no restriction on this voltage due to the magnitude of the voltage which is applied to the V^+ terminal of the LM193 package. The output can also be used as a simple SPST switch to ground (when a pull-up resistor is not used). The amount of current which the output device can sink is limited by the drive available (which is independent of V^+) and the β of this device. When the maximum current limit is reached (approximately 16 mA), the output transistor will come out of saturation and the output voltage will rise very rapidly. The output saturation voltage is limited by the approximately 60Ω r_{SAT} of the output transistor. The low offset voltage of the output transistor (1.0 mV) allows the output to clamp essentially to ground level for small load currents.

Typical Applications ($V^+ = 5.0\ V_{DC}$)

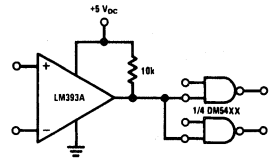
Basic Comparator



Driving CMOS



Driving TTL



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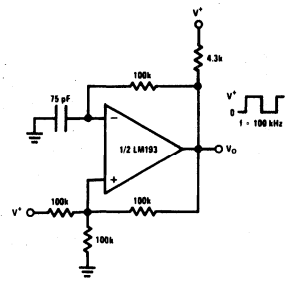
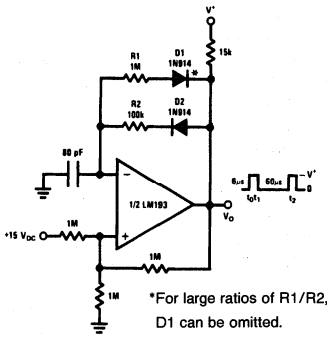
Typical Applications (Continued)

Squarewave Oscillator

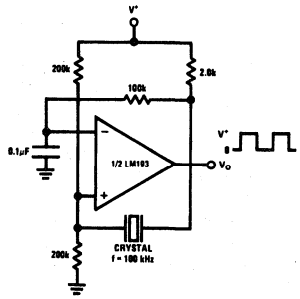


Pulse Generator

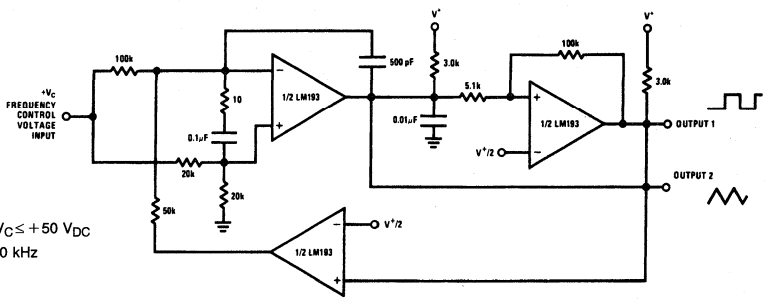


*For large ratios of R1/R2, D1 can be omitted.

Crystal Controlled Oscillator



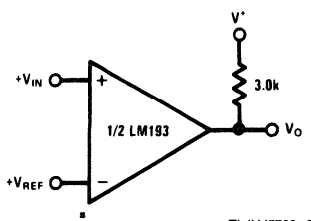
Two-Decade High-Frequency VCO



V* = +30 V_{DC}
+250 $mV_{DC} \leq V_C \leq$ +50 V_{DC}
700 Hz $\leq f_o \leq$ 100 kHz

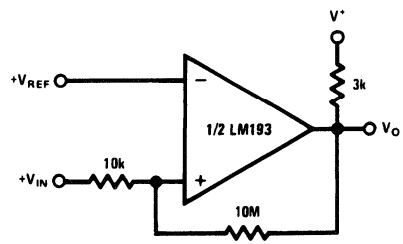
TL/H/5709–5

Basic Comparator



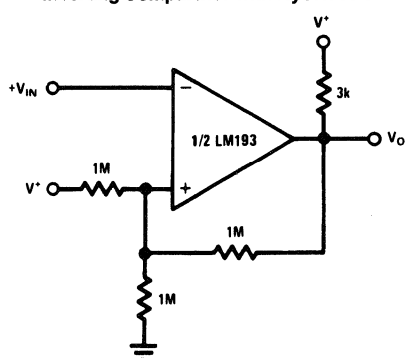
TL/H/5709–6

Non-Inverting Comparator with Hysteresis



TL/H/5709–9

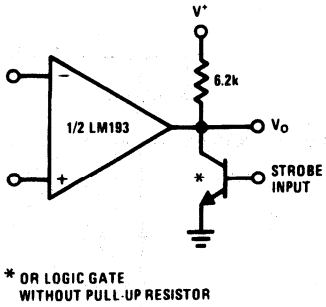
Inverting Comparator with Hysteresis



TL/H/5709–10

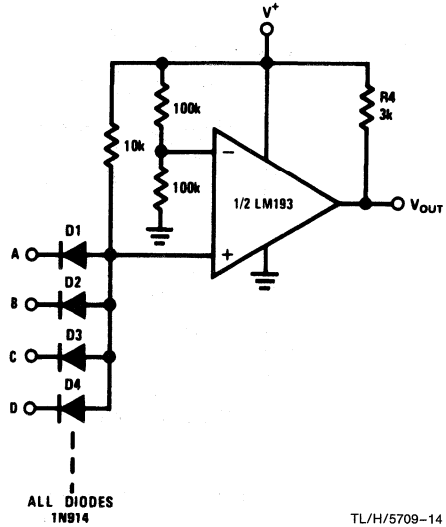
Typical Applications (Continued)

Output Strobing



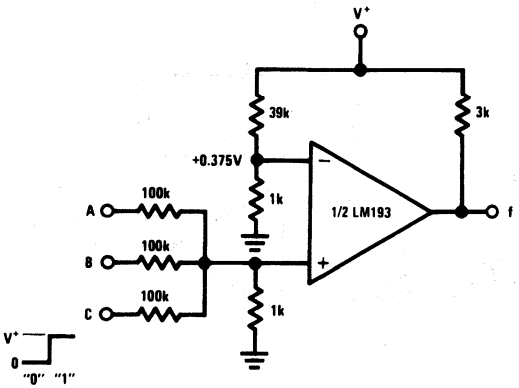
TL/H/5709–11

Large Fan-in AND Gate



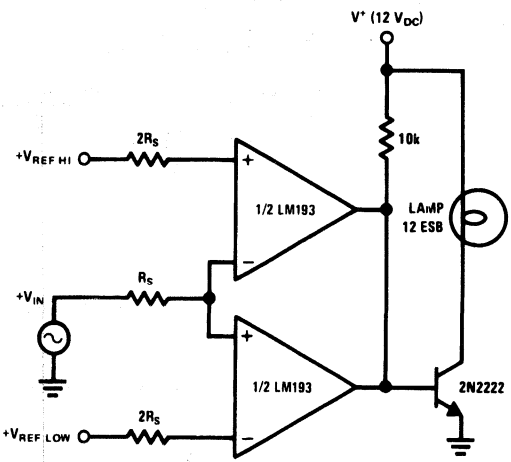
TL/H/5709–14

AND Gate



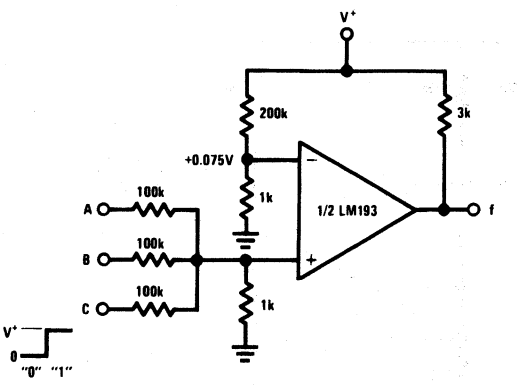
TL/H/5709–12

Limit Comparator



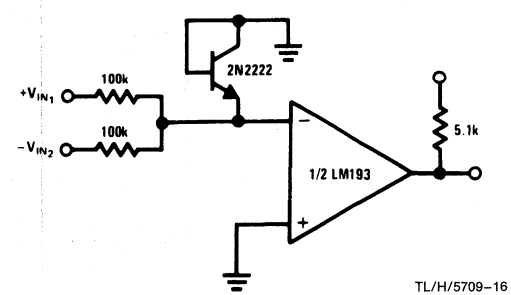
TL/H/5709–15

OR Gate



TL/H/5709–13

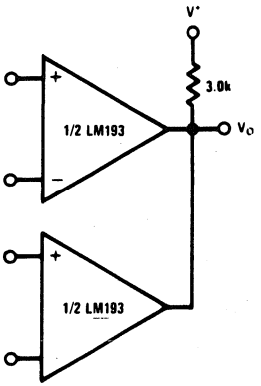
Comparing Input Voltages of Opposite Polarity



TL/H/5709–16

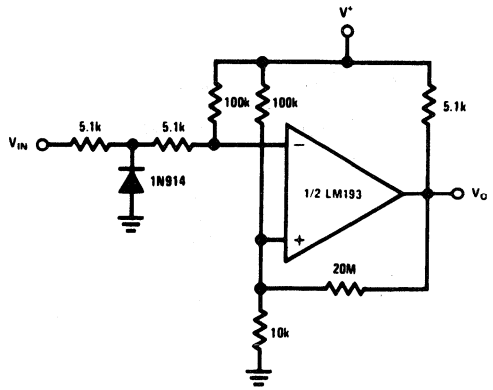
Typical Applications (Continued)

ORing the Outputs



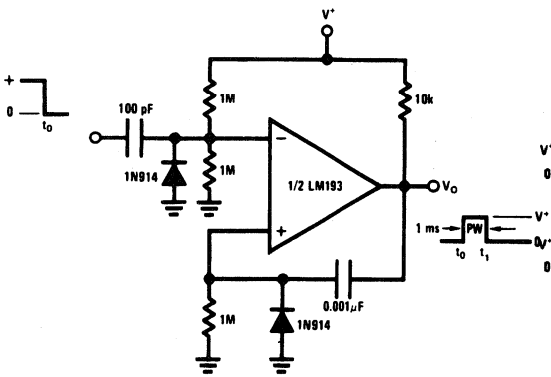
TL/H/5709–17

Zero Crossing Detector (Single Power Supply)



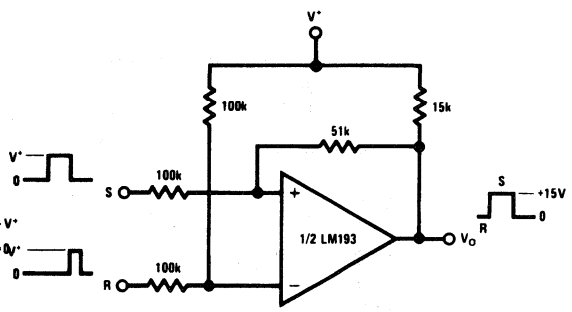
TL/H/5709–21

One-Shot Multivibrator



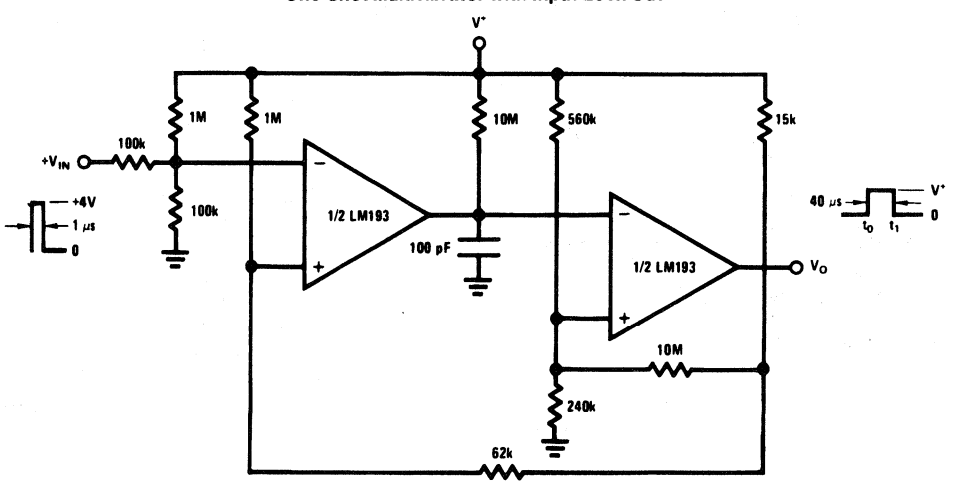
TL/H/5709–22

Bi-Stable Multivibrator



TL/H/5709–24

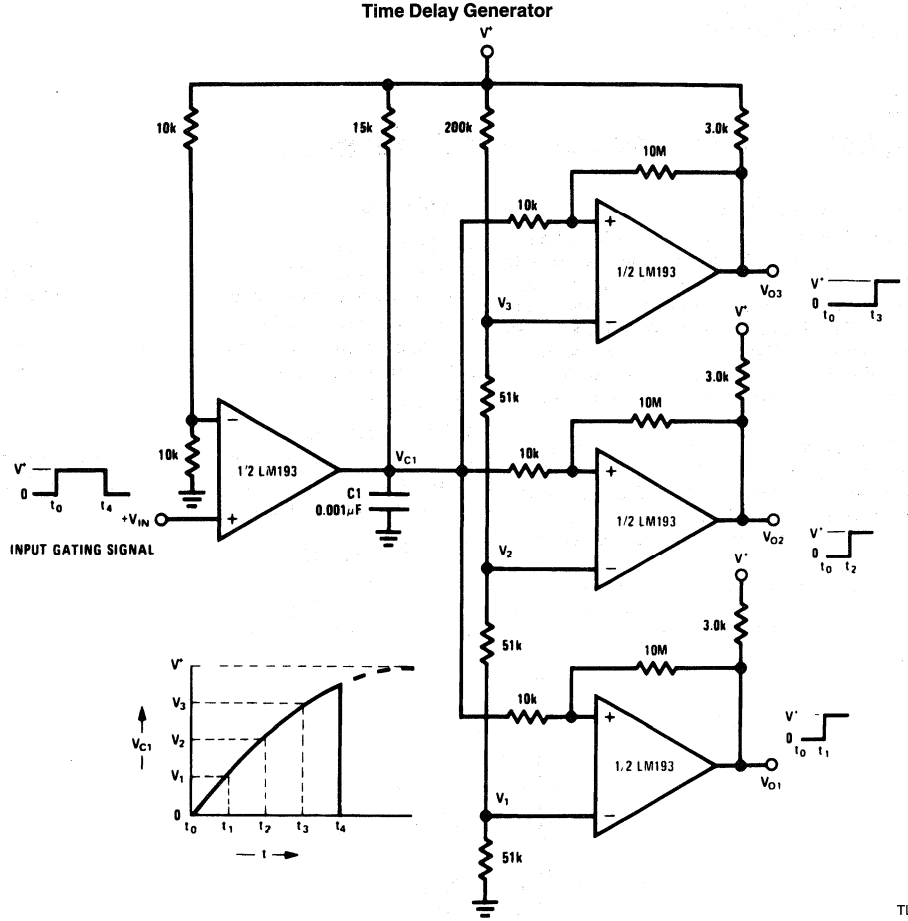
One-Shot Multivibrator with Input Lock Out



TL/H/5709–23

Typical Applications (Continued) ($V^+ = V_{DC}$)

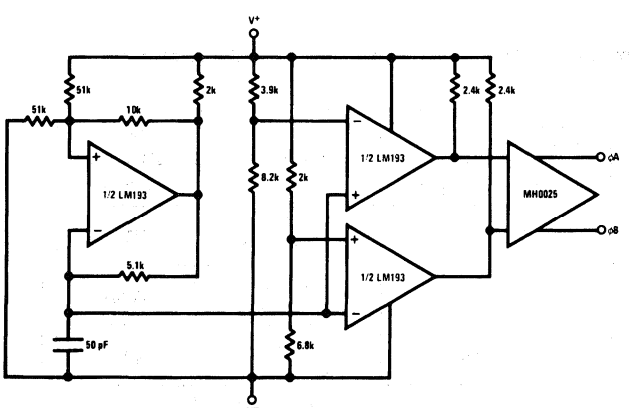
Time Delay Generator



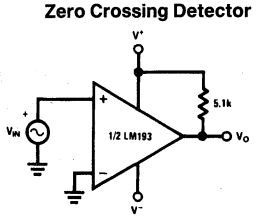
TL/H/5709–7

Split-Supply Applications ($V^+ = +15\ V_{DC}$ and $V^- = -15\ V_{DC}$)

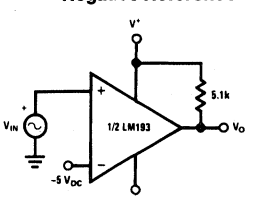
MOS Clock Driver



Zero Crossing Detector



Comparator With a Negative Reference



TL/H/5709–8

National Semiconductor

LM612
Dual-Channel Comparator and Reference

General Description

The dual-channel comparator consists of two individual comparators, having an input voltage range that extends down to the negative supply voltage V^-. The common open-collector output can be driven low by either half of the LM612. This configuration makes the LM612 ideal for use as a window comparator. The input stages of the comparator have lateral PNP input transistors which maintain low input currents for large differential input voltages and swings above V^+.

The 1.2V voltage reference, referred to the V^- terminal, is a two-terminal shunt-type band-gap similar to the LM185-1.2 series, with voltage accuracy of ±0.6% available. The reference features operation over a shunt current range of 17 μA to 20 mA, low dynamic impedance, and broad capacitive load range.

As a member of National's Super-Block™ family, the LM612 is a space-saving monolithic alternative to a multichip solution, offering a high level of integration without sacrificing performance.

Features

COMPARATORS

- Low operating current — 300 μA
- Wide supply voltage range — 4V to 36V
- Open-collector outputs
- Input common-mode range — V^- to (V^+ − 1.8V)
- Wide differential input voltage — ±36V

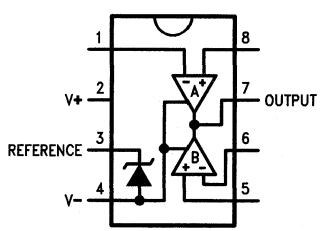
REFERENCE

- Fixed output voltage — 1.24V
- Tight initial tolerance available — ±0.6% (25°C)
- Wide operating current range — 17 μA to 20 mA
- Tolerant of load capacitance

Applications

- Voltage window comparator
- Power supply voltage monitor
- Dual-channel fault monitor

Connection Diagram



TL/H/11058–1

Top View

Ordering Information

For information about surface-mount packaging of this device, please contact the Analog Product Marketing group at National Semiconductor Corporation headquarters.

Reference Tolerances	Temperature Range		Package	NSC Package Number
	Military $-55°C \le T_J \le +125°C$	Industrial $-40°C \le T_J + 85°C$		
±0.6% at 25°C, 80 ppm/°C Max	LM612AMN	LM612AIN	8-Pin Molded DIP	N08E
	LM612AMJ/883 (Note 13)		8-Pin Ceramic DIP	J08A
±2.0% at 25°C, 150 ppm/°C Max	LM612MN	LM612IN	8-Pin Molded DIP	N08E
		LM612IM	8-Pin Narrow Surface Mount	M08A

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Voltage on Any Pin Except V_R (referred to V^- pin)
(Note 2) 36V (Max)
(Note 3) −0.3V (Min)
Current through Any Input Pin and V_R Pin ±20 mA
Differential Input Voltage ±36V
Output Short-Circuit Duration (Note 4)
Storage Temperature Range $-65°C \le T_J \le +150°C$
Maximum Junction Temperature 150°C

Thermal Resistance, Junction-to-Ambient (Note 5)
N Package 100°C/W
Soldering Information
N Package
Soldering (10 seconds) 260°C
ESD Tolerance (Note 6) ±1 kV

Operating Temperature Range

LM612AI, LM612I $-40°C \le T_J \le +85°C$
LM612AM, LM612M $-55°C \le T_J \le +125°C$

Electrical Characteristics

These specifications apply for $V^- = GND = 0V$, $V^+ = 5V$, $V_{CM} = V_{OUT} = V^+/2$, $I_R = 100\ \mu A$, unless otherwise specified. Limits in standard typeface are for $T_J = 25°C$; limits in **boldface type** apply over the **Operating Temperature Range.**

Symbol	Parameter	Conditions	Typical (Note 7)	LM612AM LM612AI Limits (Note 8)	LM612M LM612I Limits (Note 8)	Units
COMPARATORS						
I_S	Total Supply Current	V^+ Current, $R_{LOAD} = \infty$, $3V \le V^+ \le 36V$	150 **170**	250 **300**	250 **300**	μA Max μA Max
V_{OS}	Offset Voltage over V^+ Range	$4V \le V^+ \le 36V$, $R_L = 15\ k\Omega$	1.0 **2.0**	3.0 **6.0**	5.0 **7.0**	mV Max mV Max
V_{OS}	Offset Voltage over V_{CM} Range	$0V \le V_{CM} \le (V^+ - 1.8V)$ $V^+ = 30V$, $R_L = 15\ k\Omega$	1.0 **1.5**	3.0 **6.0**	5.0 **7.0**	mV Max mV Max
$\frac{\Delta V_{OS}}{\Delta T}$	Average Offset Voltage Drift		**15**			μV/°C
I_B	Input Bias Current		5 **8**	25 **30**	35 **40**	nA Max nA Max
I_{OS}	Input Offset Current		0.2 **0.3**	4 **5**	4 **5**	nA Max nA Max
A_V	Voltage Gain	$R_L = 10\ k\Omega$ to 36V, $2V \le V_{OUT} \le 27V$	500 **100**	50	50	V/mV Min V/mV
t_R	Large Signal Response Time	$V_{+IN} = 1.4V$, V_{-IN} = TTL Swing, $R_L = 5.1\ k\Omega$	1.5 **2.0**			μs μs
I_{SINK}	Output Sink Current	$V_{+IN} = 0V$, $V_{-IN} = 1V$, $V_{OUT} = 1.5V$	20 **13**	10 **8**	10 **8**	mA Min mA Min
		$V_{OUT} = 0.4V$	2.8 **2.4**	1.0 **0.5**	0.8 **0.5**	mA Min mA Min
I_L	Output Leakage Current	$V_{+IN} = 1V$, $V_{-IN} = 0V$, $V_{OUT} = 36V$	0.1 **0.2**	10	10	μA Max μA

Electrical Characteristics These specifications apply for $V^- = GND = 0V$, $V^+ = 5V$, $V_{CM} = V_{OUT} = V^+/2$, $I_R = 100\ \mu A$, unless otherwise specified. Limits in standard typeface are for $T_J = 25°C$; limits in **boldface type** apply over the **Operating Temperature Range.** (Continued)

Symbol	Parameter	Conditions	Typical (Note 7)	LM612AM LM612AI Limits (Note 8)	LM612M LM612I Limits (Note 8)	Units
VOLTAGE REFERENCE (Note 9)						
V_R	Reference Voltage		1.244	1.2365 1.2515 (±0.6%)	1.2191 1.2689 (±2%)	V Min V Max
$\frac{\Delta V_R}{\Delta T}$	Average Drift with Temperature	(Note 10)	**18**	**80**	**150**	ppm/°C Max
$\frac{\Delta V_R}{kH}$	Average Drift with Time	$T_J = 40°C$ $T_J = 150°C$	400 1000			ppm/kH ppm/kH
$\frac{\Delta V_R}{\Delta T_J}$	Hysteresis	(Note 11)	**3.2**			μV/°C
$\frac{\Delta V_R}{\Delta I_R}$	V_R Change with Current	$V_{R[100\ \mu A]} - V_{R[17\ \mu A]}$	0.05 **0.1**	1 **1.1**	1 **1.1**	mV Max mV Max
		$V_{R[10\ mA]} - V_{R[100\ \mu A]}$ (Note 12)	1.5 **2.0**	5 **5.5**	5 **5.5**	mV Max mV Max
R	Resistance	$\Delta V_{R[10\ mA\ to\ 0.1\ mA]}/9.9\ mA$ $\Delta V_{R[100\ \mu A\ to\ 17\ \mu A]}/83\ \mu A$	0.2 0.6	**0.56** **13**	**0.56** **13**	Ω Max Ω Max
$\frac{\Delta V_R}{\Delta V^+}$	V_R Change with V^+ Change	$V_{R[V+ = 5V]} - V_{R[V+ = 36V]}$	0.1 **0.1**	1.2 **1.3**	1.2 **1.3**	mV Max mV Max
		$V_{R[V+ = 5V]} - V_{R[V+ = 3V]}$	0.01 **0.01**	1 **1.5**	1 **1.5**	mV Max mV Max
e_n	Voltage Noise	BW = 10 Hz to 10 kHz	30			μV_{RMS}

Note 1: Absolute maximum ratings indicate limits beyond which damage to the component may occur. Electrical specifications do not apply when operating the device beyond its rated operating conditions.

Note 2: Input voltage above V^+ is not allowed. As long as one input pin voltage remains inside the common-mode range, the comparator will deliver the correct output.

Note 3: More accurately, it is excessive current flow, with resulting excess heating, that limits the voltages on all pins. When any pin is pulled a diode drop below V^-, a parasitic NPN transistor turns ON. No latch-up will occur as long as the current through that pin remains below the Maximum Rating. Operation is undefined and unpredictable when any parasitic diode or transistor is conducting.

Note 4: Shorting the Output to V^- will not cause power dissipation, so it may be continuous. However, shorting the Output to any more positive voltage (including V^+), will cause 80 mA (typ.) to be drawn through the output transistor. This current multiplied by the applied voltage is the power dissipation in the output transistor. If this total power causes the junction temperature to exceed 150°C, degraded reliability or destruction of the device may occur. To determine junction temperature, see Note 5.

Note 5: Junction temperature may be calculated using $T_J = T_A + P_D\ \theta_{JA}$. The given thermal resistance is worst-case for packages in sockets in still air. For packages soldered to copper-clad board with dissipation from one comparator or reference output transistor, nominal θ_{JA} is 90°C/W for the N package.

Note 6: Human body model, 100 pF discharged through a 1.5 kΩ resistor.

Note 7: Typical values in standard typeface are for $T_J = 25°C$; values in **boldface type** apply for the full operating temperature range. These values represent the most likely parametric norm.

Note 8: All limits are guaranteed for $T_J = 25°C$ (standard type face) or over the full operating temperature range **(bold type face)**.

Note 9: V_R is the reference output voltage, nominally 1.24V.

Note 10: Average reference drift is calculated from the measurement of the reference voltage at 25°C and at the temperature extremes. The drift, in ppm/°C, is $10^6 \bullet \Delta V_R/V_{R[25°C]} \bullet \Delta T_J$, where ΔV_R is the lowest value subtracted from the highest, $V_{R[25°C]}$ is the value at 25°C, and ΔT_J is the temperature range. This parameter is guaranteed by design and sample testing.

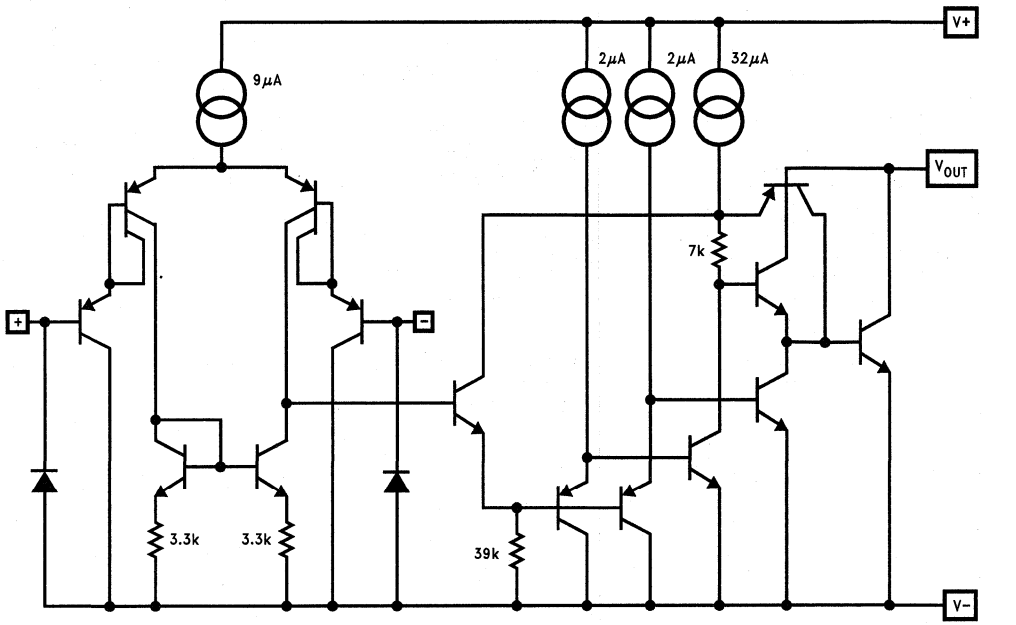
Note 11: Hysteresis is the change in V_R caused by a change in T_J, after the reference has been "dehysterized". To dehysterize the reference; that is minimize the hysteresis to the typical value, its junction temperature should be cycled in the following pattern, spiralling in toward 25°C: 25°C, 85°C, −40°C, 70°C, 0°C, 25°C.

Note 12: Low contact resistance is required for accurate measurement.

Note 13: A military RETS 612AMX electrical test specification is available on request. The military screened parts can also be procured as a Standard Military Drawing.

Simplified Schematic Diagrams

Comparator



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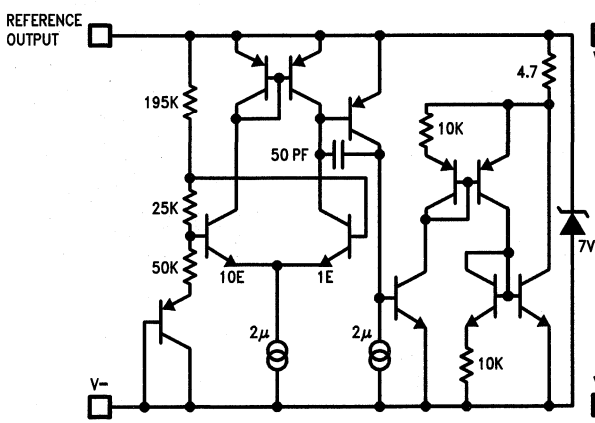
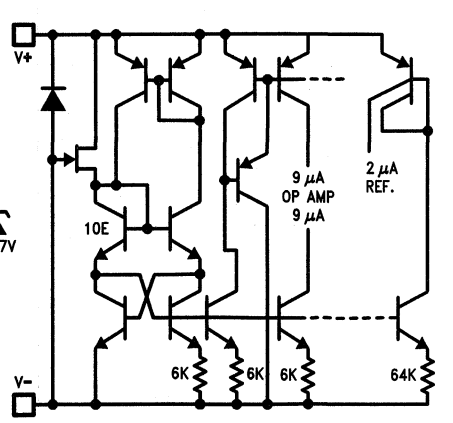
Reference



Bias

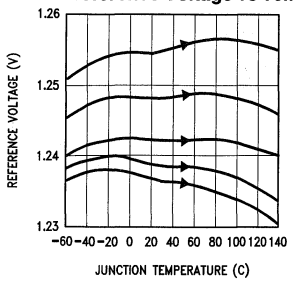


TL/H/11058–3

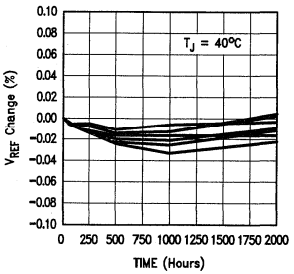
Typical Performance Characteristics (Reference)

T_J = 25°C, V^- = 0V, unless otherwise noted

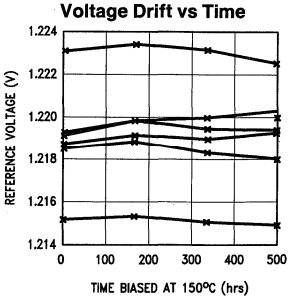
Reference Voltage vs Temp.



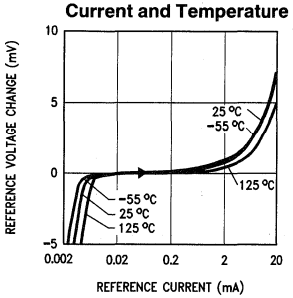
Reference Voltage Drift vs Time



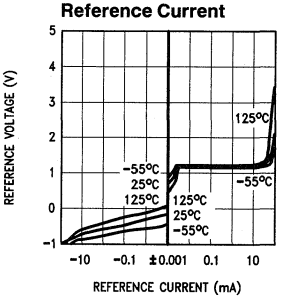
Accelerated Reference Voltage Drift vs Time



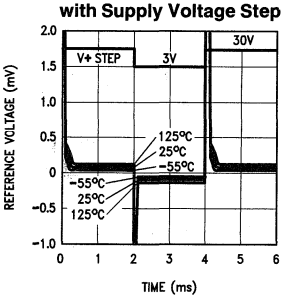
Reference Voltage vs Current and Temperature



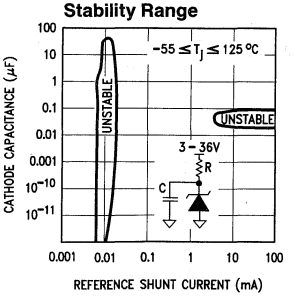
Reference Voltage vs Reference Current



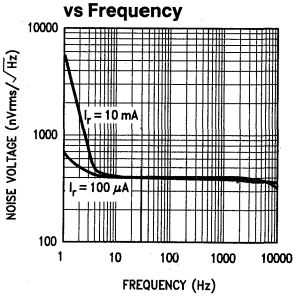
Reference Voltage Change with Supply Voltage Step



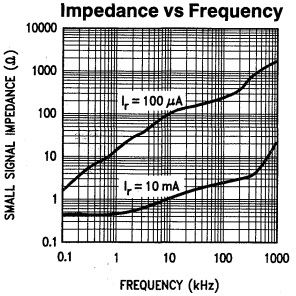
Reference AC Stability Range



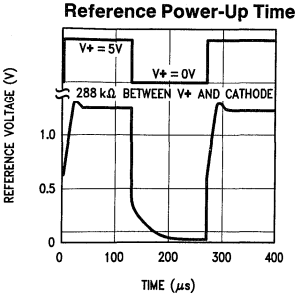
Reference Noise Voltage vs Frequency



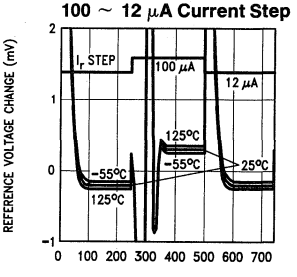
Reference Small-Signal Impedance vs Frequency



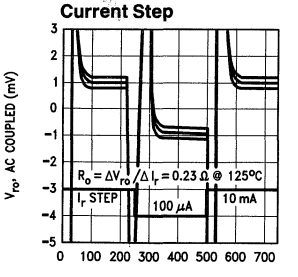
Reference Power-Up Time



Reference Voltage with 100 ~ 12 μA Current Step



Reference Step Response for 100 μA ~ 10 mA Current Step

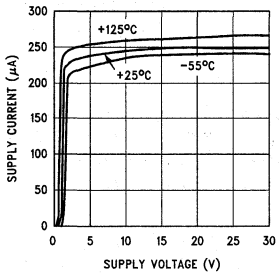


TL/H/11058–4

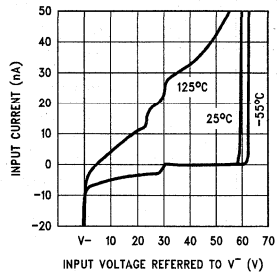
Typical Performance Characteristics (Comparators)

T_J = 25°C, V^+ = 5V, V^- = 0V

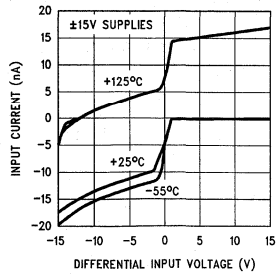
Supply Current vs Supply Voltage



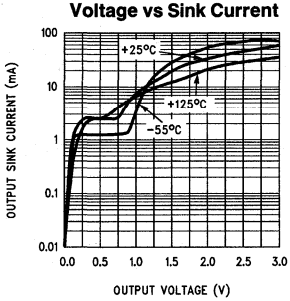
Input Bias Current vs Common-Mode Voltage



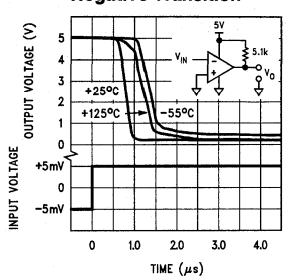
Input Current vs Differential Input Voltage



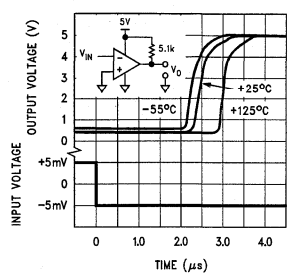
Output Saturation Voltage vs Sink Current



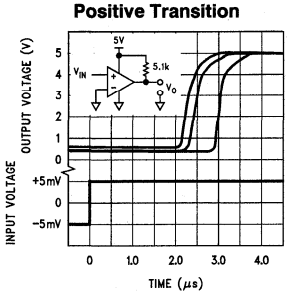
Small-Signal Response Times—Inverting Input, Negative Transition



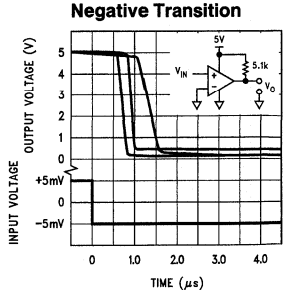
Small-Signal Response Times—Inverting Input, Positive Transition



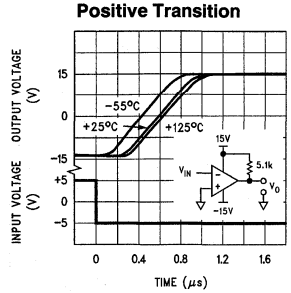
Small-Signal Response Times—Non-Inverting Input, Positive Transition



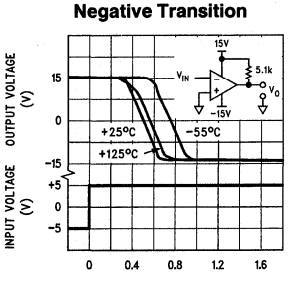
Small-Signal Response Times—Non-Inverting Input, Negative Transition



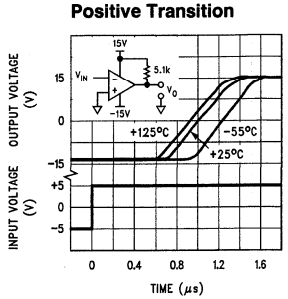
Large-Signal Response Times—Inverting Input, Positive Transition



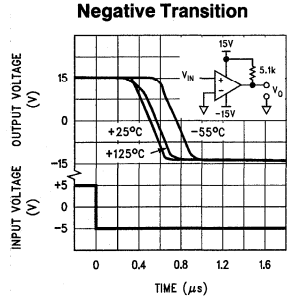
Large-Signal Response Times—Inverting Input, Negative Transition



Large-Signal Response Times—Non-Inverting Input, Positive Transition



Large-Signal Response Times—Non-Inverting Input, Negative Transition



TL/H/11058–6

Application Information

VOLTAGE REFERENCE

Reference Biasing

The voltage reference is of a shunt regulator topology that models as a simple zener diode. With current I_R flowing in the "forward" direction there is the familiar diode transfer function. I_R flowing in the reverse direction forces the reference voltage to be developed from cathode to anode.

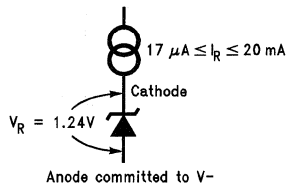


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FIGURE 1. 1.24V Reference is Developed between Cathode and Anode; Current Source I_R is External

The reference equivalent circuit reveals how V_R is held at the constant 1.2V by feedback for a wide range of reverse current.

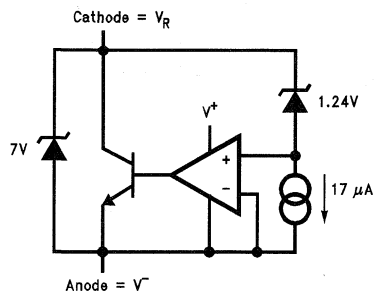

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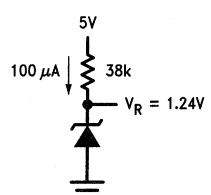
FIGURE 2. Reference Equivalent Circuit

To generate the required reverse current, typically a resistor is connected from a supply voltage higher than the reference voltage to the Reference Output pin. Varying that voltage, and so varying I_R, has small effect with the equivalent series resistance of less than an ohm at the higher currents. Alternatively, an active current source, such as the LM134 series, may generate I_R.



TL/H/11058–10

FIGURE 3. 1.2V Reference

Capacitors in parallel with the reference are allowed. See the Reference AC Stability Range typical curve for capacitance values—from 20 μA to 3 mA the reference is stable for any value of capacitance. With the reference's wide stability range with resistive and capacitive loads, a wide range of RC filter values will perform noise filtering when necessary.

Reference Hysteresis

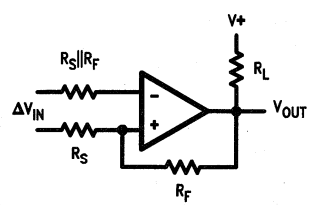
The reference voltage depends, slightly, on the thermal history of the die. Competitive micro-power products vary—always check the datasheet for any given device. Do not assume that no specification means no hysteresis.

COMPARATORS

Either comparator or the reference may be biased in any way with no effect on the other sections of the LM612, except when a substrate diode conducts (see Electrical Characteristics Note 3). For example, one or both inputs of one comparator may be outside the input voltage range limits, the reference may be unpowered, and the other comparator will still operate correctly. The inverting input of an unused comparator should be tied to V^- and the non-inverting tied to V^+.

Hysteresis

Any comparator may oscillate or produce a noisy output if the applied differential input voltage is near the comparator's offset voltage. This usually happens when the input signal is moving very slowly across the comparator's switching threshold. This problem can be prevented by the addition of hysteresis, or positive feedback, as shown in *Figure 4*.



TL/H/11058–11

FIGURE 4. R_S and R_F Add Hysteresis to Comparator

The amount of hysteresis added in *Figure 4* is

$$V_H = V^+ \times \frac{R_S}{(R_F + R_S)}$$

$$\approx V^+ \times \frac{R_S}{R_F} \qquad \text{for } R_F >> R_S$$

A good rule of thumb is to add hysteresis of at least the maximum specified offset voltage. More than about 50 mV

Application Information (Continued)

of hysteresis can substantially reduce the accuracy of the comparator, since the offset voltage is effectively being increased by the hysteresis when the comparator output is high.

It is often a good idea to decrease the amount of hysteresis until oscillations are observed, then use three times that minimum hysteresis in the final circuit. Note that the amount of hysteresis needed is greatly affected by layout. The amount of hysteresis should be rechecked each time the layout is changed, such as changing from a breadboard to a P.C. board.

Input Stage

The input stage uses lateral PNP input transistors which, unlike those of many op amps, have breakdown voltage BV_{EBO} equal to the absolute maximum supply voltage. Also, they have no diode clamps to the positive supply nor across the inputs. These features make the inputs look like high impedances to input sources producing large differential and common-mode voltages.

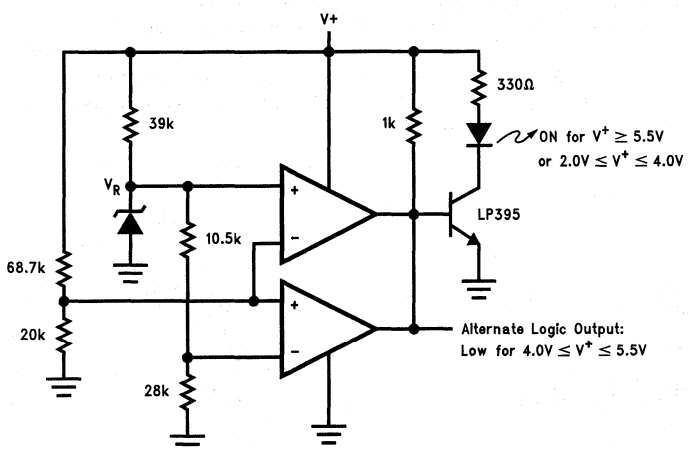
The guaranteed common-mode input voltage range for an LM612 is $V^- \leq V_{CM} \leq (V^+ - 1.8V)$, over temperature. This is the voltage range in which the comparisons must be made. If both inputs are within this range, the output will be at the correct state. If one input is within this range, and the other input is less than $(V^- + 32V)$, even if this is greater than V^+, the output will be at the correct state. If, however, either or both inputs are driven below V^-, and either input current exceeds 10 μA, the output state is not guaranteed to be correct. If both inputs are above $(V^+ - 1.8V)$, the output state is also not guaranteed to be correct.

Output Stage

The comparators have a common open-collector output stage which requires a pull-up resistor to a positive supply voltage for the output to switch properly. When the internal output transistor is off, the output (HIGH) voltage will be pulled up to this external positive voltage.

To ensure that the LOW output voltage is under the TTL-low threshold, the output transistor's load current must be less than 0.8 mA (over temperature) when it turns on. This impacts the minimum value of the pull-up resistor.

Typical Applications



TL/H/11058–12

Power Supply Monitor with Indicator

National Semiconductor

LM613 Dual Operational Amplifiers, Dual Comparators, and Adjustable Reference

General Description

The LM613 consists of dual op-amps, dual comparators, and a programmable voltage reference in a 16-pin package. The op-amps out-performs most single-supply op-amps by providing higher speed and bandwidth along with low supply current. This device was specifically designed to lower cost and board space requirements in transducer, test, measurement, and data acquisition systems.

Combining a stable voltage reference with wide output swing op-amps makes the LM613 ideal for single supply transducers, signal conditioning and bridge driving where large common-mode-signals are common. The voltage reference consists of a reliable band-gap design that maintains low dynamic output impedance (1Ω typical), excellent initial tolerance (0.6%), and the ability to be programmed from 1.2V to 6.3V via two external resistors. The voltage reference is very stable even when driving large capacitive loads, as are commonly encountered in CMOS data acquisition systems.

As a member of National's Super-Block™ family, the LM613 is a space-saving monolithic alternative to a multi-chip solution, offering a high level of integration without sacrificing performance.

Features

OP AMP

- Low operating current (Op Amp) 300 μA
- Wide supply voltage range 4V to 36V
- Wide common-mode range V^- to (V^+ − 1.8V)
- Wide differential input voltage ±36V
- Available in plastic package rated for Military Temp. Range Operation

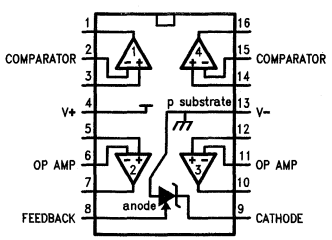
REFERENCE

- Adjustable output voltage 1.2V to 6.3V
- Tight initial tolerance available ±0.6%
- Wide operating current range 17 μA to 20 mA
- Tolerant of load capacitance

Applications

- Transducer bridge driver
- Process and mass flow control systems
- Power supply voltage monitor
- Buffered voltage references for A/D's

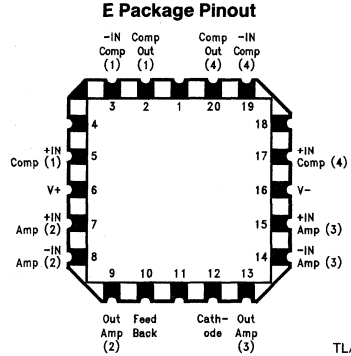
Connection Diagrams



Top View

TL/H/9226-1

E Package Pinout



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Ordering Information

Reference Tolerance & V_{OS}	Temperature Range			Package	NSC Drawing
	Military $-55°C \le T_A \le +125°C$	Industrial $-40°C \le T_A \le +85°C$	Commercial $0°C \le T_A \le +70°C$		
+0.6% 80 ppm/°C Max. $V_{OS} \le 3.5$ mV	LM613AMN	LM613AIN	—	16-Pin Molded DIP	N16E
	LM613AMJ/883 (Note 14)	—	—	16-Pin Ceramic DIP	J16A
	LM613AME/883 (Note 14)	—	—	20-Pin LCC	E20A
±2.0% 150 ppm/°C Max. $V_{OS} \le 5.0$ mV Max.	LM613MN	LM613IN	LM613CN	16-Pin Molded DIP	N16E
	—	LM613IWM		16-Pin Wide Surface Mount	M16B

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Voltage on Any Pin Except V_R (referred to V^- pin)
(Note 2) 36V (Max)
(Note 3) −0.3V (Min)

Current through Any Input Pin & V_R Pin ±20 mA

Differential Input Voltage
Military and Industrial ±36V
Commercial ±32V

Storage Temperature Range $-65°C \le T_J \le +150°C$

Maximum Junction Temperature (Note 4) 150°C

Thermal Resistance, Junction-to-Ambient (Note 5)
N Package 100°C/W
WM Package 150°C/W

Soldering Information (10 Seconds)
N Package 260°C
WM Package 220°C

ESD Tolerance (Note 6) ±1 kV

Operating Temperature Range

LM613AI, LM613BI $-40°C$ to $+85°C$
LM613AM, LM613M $-55°C$ to $+125°C$
LM613C $0°C \le T_J \le +70°C$

Electrical Characteristics

These specifications apply for $V^- = GND = 0V$, $V^+ = 5V$, $V_{CM} = V_{OUT} = 2.5V$, $I_R = 100\ \mu A$, FEEDBACK pin shorted to GND, unless otherwise specified. Limits in standard typeface are for $T_J = 25°C$; limits in **boldface type** apply over the **Operating Temperature Range**.

Symbol	Parameter	Conditions	Typical (Note 7)	LM613AM LM613AI Limits (Note 8)	LM613M LM613I LM613C Limits (Note 8)	Units
I_S	Total Supply Current	$R_{LOAD} = \infty$, $4V \le V^+ \le 36V$ (32V for LM613C)	450 **550**	940 **1000**	1000 **1070**	μA (Max) μA (Max)
V_S	Supply Voltage Range		2.2 **2.9**	2.8 **3**	2.8 **3**	V (Min) V (Min)
			46 **43**	36 **36**	32 **32**	V (Max) V (Max)
OPERATIONAL AMPLIFIERS						
V_{OS1}	V_{OS} Over Supply	$4V \le V^+ \le 36V$ $(4V \le V^+ \le 32V$ for LM613C)	1.5 **2.0**	3.5 **6.0**	5.0 **7.0**	mV (Max) mV (Max)
V_{OS2}	V_{OS} Over V_{CM}	V_{CM} = 0V through V_{CM} = $(V^+ - 1.8V)$, $V^+ = 30V$, $V^- = 0V$	1.0 **1.5**	3.5 **6.0**	5.0 **7.0**	mV (Max) mV (Max)
$\frac{V_{OS3}}{\Delta T}$	Average V_{OS} Drift	(Note 8)	**15**			μV/°C (Max)
I_B	Input Bias Current		10 **11**	25 **30**	35 **40**	nA (Max) nA (Max)
I_{OS}	Input Offset Current		0.2 **0.3**	4 **5**	4 **5**	nA (Max) nA (Max)
$\frac{I_{OS1}}{\Delta T}$	Average Offset Current		**4**			pA/°C
R_{IN}	Input Resistance	Differential	1000			MΩ
C_{IN}	Input Capacitance	Common-Mode	6			pF
e_n	Voltage Noise	f = 100 Hz, Input Referred	74			$nV/\sqrt{Hz}$
I_n	Current Noise	f = 100 Hz, Input Referred	58			$fA/\sqrt{Hz}$
CMRR	Common-Mode Rejection Ratio	$V^+ = 30V$, $0V \le V_{CM} \le (V^+ - 1.8V)$ $CMRR = 20 \log (\Delta V_{CM}/\Delta V_{OS})$	95 **90**	80 **75**	75 **70**	dB (Min) dB (Min)
PSRR	Power Supply Rejection Ratio	$4V \le V^+ \le 30V$, $V_{CM} = V^+/2$, $PSRR = 20 \log (\Delta V^+/V_{OS})$	110 **100**	80 **75**	75 **70**	dB (Min) dB (Min)
A_V	Open Loop Voltage Gain	$R_L = 10\ k\Omega$ to GND, $V^+ = 30V$, $5V \le V_{OUT} \le 25V$	500 **50**	100 **40**	94 **40**	V/mV (Min)

Electrical Characteristics

These specifications apply for V^- = GND = 0V, V^+ = 5V, V_{CM} = V_{OUT} = 2.5V, I_R = 100 μA, FEEDBACK pin shorted to GND, unless otherwise specified. Limits in standard typeface are for T_J = 25°C; limits in **boldface type** apply over **Operating Temperature Range**. (Continued)

Symbol	Parameter	Conditions	Typical (Note 7)	LM613AM LM613AI Limits (Note 8)	LM613M LM613I LM613C Limits (Note 8)	Units
OPERATIONAL AMPLIFIERS (Continued)						
SR	Slew Rate	V^+ = 30V (Note 9)	0.70 **0.65**	0.55 **0.45**	0.50 **0.45**	V/μs
GBW	Gain Bandwidth	C_L = 50 pF	0.8 **0.5**			MHz MHz
V_{O1}	Output Voltage Swing High	R_L = 10 kΩ to GND, V^+ = 36V (32V for LM613C)	$V^+ - 1.4$ **$V^+ - 1.6$**	$V^+ - 1.7$ **$V^+ - 1.9$**	$V^+ - 1.8$ **$V^+ - 1.9$**	V (Min) V (Min)
V_{O2}	Output Voltage Swing Low	R_L = 10 kΩ to V^+, V^+ = 36V (32V for LM613C)	$V^- + 0.8$ **$V^- + 0.9$**	$V^- + 0.9$ **$V^- + 1.0$**	$V^- + 0.95$ **$V^- + 1.0$**	V (Max) V (Max)
I_{OUT}	Output Source Current	V_{OUT} = 2.5V, V^+_{IN} = 0V, V^-_{IN} = −0.3V	25 **15**	20 **13**	16 **13**	mA (Min) mA (Min)
I_{SINK}	Output Sink Current	V_{OUT} = 1.6V, V^+_{IN} = 0V, V^-_{IN} = 0.3V	17 **9**	14 **8**	13 **8**	mA (Min) mA (Min)
I_{SHORT}	Short Circuit Current	V_{OUT} = 0V, V^+_{IN} = 3V, V^-_{IN} = 2V	30 **40**	50 **60**	50 **60**	mA (Max) mA (Max)
		V_{OUT} = 5V, V^+_{IN} = 2V, V^-_{IN} = 3V	30 **32**	60 **80**	70 **90**	mA (Max) mA (Max)
COMPARATORS						
V_{OS}	Offset Voltage	4V ≤ V^+ ≤ 36V (32V for LM613C), R_L = 15 kΩ	1.0 **2.0**	3.0 **6.0**	5.0 **7.0**	mV (Max) mV (Max)
$\frac{V_{OS}}{V_{CM}}$	Offset Voltage over V_{CM}	0V ≤ V_{CM} ≤ 36V V^+ = 36V, (32V for LM613C)	1.0 **1.5**	3.0 **6.0**	5.0 **7.0**	mV (Max) mV (Max)
$\frac{V_{OS}}{\Delta T}$	Average Offset Voltage Drift		**15**			μV/°C (Max)
I_B	Input Bias Current		5 **8**	25 **30**	35 **40**	nA (Max) nA (Max)
I_{OS}	Input Offset Current		0.2 **0.3**	4 **5**	4 **5**	nA (Max) nA (Max)
A_V	Voltage Gain	R_L = 10 kΩ to 36V (32V for LM613C) 2V ≤ V_{OUT} ≤ 27V	500 **100**			V/mV V/mV
t_r	Large Signal Response Time	V^+_{IN} = 1.4V, V^-_{IN} = TTL Swing, R_L = 5.1 kΩ	1.5 **2.0**			μs μs
I_{SINK}	Output Sink Current	V^+_{IN} = 0V, V^-_{IN} = 1V, V_{OUT} = 1.5V	20 **13**	10 **8**	10 **8**	mA (Min) mA (Min)
		V_{OUT} = 0.4V	2.8 **2.4**	1.0 **0.5**	0.8 **0.5**	mA (Min) mA (Min)
I_{LEAK}	Output Leakage Current	V^+_{IN} = 1V, V^-_{IN} = 0V, V_{OUT} = 36V (32V for LM613C)	0.1 **0.2**	10	10	μA (Max) μA (Max)

Electrical Characteristics These specifications apply for V^- = GND = 0V, V^+ = 5V, V_{CM} = V_{OUT} = 2.5V, I_R = 100 μA, FEEDBACK pin shorted to GND, unless otherwise specified. Limits in standard typeface are for T_J = 25°C; limits in **boldface type** apply over **Operating Temperature Range.** (Continued)

Symbol	Parameter	Conditions	Typical (Note 7)	LM613AM LM613AI Limits (Note 8)	LM613M LM613I LM613C Limits (Note 8)	Units
VOLTAGE REFERENCE						
V_R	Voltage Reference	(Note 10)	1.244	1.2365 1.2515 (±0.6%)	1.2191 1.2689 (±2%)	V (Min) V (Max)
$\frac{\Delta V_R}{\Delta T}$	Average Temp. Drift	(Note 11)	**10**	**80**	**150**	ppm/°C (Max)
$\frac{\Delta V_R}{\Delta T_J}$	Hysteresis	(Note 12)	**3.2**			μV/°C
$\frac{\Delta V_R}{\Delta I_R}$	V_R Change with Current	$V_{R(100\ \mu A)} - V_{R(17\ \mu A)}$	0.05 **0.1**	1 **1.1**	1 **1.1**	mV (Max) mV (Max)
		$V_{R(10\ mA)} - V_{R(100\ \mu A)}$ (Note 13)	1.5 **2.0**	5 **5.5**	5 **5.5**	mV (Max) mV (Max)
R	Resistance	$\Delta V_{R(10 \rightarrow 0.1\ mA)}/9.9\ mA$ $\Delta V_{R(100 \rightarrow 17\ \mu A)}/83\ \mu A$	**0.2** **0.6**	**0.56** **13**	**0.56** **13**	Ω (Max) Ω (Max)
$\frac{V_R}{\Delta V_{RO}}$	V_R Change with High V_{RO}	$V_{R(Vro = Vr)} - V_{R(Vro = 6.3V)}$ (5.06V between Anode and FEEDBACK)	2.5 **2.8**	7 **10**	7 **10**	mV (Max) mV (Max)
$\frac{V_R}{\Delta V^+}$	V_R Change with V_{ANODE} Change	$V_{R(V^+ = 5V)} - V_{R(V^+ = 36V)}$ (V^+ = 32V for LM613C)	0.1 **0.1**	1.2 **1.3**	1.2 **1.3**	mV (Max) mV (Max)
		$V_{R(V^+ = 5V)} - V_{R(V^+ = 3V)}$	0.01 **0.01**	1 **1.5**	1 **1.5**	mV (Max) mV (Max)
I_{FB}	FEEDBACK Bias Current	$V_{ANODE} \leq V_{FB} \leq 5.06V$	22 **29**	35 **40**	50 **55**	nA (Max) nA (Max)
e_n	V_R Noise	10 Hz to 10 kHz, $V_{RO} = V_R$	30			μV_{RMS}

Note 1: Absolute maximum ratings indicate limits beyond which damage to the component may occur. Electrical specifications do not apply when operating the device beyond its rated operating conditions.

Note 2: Input voltage above V^+ is allowed. As long as one input pin voltage remains inside the common-mode range, the comparator will deliver the correct output.

Note 3: More accurately, it is excessive current flow, with resulting excess heating, that limits the voltages on all pins. When any pin is pulled a diode drop below V^-, a parasitic NPN transistor turns ON. No latch-up will occur as long as the current through that pin remains below the Maximum Rating. Operation is undefined and unpredictable when any parasitic diode or transistor is conducting.

Note 4: Simultaneous short-circuit of multiple comparators while using high supply voltages may force junction temperature above maximum, and thus should not be continuous.

Note 5: Junction temperature may be calculated using $T_J = T_A + P_D\ \theta_{JA}$. The given thermal resistance is worst-case for packages in sockets in still air. For packages soldered to copper-clad board with dissipation from one comparator or reference output transistor, nominal θ_{JA} is 90°C/W for the N package, and 135°C/W for the WM package.

Note 6: Human body model, 100 pF discharged through a 1.5 kΩ resistor.

Note 7: Typical values in standard typeface are for T_J = 25°C; values in **bold face type** apply for the full operating temperature range. These values represent the most likely parametric norm.

Note 8: All limits are guaranteed at room temperature (standard type face) or at operating temperature extremes **(bold type face).**

Note 9: Slew rate is measured with the op amp in a voltage follower configuration. For rising slew rate, the input voltage is driven from 5V to 25V, and the output voltage transition is sampled at 10V and @ 20V. For falling slew rate, the input voltage is driven from 25V to 5V, and the output voltage transition is sampled at 20V and 10V.

Note 10: V_R is the Cathode-to-feedback voltage, nominally 1.244V.

Note 11: Average reference drift is calculated from the measurement of the reference voltage at 25°C and at the temperature extremes. The drift, in ppm/°C, is $10^6 \bullet \Delta V_R / (V_{R[25°C]} \bullet \Delta T_J)$, where ΔV_R is the lowest value subtracted from the highest, $V_{R[25°C]}$ is the value at 25°C, and ΔT_J is the temperature range. This parameter is guaranteed by design and sample testing.

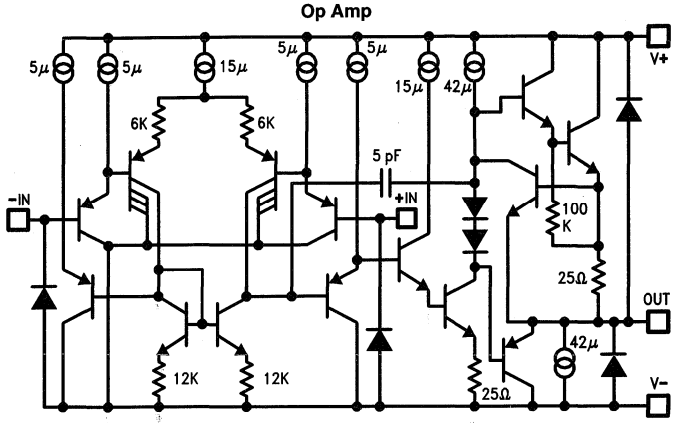
Note 12: Hysteresis is the change in V_R caused by a change in T_J, after the reference has been "dehysterized". To dehysterize the reference; that is minimize the hysteresis to the typical value, its junction temperature should be cycled in the following pattern, spiraling in toward 25°C: 25°C, 85°C, −40°C, 70°C, 0°C, 25°C.

Note 13: Low contact resistance is required for accurate measurement.

Note 14: A military RETS 613AMX electrical test specification is available on request. The Military screened parts can also be procured as a Standard Military Drawing.

Simplified Schematic Diagrams

Op Amp



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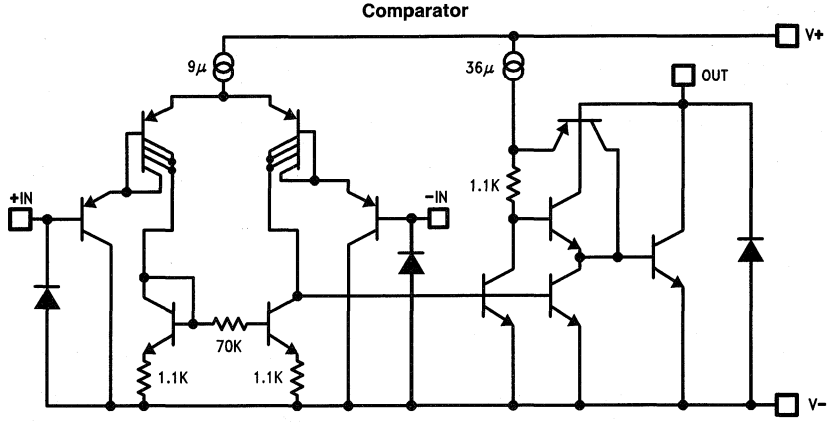
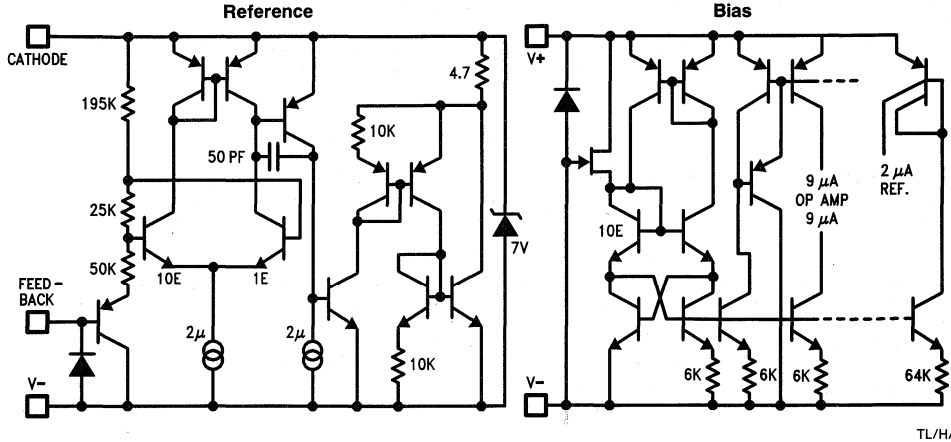
Comparator



TL/H/9226–3

Reference

Bias

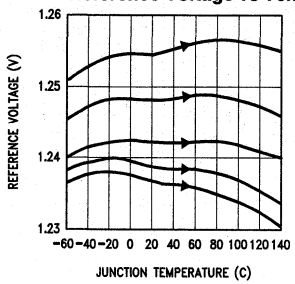


TL/H/9226–4

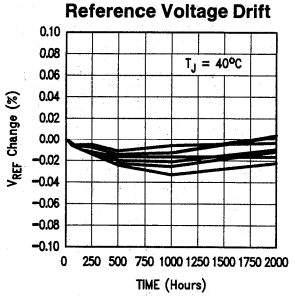
Typical Performance Characteristics (Reference)

T_J = 25°C, FEEDBACK pin shorted to V^- = 0V, unless otherwise noted

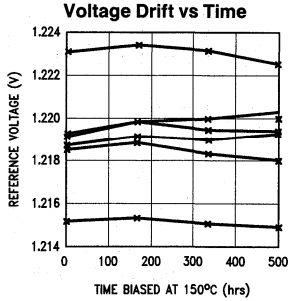
Reference Voltage vs Temp.



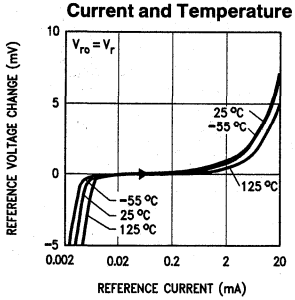
Reference Voltage Drift



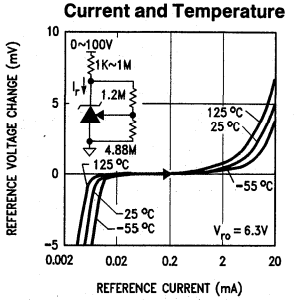
Accelerated Reference Voltage Drift vs Time



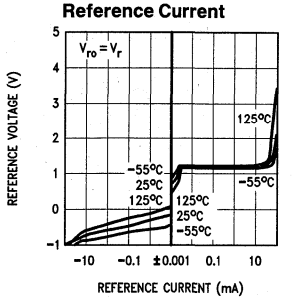
Reference Voltage vs Current and Temperature



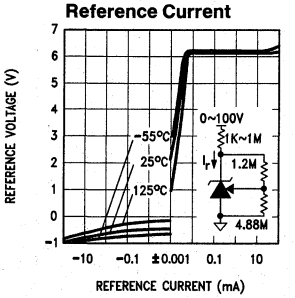
Reference Voltage vs Current and Temperature



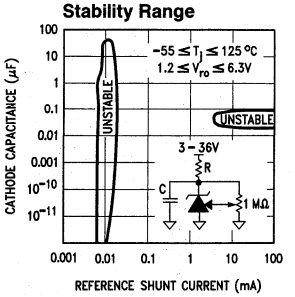
Reference Voltage vs Reference Current



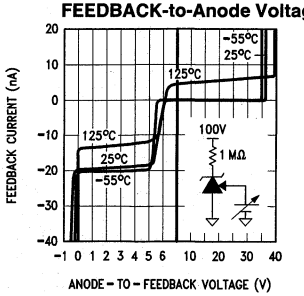
Reference Voltage vs Reference Current



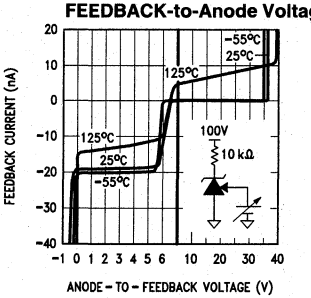
Reference AC Stability Range



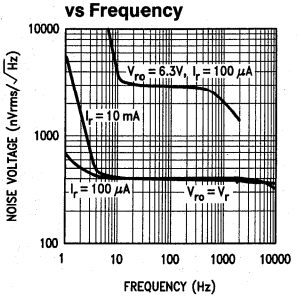
FEEDBACK Current vs FEEDBACK-to-Anode Voltage



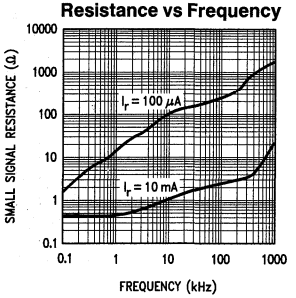
FEEDBACK Current vs FEEDBACK-to-Anode Voltage



Reference Noise Voltage vs Frequency



Reference Small-Signal Resistance vs Frequency



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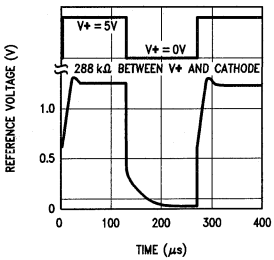
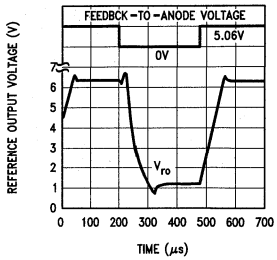
Typical Performance Characteristics (Reference) (Continued)

T_J = 25°C, FEEDBACK pin shorted to V^- = 0V, unless otherwise noted

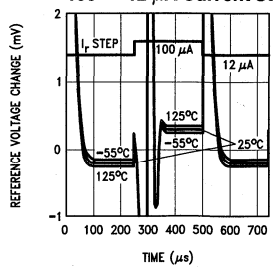
Reference Power-Up Time



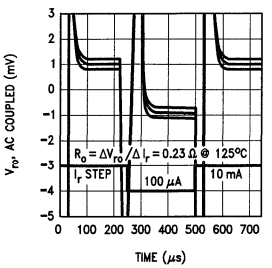
Reference Voltage with FEEDBACK Voltage Step



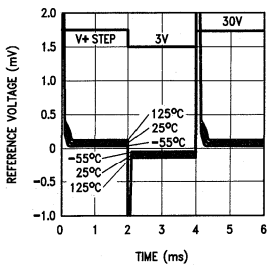
Reference Voltage with 100 ~ 12 μA Current Step



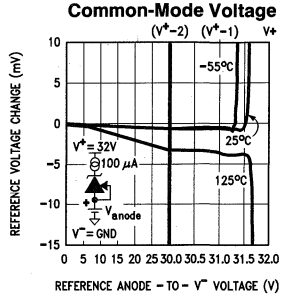
Reference Step Response for 100 μA ~ 10 mA Current Step



Reference Voltage Change with Supply Voltage Step



Reference Change vs Common-Mode Voltage

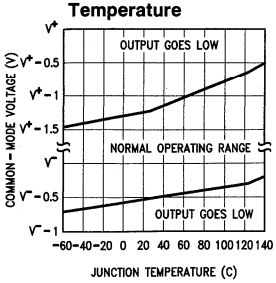


TL/H/9226–6

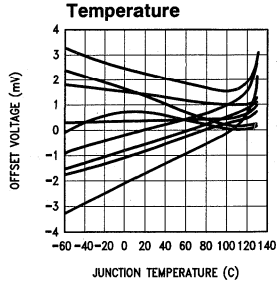
Typical Performance Characteristics (Op Amps)

V^+ = 5V, V^- = GND = 0V, V_{CM} = $V^+/2$, V_{OUT} = $V^+/2$, T_J = 25°C, unless otherwise noted

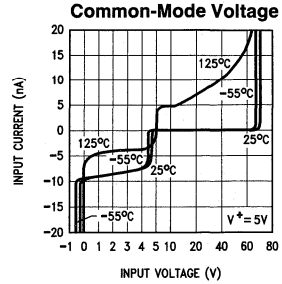
Input Common-Mode Voltage Range vs Temperature



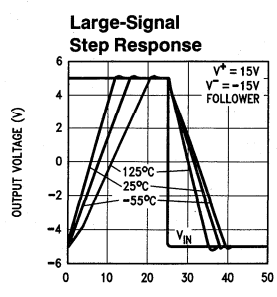
V_{OS} vs Junction Temperature



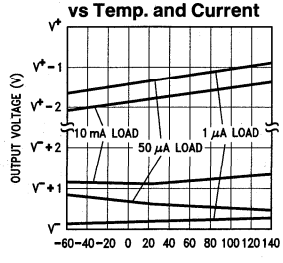
Input Bias Current vs Common-Mode Voltage



Large-Signal Step Response



Output Voltage Swing vs Temp. and Current

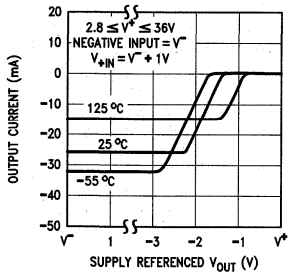


TL/H/9226–7

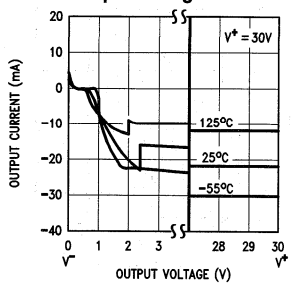
Typical Performance Characteristics (Op Amps) (Continued)

$V^+ = 5V$, $V^- = GND = 0V$, $V_{CM} = V^+/2$, $V_{OUT} = V^+/2$, $T_J = 25°C$, unless otherwise noted

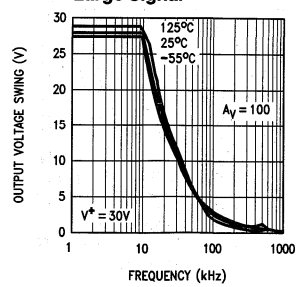
Output Source Current vs Output Voltage and Temp.



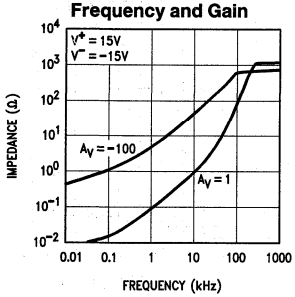
Output Sink Current vs Output Voltage



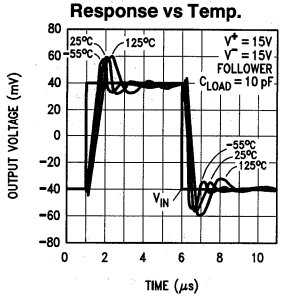
Output Swing, Large Signal



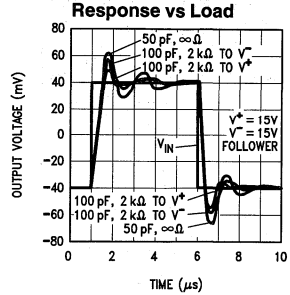
Output Impedance vs Frequency and Gain



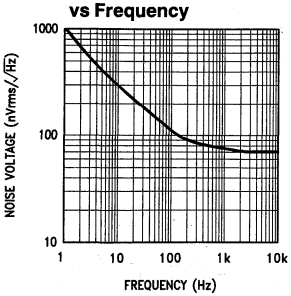
Small Signal Pulse Response vs Temp.



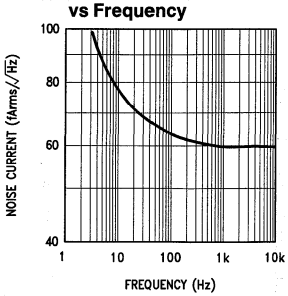
Small-Signal Pulse Response vs Load



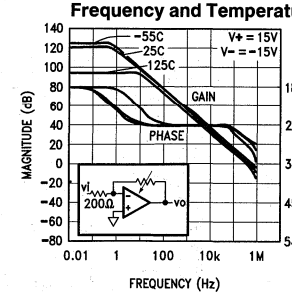
Op Amp Voltage Noise vs Frequency



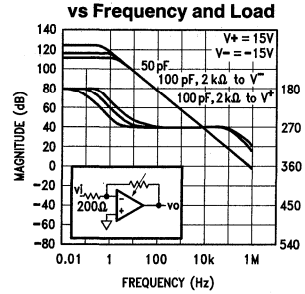
Op Amp Current Noise vs Frequency



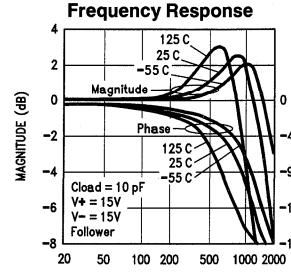
Small-Signal Voltage Gain vs Frequency and Temperature



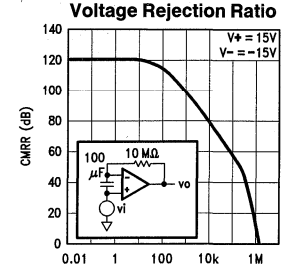
Small-Signal Voltage Gain vs Frequency and Load



Follower Small-Signal Frequency Response



Common-Mode Input Voltage Rejection Ratio



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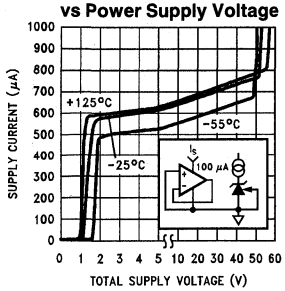
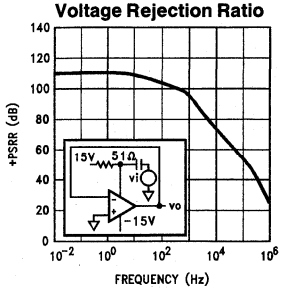
Typical Performance Characteristics (Op Amps) (Continued)

$V^+ = 5V$, $V^- = GND = 0V$, $V_{CM} = V^+/2$, $V_{OUT} = V^+/2$, $T_J = 25°C$, unless otherwise noted

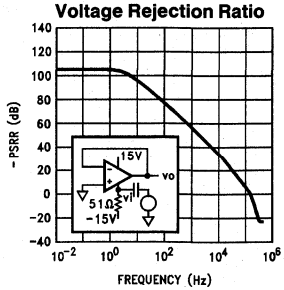
Power Supply Current vs Power Supply Voltage



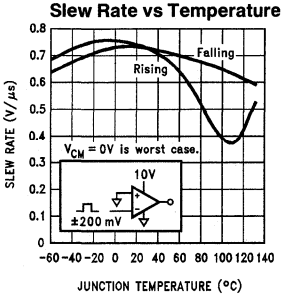
Positive Power Supply Voltage Rejection Ratio



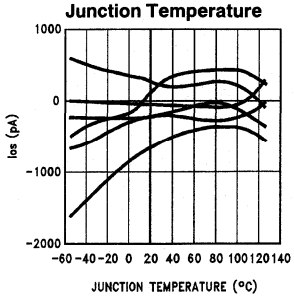
Negative Power Supply Voltage Rejection Ratio



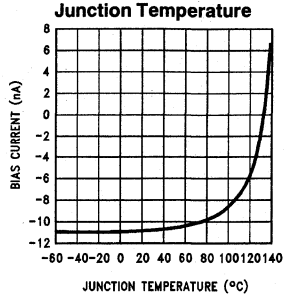
Slew Rate vs Temperature



Input Offset Current vs Junction Temperature



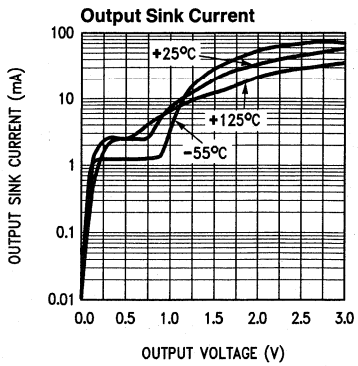
Input Bias Current vs Junction Temperature



TL/H/9226-9

Typical Performance Characteristics (Comparators)

Output Sink Current



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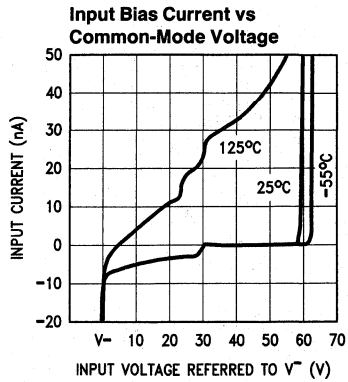
Input Bias Current vs Common-Mode Voltage



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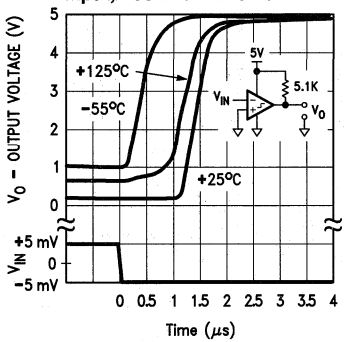
Typical Performance Characteristics (Comparators) (Continued)

Comparator Response Times—Inverting Input, Positive Transition



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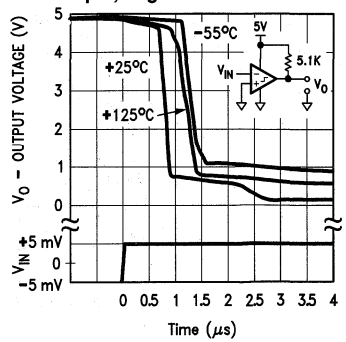
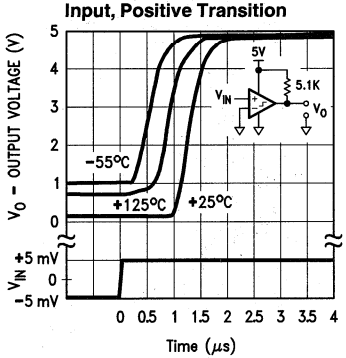
Comparator Response Times—Inverting Input, Negative Transition



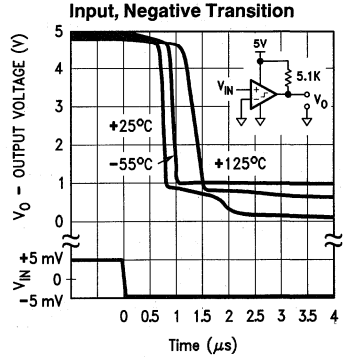
TL/H/9226–13

Comparator Response Times—Non-Inverting Input, Positive Transition



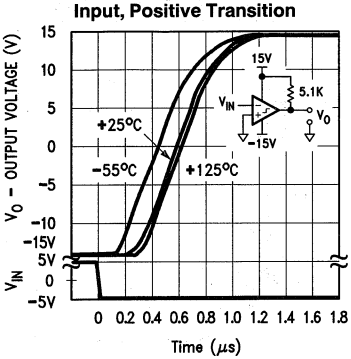
TL/H/9226–14

Comparator Response Times—Non-Inverting Input, Negative Transition



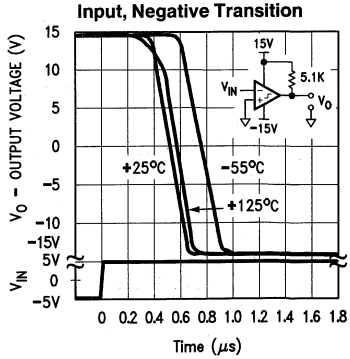
TL/H/9226–15

Comparator Response Times—Inverting Input, Positive Transition



TL/H/9226–16

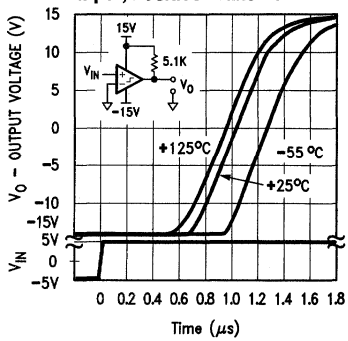
Comparator Response Times—Inverting Input, Negative Transition



TL/H/9226–17

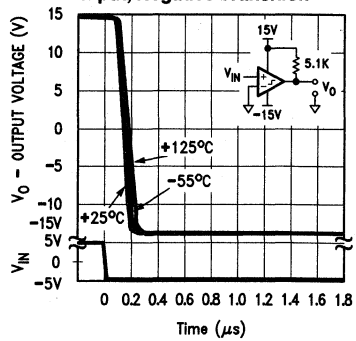
Typical Performance Characteristics (Comparators) (Continued)

Comparator Response Times—Non-Inverting Input, Positive Transition



TL/H/9226–18

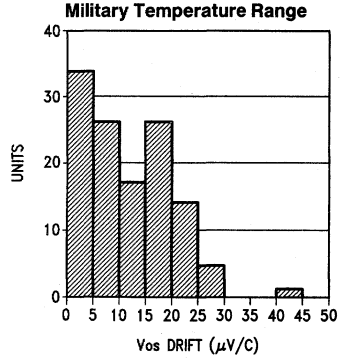
Comparator Response Times—Non-Inverting Input, Negative Transition



TL/H/9226–19

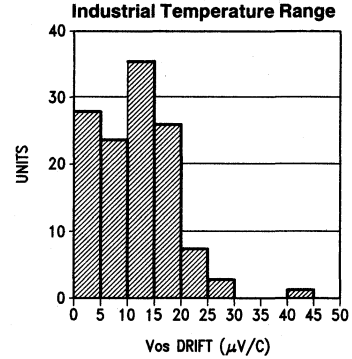
Typical Performance Distributions

Average V_{OS} Drift Military Temperature Range



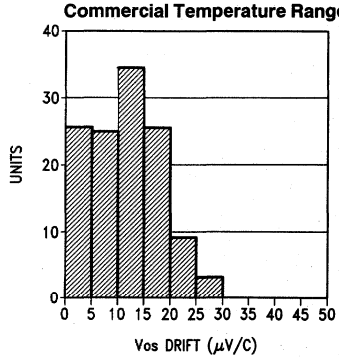
TL/H/9226–20

Average V_{OS} Drift Industrial Temperature Range



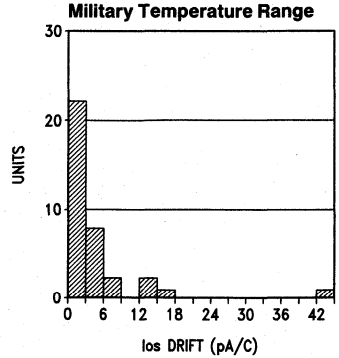
TL/H/9226–21

Average V_{OS} Drift Commercial Temperature Range



TL/H/9226–22

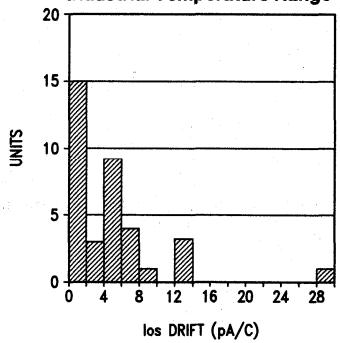
Average I_{OS} Drift Military Temperature Range



TL/H/9226–23

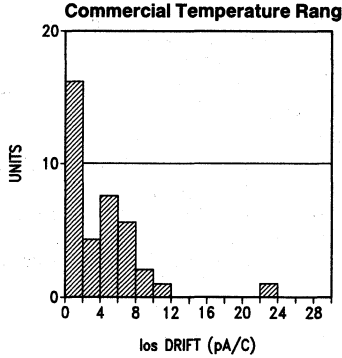
Typical Performance Distributions (Continued)

Average I_{OS} Drift Industrial Temperature Range



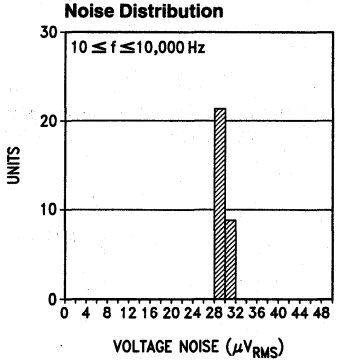
TL/H/9226-24

Average I_{OS} Drift Commercial Temperature Range



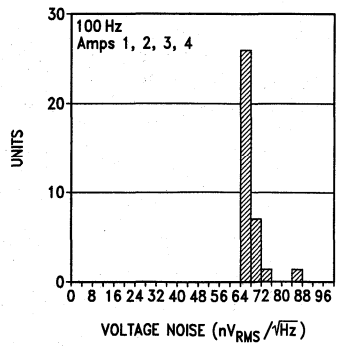
TL/H/9226-25

Voltage Reference Broad-Band Noise Distribution



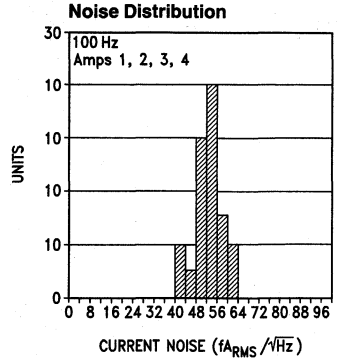
TL/H/9226-26

Op Amp Voltage Noise Distribution



TL/H/9226-27

Op Amp Current Noise Distribution



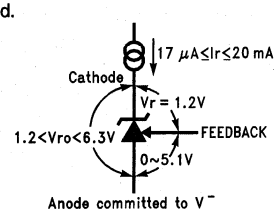
TL/H/9226-28

Application Information

VOLTAGE REFERENCE

Reference Biasing

The voltage reference is of a shunt regulator topology that models as a simple zener diode. With current I_r flowing in the "forward" direction there is the familiar diode transfer function. I_r flowing in the reverse direction forces the reference voltage to be developed from cathode to anode. The cathode may swing from a diode drop below V^- to the reference voltage or to the avalanche voltage of the parallel protection diode, nominally 7V. A 6.3V reference with $V^+ = 3V$ is allowed.



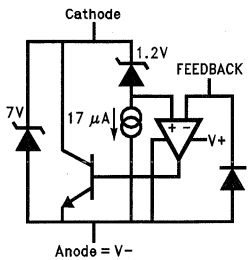
TL/H/9226-29

FIGURE 1. Voltage Associated with Reference (current source I_r is external)

Application Information (Continued)

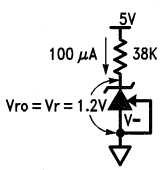
The reference equivalent circuit reveals how V_r is held at the constant 1.2V by feedback, and how the FEEDBACK pin passes little current.

To generate the required reverse current, typically a resistor is connected from a supply voltage higher than the reference voltage. Varying that voltage, and so varying I_r, has small effect with the equivalent series resistance of less than an ohm at the higher currents. Alternatively, an active current source, such as the LM134 series, may generate I_r.



TL/H/9226–30

FIGURE 2. Reference Equivalent Circuit



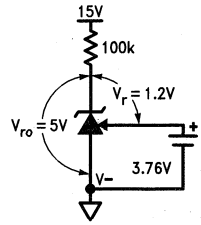
TL/H/9226–31

FIGURE 3. 1.2V Reference

Capacitors in parallel with the reference are allowed. See the Reference AC Stability Range typical curve for capacitance values—from 20 μA to 3 mA any capacitor value is stable. With the reference's wide stability range with resistive and capacitive loads, a wide range of RC filter values will perform noise filtering.

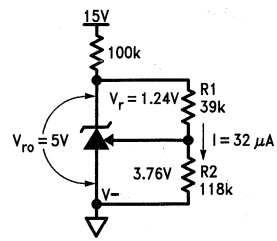
Adjustable Reference

The FEEDBACK pin allows the reference output voltage, V_{ro}, to vary from 1.24V to 6.3V. The reference attempts to hold V_r at 1.24V. If V_r is above 1.24V, the reference will conduct current from Cathode to Anode; FEEDBACK current always remains low. If FEEDBACK is connected to Anode, then $V_{ro} = V_r = 1.24V$. For higher voltages FEEDBACK is held at a constant voltage above Anode—say 3.76V for $V_{ro} = 5V$. Connecting a resistor across the constaint V_r generates a current $I = R1/V_r$ flowing from Cathode into FEEDBACK node. A Thevenin equivalent 3.76V is generated from FEEDBACK to Anode with $R2 = 3.76/I$. Keep I greater than one thousand times larger than FEEDBACK bias current for <0.1% error—$I \geq 32$ μA for the military grade over the military temperature range ($I \geq 5.5$ μA for a 1% untrimmed error for a commercial part).



TL/H/9226–32

FIGURE 4. Thevenin Equivalent of Reference with 5V Output



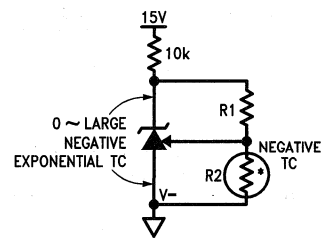
TL/H/9226–33

R1 = Vr/I = 1.24/32μ = 39k

R2 = R1 {(Vro/Vr) − 1} = 39k {(5/1.24) − 1)} = 118k

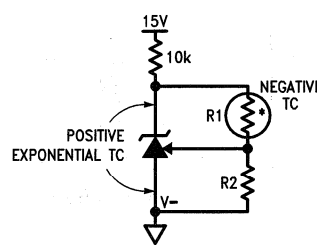
FIGURE 5. Resistors R1 and R2 Program Reference Output Voltage to be 5V

Understanding that V_r is fixed and that voltage sources, resistors, and capacitors may be tied to the FEEDBACK pin, a range of V_r temperature coefficients may be synthesized.



TL/H/9226–34

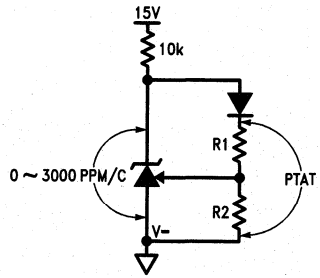
FIGURE 6. Output Voltage has Negative Temperature Coefficient (TC) if R2 has Negative TC



TL/H/9226–35

FIGURE 7. Output Voltage has Positive TC if R1 has Negative TC

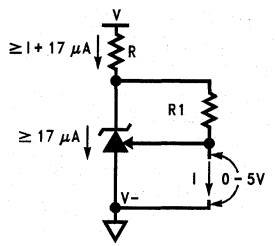
Application Information (Continued)



TL/H/9226–36

FIGURE 8. Diode in Series with R1 Causes Voltage Across R1 and R2 to be Proportional to Absolute Temperature (PTAT)

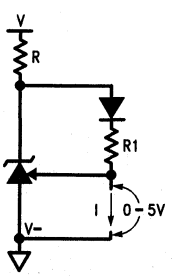
Connecting a resistor across Cathode-to-FEEDBACK creates a 0 TC current source, but a range of TCs may be synthesized.



TL/H/9226–37

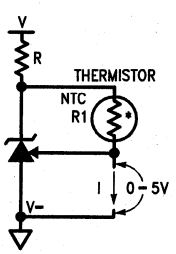
$I = Vr/R1 = 1.24/R1$

FIGURE 9. Current Source is Programmed by R1



TL/H/9226–38

FIGURE 10. Proportional-to-Absolute-Temperature Current Source



TL/H/9226–39

FIGURE 11. Negative-TC Current Source

Reference Hysteresis

The reference voltage depends, slightly, on the thermal history of the die. Competitive micro-power products vary—always check the data sheet for any given device. Do not assume that no specification means no hysteresis.

OPERATIONAL AMPLIFIERS AND COMPARATORS

Any amp, comparator, or the reference may be biased in any way with no effect on the other sections of the LM613, except when a substrate diode conducts (see Electrical Characteristics Note 1). For example, one amp input may be outside the common-mode range, another amp may be operating as a comparator, and all other sections may have all terminals floating with no effect on the others. Tying inverting input to output and non-inverting input to V^- on unused amps is preferred. Unused comparators should have non-inverting input and output tied to V^+, and inverting input tied to V^-. Choosing operating points that cause oscillation, such as driving too large a capacitive load, is best avoided.

Op Amp Output Stage

These op amps, like the LM124 series, have flexible and relatively wide-swing output stages. There are simple rules to optimize output swing, reduce cross-over distortion, and optimize capacitive drive capability:

1) Output Swing: Unloaded, the 42 μA pull-down will bring the output within 300 mV of V^- over the military temperature range. If more than 42 μA is required, a resistor from output to V^- will help. Swing across any load may be improved slightly if the load can be tied to V^+, at the cost of poorer sinking open-loop voltage gain.
2) Cross-Over Distortion: The LM613 has lower cross-over distortion (a 1 V_{BE} deadband versus 3 V_{BE} for the LM124), and increased slew rate as shown in the characteristic curves. A resistor pull-up or pull-down will force class-A operation with only the PNP or NPN output transistor conducting, eliminating cross-over distortion.
3) Capacitive Drive: Limited by the output pole caused by the output resistance driving capacitive loads, a pull-down resistor conducting 1 mA or more reduces the output stage NPN r_e until the output resistance is that of the current limit 25Ω. 200 pF may then be driven without oscillation.

Comparator Output Stage

The comparators, like the LM139 series, have open-collector output stages. A pull-up resistor must be added from each output pin to a positive voltage for the output transistor to switch properly. When the output transistor is OFF, the output voltage will be this external positive voltage.

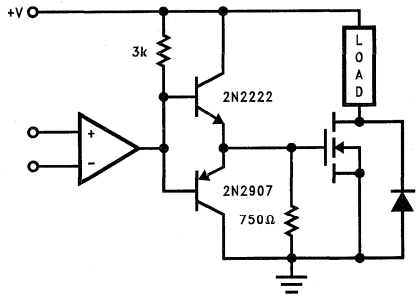
For the output voltage to be under the TTL-low voltage threshold when the output transistor is ON, the output current must be less than 8 mA (over temperature). This impacts the minimum value of pull-up resistor.

The offset voltage may increase when the output voltage is low and the output current is less than 30 μA. Thus, for best accuracy, the pull-up resistor value should be low enough to allow the output transistor to sink more than 30 μA.

Op Amp and Comparator Input Stage

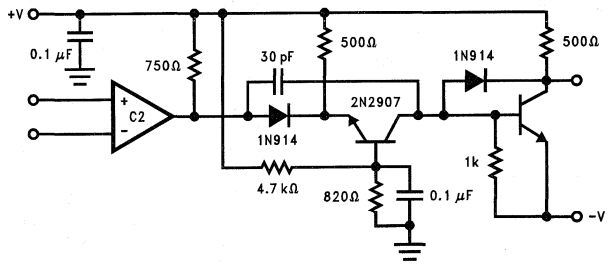
The lateral PNP input transistors, unlike those of most op amps, have BV_{EBO} equal to the absolute maximum supply voltage. Also, they have no diode clamps to the positive supply nor across the inputs. These features make the inputs look like high impedances to input sources producing large differential and common-mode voltages.

Typical Applications



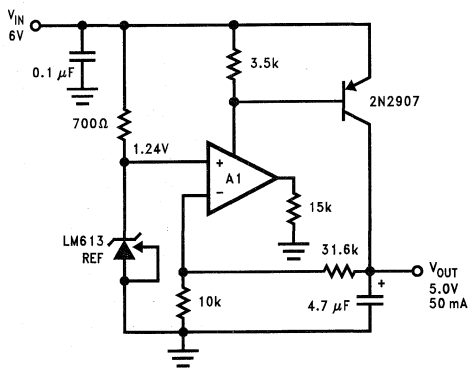
TL/H/9226–40

FIGURE 12. High Current, High Voltage Switch



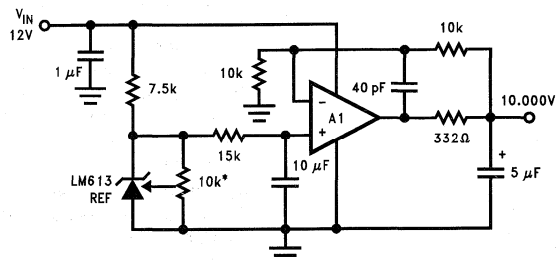
TL/H/9226–41

FIGURE 13. High Speed Level Shifter. Response time is approximately 1.5 μs, where output is either approximately +V or −V.



TL/H/9226–42

FIGURE 14. Low Voltage Regulator. Dropout voltage is approximately 0.2V.

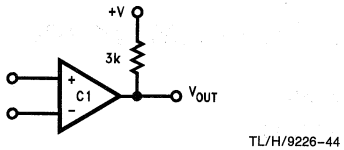


*10k must be low t.c. trimpot

TL/H/9226–43

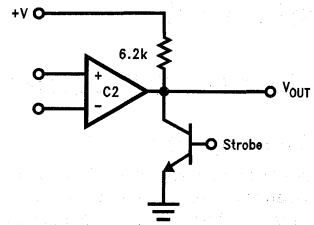
FIGURE 15. Ultra Low Noise, 10.00V Reference. Total output noise is typically 14 μV_{RMS}.

Typical Applications (Continued)



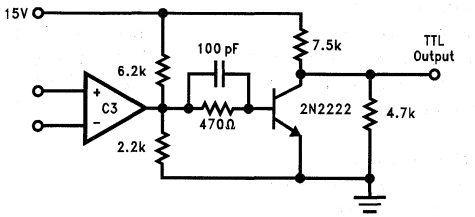
TL/H/9226–44

FIGURE 16. Basic Comparator



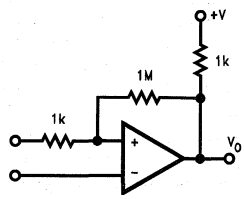
TL/H/9226–45

FIGURE 17. Basic Comparator with External Strobe



TL/H/9226–46

FIGURE 18. Wide-Input Range Comparator with TTL Output



TL/H/9226–47

FIGURE 19. Comparator with Hysteresis ($\Delta V_H = {}^{+}V(1k/1M)$)

National Semiconductor

LM615 Quad Comparator and Adjustable Reference

General Description

The comparators have an input range which extends to the negative supply, and have open-collector outputs. Improved over the LM139 series, the input stages of the comparators have lateral PNP input transistors which enable low input currents for large differential input voltages and swings above V^+.

The voltage reference is a three-terminal shunt-type bandgap, and is referred to the V^- terminal. Two resistors program the reference from 1.24V to 6.3V, with accuracy of ±0.6% available. The reference features operation over a shunt current range of 17 μA to 20 mA, low dynamic impedance, broad capacitive load range, and cathode terminal voltage ranging from a diode-drop below V^- to above V^+.

As a member of National's Super-Block™ family, the LM615 is a space-saving monolithic alternative to a multichip solution, offering a high level of integration without sacrificing performance.

Features

COMPARATORS

■ Low operating current	600 μA
■ Wide supply voltage range	4V to 36V
■ Open-collector outputs	
■ Input common-mode range	V^- to (V^+ − 1.8V)
■ Wide differential input voltage	±36V

REFERENCE

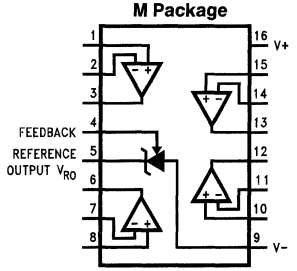
■ Adjustable output voltage	1.24V to 6.3V
■ Tight initial tolerance available	±0.6% (25°C)
■ Wide operating current range	17 μA to 20 mA
■ Tolerant of load capacitance	

Applications

- Adjustable threshold detector
- Time-delay generator
- Voltage window comparator
- Power supply monitor
- RGB level detector

Connection Diagram

M Package



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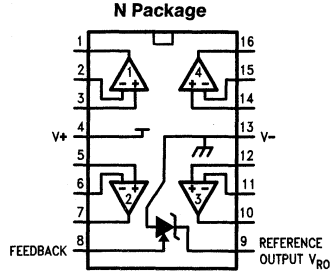
Top View

N Package



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Top View

Ordering Information

For information about surface-mount packaging of this device, please contact the Analog Product Marketing group at National Semiconductor Corp. headquarters.

Reference Tolerances	Temperature Range		Package	NSC Package Number
	Military $-55°C \le T_J \le +125°C$	Industrial $-40°C \le T_J \le +85°C$		
±0.6% at 25°C, 80 ppm/°C max	LM615AMN	LM615AIN	16-Pin Molded DIP	N16A
	LM615AMJ/883 (Note 13)		16-Pin Ceramic DIP	J16A
±2.0% at 25°C, 150 ppm/°C max	LM615MN	LM615IN	16-Pin Molded DIP	N16A
		LM615IM	16-Pin Narrow Surface Mount	M16A

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Voltage on Any Pin Except V_{RO} (referred to V−pin)
(Note 2) 36V (Max)
(Note 3) −0.3V (Min)

Current through Any Input Pin and V_{RO} Pin ±20 mA

Differential Input Voltage ±36V

Output Short-Circuit Duration (Note 4)

Storage Temperature Range $-65°C \le T_J \le +150°C$

Maximum Junction Temperature 150°C

Thermal Resistance, Junction-to-Ambient (Note 5)
N Package 95°C/W

Soldering Information
N Package Soldering (10 seconds) 260°C

ESD Tolerance (Note 6) ±1 kV

Operating Temperature Range

LM615AI, LM615I $-40°C \le T_J \le \pm 85°C$

LM615A, LM615M $-55°C \le T_J \le +125°C$

Electrical Characteristics

These specifications apply for $V^- = GND = 0V$, $V^+ = 5V$, $V_{CM} = V_{OUT} = V^+/2$, $I_R = 100\ \mu A$, FEEDBACK pin shorted to GND, unless otherwise specified. Limits in standard typeface are for $T_J = 25°C$; limits in **boldface type** apply over the **Operating Temperature Range.**

Symbol	Parameter	Conditions	Typical (Note 7)	LM615AM LM615AI Limits (Note 8)	LM615M LM615I Limits (Note 8)	Units
COMPARATORS						
I_S	Total Supply Current	V^+ Current, $R_{LOAD} = \infty$, $3V \le V^+ \le 36V$	250 **350**	550 **600**	600 **650**	μA max μA max
V_{OS}	Offset Voltage over V^+ Range	$4V \le V^+ \le 36V$, $R_L = 15\ k\Omega$	1.0 **2.0**	3.0 **6.0**	5.0 **7.0**	mV max mV max
V_{OS}	Offset Voltage over V_{CM} Range	$0V \le V_{CM} \le (V^+ - 1.8V)$ $V^+ = 30V$, $R_L = 15\ k\Omega$	1.0 **1.5**	3.0 **6.0**	5.0 **7.0**	mV max mV max
$\frac{\Delta V_{OS}}{\Delta T}$	Average Offset Voltage Drift		**15**			μV/°C
I_B	Input Bias Current		−5 **−8**	25 **30**	35 **40**	nA max nA max
I_{OS}	Input Offset Current		0.2 **0.3**	4 **5**	4 **5**	nA max nA max
A_V	Voltage Gain	$R_L = 10\ k\Omega$ to 36V, $2V \le V_{OUT} \le 27V$	500 **100**	50	50	V/mV min V/mV
t_R	Large Signal Response Time	$V_{+IN} = 1.4V$, V_{-IN} = TTL Swing, $R_L = 5.1\ k\Omega$	1.5 **2.0**			μs μs
I_{SINK}	Output Sink Current	$V_{+IN} = 0V$, $V_{-IN} = 1V$, $V_{OUT} = 1.5V$	20 **13**	10 **8**	10 **8**	mA min mA min
		$V_{OUT} = 0.4V$	2.8 **2.4**	1.0 **0.5**	0.8 **0.5**	mA min mA min
I_L	Output Leakage Current	$V_{+IN} = 1V$, $V_{-IN} = 0V$, $V_{OUT} = 36V$	0.1 **0.2**	10	10	μA max μA

Electrical Characteristics

These specifications apply for V^- = GND = 0V, V^+ = 5V, V_{CM} = V_{OUT} = $V^+/2$, I_R = 100 μA, FEEDBACK pin shorted to GND, unless otherwise specified. Limits in standard typeface are for T_J = 25°C; limits in **boldface type** apply over the **Operating Temperature Range.** (Continued)

Symbol	Parameter	Conditions	Typical (Note 7)	LM615AM LM615AI Limits (Note 8)	LM615M LM615I Limits (Note 8)	Units
VOLTAGE REFERENCE (Note 9)						
V_R	Reference Voltage		1.244	1.2365 1.2515 (±0.6%)	1.2191 1.2689 (±2%)	V min V max
$\frac{\Delta V_R}{\Delta T}$	Average Drift with Temperature	(Note 10)	**18**	**80**	**150**	ppm/°C max
$\frac{\Delta V_R}{kH}$	Average Drift with Time	T_J = 40°C T_J = 150°C	400 1000			ppm/kH ppm/kH
$\frac{\Delta V_R}{\Delta T_J}$	Hysteresis	(Note 11)	**3.2**			μV/°C
$\frac{\Delta V_R}{\Delta I_R}$	V_R Change with Current	$V_{R[100\ \mu A]} - V_{R[17\ \mu A]}$	0.05 **0.1**	1 **1.1**	1 **1.1**	mV max mV max
		$V_{R[10\ mA]} - V_{R[100\ \mu A]}$ (Note 12)	1.5 **2.0**	5 **5.5**	5 **5.5**	mV max mV max
R	Resistance	$\Delta V_{R[10\ mA\ to\ 0.1\ mA]}/9.9\ mA$ $\Delta V_{R[100\ \mu A\ to\ 17\ \mu A]}/83\ \mu A$	0.2 0.6	**0.56** **13**	**0.56** **13**	Ω max Ω max
$\frac{\Delta V_R}{\Delta V_{RO}}$	V_R Change with V_{RO}	$V_{R[V_{RO} = V_R]} - V_{R[V_{RO} = 6.3V]}$	2.5 **2.8**	5 **10**	5 **10**	mV max mV max
$\frac{\Delta V_R}{\Delta V^+}$	V_R Change with V^+ Change	$V_{R[V+ = 5V]} - V_{R[V+ = 36V]}$	0.1 **0.1**	1.2 **1.3**	1.2 **1.3**	mV max mV max
		$V_{R[V+ = 5V]} - V_{R[V+ = 3V]}$	0.01 **0.01**	1 **1.5**	1 **1.5**	mV max mV max
I_{FB}	FEEDBACK Bias Current	$V^- \le V_{FB} \le 5.06V$	22 **29**	35 **40**	50 **55**	nA max nA max
e_n	Voltage Noise	BW = 10 Hz to 10 kHz	30			μV_{RMS}

Note 1: Absolute maximum ratings indicate limits beyond which damage to the component may occur. Electrical specifications do not apply when operating the device beyond its rated operating conditions.

Note 2: Input voltage above V^+ is allowed. As long as one input pin voltage remains inside the common-mode range, the comparator will deliver the correct output.

Note 3: More accurately, it is excessive current flow, with resulting excess heating, that limits the voltages on all pins. When any pin is pulled a diode drop below V^-, a parasitic NPN transistor turns ON. No latch-up will occur as long as the current through that pin remains below the Maximum Rating. Operation is undefined and unpredictable when any parasitic diode or transistor is conducting.

Note 4: Shorting an Output to V^- will not cause power dissipation, so it may be continuous. However, shorting an Output to any more positive voltage (including V^+), will cause 80 mA (typ.) to be drawn through the output transistor. This current multiplied by the applied voltage is the power dissipation in the output transistor. If the total power from all shorted outputs causes the junction temperature to exceed 150°C, degraded reliability or destruction of the device may occur. To determine junction temperature, see Note 5.

Note 5: Junction temperature may be calculated using $T_J = T_A + P_D\ \theta_{JA}$. The given thermal resistance is worst-case for packages in sockets in still air. For packages soldered to copper-clad board with dissipation from one comparator or reference output transistor, nominal θ_{JA} is 80 °C/W for the N package.

Note 6: Human body model, 100 pF discharge through a 1.5 kΩ resistor.

Note 7: Typical values in standard typeface are for T_J = 25°C; values in **boldface type** apply for the full operating temperature range. These values represent the most likely parametric norm.

Note 8: All limits are guaranteed for T_J = +25°C (standard type face) or over the full operating temperature range **(bold type face)**.

Note 9: V_{RO} is the reference output voltage, which may be set for 1.2V to 6.3V (see Application Information). V_R is the V_{RO}-to-FEEDBACK voltage (nominally 1.244V).

Note 10: Average reference drift is calculated from the measurement of the reference voltage at 25°C and at the temperature extremes. The drift, in ppm/°C, is $10^6 \cdot \Delta V_R/V_{R[25°C]} \cdot \Delta T_J$, where ΔV_R is the lowest value subtracted from the highest, $V_{R[25°C]}$ is the value at 25°C, and ΔT_J is the temperature range. This parameter is guaranteed by design and sample testing.

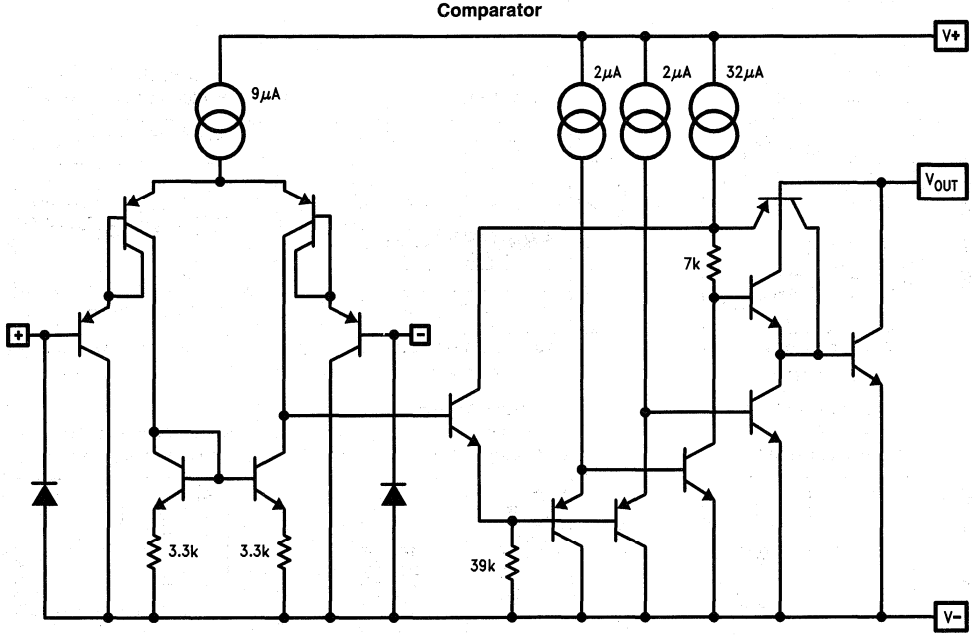
Note 11: Hysteresis is the change in V_{RO} caused by a change in T_J, after the reference has been "dehysterized." To dehysterize the reference; that is minimize the hysteresis to the typical value, its junction temperature should be cycled in the following pattern, spiraling in toward 25°C: 25°C, 85°C, −40°C, 70°C, 0°C, 25°C.

Note 12: Low contact resistance is required for accurate measurement.

Note 13: A military RETS electrical test specification is available on request. The LM615AMJ/883 may also be procured as a Standard Military Drawing.

Simplified Schematic Diagrams

Comparator



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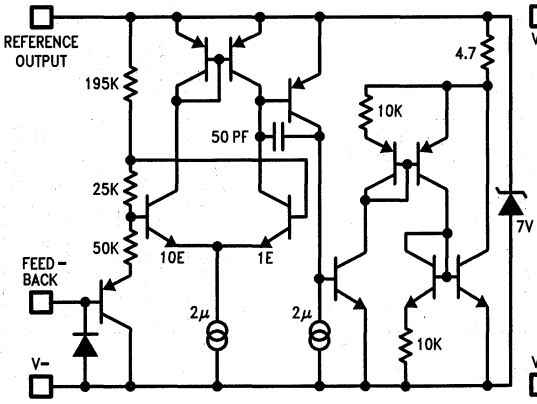
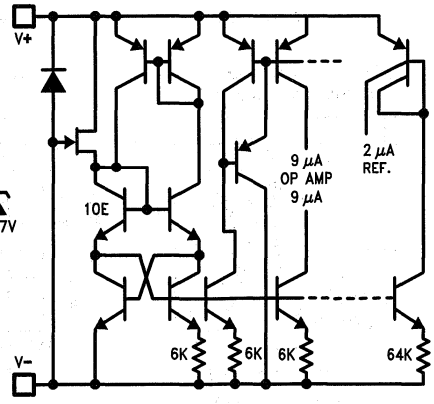
Reference



Bias



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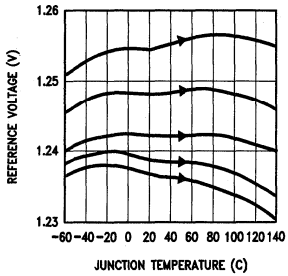
3

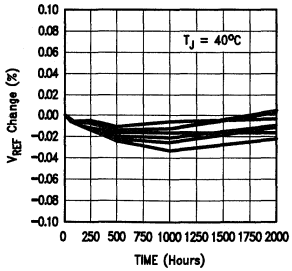
Typical Performance Characteristics (Reference)

T_J = 25°C, FEEDBACK pin shorted to V^- = 0V, unless otherwise noted.

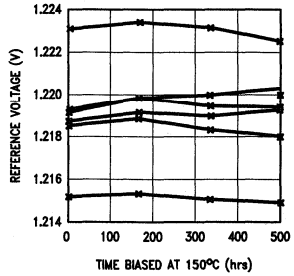
Reference Voltage vs Temperature



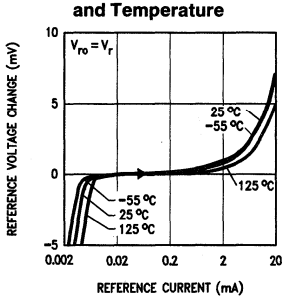
Reference Voltage Drift vs Time



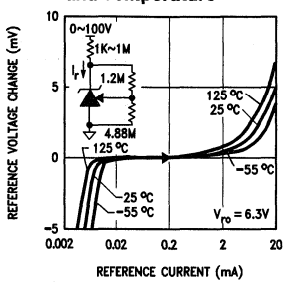
Accelerated Reference Voltage Drift vs Time



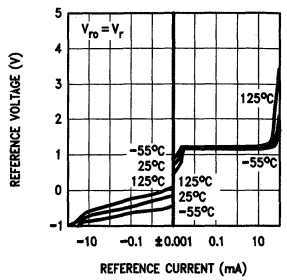
Reference Voltage vs Current and Temperature



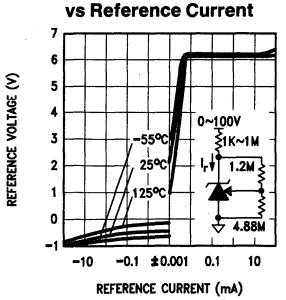
Reference Voltage vs Current and Temperature



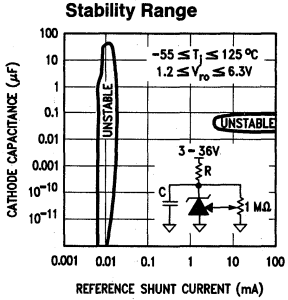
Reference Voltage vs Reference Current



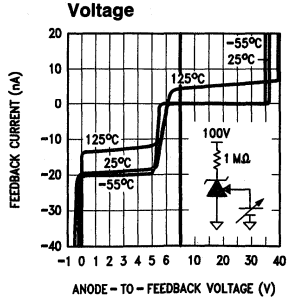
Reference Voltage vs Reference Current



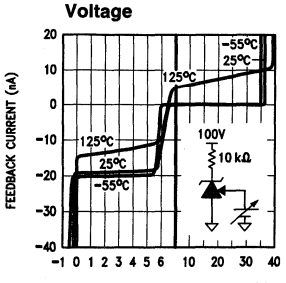
Reference AC Stability Range



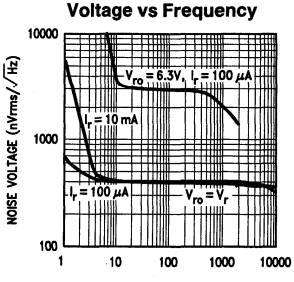
FEEDBACK Current vs FEEDBACK-to-V^- Voltage



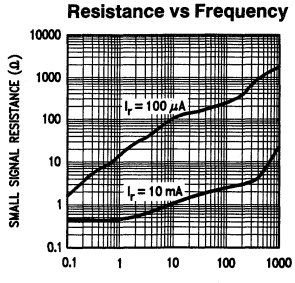
FEEDBACK Current vs FEEDBACK-to-V^- Voltage



Reference Noise Voltage vs Frequency



Reference Small-Signal Resistance vs Frequency



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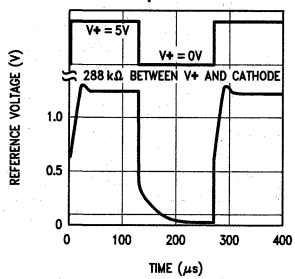
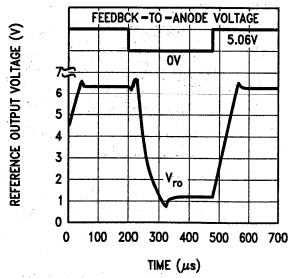
Typical Performance Characteristics (Reference) (Continued)

T_J = 25°C, FEEDBACK pin shorted to V^- = 0V, unless otherwise noted.

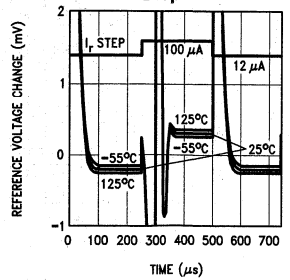
Reference Power-Up Time



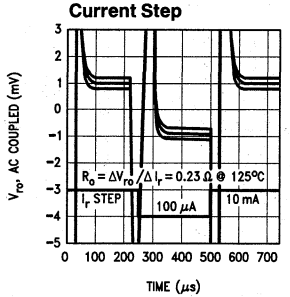
Reference Voltage with FEEDBACK Voltage Step



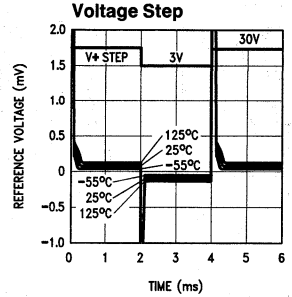
Reference Voltage with 100 ~ 12 μA Current Step



Reference Step Response for 100 μ ~ 10 mA Current Step



Reference Voltage Change with Supply Voltage Step



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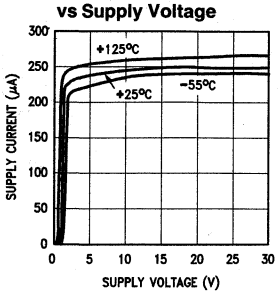
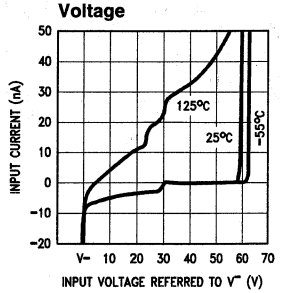
Typical Performance Characteristics (Comparators)

T_J = 25°C, V^+ = 5V, V^- = 0V, unless otherwise noted

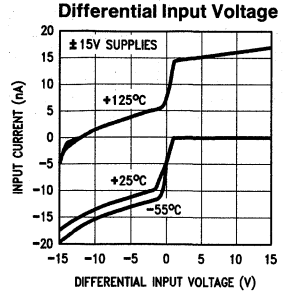
Supply Current vs Supply Voltage



Input-Bias Current vs Common-Mode Voltage



Input Current vs Differential Input Voltage



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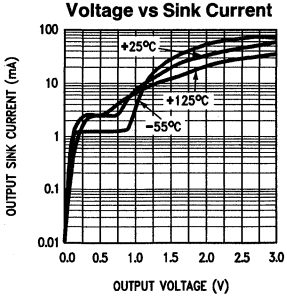
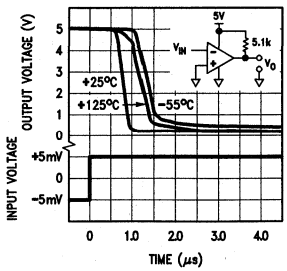
Typical Performance Characteristics (Comparators) (Continued)

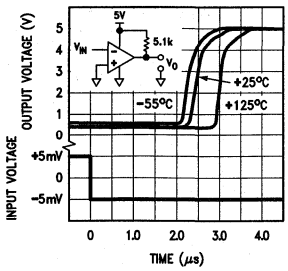
Output Saturation Voltage vs Sink Current



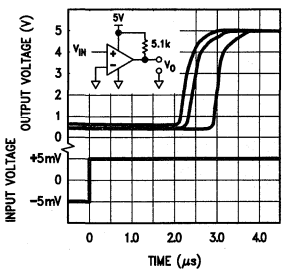
Small-Signal Response Times—Inverting Input, Negative Transition



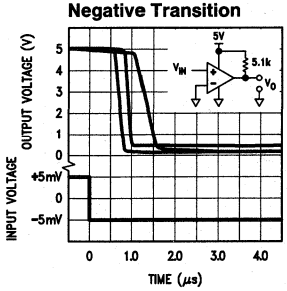
Small-Signal Response Times—Inverting Input, Positive Transition



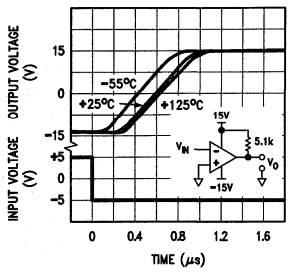
Small-Signal Response Times Non-Inverting Input, Positive Transition



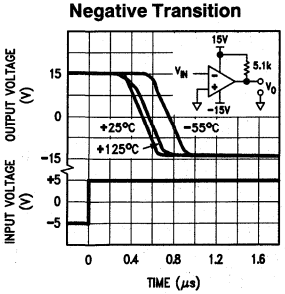
Small-Signal Response Times—Non-Inverting Input, Negative Transition



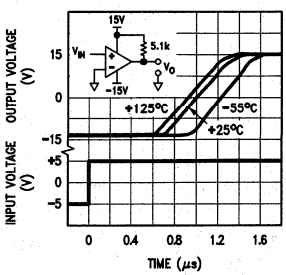
Large-Signal Response Times—Inverting Input, Positive Transition



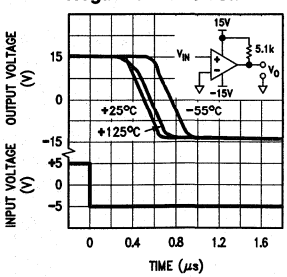
Large-Signal Response Times-Inverting Input, Negative Transition



Large-Signal Response Times—Non-Inverting Input, Positive Transition



Large-Signal Response Times—Non-Inverting Input, Negative Transition



TL/H/11057–8

Application Information

VOLTAGE REFERENCE

Reference Biasing

The voltage reference is of a shunt regulator topology that models as a simple zener diode. With current I_r flowing in the "forward" direction there is the familiar diode transfer function. I_r flowing in the reverse direction forces the reference voltage to be developed from cathode to anode. The cathode may swing from a diode drop below V^- to the reference voltage or to the avalanche voltage of the parallel protection diode, nominally 7V. A 6.3V reference with V^+ = 3V is allowed.

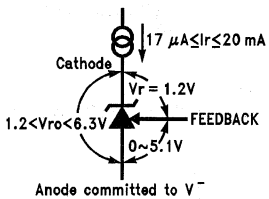


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FIGURE 1. Voltage Associated with Reference (Current Source I_r is External)

The reference equivalent circuit reveals how V_r is held at the constant 1.2V by feedback, and how the FEEDBACK pin passes little current.

To generate the required reverse current, typically a resistor is connected from a supply voltage higher than the reference voltage. Varying that voltage, and so varying I_r, has small effect with the equivalent series resistance of less than an ohm at the higher currents. Alternatively, an active current source, such as the LM134 series, may generate I_r.

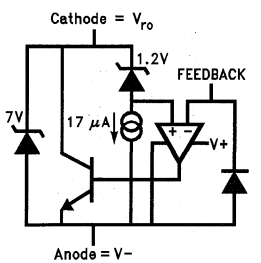

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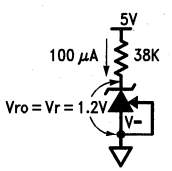
FIGURE 2. Reference Equivalent Circuit



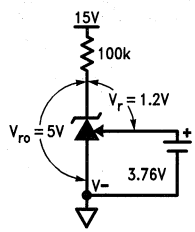
TL/H/11057–11

FIGURE 3. 1.2V Reference

Capacitors in parallel with the reference are allowed. See the Reference AC Stability Range typical curve for capacitance values—from 20 μA to 3 mA any capacitor value is stable. With the reference's wide stability range with resistive and capacitive loads, a wide range of RC filter values will perform noise filtering.

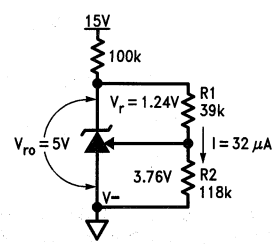
Adjustable Reference

The FEEDBACK pin allows the reference output voltage, V_{ro}, to vary from 1.24V to 6.3V. The reference attempts to hold V_r at 1.24V. If V_r is above 1.24V, the reference will conduct current from Cathode to Anode; FEEDBACK current always remains low. If FEEDBACK is connected to Anode, then V_{ro} = V_r = 1.24V. For higher voltages FEEDBACK is held at a constant voltage above Anode—say 3.76V for V_{ro} = 5V. Connecting a resistor across the constant V_r generates a current I = $R1/V_r$ flowing from Cathode into FEEDBACK node. A Thevenin equivalent 3.76V is generated from FEEDBACK to Anode with R2 = 3.76/I. Keep I greater than one thousand times larger than FEEDBACK bias current for <0.1% error—I ≥ 32 μA for the military grade over the military temperature range (I ≥ 5.5 μA for a 1% untrimmed error for an industrial temperature range part).



TL/H/11057–12

FIGURE 4. Thevenin Equivalent of Reference with 5V Output



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R1 = V_r/I = 1.24/32μ = 39k
R2 = R1 [(V_{ro}/V_r) − 1] = 39k [(5/1.24) − 1] = 118k

FIGURE 5. Resistors R1 and R2 Program Reference Output Voltage to be 5V

Application Information (Continued)

Understanding that V_r is fixed and that voltage sources, resistors, and capacitors may be tied to the FEEDBACK pin, a range of V_r temperature coefficients may be synthesized.

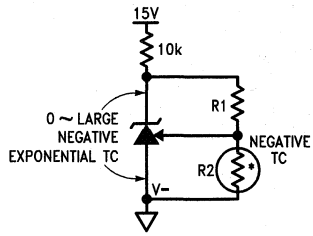

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FIGURE 6. Output Voltage has Negative Temperature Coefficient (TC) if R2 has Negative TC

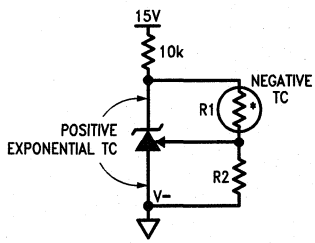

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FIGURE 7. Output Voltage has Positive TC if R1 has Negative TC

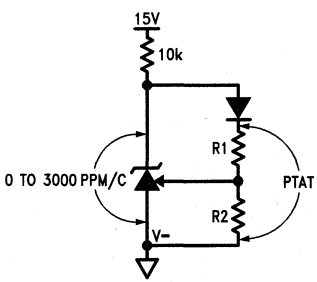

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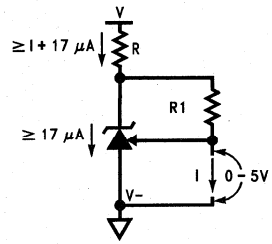
FIGURE 8. Diode in Series with R1 Causes Voltage Across R1 and R2 to be Proportional to Absolute Temperature (PTAT)

Connecting a resistor across V_{RO}-to-FEEDBACK creates a 0 TC current source, but a range of TCs may be synthesized.



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$I = V_r/R1 = 1.24/R1$

FIGURE 9. Current Source is Programmed by R1

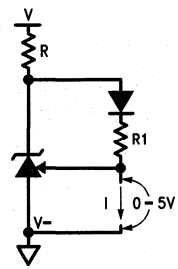

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FIGURE 10. Proportional-to-Absolute-Temperature Current Source

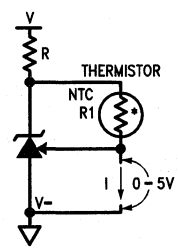

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FIGURE 11. Negative-TC Current Source

Reference Hysteresis

The reference voltage depends, slightly, on the thermal history of the die. Competitive micro-power products vary—always check the data sheet for any given device. Do not assume that no specification means no hysteresis.

Application Information (Continued)

COMPARATORS

Any of the comparators or the reference may be biased in any way with no effect on the other sections of the LM615, except when a substrate diode conducts (see Electrical Characteristics Note 3). For example, one or both inputs of one comparator may be outside the input voltage range limits, the reference may be unpowered, and the other comparators will still operate correctly. Unused comparators should have inverting input and output tied to V^-, and non-inverting input tied to V^+.

Hysteresis

Any comparator may oscillate or produce a noisy output if the applied differential input voltage is near the comparator's offset voltage. This usually happens when the input signal is moving very slowly across the comparator's switching threshold. This problem can be prevented by the addition of hysteresis, or positive feedback, as shown in *Figure 12*.

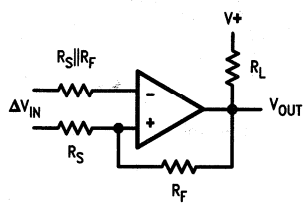

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FIGURE 12. R_S and R_F Add Hysteresis to Comparator

The amount of hysteresis added in *Figure 12* is

$$V_H = V^+ \times \frac{R_S}{(R_F + R_S)}$$

$$\approx V^+ \times \frac{R_S}{R_F} \quad \text{for } R_F \gg R_S$$

A good rule of thumb is to add hysteresis of at least the maximum specified offset voltage. More than about 50 mV of hysteresis can substantially reduce the accuracy of the comparator, since the offset voltage is effectively being increased by the hysteresis when the comparator output is high.

It is often a good idea to decrease the amount of hysteresis until oscillations are observed, then use three times that minimum hysteresis in the final circuit. Note that the amount of hysteresis needed is greatly affected by layout. The amount of hysteresis should be rechecked each time the layout is changed, such as changing from a breadboard to a P.C. board.

Input Stage

The input stage uses lateral PNP input transistors which, unlike those of many op amps, have breakdown voltage BV_{EBO} equal to the absolute maximum supply voltage. Also, they have no diode clamps to the positive supply nor across the inputs. These features make the inputs look like high impedances to input sources producing large differential and common-mode voltages.

The guaranteed common-mode input voltage range for an LM615 is $V^- \leq V_{CM} \leq (V^+ - 1.8V)$, over temperature. This is the voltage range in which the comparisons must be made. If both inputs are within this range, the output will be at the correct state. If one input is within this range, and the other input is less than $(V^- + 32V)$, even if this is greater than V^+, the output will be at the correct state. If, however, either or both inputs are driven below V^-, and either input current exceeds 10 μA, the output state is not guaranteed to be correct. If both inputs are above $(V^+ - 1.8V)$, the output state is also not guaranteed to be correct.

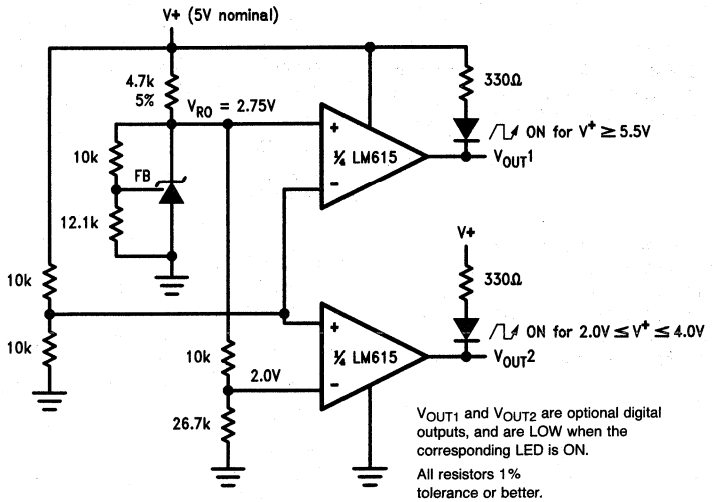
Output Stage

The comparators have open-collector output stages which require a pull-up resistor from each output pin to a positive supply voltage of the output to switch properly. When the internal output transistor is off, the output (HIGH) voltage will be pulled up to this external positive voltage.

To ensure that the LOW output voltage is under the TTL-low threshold, the output transistor's load current must be less than 0.8 mA (over temperature) when it turns on. This impacts the minimum value of the pull-up resistor.

Typical Applications

Power Supply Monitor



V_{OUT1} and V_{OUT2} are optional digital outputs, and are LOW when the corresponding LED is ON.

All resistors 1% tolerance or better.

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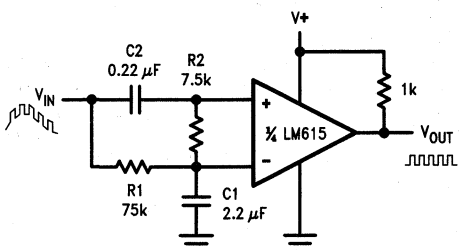
Tracking Comparator



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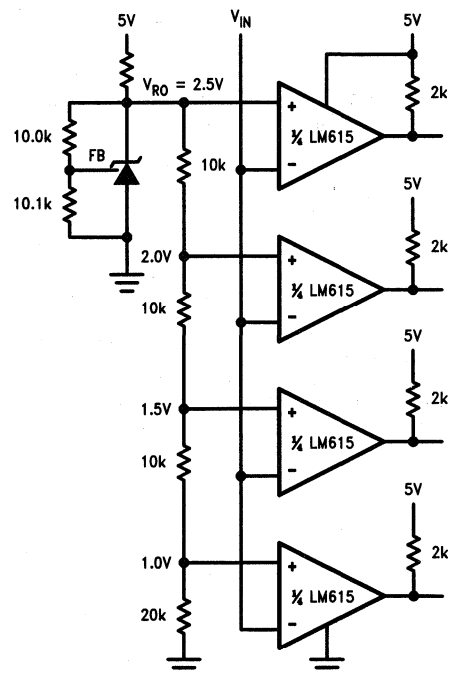
R1–C1 removes the low-frequency signal component, so that through R2–C2 the higher-frequency component is detected.

4-Threshold Level Detector



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National Semiconductor

LM710 Voltage Comparator

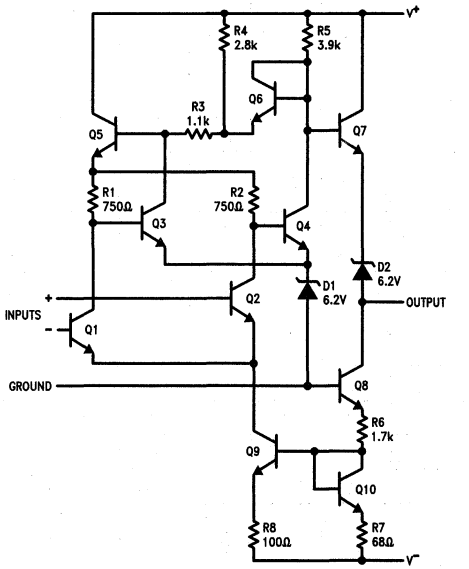
General Description

The LM710 series are high-speed voltage comparators intended for use as an accurate, low-level digital level sensor or as a replacement for operational amplifiers in comparator applications where speed is of prime importance. The circuit has a differential input and a single-ended output, with saturated output levels compatible with practically all types of integrated logic.

The device is built on a single silicon chip which insures low offset and thermal drift. The use of a minimum number of stages along with minority-carrier lifetime control (gold doping) makes the circuit much faster than operational amplifiers in saturating comparator applications. In fact, the low stray and wiring capacitances that can be realized with monolithic construction make the device difficult to duplicate with discrete components operating at equivalent power levels.

The LM710 series are useful as pulse height discriminators, voltage comparators in high-speed A/D converters or go, no-go detectors in automatic test equipment. They also have applications in digital systems as an adjustable-threshold line receiver or an interface between logic types. In addition, the low cost of the units suggests them for applications replacing relatively simple discrete component circuitry.

Schematic and Connection Diagrams



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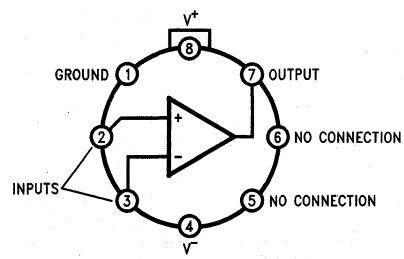
Metal Can Package



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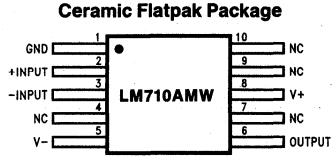
Top View

Note: Pin 4 is connected to case.

Order Number LM710AMH/883*, LM710H, LM710H/883 or LM710CH
See NS Package Number H08C

Ceramic Flatpak Package



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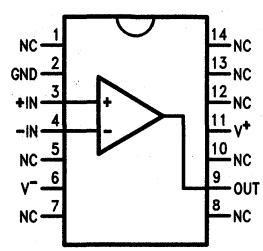
Order Number LM710AMW/883*
See NS Package Number W10A

Dual-In-Line Package



TL/H/10410–3

Top View

Order Number LM710AMJ/883* or LM710CN
See NS Package Number N14A or J14A

*Also available per JM38510/10301

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Positive Supply Voltage	+14V
Negative Supply Voltage	−7V
Peak Output Current	10 mA
Output Short Circuit Duration	10 seconds
Differential Input Voltage	±5V
Input Voltage	±7V

Power Dissipation	
TO-99 (Note 1)	700 mW
Plastic Dual-In-Line Package (Note 2)	950 mW
Operating Temperature Range	
LM710	−55°C to +125°C
LM710C	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec.)	260°C

Electrical Characteristics (Note 3)

Parameter	Conditions	LM710			LM710C			Units
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	$R_S \leq 200\Omega$, $V_{CM} = 0V$, $T_A = 25°C$		0.6	2.0		1.6	5.0	mV
Input Offset Current	$V_{OUT} = 1.4V$, $T_A = 25°C$		0.75	3.0		1.8	5.0	μA
Input Bias Current	$T_A = 25°C$		13	20		16	25	μA
Voltage Gain	$T_A = 25°C$	1250	1700		1000	1500		
Output Resistance	$T_A = 25°C$		200			200		Ω
Output Sink Current	$V_{OUT} = 0$, $T_A = 25°C$ $\Delta V_{IN} \geq 5$ mV $\Delta V_{IN} \geq 10$ mV	2.0	2.5		 1.6	 2.5		 mA mA
Response Time	$T_A = 25°C$ (Note 4)		40			40		ns
Input Offset Voltage	$R_S \leq 200\Omega$, $V_{CM} = 0V$			3.0			6.5	mV
Average Temperature Coefficient of Input Offset Voltage	$T_{MIN} \leq T_A \leq T_{MAX}$ $R_S \leq 50\Omega$		3.0	10		5.0	20	μV/°C
Input Offset Current	$T_A = T_{A\,MAX}$ $T_A = T_{A\,MIN}$		0.25 1.8	3.0 7.0			7.5 7.5	μA μA
Average Temperature Coefficient of Input Offset Current	$25°C \leq T_A \leq T_{MAX}$ $T_{MIN} \leq T_A \leq 25°C$		5.0 15	25 75		15 24	50 100	nA/°C nA/°C
Input Bias Current	$T_A = T_{MIN}$		27	45		25	40	μA
Input Voltage Range	$V^- = -7V$	±5.0			±5.0			V
Common-Mode Rejection Ratio	$R_S \leq 200\Omega$	80	100		70	98		dB
Differential Input Voltage Range		±5.0			±5.0			V
Voltage Gain		1000			800			V/V
Positive Output Level	-5 mA $\leq I_{OUT} \leq 0$ $V_{IN} \geq 5$ mV $V_{IN} \geq 10$ mV	2.5	3.2	4.0	 2.5	 3.2	 4.0	 V V
Negative Output Level	$V_{IN} \geq 5$ mV $V_{IN} \geq 10$ mV	−1.0	−0.5	0	 −1.0	 −0.5	 0	V V
Output Sink Current	$V_{IN} \geq 5$ mV, $V_{OUT} = 0$ $T_A = 125°C$ $T_A = -55°C$	 0.5 1.0	 1.7 2.3					 mA mA
	$V_{IN} \geq 10$ mV, $V_{OUT} = 0$ $0°C \leq T_A \leq +70°C$				0.5			mA

Electrical Characteristics (Note 3) (Continued)

Parameter	Conditions	LM710			LM710C			Units
		Min	Typ	Max	Min	Typ	Max	
Positive Supply Current	$V_{IN} \geq 5$ mV		5.2	9.0				mA
	$V_{IN} \geq 10$ mV					5.2	9.0	mA
Negative Supply Current	$V_{IN} \geq 5$ mV		4.6	7.0				mA
	$V_{IN} \geq 10$ mV					4.6	7.0	mA
Power Consumption	$I_{OUT} = 0$							
	$V_{IN} \geq 5$ mV		90	150				mW
	$V_{IN} \geq 10$ mV						150	mW

Note 1: Rating applies for ambient temperatures of 25°C; derate linearly at 5.6 mW/°C for ambient temperatures above 25°C.

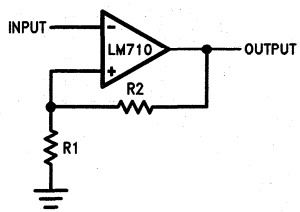
Note 2: Derate linearly at 9.5 mW/°C for ambient temperatures above 25°C.

Note 3: These specifications appy for $V^+ = 12V$, $V^- = -6V$, $-55°C \leq T_A \leq +125°C$ for LM710 and $0°C \leq T_A \leq +70°C$ for LM710C unless otherwise specified: The input offset voltage and input offset current (see definitions) are specified for a logic threshold voltage of 1.8V at −55°C, 1.4V at 25°C, and 1V at 125°C for LM710 and 1.5V at 0°C, 1.4V at 25°C, and 1.2V at 70°C for LM710C.

Note 4: The response time specified (see definitions) is for a 100 mV input step with 5 mV overdrive (LM710) or a 10 mV overdrive (LM710C).

Typical Applications

Schmitt Trigger



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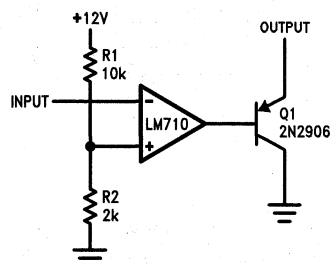
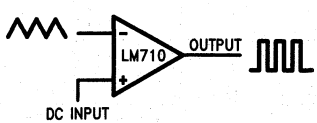
Line Receive with Increased Output Sink Current



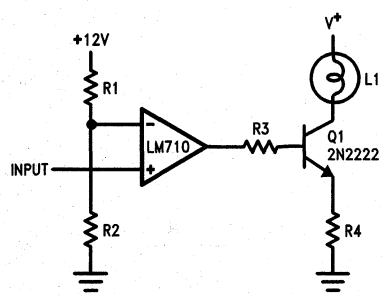
TL/H/10410–5

Pulse Width Modulator



TL/H/10410–6

Level Detector with Lamp Driver



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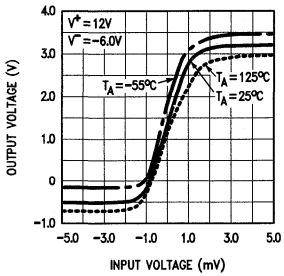
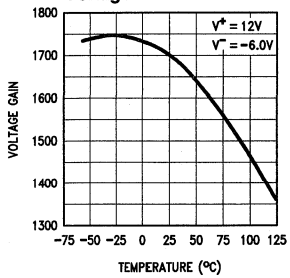
Typical Performance Characteristics

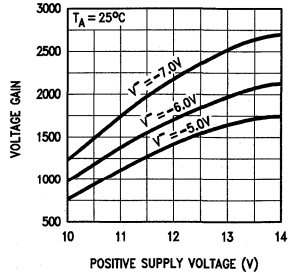
Transfer Function



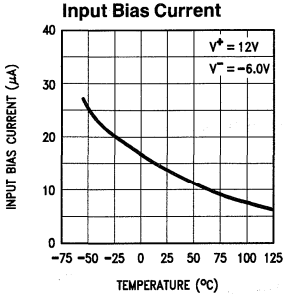
Voltage Gain



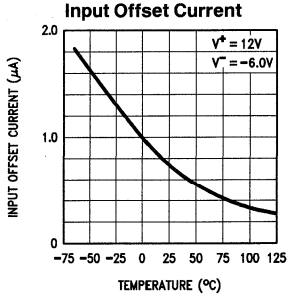
Voltage Gain



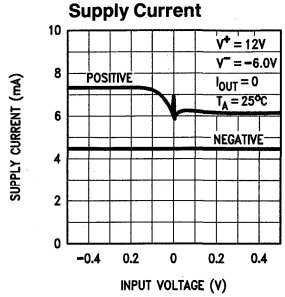
Input Bias Current



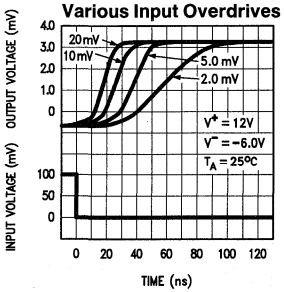
Input Offset Current



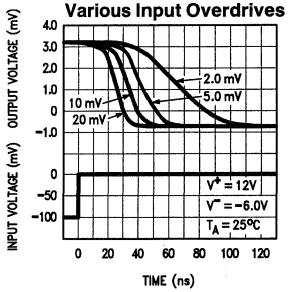
Supply Current



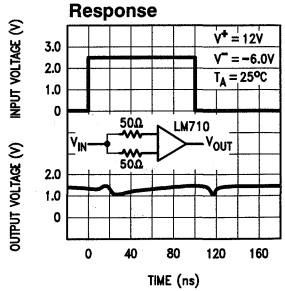
Response Time for Various Input Overdrives



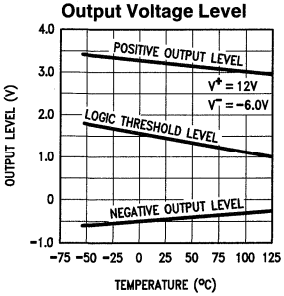
Response Time for Various Input Overdrives



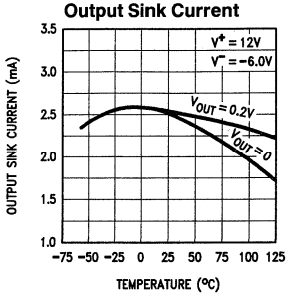
Common Mode Pulse Response



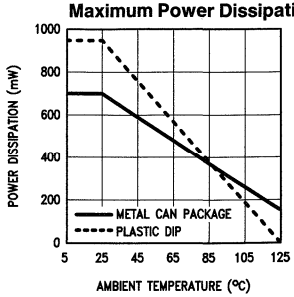
Output Voltage Level



Output Sink Current



Maximum Power Dissipation



TL/H/10410–8

National Semiconductor

LM760
High Speed Differential Comparator

General Description

The LM760 is a differential voltage comparator offering considerable speed improvement over the LM710 family and operates from symmetric supplies of ±4.5V to ±6.5V. The LM760 can be used in high speed analog-to-digital conversion systems and as a zero crossing detector in disc file and tape amplifiers. The LM760 output features balanced rise and fall times for minimum skew and close matching between the complementary outputs. The outputs are TTL compatible with a minimum sink capability of two gate loads.

Features

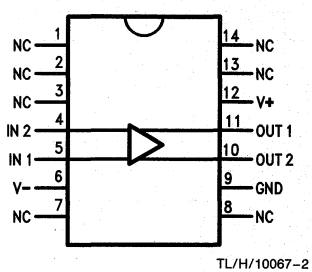
- Guaranteed high speed— 25 ns response time
- Guaranteed delay matching on both outputs
- Complementary TTL compatible outputs
- High sensitivity
- Standard supply voltages

Applications

- High speed A-to-D
- Peak or zero detector

Connection Diagrams

14-Lead DIP



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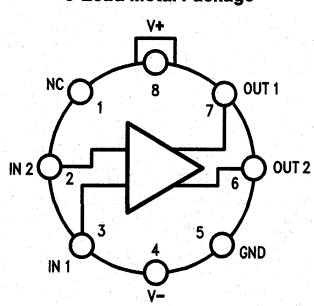
Top View

8-Lead Metal Package



Lead 4 connected to case

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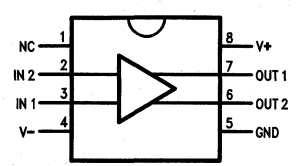
Top View

8-Lead DIP



TL/H/10067–3

Top View

Ordering Information

Temperature Range		Package Type	NSC Package Drawing
Military −55°C to +125°C	**Commercial 0°C to +70°C**		
LM760J-14	LM760CJ-14	14-lead Ceramic DIP	J14A
LM760J	LM760CJ	8-lead Ceramic DIP	J08A
LM760H	LM760CH	8-lead Metal Can	H08A
	LM760CN	8-lead Plastic DIP	N08E

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature Range
- Metal Can and Ceramic DIP: −65°C to +175°C
- Molded DIP: −65°C to +150°C

Operating Temperature Range
- Military (LM760): −55°C to +125°C
- Commercial (LM760C): 0°C to +70°C

Lead Temperature
- Metal Can and Ceramic DIP (Soldering, 60 sec.): 300°C
- Molded DIP (Soldering, 10 sec.): 265°C

Internal Power Dissipation (Notes 1, 2)
- 8L-Metal Can: 1.00W
- 14L-Ceramic DIP: 1.36W
- 8L-Ceramic DIP: 1.30W

Positive Supply Voltage: +8.0V

Negative Supply Voltage: −8.0V

Peak Output Current: 10 mA

Differential Input Voltage: ±5.0V

Input Voltage: $V^+ \geq V_I \geq V^-$

ESD Susceptibility: TBD

LM760
Electrical Characteristics

V_{CC} = ±4.5V to ±6.5V, T_A = −55°C to +125°C, T_A = 25°C for typical figures, unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IO}	Input Offset Voltage	$R_S \leq 200\Omega$		1.0	6.0	mV
I_{IO}	Input Offset Current			0.5	7.5	μA
I_{IB}	Input Bias Current			8.0	60	μA
R_O	Output Resistance (Either Output)	$V_O = V_{OH}$		100		Ω
t_{PD}	Response Time	T_A = 25°C (Note 3)		18	30	ns
		T_A = 25°C (Note 4)			25	
		(Note 5)		16		
Δt_{PD}	Response Time Difference between Outputs (Note 1) (t_{PD} of $+V_{I1}$) − (t_{PD} of $-V_{I2}$)	T_A = 25°C			5.0	ns
	(t_{PD} of $+V_{I2}$) − (t_{PD} of $-V_{I1}$)	T_A = 25°C			5.0	
	(t_{PD} of $+V_{I1}$) − (t_{PD} of $+V_{I2}$)	T_A = 25°C			7.5	
	(t_{PD} of $-V_{I1}$) − (t_{PD} of $-V_{I2}$)	T_A = 25°C			7.5	
R_I	Input Resistance	f = 1.0 MHz		12		kΩ
C_I	Input Capacitance	f = 1.0 MHz		8.0		pF
$\Delta V_{IO}/\Delta T$	Average Temperature Coefficient of Input Offset Voltage	R_S = 50Ω, T_A = −55°C to +125°C		3.0		μV/°C
$\Delta I_{IO}/\Delta T$	Average Temperature Coefficient of Input Offset Current	T_A = +25°C to +125°C		2.0		nA/°C
		T_A = +25°C to −55°C		7.0		
V_{IR}	Input Voltage Range	V_{CC} = ±6.5V	±4.0	±4.5		V
V_{IDR}	Differential Input Voltage Range			±5.0		V
V_{OH}	Output Voltage HIGH (Either Output)	0 mA ≤ I_{OH} ≤ 5.0 mA, V_{CC} = +5.0V	2.4	3.2		V
		I_{OH} = 80 μA, V_{CC} = ±4.5V	2.4	3.0		
V_{OL}	Output Voltage LOW (Either Output)	I_{OL} = 3.2 mA		0.25	0.4	V
I^+	Positive Supply Current	V_{CC} = ±6.5V		18	32	mA
I^-	Negative Supply Current	V_{CC} = ±6.5V		9.0	16	mA

LM760C
Electrical Characteristics

V_{CC} = ±4.5V to ±6.5V, T_A = 0°C to +70°C, T_A = 25°C for typical figures, unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IO}	Input Offset Voltage	$R_S \leq 200\Omega$		1.0	6.0	mV
I_{IO}	Input Offset Current			0.5	7.5	μA
I_{IB}	Input Bias Current			8.0	60	μA
R_O	Output Resistance (Either Output)	$V_O = V_{OH}$		100		Ω
t_{PD}	Response Time	T_A = 25°C (Note 3)		18	30	ns
		T_A = 25°C (Note 4)			25	
		(Note 5)		16		
Δt_{PD}	Response Time Difference between Outputs (Note 1) (t_{PD} of $+V_{I1}$) − (t_{PD} of $-V_{I2}$)	T_A = 25°C			5.0	ns
	(t_{PD} of $+V_{I2}$) − (t_{PD} of $-V_{I1}$)	T_A = 25°C			5.0	
	(t_{PD} of $+V_{I1}$) − (t_{PD} of $+V_{I2}$)	T_A = 25°C			10	
	(t_{PD} of $-V_{I1}$) − (t_{PD} of $-V_{I2}$)	T_A = 25°C			10	
R_I	Input Resistance	f = 1.0 MHz		12		kΩ
C_I	Input Capacitance	f = 1.0 MHz		8.0		pF
$\Delta V_{IO}/\Delta T$	Average Temperature Coefficient of Input Offset Voltage	R_S = 50Ω, T_A = 0°C to +70°C		3.0		μV/°C
$\Delta I_{IO}/\Delta T$	Average Temperature Coefficient of Input Offset Current	T_A = +25°C to +70°C		5.0		nA/°C
		T_A = +25°C to 0°C		10		
V_{IR}	Input Voltage Range	V_{CC} = ±6.5V	±4.0	±4.5		V
V_{IDR}	Differential Input Voltage Range			±5.0		V
V_{OH}	Output Voltage HIGH (Either Output)	0 mA ≤ I_{OH} ≤ 5.0 mA, V_{CC} = +5.0V	2.4	3.2		V
		I_{OH} = 80 μA, V_{CC} = ±4.5V	2.5	3.0		
V_{OL}	Output Voltage LOW (Either Output)	I_{OL} = 3.2 mA		0.25	0.4	V
I^+	Positive Supply Current	V_{CC} = ±6.5V		18	34	mA
I^-	Negative Supply Current	V_{CC} = ±6.5V		9.0	16	mA

Note 1: $T_{J\ Max}$ = 175°C.

Note 2: Ratings apply to ambient temperature at 25°C. Above this temperature, derate the 8L-Metal Can at 6.7 mW/°C, the 14L-Ceramic DIP at 9.1 mW/°C, and the 8L-Ceramic DIP at 8.7 mW/°C.

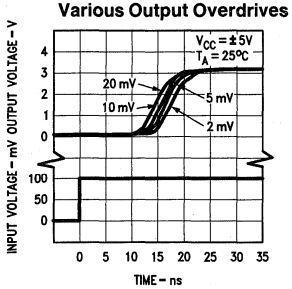
Note 3: Response time measured from the 50% point of a 30 mV_{P-P} 10 MHz sinusoidal input to the 50% point of the output.

Note 4: Response time measured from the 50% point of a 2.0 V_{P-P} 10 MHz sinusoidal input to the 50% point of the output.

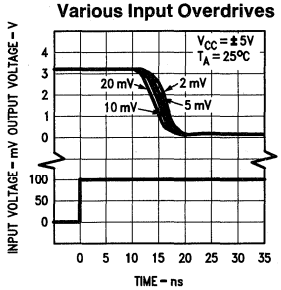
Note 5: Response time measured from the start of a 100 mV input step with 5.0 mV overdrive to the time when the output crosses the logic threshold.

Typical Performance Characteristics

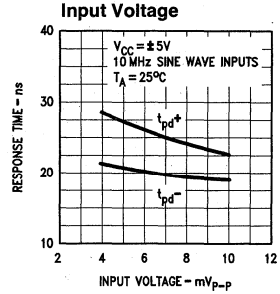
Response Time for Various Output Overdrives



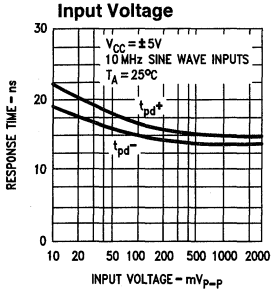
Response Time for Various Input Overdrives



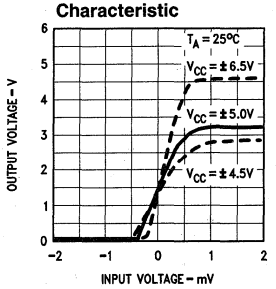
Response Time vs Input Voltage



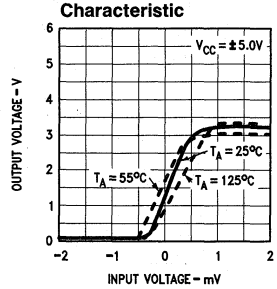
Response Time vs Input Voltage



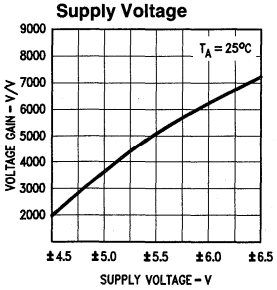
Voltage Transfer Characteristic



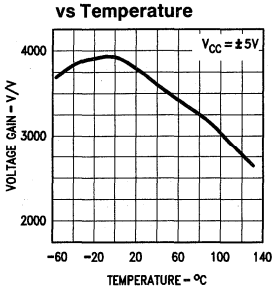
Voltage Transfer Characteristic



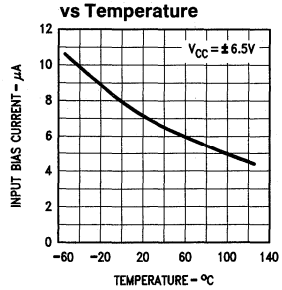
Voltage Gain vs Supply Voltage



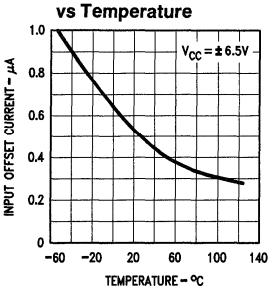
Voltage Gain vs Temperature



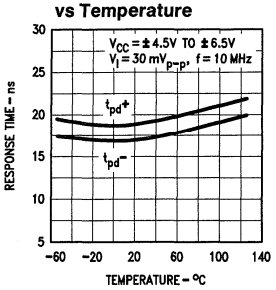
Input Bias Current vs Temperature



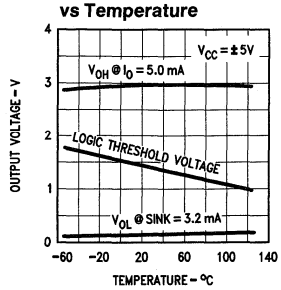
Input Offset Current vs Temperature



Response Time vs Temperature



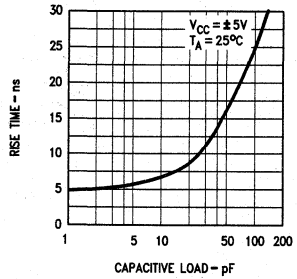
Output Voltage Levels vs Temperature



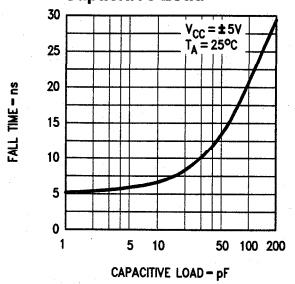
TL/H/10067–5

Typical Performance Characteristics (Continued)

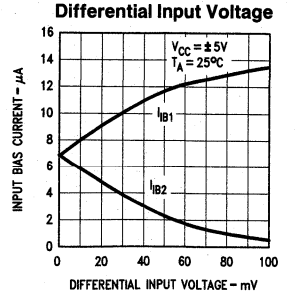
Rise Time vs Capacitive Load



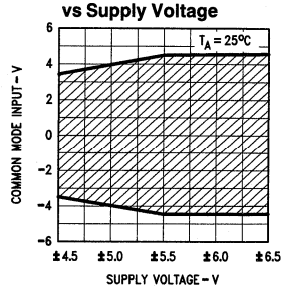
Fall Time vs Capacitive Load



Input Bias Current vs Differential Input Voltage

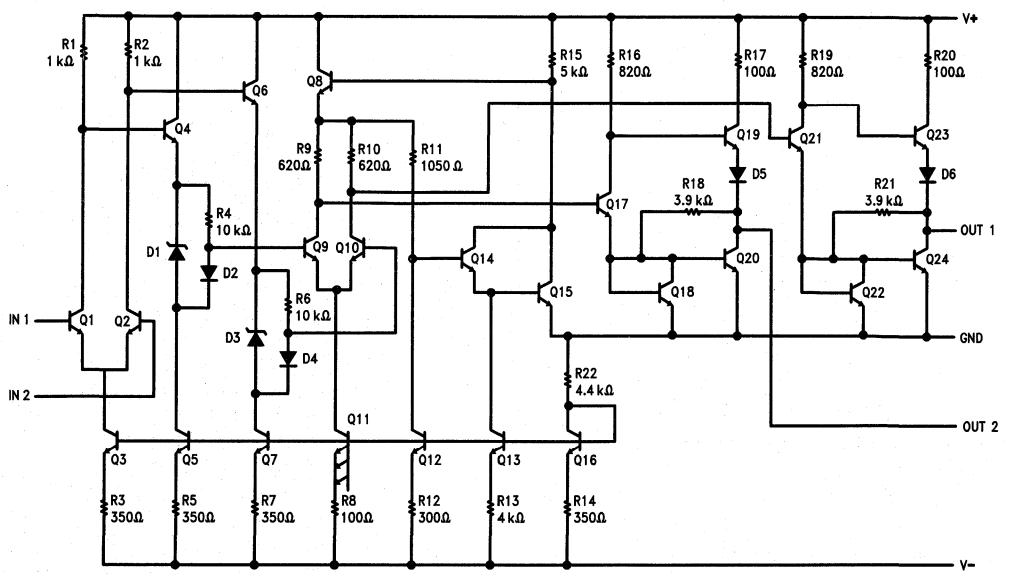


Common Mode Range vs Supply Voltage



TL/H/10067–6

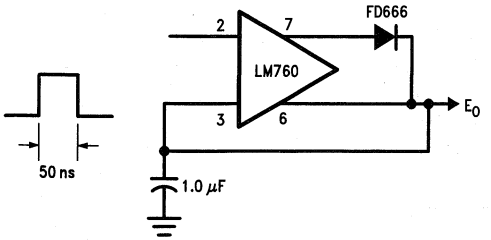
Equivalent Circuit



TL/H/10067–4

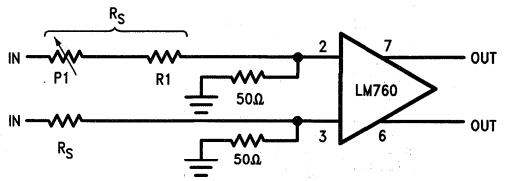
Typical Applications (Note 1)

Fast Positive Peak Detector



TL/H/10067–7

Line Receiver with High Common Mode Range



TL/H/10067–10

Common mode range = $\pm 4 \times \frac{R_S}{50}$ V

Differential Input Sensitivity = $5 \times \frac{R_S}{50}$ mV

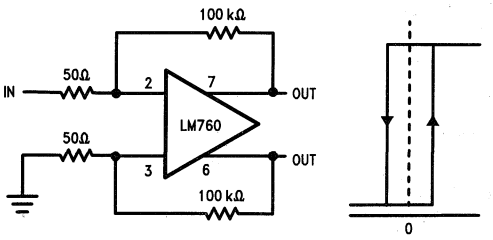
P_1 must be adjusted for optimum common mode rejection.

For R_S = 200Ω:

Common mode range = ±16V

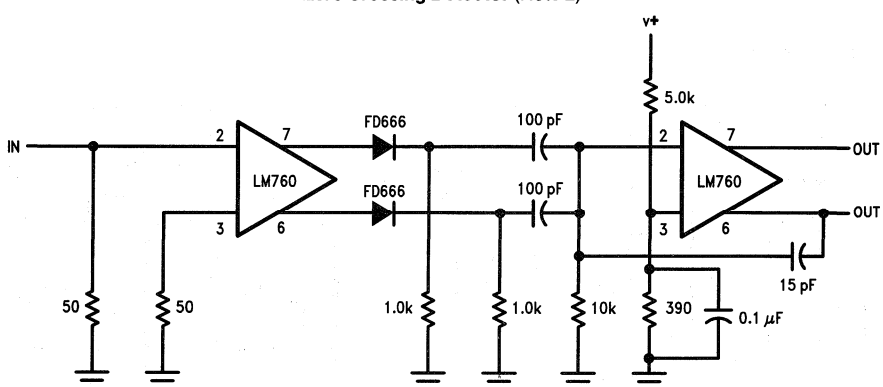
Sensitivity = 20 mV

Level Detector with Hysteresis



TL/H/10067–8

Zero Crossing Detector (Note 2)



TL/H/10067–9

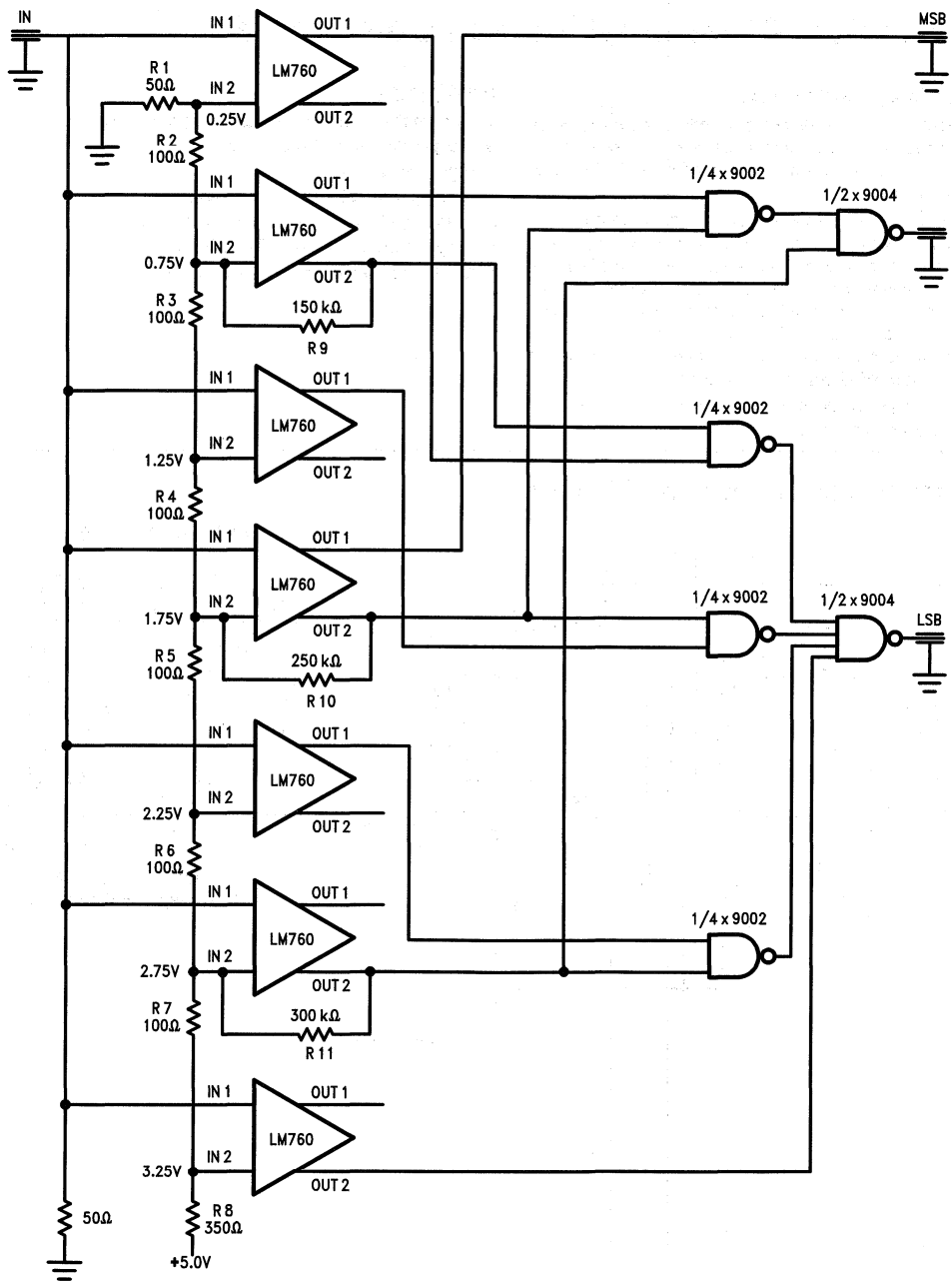
Total delay = 30 ns
Input Frequency = 300 Hz to 3.0 MHz
Minimum input voltage = 20 mV_{P-P}

Note 1: Lead numbers shown are for Metal Package only.

Note 2: All resistor values in ohms.

Typical Applications (Note 1) (Continued)

High Speed 3-Bit A/D Converter



TL/H/10067–11

Input voltage range = 3.5V
Typical conversion speed = 30 ns

National Semiconductor

LM1414 Dual Differential Voltage Comparator

General Description

The LM1414 is a dual differential voltage comparator intended for applications requiring high accuracy and fast response times. The device is constructed on a single monolithic silicon chip.

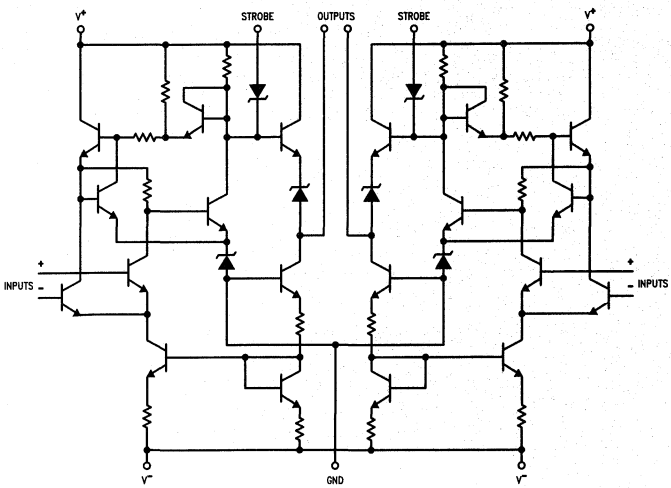
The LM1414 is useful as a variable threshold Schmitt trigger, a pulse height discriminator, a voltage comparator in high-speed A/D converters, a memory sense amplifier or a high noise immunity line receiver. The output of the comparator is compatible with all integrated logic forms. The LM1414 meets or exceeds the specifications for the MC1414 and is a pin-for-pin replacement. The LM1414 is available in a molded dual-in-line package.

The LM1414 is specified for operation over the 0°C to +70°C temperature range.

Features

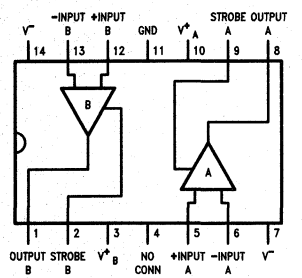
- Two totally separate comparators per package
- Independent strobe capability
- High speed 30 ns typ
- Low input offset voltage and current
- High output sink current over temperature
- Output compatible with TTL/DTL logic
- Molded or ceramic dual-in-line package

Schematic and Connection Diagrams



TL/H/10411–1

Dual-In-Line Package



TL/H/10411–2

Order Number LM1414N
See NS Package Number N14A

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Positive Supply Voltage	+14.0V
Negative Supply Voltage	−7.0V
Peak Output Current	10 mA
Differential Input Voltage	±5.0V
Input Voltage	±7.0V
Power Dissipation (Note 2)	1000 mW
Operating Temperature Range LM1414	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec.)	300°C

Electrical Characteristics for $T_A = 25°C$, $V^+ = +12V$, $V^- = -6V$, unless otherwise specified

Parameter	Conditions	LM1414			Units
		Min	Typ	Max	
Input Offset Voltage	$R_S \le 200\Omega$, $V_{CM} = 0V$, $V_{OUT} = 1.4V$		1.0	5.0	mV
Input Offset Current	$V_{CM} = 0V$, $V_{OUT} = 1.4V$		1.2	5.0	μA
Input Bias Current				25	μA
Voltage Gain		1000			
Output Resistance			200		Ω
Differential Input Voltage Range		±5.0			V
Input Voltage Range	$V^- = -7.0V$	±5.0			V
Common Mode Rejection Ratio	$R_S \le 200\Omega$, $V^- = -7.0V$	70	100		dB
Positive Output Voltage	$V_{IN} \ge 7.0$ mV, $0 \le I_{OUT} \le -5.0$ mA	2.5	3.2	4.0	V
Negative Output Voltage	$V_{IN} \le -7.0$ mV	−1.0	−0.5	0	V
Strobed Output Voltage	$V_{STROBE} \le 0.3V$	−1.0	−0.5	0	V
Strobe "0" Current	$V_{STROBE} = 100$ mV		−1.2	−2.5	mA
Positive Supply Current	$V_{IN} \le -7$ mV			18	mA
Negative Supply Current	$V_{IN} \le -7$ mV			−14	mA
Power Consumption			180	300	mW
Response Time	(Note 3)		30		ns
LM1414: The following apply for $T_L \le T_A < T_H$ (Note 4) unless otherwise specified					
Input Offset Voltage	$R_S \le 200\Omega$, $V_{OUT} = 1.8V$ for $T_A = T_L$ $V_{CM} = 0V$, $V_{OUT} = 1.0V$ for $T_A = T_H$			6.5 6.5	mV mV
Input Bias Current				40	μA
Temperature Coefficient of Input Offset Voltage			5.0		μV/°C
Input Offset Current	$V_{CM} = 0V$, $V_{OUT} = 1.8V$, $T_A = T_L$ $V_{CM} = 0V$, $V_{OUT} = 1.0V$, $T_A = T_H$			7.5 7.5	μA μA
Voltage Gain		800			
Output Sink Current	$V_{IN} \le -9.0$ mV, $V_{OUT} \ge 0V$	1.6	2.5		mA

Note 1: Voltage values are with respect to network ground terminal. Positive current is defined as current into the referenced pin.

Note 2: LM1414 molded package: The maximum junction temperature is +125°C, for operating at elevated temperatures, devices must be derated linearly at 10 mW/°C.

Note 3: The response time specified (see definitions) for a 100 mV input step with 5 mV overdrive.

Note 4: For LM1414, $T_L = 0°C$, $T_H = +70°C$.

National Semiconductor

LM1801 Battery Operated Power Comparator

General Description

The LM1801 is an extremely low power comparator with a high current, open-collector output stage. The typical supply current is only 7 μA, yet in its switched state the comparator can source or sink 0.5A. The LM1801 is designed to operate in a standby mode for 1 year, powered by a 9V alkaline battery. Provision is made for operation from supplies of up to 14V. An internal 14.5V zener clamp may be used for supply regulation in line operated applications.

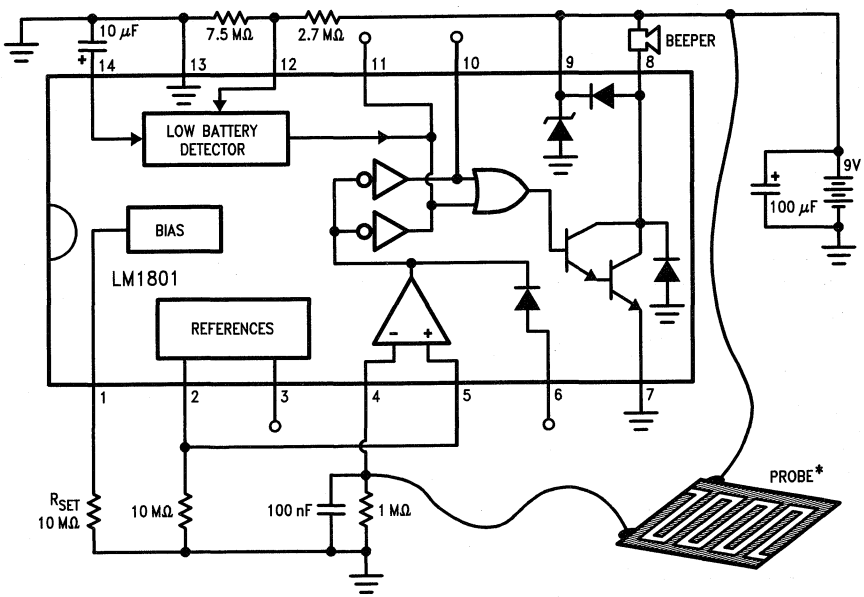
The low battery detector and stand-by current drain are externally programmed by resistors. A parallel output is provided to "OR" as many as 9 comparators, and a feedback pin allows adding hysteresis or latching functions. Two on-chip voltage sources can serve as bias points for the comparator inputs or as references for other circuit functions.

Features

- 8V to 14V operation
- Direct drive to horn
- Internal zener for supply regulation
- Parallel comparator capability
- Extremely low stand-by current drain
- 2 references on chip
- Low battery detector
- 0.5A output transistor
- Output clamp diodes on chip

Applications

- Intrusion alarms
- Water leak detectors
- Gas leak detectors
- Overvoltage crowbars
- Battery operated monitors



TL/H/9139–1

*Alarm sounds when probe conductors are bridged with water droplets. A suitable probe can be etched in copper clad board.

FIGURE 1. Water Leak Detector

Order Number LM1801N
See NS Package Number N14A

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	14V
Input Voltage	−0.3V to 14V
Input Differential Voltage	±14V
Power Dissipation (Note 1)	1176 mW
Operating Temperature Range	0°C to +70°C
Storage Temperature Range	−65°C to +125°C
Lead Temperature (Soldering, 10 sec.)	260°C

ESD rating to be determined.

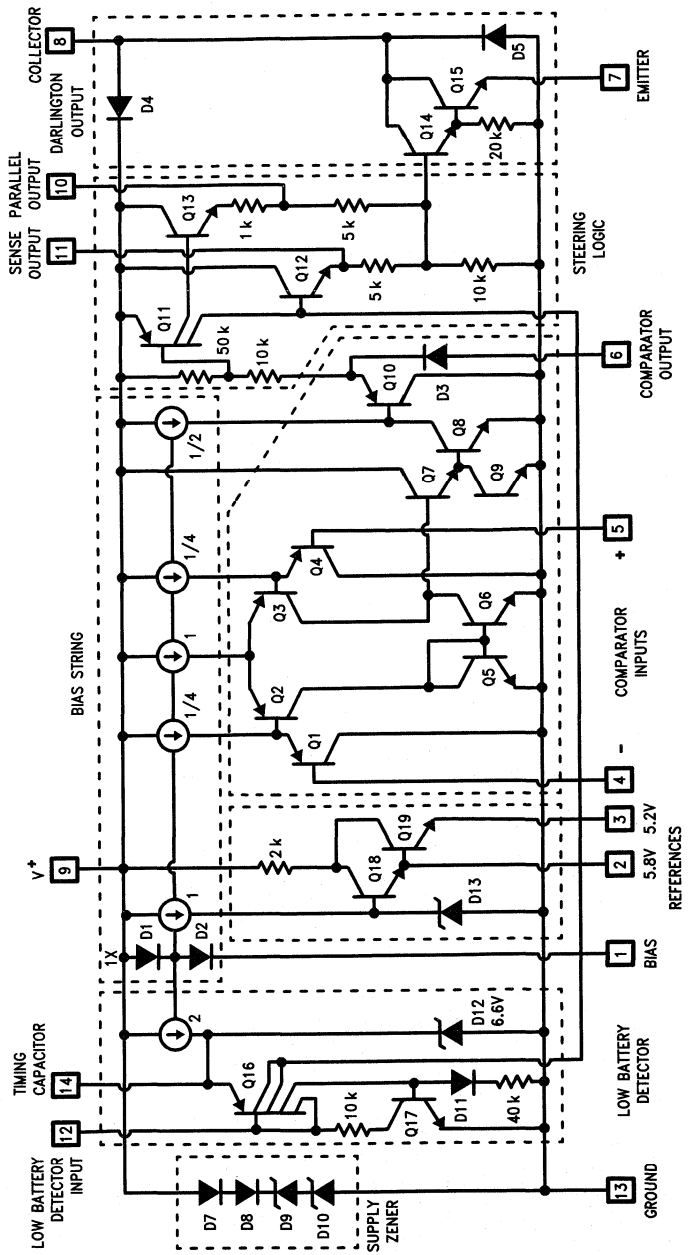
Electrical Characteristics (Note 2)

Parameter	Conditions	Min	Typ	Max	Units
Comparator					
Input Offset Voltage			5	15	mV
Input Bias Current			2	10	nA
Input Offset Current			0.5	8	nA
Pin 6 Output Low	I_{SINK} = 100 μA		1.5		V
Output Stage (Pin 8)					
Leakage Current			5	100	nA
Saturation Voltage	I_8 = 200 mA		0.7	1.3	V
Saturation Voltage	I_8 = 500 mA		1.9		V
Common Alarm Line (Pin 10)					
Drive Capabilities	V4 > V5				
Output Voltage High			6.8		V
Output Current	V10 = 0.0V		6.5		mA
Driver Requirements	V5 > V4				
Input Voltage			3.6		V
Input Current	V8 = 1.5V, I_8 = 200 mA		0.4		mA
Regulator					
Pin 2 Reference Voltage			5.8		V
Temperature Coefficient			5		mV/°C
Pin 3 Reference Voltage			5.2		V
Temperature Coefficient			7		mV/°C
Battery Check Oscillator					
Threshold Voltage (Pin 12)		5.5	6.0	6.5	V
Period	V^+ = 7.5V, C1 = 10 μF		40	50	s
Beep Pulse Width	V^+ = 7.5V, C1 = 10 μF		60		ms
Supply Current (Note 3)			6	8	μA
Zener Clamp Voltage, V9	I_9 = 1 mA		14.5		V

Note 1: For operating at elevated temperatures, the device must be derated based on a 125°C maximum junction temperature and a thermal resistance of 85°C/W junction to ambient.

Note 2: R_{SET} = 10 MΩ, V^+ = 9V, T_A = 25°C, *(Figure 1).*

Note 3: Output OFF.



TL/H/9139–2

FIGURE 2. LM1801 Internal Schematic

Applications Hints

CIRCUIT OPERATION

The LM1801 includes a bias string, comparator, steering logic, output transistor, supply clamp, low voltage detector, and reference. An internal schematic is shown in *Figure 2.*

The chip is biased by a group of current sources that are controlled externally by a fixed resistor, R_{set}. In normal, or standby operation the supply current drain is nominally 6 times the set current at pin 1. The voltage at pin 1 is two forward diode potentials (D1 + D2 = 1.2V typical) less than the positive supply voltage. Practical values of R_{set} range from 100 kΩ to 10 MΩ. Higher currents are useful where speed is important, while lower currents promote long battery life.

The total standby current drain of the LM1801 will include, in addition to the above, the current drawn by the external circuits connected at pins 2, 3, and 12. These are the resistive dividers used to set the low battery threshold and comparator threshold.

The voltage comparator consists of devices Q1 through Q10. The input features a common mode range from less than 300 mV to $V^+ - 1.2V$. If the non-inverting input is within this range, the output state remains valid for inverting inputs of 0V to V^+. If the inverting input is within the common mode range, valid comparisons hold for non-inverting inputs of 300 mV to V^+. The comparator may not switch low if the positive input is grounded.

With a set resistance of 10 MΩ, comparator input bias currents of 2 nA are typical. This allows the use of high-value resistors (10 MΩ) at the comparator inputs which help minimize total supply current. The comparator's output is available through a steering diode (D3) for latching or hysteresis functions.

The comparator output is also coupled internally to the steering logic (Q11–Q13). The comparator, low battery detector, and parallel output (pin 10) functions are OR'd in the logic circuit. In addition, the comparator output is steered to the parallel output. If the parallel outputs (pin 10) of two or more chips are wired together along with a common ground, the comparator on any one chip can cause all of the other output stages to switch, as well as its own output. Outputs are switched when the inverting comparator input is positive with respect to the non-inverting input. Low battery functions are coupled to the steering logic via Q12, and therefore do not affect the parallel output (Q13).

If the sense outputs (pin 11) of two or more chips are wired together, the comparator and low battery detector will cause all outputs to switch.

The output transistor is a 0.5A Darlington. Included in this structure are two clamp diodes. D4 clamps positive collector voltage excursions to the supply, and D5 clamps negative excursions to ground.

The output transistor is normally operated with the emitter grounded. Under these conditions the collector is guaranteed to saturate no higher than 1.3V at 200 mA. 1.9V saturation voltage is typical at 500 mA. The emitter may also be used as an output, and it can swing from ground potential up to 5V on a 9V supply. Emitter swing in the positive direction is limited in the parallel output mode.

A low battery detector with a 6V threshold is also included on chip. This circuit consists of Q16, Q17, D11, and D12. When pin 12, the battery sense input, is higher than 6V, D12 clamps the emitter of Q16 to 6.6V, and the output from the current source flows through the zener to ground. If pin 14 drops below 6V, Q16 is biased ON, and current is drawn away from the zener and into Q16. The SCR formed by Q16 and Q17 is triggered when Q16 is biased ON. The capacitor at pin 14 is discharged, part of its charge flows to the steering logic to pulse the output transistor, and the remainder holds the SCR in its ON state.

When the timing capacitor has discharged, conduction in Q16 and Q17 is commutated. Note that the output from the current source is less than the sustaining current required by the SCR. The current source slowly charges the capacitor until the voltage across it rises 0.6V above pin 12, where the cycle repeats itself. If pin 12 rises above 6V, the zener clamps the voltage at pin 14 and the low battery detector remains OFF.

Pin 12 is biased from an external resistive divider. The divider should be designed to detect at no lower than $V^+ = 7V$. The detector will continue to work at lower voltages providing pin 12 is at least 1V below the supply. For a 9V alkaline battery a threshold of 8.2V is common. A resistive divider of 2.7 MΩ and 7.5 MΩ provides the appropriate threshold.

In many applications the on-chip references can provide bias points. The references are driven from D13, and buffered by Q18 and Q19. If only one bias point is needed the first reference (pin 2) should be used, and the unused output (pin 3) may be left open. The tiny leakage currents in Q18 can cause Q19 (pin 3) to drift upward if a 10 MΩ load resistor is not included at pin 2. The combined output current from pins 2 and 3 should not exceed 1 mA. If neither reference output is used, pins 2 and 3 should be left open.

The last section of the LM1801 is the supply zener. It is built from a series combination of two diodes and two zeners. The breakdown voltage at 1 mA is 14.5V, and the series resistance is about 200Ω. In line operated applications the zener may be used for supply regulation or transient protection. The zener is designed to carry up to 10 mA.

Applications Hints (Continued)

DESIGN HINTS

If the comparator inputs are subjected to electrostatic discharges (ESD), a series resistance is recommended to provide protection. Given the low input bias currents, 100 kΩ resistors can be added without affecting circuit performance, yet they greatly enhance static protection. The LM1801 is not designed to withstand reverse battery.

With a 10 MΩ R_{set}, the LM1801 responds to an input in approximately 2.5 μs, and turns OFF in 200 μs. Higher set currents decrease the response time. With R_{set} = 1 MΩ, the output switches low in 0.5 μs, and high in 50 μs, and with R_{set} = 100 kΩ, the response times are reduced to 0.2 μs and 12 μs.

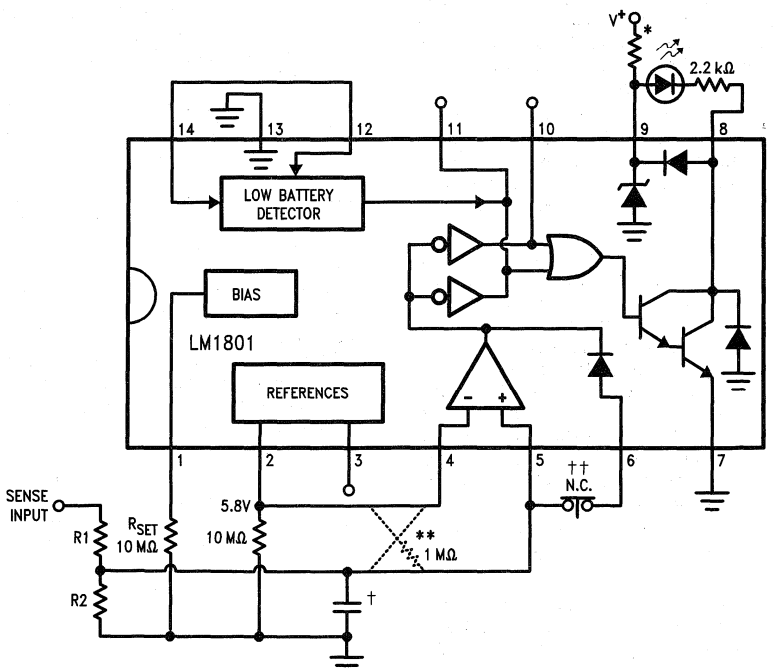
When the circuit is in the standby state (V5 > V4), the current consumption in a typical application such as *Figure 1* is less than approximately 7 μA. However, when the comparator switches LOW (V4 > V5), the supply current increases to 3 mA owing to the Darlington base current. Therefore, to realize maximum battery life, any application should be devised so that V5 > V4 in the standby or resting state.

The output stage can drive lamps, LEDs, buzzers, beepers, relays, motors, and solenoids. However, the low battery detector is not compatible with every load. Since the low battery detector generates only a short pulse (60 ms typical), it is intended for use with buzzers and beepers. Depending on the response time and resonant frequency, some buzzers may only produce a single click. Self-oscillating beepers usually start instantly and produce a recognizable "tweet" when a low battery condition is detected. Incandescent lamps, large relays and solenoids will do absolutely nothing when pulsed by the low battery detector.

Self-oscillating beepers are readily available, such as the Sonalert SNP428 and the Panasonic EAL-069A. These units are guaranteed to self-start when power is applied.

To defeat the low battery detector, short pins 12 and 14 together, and do not connect them to anything else.

Circuit board assembly procedures should include a thorough cleaning to remove flux and other residues. The input pins are often biased by very high impedance sources and even a 10 MΩ leakage path can upset circuit operation.



TL/H/9139–3

$R_1 + R_2 = 10\ M\Omega$

$V_{TRIP} = \left(\frac{R_1 + R_2}{R_2}\right) 5.8V$

Minimum trip voltage = 5.8V

*Use series resistor for supplies > 14V. Select for I_{ZENER} = 5 mA.

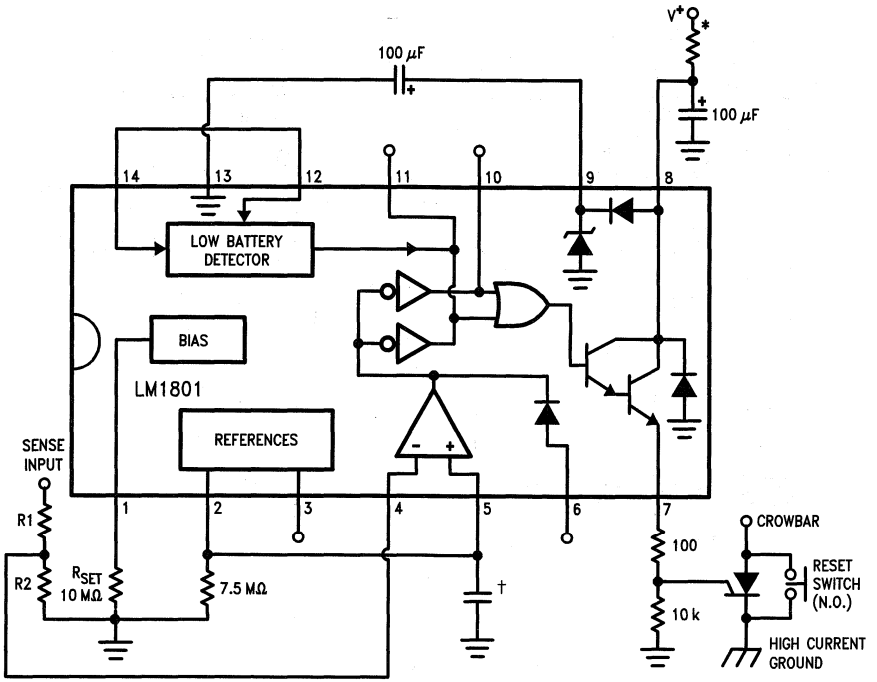
**Reverse connections and add 1 MΩ resistor for overvoltage indication.

†Optional filter capacitor, 1 nF to 100 nF.

††Push to reset. Eliminate pin 6 connection for non-latching operation.

FIGURE 3. Under (Over) Voltage Indicator

Applications Hints (Continued)



TL/H/9139–4

$R_1 + R_2 = 10\ M\Omega$

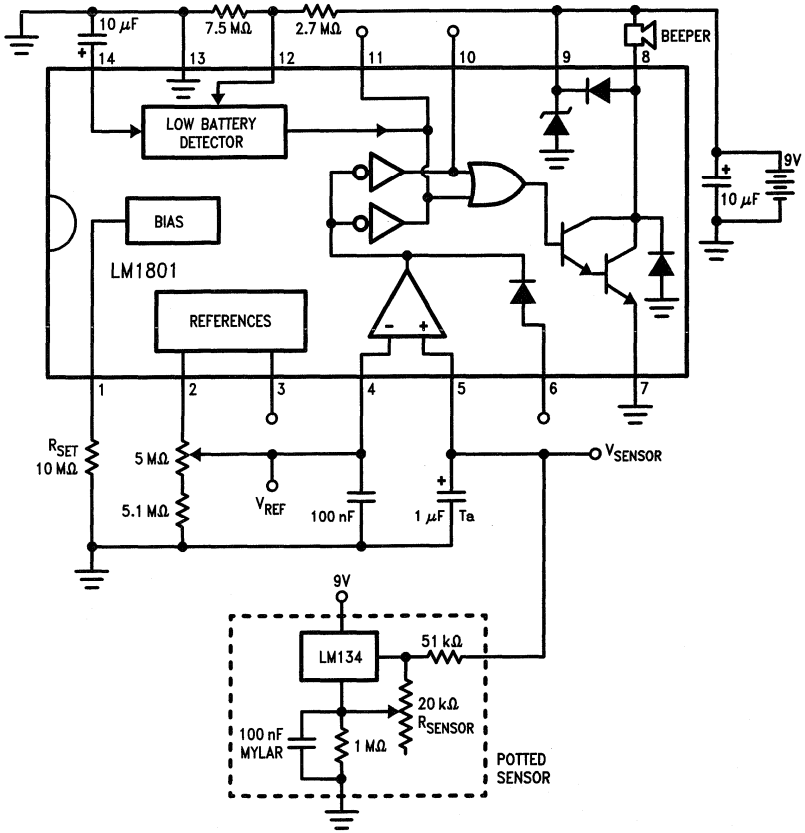
$V_{TRIP} = \left(\frac{R_1 + R_2}{R_2}\right) 5.8V$

*Use series resistor for supplies > 14V.

†Optional filter capacitor, 1 nF to 100 nF.

FIGURE 4. Overvoltage Crowbar

Applications Hints (Continued)



TL/H/9139–5

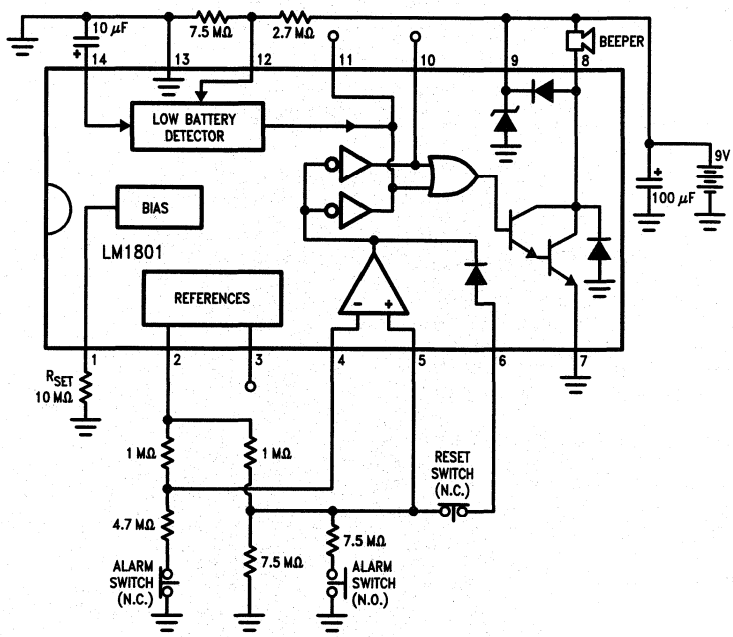
To set trip point, trim V_{REF} to 4.5V. Trim R_{SENSOR} at room temperature (23°C) for:

$$V_{SENSOR} = 4.5\left(\frac{273 + 23}{T_X + 273}\right)$$

where T_X is the desired trip point temperature in °C. As shown, the alarm is activated for over temperature conditions. Reverse the comparator connections for under temperature alarm. The 20 kΩ potentiometer allows an adjustment range of −55°C to +60°C. Add a 10k fixed resistance in series with the potentiometer for a +50°C to +125°C adjustment range. R_{SENSOR} can be replaced by a fixed resistor once the desired value is found. V_{REF} is used as a final adjustment.

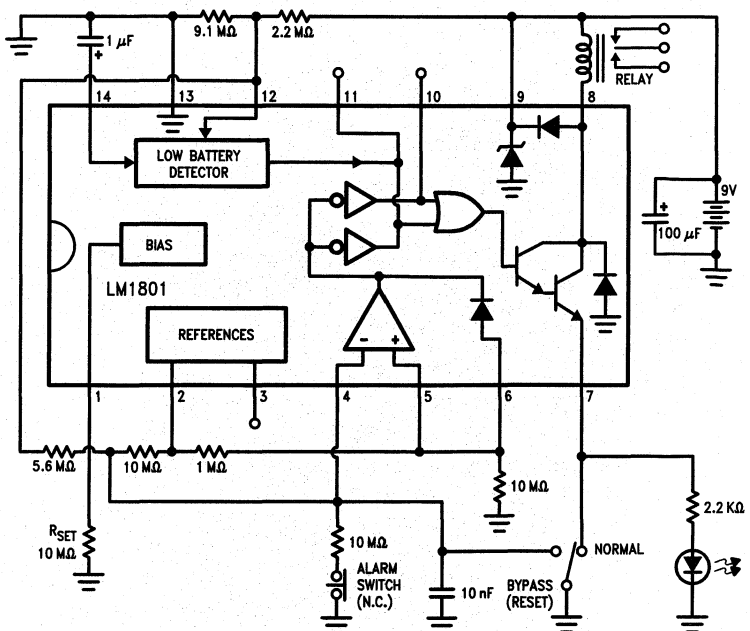
FIGURE 5. Over (Under) Temperature Alarm

Applications Hints (Continued)



TL/H/9139–6

FIGURE 6. Simple Alarm Circuit



TL/H/9139–7

FIGURE 7. Full-Featured Intrusion Alarm

National Semiconductor

LM6685
Ultra Fast Single Latched Comparator

General Description

The LM6685 is an ultra fast single voltage comparator manufactured with an advanced high speed bipolar process that makes possible very short propagation delays (2.6 ns) with excellent matching characteristics. The comparator has differential analog inputs and complementary logic outputs compatible with most forms of ECL. The output current capability is adequate for driving terminated 50Ω transmission lines. The low input offsets and short delays make this comparator especially suitable for high speed precision analog to digitial processing.

The LM6685 is functionally compatible with AD96685 and SP9685.

Features

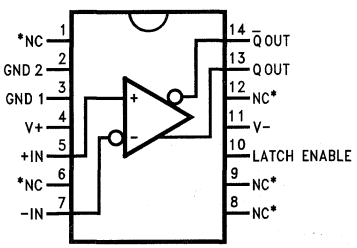
- 2.6 ns Typical Propagation Delay
- Complementary ECL Outputs
- 50Ω Line Driving Capability
- Built-In Latch
- Typical Output Skew 0.2 ns
- Propagation Delay Constant with Overdrive

Applications

- High-speed analog-to-digital processing
- High-speed window comparator

Connection Diagrams

Plastic SO

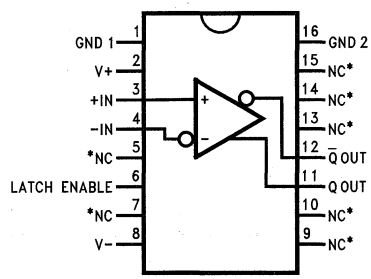


TL/H/10068–2

Top View

*No connection should be made to pin.

Plastic DIP



TL/H/10068–3

Top View

Ordering Information

Temperature Range	Package	NSC Package Number
−30°C to +85°C		
LM6685IN	Molded DIP	N16A
LM6685IM	Surface Mount	M14A

Absolute Maximum Ratings (Note 4)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature Range
Molded DIP and Surface Mount −65°C to +150°C

Lead Temperature
Molded DIP and Surface Mount
(Soldering, 10 seconds) 265°C

Internal Power Dissipation (Note 1)
16L-Molded DIP 1.36W
14L-Surface Mount 0.87W

Positive Supply Voltage +7.0V
Negative Supply Voltage −7.0V
Junction Temperature 150°C
Input Voltage ±4.0V
Differential Input Voltage ±6.0V
Output Current 30 mA

Operating Ratings (Note 4)

Temperature Range
Industrial −30°C to +85°C
Positive Supply Voltage +6.0V
Negative Supply Voltage −5.2V
Minimum Operating Voltage
V^+ to V^- 9.7V
Thermal Resistance (Note 5)

DC Electrical Characteristics (Note 2)

Symbol	Parameter	Conditions	LM6685I			Units
			Typ	Min	Max	
V_{IO}	Input Offset Voltage	$R_S \leq 100\Omega$, $T_A = 25°C$	0.3	−1.9	+1.9	mV
		$R_S \leq 100\Omega$		−2.5	+2.5	
$\Delta V_{IO}/\Delta T$	Average Temperature Coefficient of Input Offset Voltage	$R_S \leq 100\Omega$	1.3			μV/°C
I_{IO}	Input Offset Current	$25°C \leq T_A \leq T_{A\,Max}$	0.1	−1.0	+1.0	μA
		$T_A = T_{A\,Min}$	0.2	−1.3	+1.3	
I_{IB}	Input Bias Current	$25°C \leq T_A \leq T_{A\,Max}$	4.0		9	μA
		$T_A = T_{A\,Min}$	5.0		11	
V_{CM}	Common Mode Voltage Range			−3.3	+3.3	V
CMR	Common Mode Rejection	$R_S \leq 100\Omega$, (Note 6) $-3.3V \leq V_{CM} \leq +3.3V$	106	80		dB
PSRR	Power Supply Rejection Ratio	$R_S \leq 100\Omega$, $\Delta V_S = \pm 5\%$ (Note 6)	85	70		dB
V_{OH}	Output Voltage HIGH	$T_A = 25°C$	−0.885	−0.960	−0.810	V
		$T_A = T_{A\,Min}$	−0.975	−1.060	−0.890	
		$T_A = T_{A\,Max}$	−0.795	−0.890	−0.700	
V_{OL}	Output Voltage LOW	$T_A = 25°C$	−1.750	−1.850	−1.650	V
		$T_A = T_{A\,Min}$	−1.783	−1.890	−1.675	
		$T_A = T_{A\,Max}$	−1.725	−1.825	−1.625	
I+	Positive Supply Current		15		19	mA
I−	Negative Supply Current		17		23	mA
P_C	Power Consumption		200		270	mW

Switching Characteristics V_{IN} = 100 mV with overdrive, V_{OD} = 10 mV (Notes 2, 3)

Symbol	Parameter	Conditions	LM6685I			Units
			Typ	Min	Max	
$t_{PD}+$, $t_{PD}-$	Propagation Delay	T_A = 25°C	2.6		3.5	ns
t_{PD} + (E), t_{PD} − (E)	Latch Enable to Output (HIGH or LOW) Display	T_A = 25°C	2.0		2.5	ns
t_S	Min Latch Set up Time	T_A = 25°C	0.5		1.0	ns
t_H	Min Latch Hold Time	T_A = 25°C	0.5		1.0	ns

Note 1: Ratings apply to ambient temperature at 25°C.

Note 2: Unless otherwise specified V+ = 6.0V, V − = −5.2V, R_L = 50Ω to termination voltage V_T = −2.0V; all switching characteristics are for a 100 mV input step with 10 mV overdirve. The specification given for V_{IO}, I_{IO}, I_{IB}, CMR, PSRR, apply for ±5% supply voltage tolerances. T_A = T_J.

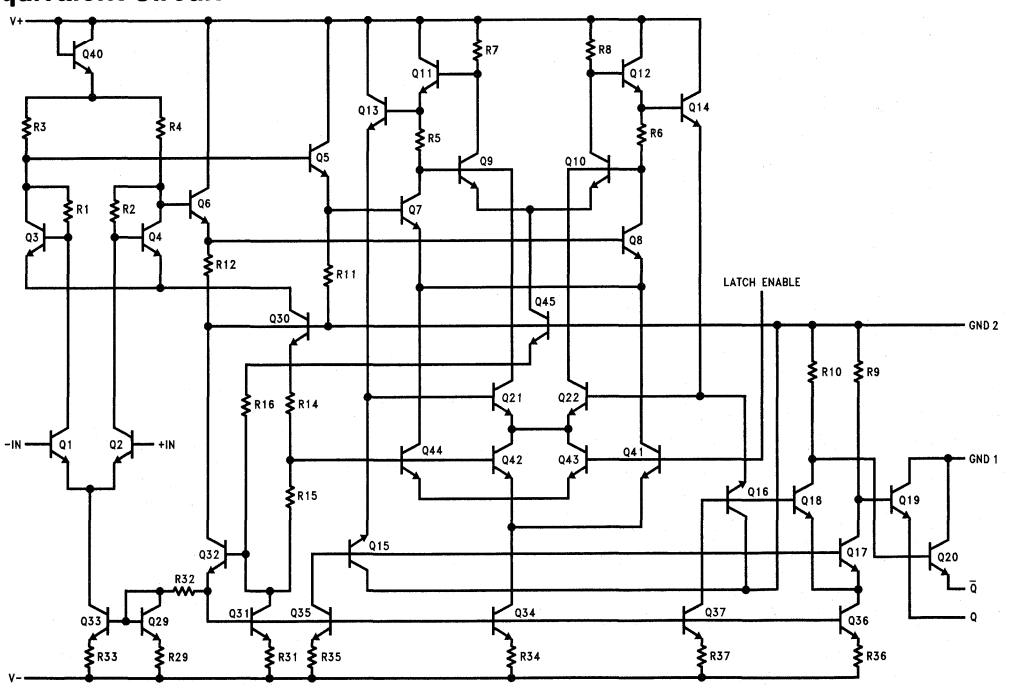
Note 3: Guaranteed but not tested in production.

Note 4: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the last conditions tested.

Note 5: The junction-to-ambient thermal resistance of the plastic molded DIP (N) is 92°C/W and the molded plastic SO(M) package is 144°C/W. All numbers apply for packages soldered directly into a PC board.

Note 6: Limit applies for 25°C only.

Equivalent Circuit



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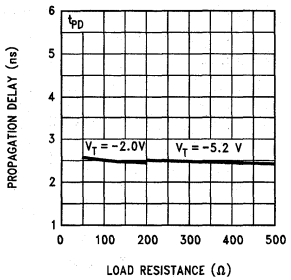
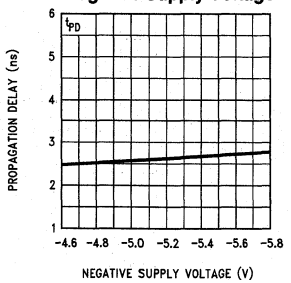
Typical Performance Characteristics

$T_A = 25°C$, $V+ = 6.0V$, $V- = -5.2V$, $V_T = -2.0V$, $R_L = 50\Omega$ and switching characteristics are for $V_{IN} = 100$ mV, $V_{OD} = 10$ mV, unless otherwise specified

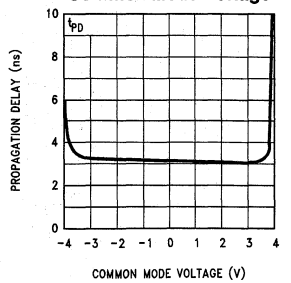
Propagation Delay vs Load Resistance



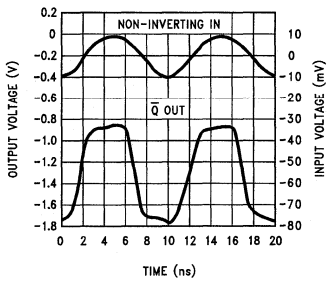
Propagation Delay vs Negative Supply Voltage



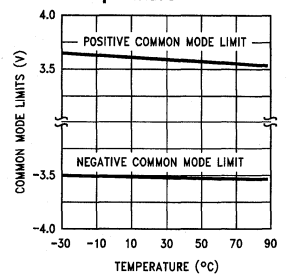
Propagation Delay vs Common Mode Voltage



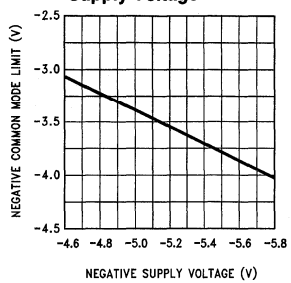
Response to 100 MHz Sine Wave



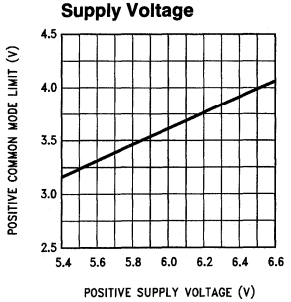
Common Mode Limits vs Temperature



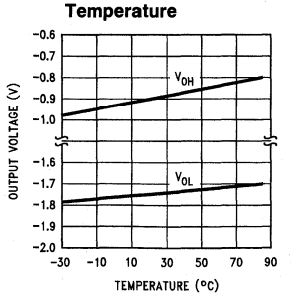
Negative Common Mode Limit vs Negative Supply Voltage



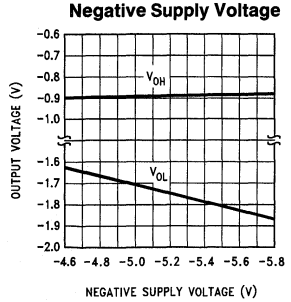
Positive Common Mode Limit vs Positive Supply Voltage



Output Levels vs Temperature



Output Levels vs Negative Supply Voltage

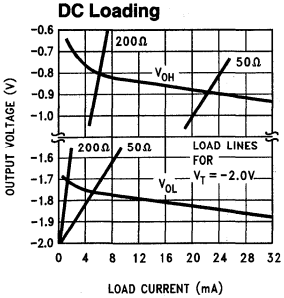


TL/H/10068–5

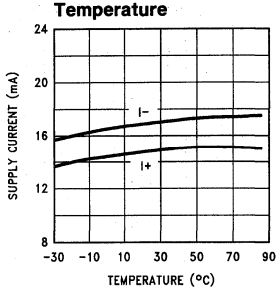
Typical Performance Characteristics

T_A = 25°C, V+ = 6.0V, V− = −5.2V, V_T = −2.0V, R_L = 50Ω and switching characteristics are for V_{IN} = 100 mV, V_{OD} = 10 mV, unless otherwise specified (Continued)

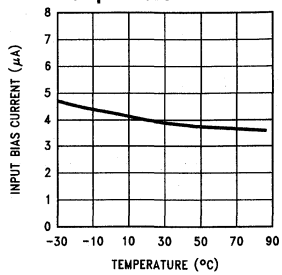
Output Levels vs DC Loading



Supply Currents vs Temperature



Input Bias Current vs Temperature



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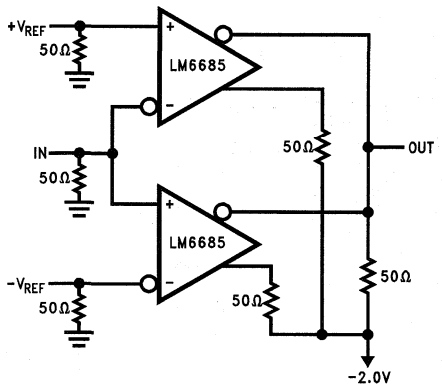
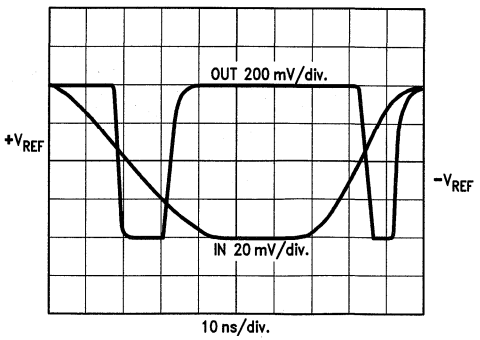
Typical Applications (T_A = 25°C)

High Speed Window Detector



TL/H/10068–7



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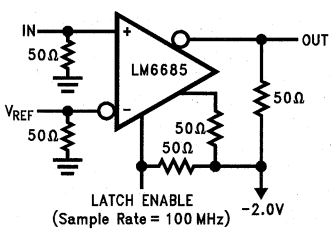
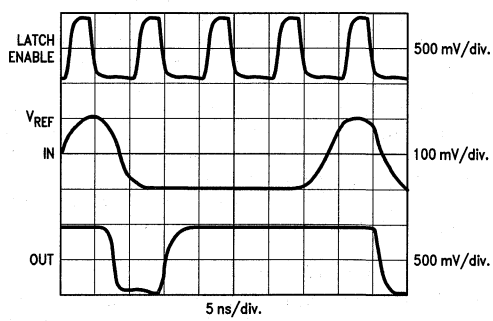
High Speed Sampling



TL/H/10068–9



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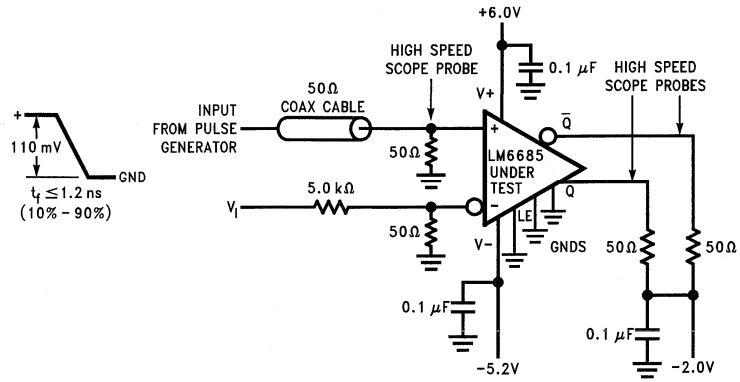
Application Information

Propagation Delay Test Circuit



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Measurement Of Propagation Delay

Propagation delays $t_{PD}+$ ($\overline{Q}$ output) and $t_{PD}-$ (Q output) are measured with input signal conditions of a 100 mV step with an overdrive of 10 mV (the overdrive is the voltage in excess of that needed to bring the output to the center of its dynamic range). Offset is compensated for by adjusting V_I until outputs are in the linear region while the Pulse Generator is disconnected. V_I is then increased in the positive direction so inverting input changes by 10 mV, i.e. the overdrive condition. Propagation delays are then measured with actual input pulse condition of +110 mV to 0V swing, with a $t_{PD}+$ or $t_{PD}-$ reading taken between the +10 mV level of the input pulse and the 50% point of the outputs.

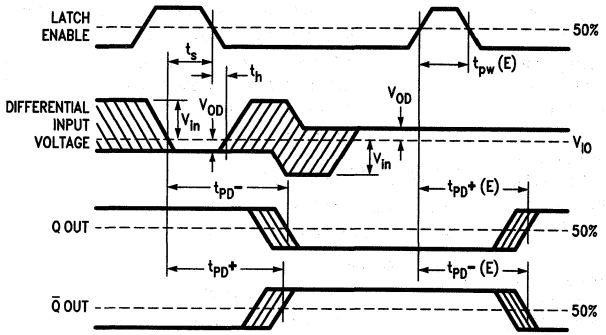
Thermal Considerations

To achieve the high speed of the LM6685, a certain amount of power must be dissipated as heat. This increases the temperature of the die relative to the ambient temperature. In order to be compatible with ECL III and ECL 10,000, which normally use air flow as a means of package cooling, the device must have an air flow across the package of 500 linear feet per minute or greater. Thus, even though different ECL circuits on a printed circuit board may have different power dissipations, all will have the same input and output levels, etc. provided each sees the same air flow and air temperature. This eases design, since the only change in characteristics between devices is due to the increase in ambient temperature of the air passing over the devices. If the LM6685 is operated without air flow, the change in electrical characteristics due to the increased die temperature must be taken into account.

Interconnection Techniques

All high speed ECL circuits require that special precautions be taken for optimum system performance. The LM6685 is particularly critical because it features very high gain (60 dB) at very high frequencies (100 MHz). A ground plane must be provided for a good, low inductance, ground current return path. The impedance at the inputs should be as low as possible and lead lengths as short as practical. It is preferable to solder the device directly to the printed circuit board instead of using a socket. Open wiring on the outputs should be limited to less than one inch, since severe ringing occurs beyond this length. For longer lengths, the printed circuit interconnections become microstrip transmission lines when backed up by a ground plane, with a characteristic impedance of 50 to 150Ω. Reflections will occur unless the line is terminated in its characteristic impedance. The termination resistors normally go to −2.0V, but a Thevenin equivalent to V− can be used at some increase in power. Best results are usually obtained with the terminating resistor at the end of the driven line. The lower impedance lines are more suitable for driving capacitive loads. The supply voltages should be decoupled with RF capacitors connected to the ground plane as close to the device supply leads as possible.

Timing Diagram



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Key to Timing Diagram

WAVEFORM	INPUTS	OUTPUTS
	MUST BE STEADY	WILL BE STEADY
	MAY CHANGE FROM H TO L	WILL BE CHANGING FROM H TO L
	MAY CHANGE FROM L TO H	WILL BE CHANGING FROM L TO H

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Note: The setup and hold times are a measure of the time required for an input signal to propagate through the first stage of the comparator to reach the latching circuitry. Input signal changes occurring before t_S will be detected and held; those occurring after t_h will not be detected. Changes between t_s and t_h may or may not be detected.

Definition of Terms

V_{IO} **Input Offset Voltage**—That voltage which must be applied between the two input terminals through two equal resistances to obtain zero voltage between the two outputs.

$\Delta V_{IO}/\Delta T$ **Average Temperature Coefficient of Input Offset Voltage**—The ratio of the change in input offset voltage over the operating temperature range to the temperature range.

I_{IO} **Input Offset Current**—The difference between the currents into the two input terminals when there is zero voltage between the two outputs.

I_{IB} **Input Bias Current**—The average of the two input currents.

R_I **Input Resistance**—The resistance looking into either input terminal with the other grounded.

C_I **Input Capacitance**—The capacitance looking into either input terminal with other grounded.

V_{CM} **Common Mode Voltage Range**—The range of voltages on the input terminals for which the offset and propagation delay specifications apply.

CMR **Common Mode Rejection**—The ratio of the input voltage range to the peak-to-peak change in input offset voltage over this range.

PSRR **Power Supply Rejection Ratio**—The ratio of the change in input offset voltage to the change in power supply voltages producing it.

V_{OH} **Output Voltage HIGH**—The logic HIGH output voltage with an external pull-down resistor returned to a negative supply.

V_{OL} **Output Voltage LOW**—The logic LOW output voltage with an external pull-down resistor returned to a negative supply.

$I+$ **Positive Supply Current**—The current required from the positive supply to operate the comparator.

$I-$ **Negative Supply Current**—The current required from the negative supply to operate the comparator.

P_C **Power Consumption**—The power dissipated by the comparator with both outputs terminated in 50Ω to −2.0V.

Switching Terms (see Timing Diagram)

t_{PD+} **Input to Output HIGH Delay**—The propagation delay measured from the time the input signal crosses the input offset voltage to the 50% point of an output LOW to HIGH transition.

t_{PD-} **Input to Output LOW Delay**—The propagation delay measured from the time the input signal crosses the input offset voltage to the 50% point of an output HIGH to LOW transition.

$t_{PD+(E)}$ **Latch Enable to Output HIGH Delay**—The propagation delay measured from the 50% point of the Latch Enable signal LOW to HIGH transition to the 50% point of an output LOW to HIGH transition.

$t_{PD-(E)}$ **Latch Enable to Output LOW Delay**—The propagation delay measured from the 50% point of the Latch Enable signal HIGH to LOW transition to the 50% point of an output HIGH to LOW transition.

t_S **Minimum Setup Time**—The minimum time before the negative transition of the Latch Enable signal that an input signal change must be present in order to be acquired and held at the outputs.

t_h **Minimum Hold Time**—The minimum time after the negative transition of the Latch Enable signal that the input signal must remain unchanged in order to be acquired and held at the outputs.

$t_{pw(E)}$ **Minimum Latch Enable Pulse Width**—The minimum time that the Latch Enable signal must be HIGH in order to acquire and hold an input signal change.

Other Symbols

T_A	Ambient temperature
R_S	Input source resistance
V_{CC}	Supply voltages
$V+$	Positive supply voltage
$V-$	Negative supply voltage
V_T	Output load terminating voltage
R_L	Output load resistance
V_{IN}	Input pulse amplitude
V_{OD}	Input overdrive
f	Frequency

National Semiconductor

LM6687
Ultra Fast Dual Voltage Comparators

General Description

The LM6687 is an ultra fast dual voltage comparator manufactured with an advanced high speed bipolar process that makes possible very short propagation delays (2.6 ns) with excellent matching characteristics. These comparators have differential analog inputs and complementary logic outputs compatible with most forms of ECL. The output current capability is adequate for driving terminated 50Ω transmission lines. The low input offsets and short delays make these comparators especially suitable for high speed precision analog-to-digital processing.

Separate latch functions are provided to allow each comparator to be independently used in a sample and hold mode. The latch function inputs are designed to be driven from the complementary outputs of a standard ECL gate. If latch enable is HIGH and $\overline{\text{latch enable}}$ is LOW, the comparator functions normally. When latch enable is driven LOW and $\overline{\text{latch enable}}$ is driven HIGH, the comparator outputs are locked in their existing logical states. Should the latch function not be used, latch enable must be connected to ground.

The LM6687 is lead compatible with the AD96687 and SP9687.

Features

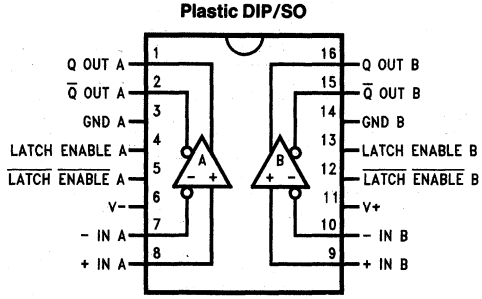
- 2.6 ns Typical propagation delay at 10 mV overdrive
- Complementary ECL outputs
- 50Ω line driving capability
- 1.0 ns Latch set up time

Applications

- High-speed analog-to-digital processing
- High-speed window comparator

Connection Diagram

Plastic DIP/SO



TL/H/10072–1

Top View

Ordering Information

Temperature Range	Package	NSC Package Number
−30°C to +85°C		
LM6687IN	Molded DIP	N16A
LM6687IM	Surface Mount	M16A

3

Absolute Maximum Ratings (Note 4)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature Range	
Molded DIP	−65°C to +150°C
Lead Temperature	
Molded DIP (Soldering, 10 sec.)	265°C
Internal Power Dissipation (Note 1)	
16L-Molded DIP	1.45W
16L-Surface Mount	0.95W
Positive Supply Voltage	+7.0V
Negative Supply Voltage	−7.0V
Junction Temperature	150°C
Input Voltage	±4.0V
Differential Input Voltage	±6.0V
Output Current	30 mA

Operating Ratings (Note 4)

Temperature Range	
Industrial	−30°C to +85°C
Positive Supply Voltage	+5.0V
Negative Supply Voltage	−5.2V
Minimum Operating Voltage (V+ to V−)	9.7V
Thermal Resistance (Note 5)	

LM6687
DC Electrical Characteristics (Note 2)

Symbol	Parameter	Conditions	LM6687I			Units
			Typ	Min	Max	
V_{IO}	Input Offset Voltage	$R_S \leq 100\Omega$, $T_A = 25°C$	0.6	−1.9	+1.9	mV
		$R_S \leq 100\Omega$		−2.5	+2.5	
$\Delta V_{IO}/\Delta T$	Average Temperature Coefficient of Input Offset Voltage (Note 3)	$R_S \leq 100\Omega$	2.5			μV/°C
I_{IO}	Input Offset Current (Note 3)	$25°C \leq T_A \leq T_{A\,Max}$	0.1	−1.0	+1.0	μA
		$T_A = T_{A\,Min}$	0.1	−1.3	+1.3	
I_{IB}	Input Bias Current	$25°C \leq T_A \leq T_{A\,Max}$	3.0		9	μA
		$T_A = T_{A\,Min}$	4.0		11	
V_{CM}	Input Common Mode Range		+2.7	−3.3	+2.7	V
CMR	Common Mode Rejection	$R_S \leq 100\Omega$, (Note 6) $-3.3 \leq V_{CM} \leq +2.7V$	112	80		dB
PSRR	Power Supply Rejection Ratio	$R_S \leq 100\Omega$, $\Delta V_S = \pm 5\%$ (Note 6)	80	70		dB
V_{OH}	Output Voltage HIGH	$T_A = 25°C$	−0.885	−0.960	−0.810	V
		$T_A = T_{A\,Min}$	−0.975	−1.060	−0.890	
		$T_A = T_{A\,Max}$	−0.795	−0.890	−0.700	
V_{OL}	Output Voltage LOW	$T_A = 25°C$	−1.750	−1.850	−1.650	V
		$T_A = T_{A\,Min}$	−1.783	−1.890	−1.675	
		$T_A = T_{A\,Max}$	−1.725	−1.825	−1.625	
I^+	Positive Supply Current		25		32	mA
I^-	Negative Supply Current		30		38	mA
P_C	Power Consumption		340		420	mW

Switching Characteristics V_{IN} = 100 mV, V_{OD} = 10 mV (Notes 2, 3)

Symbol	Parameter	Conditions	LM6687I			Units
			Typ	Min	Max	
t_{PD+}, t_{PD-}	Propagation Delay (Note 3)	T_A = 25°C	2.6		3.5	ns
t_S	Minimum Latch Set Up Time (Note 3)	T_A = 25°C	0.5		1.0	ns

Note 1: Ratings apply to ambient temperature at 25°C.

Note 2: Unless otherwise specified $V^+ = +5.0V$, $V^- = -5.2V$, $R_L = 50\Omega$ to termination voltage $V_T = -2.0V$; all switching characteristics are for a 100 mV input step with 10 mV overdrive. The specifications given for V_{IO}, I_{IO}, I_{IB}, CMR, PSRR, apply over the full V_{CM} range and for ±5% supply voltage tolerances. $T_A = T_J$.

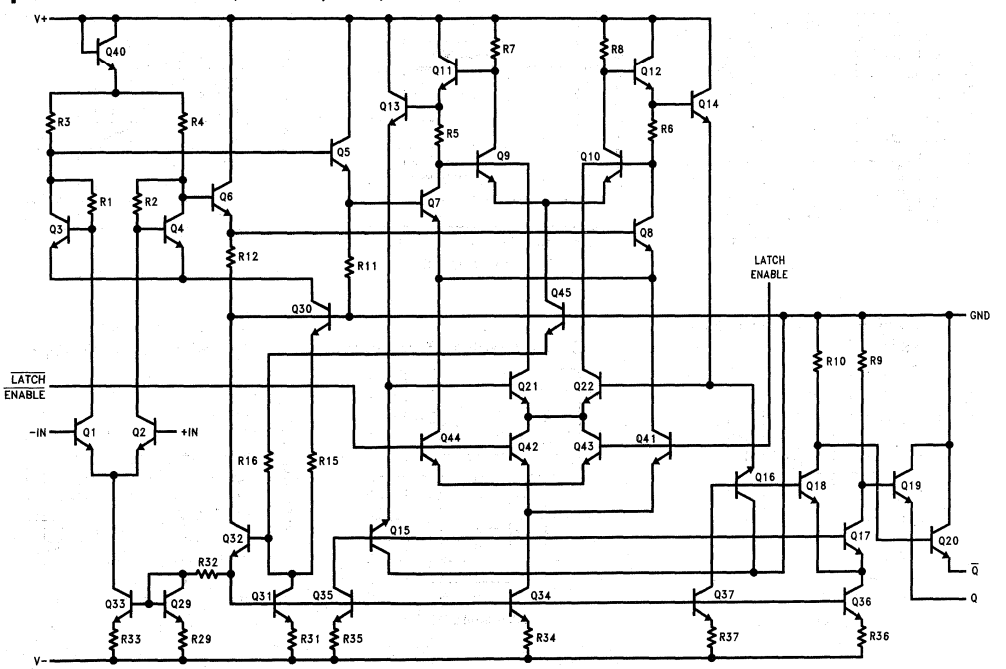
Note 3: Guaranteed, but not tested in production.

Note 4: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed.

Note 5: The junction-to-ambient thermal resistance of the molded plastic DIP (N) is 86°C/W, the molded plastic SO (M) package is 132°C/W. All numbers apply for packages soldered directly into a PC board.

Note 6: Limit applies for 25°C only.

Equivalent Circuit (Each Comparator)

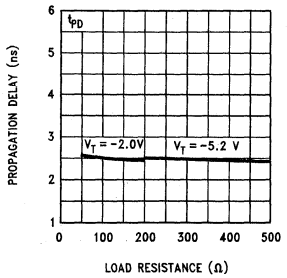


TL/H/10072–2

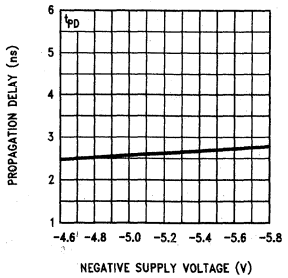
Typical Performance Characteristics

T_A = 25°C, V+ = 5.0V, V− = −5.2V, V_T = −2.0V, R_L = 50Ω and switching characteristics are for V_{IN} = 100 mV, V_{OD} = 10 mV, unless otherwise specified

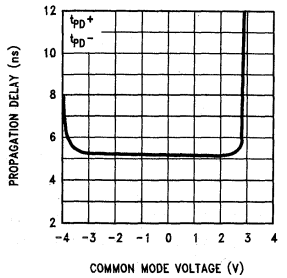
Propagation Delays vs Load Resistance



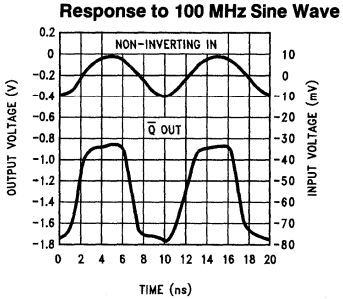
Propagation Delay vs Negative Supply Voltage



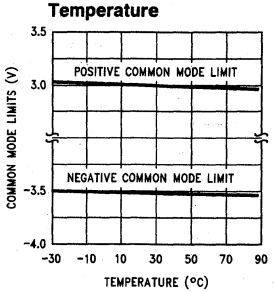
Propagation Delay vs Common Mode Voltage



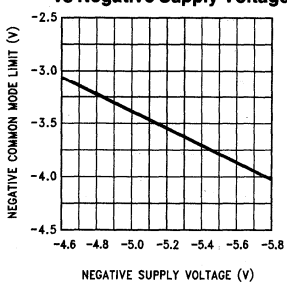
Response to 100 MHz Sine Wave



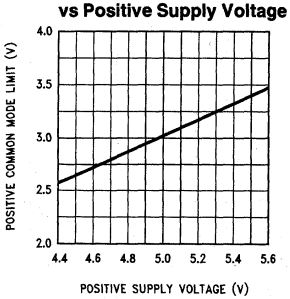
Common Mode Limits vs Temperature



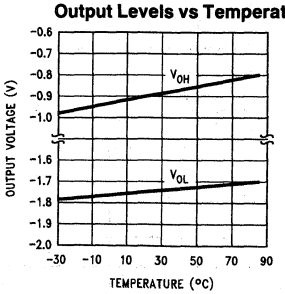
Negative Common Mode Limit vs Negative Supply Voltage



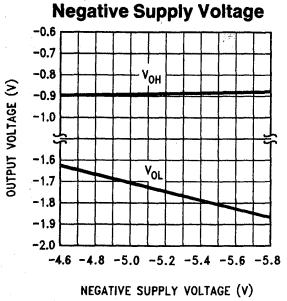
Positive Common Mode Limit vs Positive Supply Voltage



Output Levels vs Temperature



Output Levels vs Negative Supply Voltage

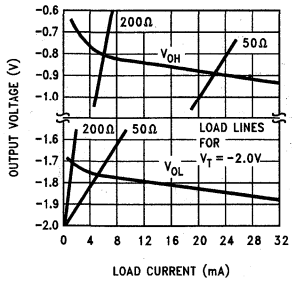


TL/H/10072–3

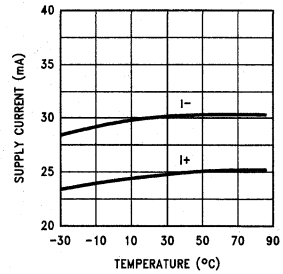
Typical Performance Characteristics

T_A = 25°C, V+ = 5.0V, V− = −5.2V, V_T = −2.0V, R_L = 50Ω and switching characteristics are for V_{IN} = 100 mV, V_{OD} = 10 mV, unless otherwise specified (Continued)

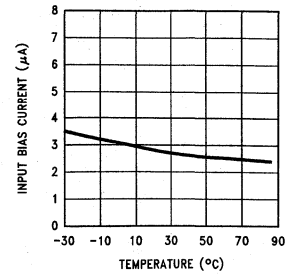
Output Levels vs DC Loading



Supply Currents vs Temperature



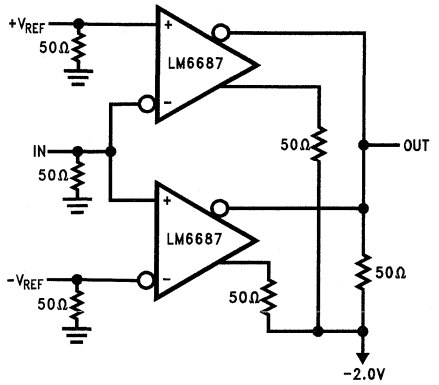
Input Bias Current vs Temperature



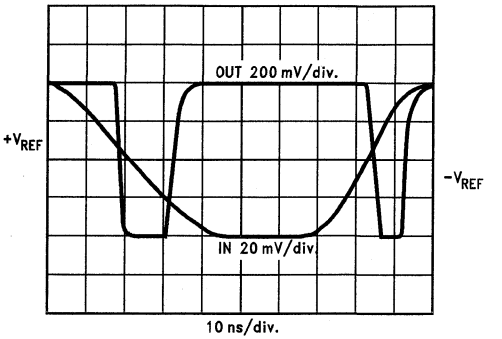
TL/H/10072–4

Typical Applications (T_A = 25°C)

High Speed Window Detector

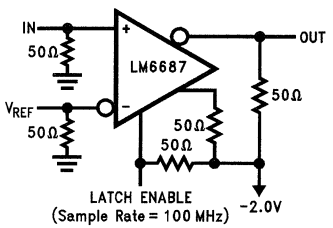


TL/H/10072-5

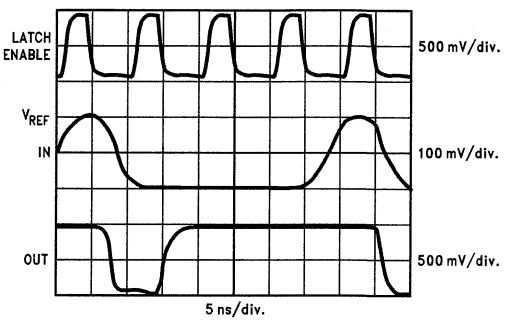


TL/H/10072-6

High Speed Sampling

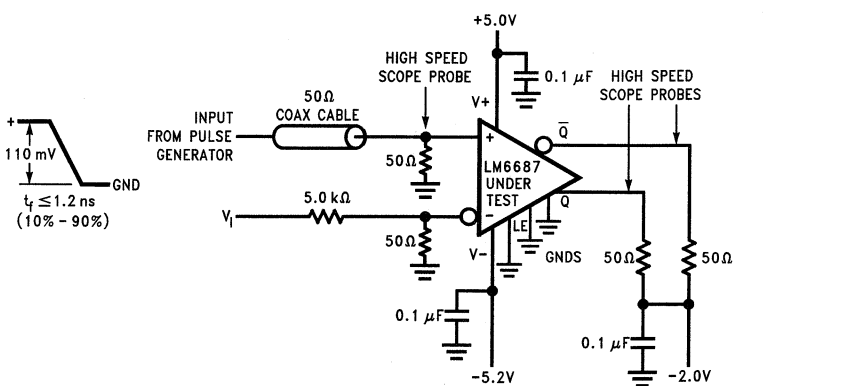


TL/H/10072-7



TL/H/10072-8

Application Information



TL/H/10072-9

Propagation Delay Test Circuit

Measurement Of Propagation Delay

Propagation delays $t_{PD}+$ ($\overline{Q}$ output) and $t_{PD}-$ (Q output) are measured with input signal conditions of a 100 mV step with an overdrive of 10 mV (the overdrive is the voltage in excess of that needed to bring the output to the center of its dynamic range). Offset is compensated for by adjusting V_I until outputs are in the linear region while the Pulse Generator is disconnected. V_I is then increased in the positive direction so inverting input changes by 10 mV, i.e. the overdrive condition. Propagation delays are then measured with actual input pulse condition of +110 mV to 0V swing, with a $t_{PD}+$ or $t_{PD}-$ reading taken between the +10 mV level of the input pulse and the 50% point of the outputs.

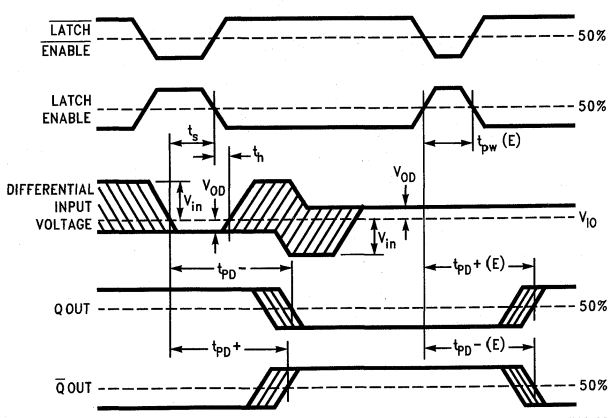
Thermal Considerations

To achieve the high speed of the LM6687, a certain amount of power must be dissipated as heat. This increases the temperature of the die relative to the ambient temperature. In order to be compatible with ECL III and ECL 10,000, which normally use air flow as a means of package cooling, the device must have an air flow across the package of 500 linear feet per minute or greater. Thus, even though different ECL circuits on a printed circuit board may have different power dissipations, all will have the same input and output levels, etc. provided each sees the same air flow and air temperature. This eases design, since the only change in characteristics between devices is due to the increase in ambient temperature of the air passing over the devices. If the LM6687 is operated without air flow, the change in electrical characteristics due to the increased die temperature must be taken into account.

Interconnection Techniques

All high speed ECL circuits require that special precautions be taken for optimum system performance. The LM6687 is particularly critical because it features very high gain (60 dB) at very high frequencies (100 MHz). A ground plane must be provided for a good, low inductance, ground current return path. The impedance at the inputs should be as low as possible and lead lengths as short as practical. It is preferable to solder the device directly to the printed circuit board instead of using a socket. Open wiring on the outputs should be limited to less than one inch, since severe ringing occurs beyond this length. For longer lengths, the printed circuit interconnections become microstrip transmission lines when backed up by a ground plane, with a characteristic impedance of 50 to 150Ω. Reflections will occur unless the line is terminated in its characteristic impedance. The termination resistors normally go to −2.0V, but a Thevenin equivalent to V− can be used at some increase in power. Best results are usually obtained with the terminating resistor at the end of the driven line. The lower impedance lines are more suitable for driving capacitive loads. The supply voltages should be decoupled with RF capacitors connected to the ground plane as close to the device supply leads as possible.

Timing Diagram



TL/H/10072–10

Key to Timing Diagram

WAVEFORM	INPUTS	OUTPUTS
	MUST BE STEADY	WILL BE STEADY
	MAY CHANGE FROM H TO L	WILL BE CHANGING FROM H TO L
	MAY CHANGE FROM L TO H	WILL BE CHANGING FROM L TO H

TL/H/10072–11

Note: The setup and hold times are a measure of the time required for an input signal to propagate through the first stage of the comparator to reach the latching circuitry. Input signal changes occurring before t_S will be detected and held; those occurring after t_h will not be detected. Changes between t_s and t_h may or may not be detected.

Definition of Terms

V_{IO} **Input Offset Voltage**—That voltage which must be applied between the two input terminals through two equal resistances to obtain zero voltage between the two outputs.

$\Delta V_{IO}/\Delta T$ **Average Temperature Coefficient of Input Offset Voltage**—The ratio of the change in input offset voltage over the operating temperature range to the temperature range.

I_{IO} **Input Offset Current**—The difference between the currents into the two input terminals when there is zero voltage between the two outputs.

I_{IB} **Input Bias Current**—The average of the two input currents.

R_I **Input Resistance**—The resistance looking into either input terminal with the other grounded.

C_I **Input Capacitance**—The capacitance looking into either input terminal with other grounded.

V_{CM} **Common Mode Voltage Range**—The range of voltages on the input terminals for which the offset and propagation delay specifications apply.

CMR **Common Mode Rejection**—The ratio of the input voltage range to the peak-to-peak change in input offset voltage over this range.

PSRR **Power Supply Rejection Ratio**—The ratio of the change in input offset voltage to the change in power supply voltages producing it.

V_{OH} **Output Voltage HIGH**—The logic HIGH output voltage with an external pull-down resistor returned to a negative supply.

V_{OL} **Output Voltage LOW**—The logic LOW output voltage with an external pull-down resistor returned to a negative supply.

$I+$ **Positive Supply Current**—The current required from the positive supply to operate the comparator.

$I-$ **Negative Supply Current**—The current required from the negative supply to operate the comparator.

P_C **Power Consumption**—The power dissipated by the comparator with both outputs terminated in 50Ω to −2.0V.

Switching Terms (see Timing Diagram)

t_{PD+} **Input to Output HIGH Delay**—The propagation delay measured from the time the input signal crosses the input offset voltage to the 50% point of an output LOW to HIGH transition.

t_{PD-} **Input to Output LOW Delay**—The propagation delay measured from the time the input signal crosses the input offset voltage to the 50% point of an output HIGH to LOW transition.

$t_{PD+(E)}$ **Latch Enable to Output HIGH Delay**—The propagation delay measured from the 50% point of the Latch Enable signal LOW to HIGH transition to the 50% point of an output LOW to HIGH transition.

$t_{PD-(E)}$ **Latch Enable to Output LOW Delay**—The propagation delay measured from the 50% point of the Latch Enable signal HIGH to LOW transition to the 50% point of an output HIGH to LOW transition.

t_S **Minimum Setup Time**—The minimum time before the negative transition of the Latch Enable signal that an input signal change must be present in order to be acquired and held at the outputs.

t_h **Minimum Hold Time**—The minimum time after the negative transition of the Latch Enable signal that the input signal must remain unchanged in order to be acquired and held at the outputs.

$t_{pw(E)}$ **Minimum Latch Enable Pulse Width**—The minimum time that the Latch Enable signal must be HIGH in order to acquire and hold an input signal change.

Other Symbols

T_A Ambient temperature
R_S Input source resistance
V_{CC} Supply voltages
$V+$ Positive supply voltage
$V-$ Negative supply voltage
V_T Output load terminating voltage
R_L Output load resistance
V_{IN} Input pulse amplitude
V_{OD} Input overdrive
f Frequency

National Semiconductor

LP265/LP365 Micropower Programmable Quad Comparator

General Description

The LP365 consists of four independent voltage comparators. The comparators can be programmed, four at the same time, for various supply currents, input currents, response times and output current drives. This is accomplished by connecting a single resistor between the V_{CC} and I_{SET} pins.

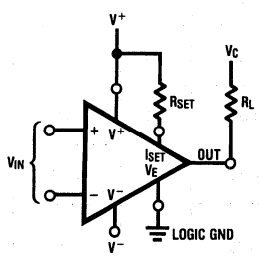
These comparators can be operated from split power supplies or from a single power supply over a wide range of voltages. The input can sense signals at ground level even with single supply operation. The unique output NPN transistor stages are uncommitted to either power supply. They can be connected directly to various logic system supplies so that they are highly flexible to interface with various logic families.

Application areas include battery power circuits, threshold detectors, zero crossing detectors, simple serial A/D converters, VCO, multivibrators, voltage converters, power sequencers, and high performance V/F converters, and RTD linearization.

Features

- Single programming resistor to tailor power consumption, input current, speed and output current drive capability
- Wide single supply voltage range or dual supplies (4 V_{DC} to 36 V_{DC} or ±2.0 V_{DC} to ±18 V_{DC})
- Low supply current drain (10 μA) and low power consumption (10 μW/comparator) @ I_{SET} = 0.5 μA V_{CC} = 5V_{DC}
- Uncommitted output stage—selectable output levels
- Output directly compatible with DTL, TTL, CMOS, MOS or other special logic families
- Input common-mode range includes ground
- Differential input voltage equal to the power supply voltage

Typical Connection



TL/H/5023–1

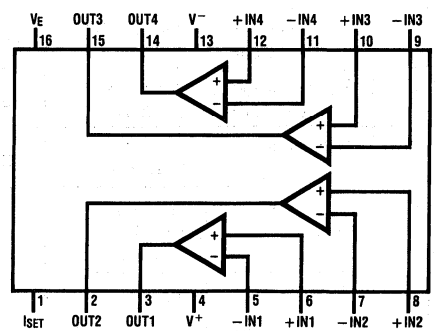
Programming Equation

$$I_{SET} = \frac{(V^+) - (V^-) - 1.3V}{R_{SET}}$$

$$I_{SUPPLY} \approx 22 \times I_{SET}$$

Connection Diagram

Dual-In-Line Package



TOP VIEW

TL/H/5023–2

Order Number LP365M, LP265N, LP365AN or LP365N
See NS Package Numbers M16A or N16A

3

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	36 V_{DC} or ± 18 V_{DC}
Differential Input Voltage	± 36 V_{DC}
Input Voltage (Note 1)	−0.3V to +36 V_{DC}
Output Short Circuit to V_E (Note 2)	Continuous
V_{OUT} with Respect to V_E	$V_E - 7V \le V_{OUT} \le V_E + 36V$
ESD Tolerance (Note 10)	2000V

	M Package	N Package
Power Dissipation (Note 3)	500 mW	500 mW
T_j Max	115°C	115°C
θ_{jA}	115°C/W	90°C/W
Lead Temp.		
(Soldering—10 sec.)		260°C
(Vapor Phase—60 sec.)	215°C	
(Infrared—15 sec.)	220°C	

Operating Temp. Range LP365: $0°C \le T_A \le +70°C$

LP265: $-40°C \le T_A \le +85°C$

Storage Temp. Range $-40°C < T_A < +150°C$

Electrical Characteristics (Note 4) Low power $V_S = 5V$, $I_{SET} = 10\ \mu A$

Symbol	Parameter	Conditions	LP365A			LP265/LP365			Units (Limit)
			Typ	Tested Limit (Note 5)	Design Limit (Note 6)	Typ	Tested Limit (Note 5)	Design Limit (Note 6)	
V_{OS}	Input Offset Voltage	$V_{CM} = 0V$, $R_S = 100$	1	3	**6**	3	6	**9**	mV (Max)
I_{OS}	Input Offset Current	$V_{CM} = 0V$ LP265	2	20	**50**	4	25	**75**	nA (Max)
						4	25	**150**	
I_B	Input Bias Current	$V_{CM} = 0V$ LP265	10	50	**125**	15	75	**200**	nA (Max)
						15	75	**300**	
A_{VOL}	Large Signal Voltage Gain	$R_L = 100k$	500	50	**50**	300	25	**25**	V/mV (Min)
V_{CM}	Input Common-Mode Voltage Range			0	**0**		0	**0**	V (Max)
				3	**3**		3	**3**	V (Min)
CMRR	Common-Mode Rejection Ratio	$0 \le V_{CM} \le 3V$	85	75	**70**	80	75	**70**	dB (Min)
PSRR	Supply Voltage Rejection Ratio	$\pm 2.5V \le V_S \le \pm 3.5V$	75	65	**65**	70	65	**65**	dB (Min)
I_S	Supply Current	All Inputs = 0V, $R_L = \infty$	215	250	**300**	225	275	**300**	μA (Max)
V_{OH}	Output Voltage High	$V_C = 5V$, $V_E = 0V$, $R_L = 100k$		4.9	**4.5**		4.9	**4.5**	V (Min)
V_{OL}	Output Voltage Low	$V_E = 0V$		0.4	**0.4**		0.4	**0.4**	V (Max)
I_{SINK}	Output Sink Current	$V_E = 0V$, $V_O = 0.4V$	2.4	1.2	**0.6**	2.0	0.8	**0.4**	mA (Min)
I_{LEAK}	Output Leakage Current	$V_C = 5V$, $V_E = 0V$	2	50	**5000**	2	100	**5000**	nA (Max)
t_R	Response Time	$V_{CC} = 5V$, $V_E = 0V$, $R_L = 5k$, $C_L = 10$ pF (Note 7)	4			4			μs

Electrical Characteristics (Continued) (Note 8) High power $V_S = \pm 15V$, $I_{SET} = 100\ \mu A$

Symbol	Parameter	Conditions	LP365A			LP265/LP365			Units (Limit)
			Typ	Tested Limit (Note 5)	Design Limit (Note 6)	Typ	Tested Limit (Note 5)	Design Limit (Note 6)	
V_{OS}	Input Offset Voltage	$V_{CM} = 0V$, $R_S = 100$	1	3	**6**	3	6	**9**	mV (Max)
I_{OS}	Input Offset Current	$V_{CM} = 0V$ LP265	5	50	**100**	10	90	**200**	nA (Max)
						10	90	**500**	
I_B	Input Bias Current	$V_{CM} = 0V$ LP265	60	200	**500**	80	300	**500**	nA (Max)
						80	300	**800**	
A_{VOL}	Large Signal Voltage Gain	$R_L = 15k$	500	100	**100**	500	100	**100**	V/mV (Min)
V_{CM}	Input Common-Mode Voltage Range			−15	**−15**		−15	**−15**	V (Max)
				13	**13**		13	**13**	V (Min)
CMRR	Common-Mode Rejection Ratio	$-15V \le V_{CM} \le 13V$	85	75	**70**	80	75	**70**	dB (Min)
PSRR	Supply Voltage Rejection Ratio	$\pm 10V \le V_S \le \pm 15V$	80	70	**70**	75	70	**70**	dB (Min)
I_S	Supply Current	All Inputs = 0V, $R_L = \infty$, LP265	2.6	3	**3.3**	2.8	3.5	**3.7**	mA (Max)
						2.8	3.5	**4.3**	
V_{OH}	Output Voltage High	$V_C = 5V$, $V_E = 0V$, $R_L = 100k$		4.9	**4.5**		4.9	**4.5**	V (Min)
V_{OL}	Output Voltage Low	$V_E = 0V$		0.4	**0.4**		0.4	**0.4**	V (Max)
I_{SINK}	Output Sink Current	$V_E = 0V$, $V_O = 0.4V$	10	8	**5.5**	7.5	6	**4**	mA (Min)
I_{LEAK}	Output Leakage Current	$V_C = 15V$, $V_E = -15V$	5	50	**5000**	5	50	**5000**	nA (Max)
t_R	Response Time	$V_{CC} = 5V$, $V_E = 0V$, $R_L = 5k$, $C_L = 10$ pF (Note 7)	1.0			1.0			μs

Note 1: The input voltage is not allowed to go 0.3V above V^+ or −0.3V below V^- as this will turn on a parasitic transistor causing large currents to flow through the device.

Note 2: Short circuits from the output to V^+ may cause excessive heating and eventual destruction. The current in the output leads and the V_E lead should not be allowed to exceed 30 mA. The output should not be shorted to V^- if $V_E \le (V^-) + 7V$.

Note 3: For operating at elevated temperatures, these devices must be derated based on a thermal resistance of θ_{jA} and T_j max. $T_j = T_A + \theta_{jA} P_D$.

Note 4: Boldface numbers apply at temperature extremes. All other numbers apply at $T_A = T_j = 25°C$. $V^+ = 5V$, $V^- = 0V$, $I_{SET} = 10\ \mu A$, $R_L = 100k$, and $V_C = 5V$ as shown in the Typical Connection diagram.

Note 5: Guaranteed and 100% production tested.

Note 6: Guaranteed (but not 100% production tested) over the operating temperature and supply voltage ranges. These limits are not used to calculate out-going quality levels.

Note 7: The response time specified is for a 100 mV input step with 5 mV overdrive.

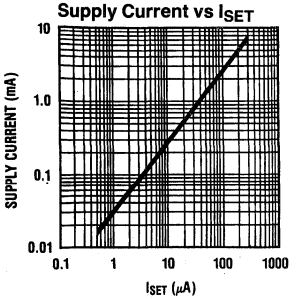
Note 8: Boldface numbers apply at temperature extremes. All other numbers apply at $T_A = T_j = 25°C$. $V^+ = +15V$, $V^- = -15V$, $I_{SET} = 100\ \mu A$, $R_L = 100k$, and $V_C = 5V$ as shown in the Typical Connection diagram.

Note 9: See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

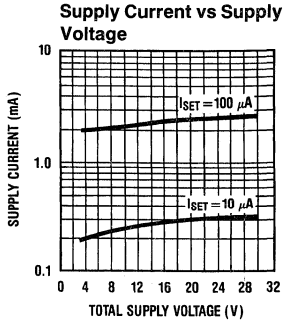
Note 10: Human body model, 1.5 kΩ in series with 100 pF.

Typical Performance Characteristics

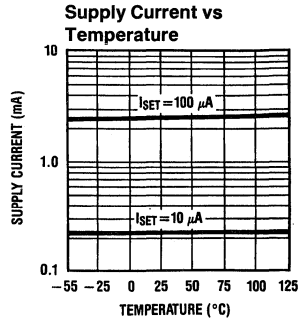
Supply Current vs I_{SET}



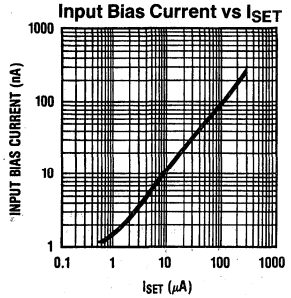
Supply Current vs Supply Voltage



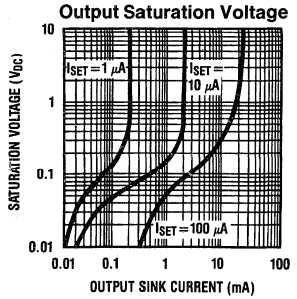
Supply Current vs Temperature



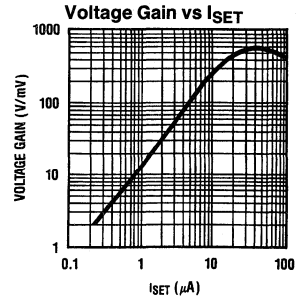
Input Bias Current vs I_{SET}



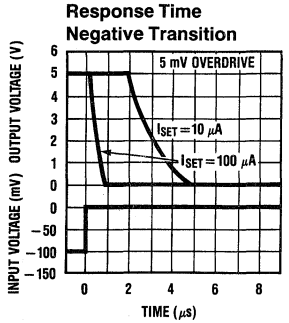
Output Saturation Voltage



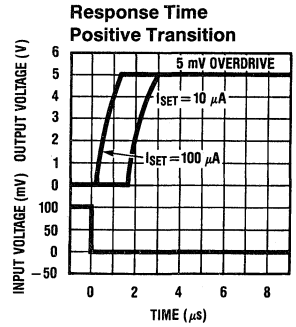
Voltage Gain vs I_{SET}



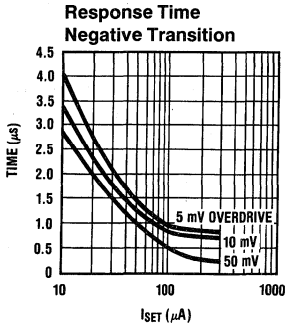
Response Time Negative Transition



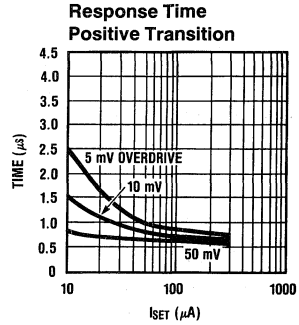
Response Time Positive Transition



Response Time Negative Transition



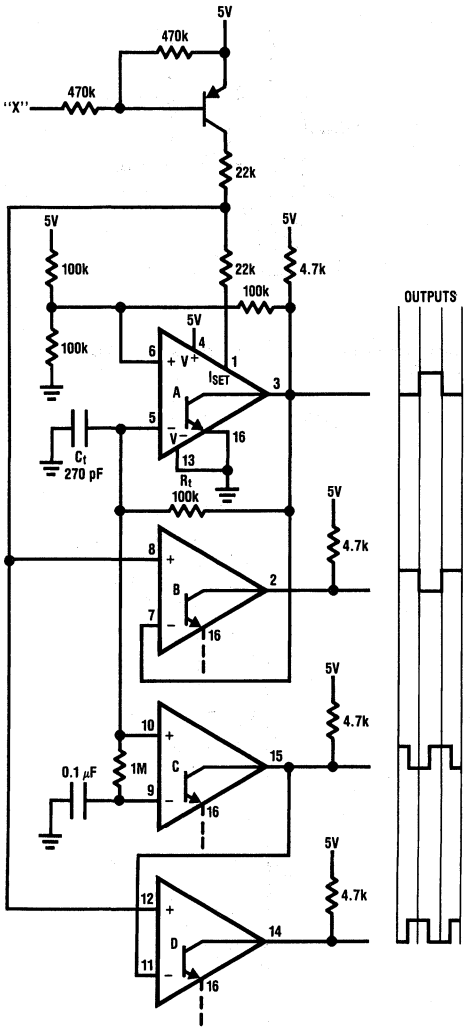
Response Time Positive Transition



TL/H/5023–3

Typical Applications

Gated 4-Phase Oscillator



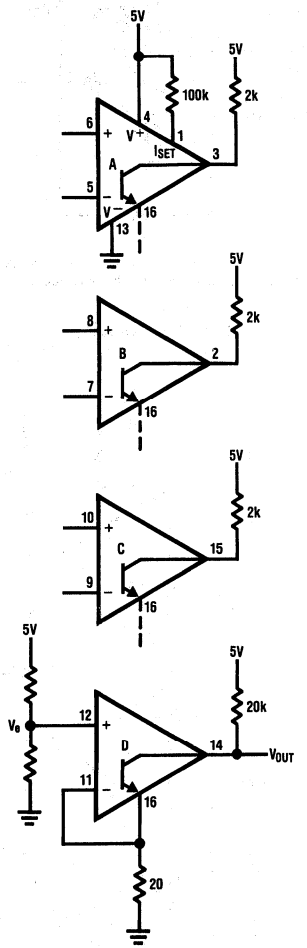
TL/H/5023–4

$f = 20$ kHz

$$f = \frac{1}{1.6 \bullet R_t \bullet C_t}$$

All four phases run when X is low. When X is high, oscillation stops and power drain is zero.

"Voting" Comparator

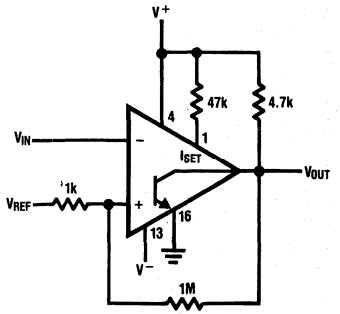


TL/H/5023–5

If V_E = 0.25V, then V_{OUT} will be low if 1 of the 3 other outputs are low. Choice of V_E = 0.50V causes V_{OUT} to be low if 2 of the 3 other outputs are low; V_E = 0.75V will cause V_{OUT} to be low if all 3 other outputs are low.

Typical Applications (Continued)

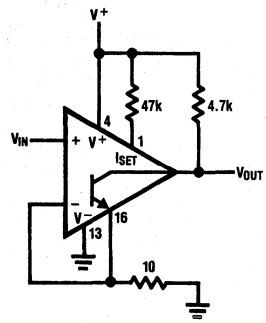
Ordinary Hysteresis



TL/H/5023–6

It is a good practice to add a few millivolts of positive feedback to prevent oscillation when the input voltage is near the threshold.

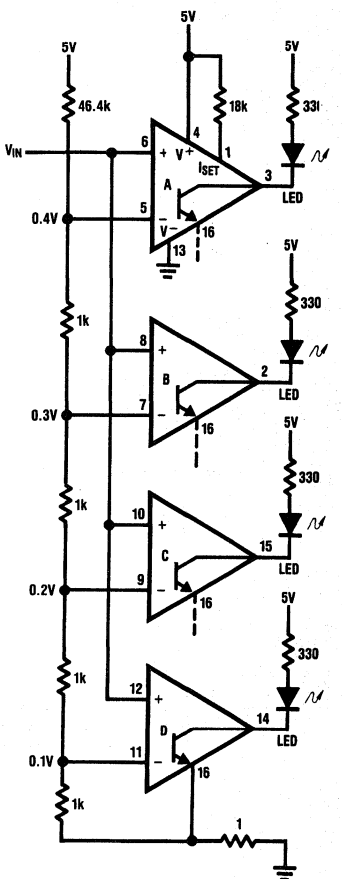
Hysteresis from Emitter



TL/H/5023–7

Positive feedback from the emitter can also prevent oscillations when V_{IN} is near the threshold.

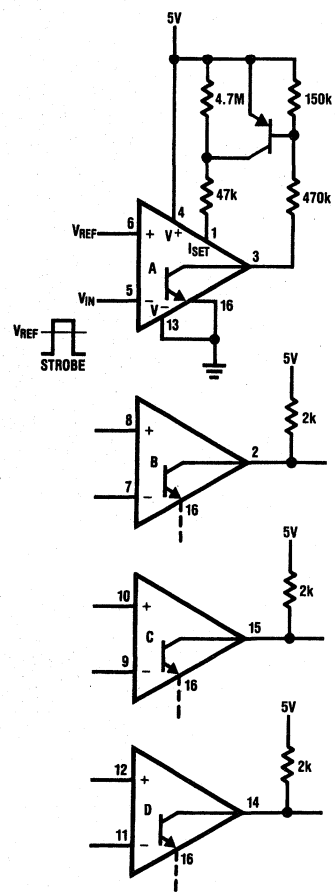
Bar-Graph Display



TL/H/5023–8

The positive feedback from pin 16 provides hysteresis.

Level-Sensitive Strobe

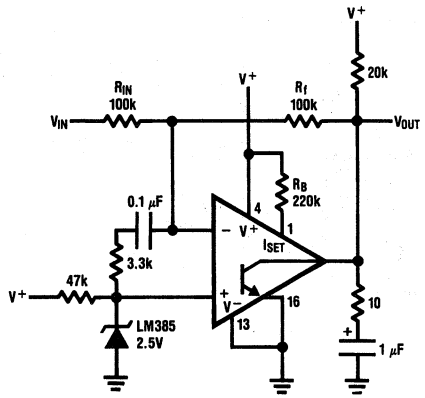


TL/H/5023–9

Comparators B, C, and D do not respond until activated by the signal applied to comparator A.

Typical Applications (Continued)

Slow Op Amp (Inverter)

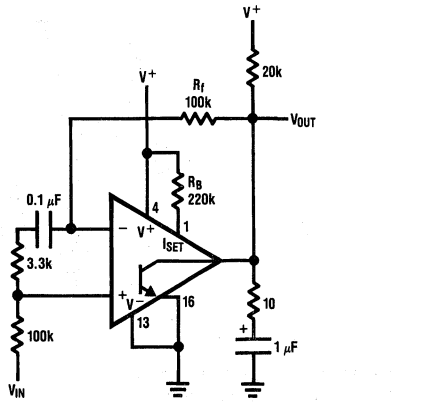


TL/H/5023–10

$R_B = V^+/20\ \mu A$

Unlike most comparators, the LP365 can be used as an op amp, if suitable R-C damping networks are used.

Slow Op Amp (Unity-Gain Follower)

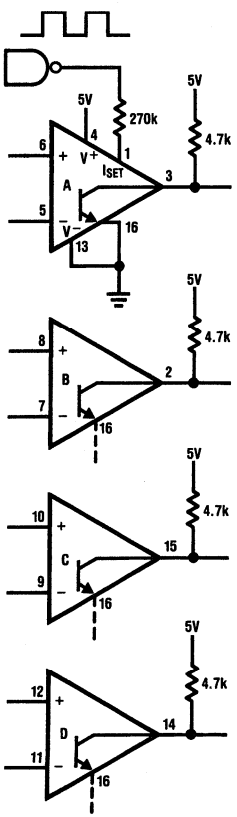


TL/H/5023–11

$R_B = V^+/20\ \mu A$

The LP365 can also be used as a high-input-impedance follower-amplifier with the damping components shown.

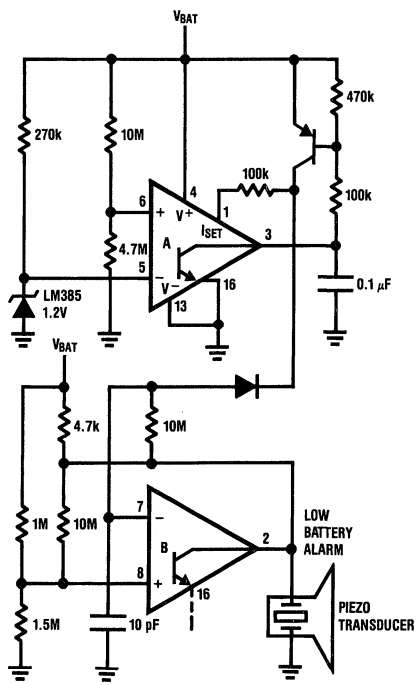
Chopping Outputs



TL/H/5023–12

Chopping the outputs by modulating the I_{SET} current allows data to be transmitted via opto-couplers, transformers, etc.

Low Battery Detector



TL/H/5023–13

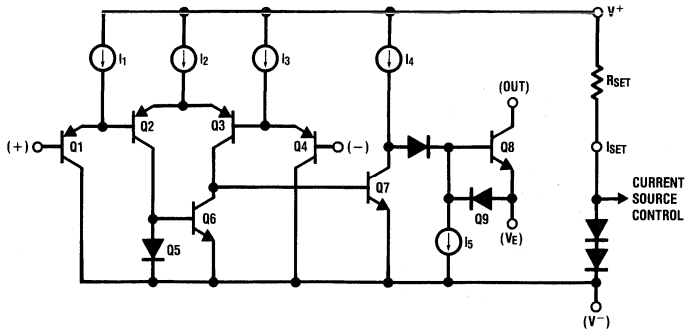
I_S @ 6V = 45 μA

I_S @ 3.8V = 1 μA

f = 3 kHz

Comparator A detects when the supply voltage drops to 4V and enables comparator B to drive a piezoelectric alarm.

Simplified Schematic



TL/H/5023–14

Current sources are programmed by I_{SET}

V_E is common to all 4 comparators

National Semiconductor

LP311 Voltage Comparator

General Description

The LP311 is a low power version of the industry-standard LM311. It takes advantage of stable high-value ion-implanted resistors to perform the same function as an LM311, with a 30:1 reduction in power drain, but only a 6:1 slowdown of response time. Thus the LP311 is well suited for battery-powered applications, and all other applications where fast response is not needed. It operates over a wide range of supply voltages from 36V down to a single 3V supply, with less than 200 μA drain, but it is still capable of driving a 25 mA load. The LP311 is quite easy to apply without any oscillation, if ordinary precautions are taken to minimize stray coupling from the output to either input or to the balance pins (as described in the LM311 datasheet Application Hints).

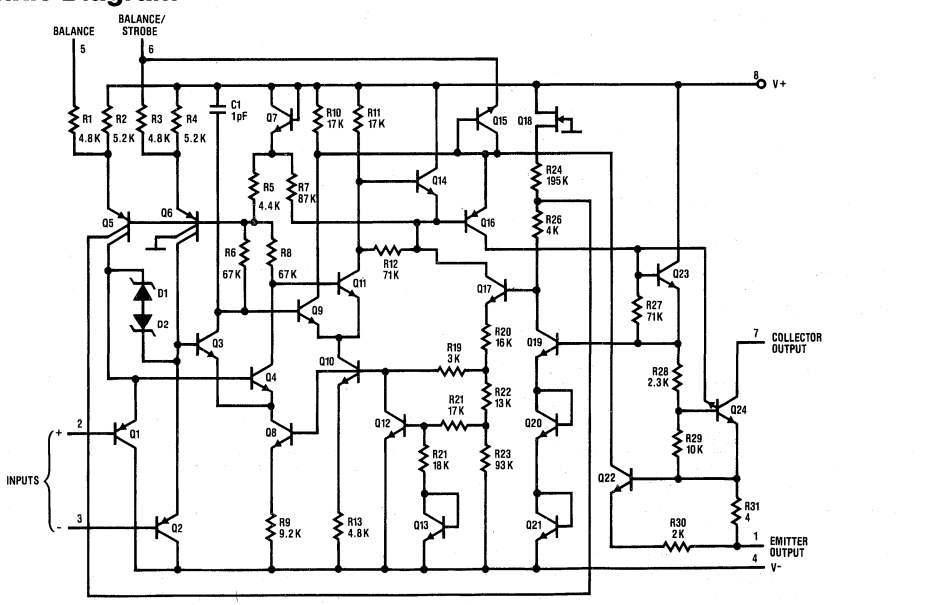
Features

- Low power drain, 900 μW on 5V supply
- Operates from $\pm$15V or a single supply as low as 3V
- Output can drive 25 mA
- Emitter output can swing below negative supply
- Response time: 1.2 μs
- Same pin-out as LM311
- Low input currents: 2 nA of offset, 15 nA of bias
- Large common-mode input range: $-$14.6V to 13.6V with $\pm$15V supply

Applications

- Level-detector for battery-powered instruments
- Low-power lamp or relay driver
- Low-power zero-crossing detector

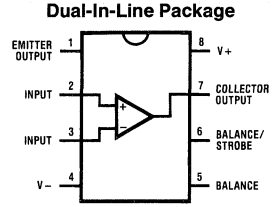
Schematic Diagram



TL/H/5711–7

Connection Diagram

Dual-In-Line Package



TL/H/5711–4

Top View

Order Number LP311M or LP311N
See NS Package Numbers M08A or N08E

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Total Supply Voltage (V_{8-4})	36V
Collector Output to Negative Supply Voltage (V_{7-4})	40V
Collector Output to Emitter Output	40V
Emitter Output to Negative Supply Voltage (V_{1-4})	±30V
Differential Input Voltage	±30V
Input Voltage (Note 1)	±15V
Power Dissipation (Note 2)	500 mW
Output Short Circuit Duration	10 sec
Operating Temperature Range	0°C to 70°C
Storage Temperature Range	−65°C to 150°C
Lead Temperature (Soldering, 10 seconds)	260°C

Electrical Characteristics

These specifications apply for V_S = ±15V and 0°C ≤ T_A ≤ 70°C, unless otherwise specified.

Parameter	Conditions	Min	Typ	Max	Units
Input Offset Voltage (Notes 3, 4)	T_A=25°C, R_S≤100k		2.0	7.5	mV
Input Offset Current (Notes 3, 4)	T_A=25°C		2.0	25	nA
Input Bias Current (Note 3)	T_A=25°C		15	100	nA
Voltage Gain	T_A = 25°C, R_L=5k	40	200		V/mV
Response Time (Note 5)	T_A=25°C		1.2		μs
Saturation Voltage (Note 6)	V_{IN}≤ −10 mV, I_{OUT}=25 mA $T_{A=25°C}$		0.4	1.5	V
Strobe Current (Note 7)	T_A=25°C	100	200	300	μA
Output Leakage Current	V_{IN}≥10 mV, V_{OUT}=35V T_A=25°C		0.2	100	nA
Input Offset Voltage (Notes 3, 4)	R_S≤100k			10	mV
Input Offset Current (Notes 3, 4)				35	nA
Input Bias Current (Note 3)				150	nA
Input Voltage Range		V^-+0.5	+13.7, −14.7	V^+−1.5	V
Saturation Voltage (Note 6)	V^+≥4.5V, V^-=0V V_{IN}≤ −10 mV, I_{SINK}≤1.6 mA		0.1	0.4	V
Positive Supply Current	T_A=25°C, Output on		150	300	μA
Negative Supply Current	T_A=25°C		80	180	μA
Minimum Operating Voltage	T_A=25°C		3.0	3.5	V

Note 1: This rating applies for ±15V supplies. The positive input voltage limit is 30V above the negative supply. The negative input voltage limit is equal to the negative supply voltage or 30V below the positive supply, whichever is less.

Note 2: The maximum junction temperature of the LP311 is 85°C. For operating at elevated temperatures, devices in the dual-in-line package must be derated based on a thermal resistance of 160°C/W, junction to ambient.

Note 3: The offset voltage, offset current and bias current specifications apply for any supply voltage from a single 4V supply up to ±15V supplies.

Note 4: The offset voltages and offset currents given are the maximum values required to drive the output within a volt of either supply with 1 mA load. Thus, these parameters define an error band and take into account the worst-case effects of voltage gain and input impedance.

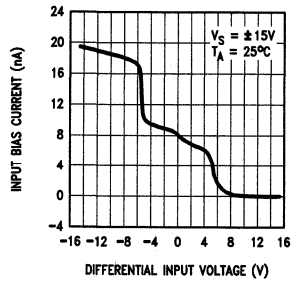
Note 5: The response time specified is for a 100 mV input step with 5 mV overdrive.

Note 6: Saturation voltage specification applies to collector-emitter voltage (V7-1) for $V_{COLLECTOR}$ ≤ (V^+ − 3V).

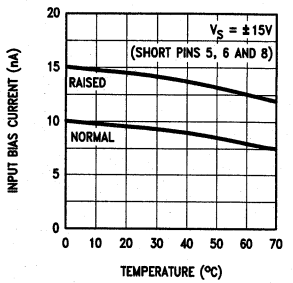
Note 7: This specification gives the range of current which must be drawn from the strobe pin to ensure the output is properly disabled. Do not short the strobe pin to ground. It should be current driven, 100 μA to 300 μA.

Typical Performance Characteristics

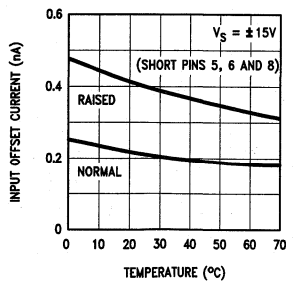
Input Characteristics



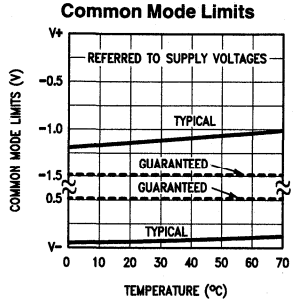
Input Bias Current



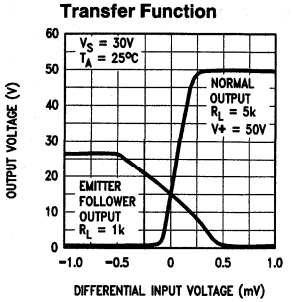
Input Offset Current



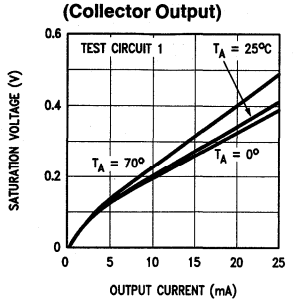
Common Mode Limits



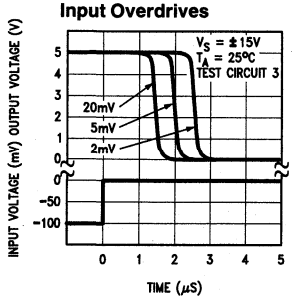
Transfer Function



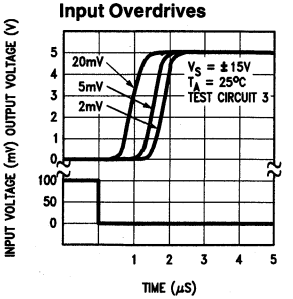
Output Saturation Voltage (Collector Output)



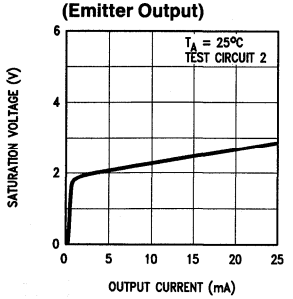
Response Time for Various Input Overdrives



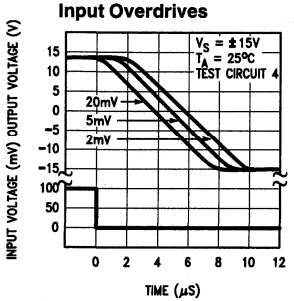
Response Time for Various Input Overdrives



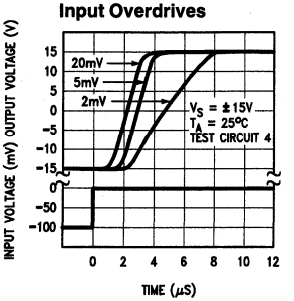
Output Saturation Voltage (Emitter Output)



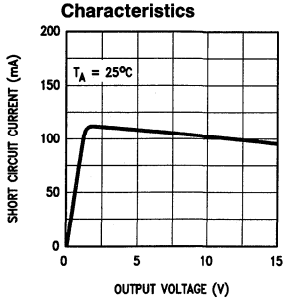
Response Time for Various Input Overdrives



Response Time for Various Input Overdrives



Output Limiting Characteristics



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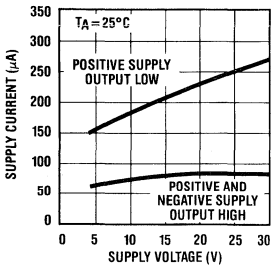
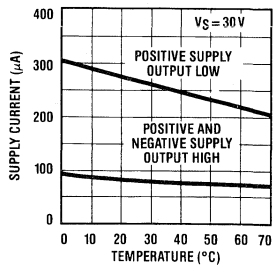
Typical Performance Characteristics (Continued)

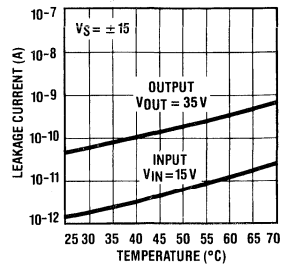
Supply Current



Supply Current



Leakage Currents



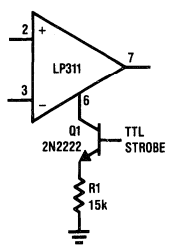
TL/H/5711–6

Applications Information

For applications information and typical applications, refer to the LM311 datasheet.

Auxiliary Circuits

Strobing



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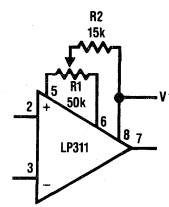
Note: Do not ground strobe pin.

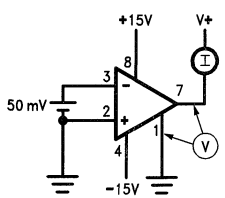
Offset Balancing



TL/H/5711–2

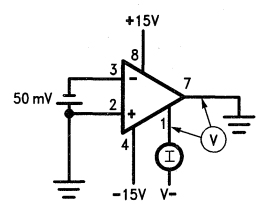
Test Circuits

Test Circuit 1 (Collector Output)



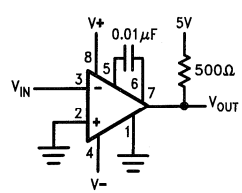
TL/H/5711–8

Test Circuit 2 (Emitter Output)



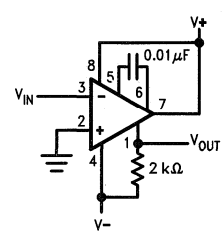
TL/H/5711–9

Test Circuit 3 (Collector Output)



TL/H/5711–10

Test Circuit 4 (Emitter Output)



TL/H/5711–11

National Semiconductor

LP339 Ultra-Low Power Quad Comparator

General Description

The LP339 consists of four independent voltage comparators designed specifically to operate from a single power supply and draw typically 60 μA of power supply drain current over a wide range of power supply voltages. Operation from split supplies is also possible and the ultra-low power supply drain current is independent of the power supply voltage. These comparators also feature a common-mode range which includes ground, even when operated from a single supply.

Applications include limit comparators, simple analog-to-digital converters, pulse, square and time delay generators; VCO's; multivibrators; high voltage logic gates. The LP339 was specifically designed to interface with the CMOS logic family. The ultra-low supply current makes the LP339 valuable in battery powered applications.

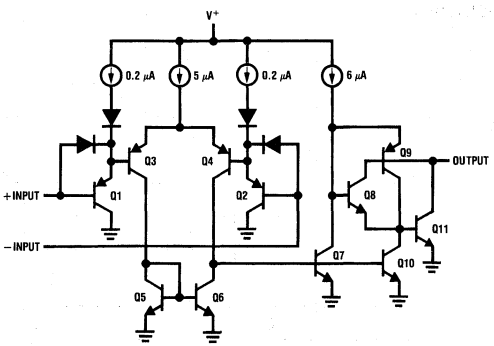
Advantages

- Ultra-low power supply drain suitable for battery applications
- Single supply operation
- Sensing at ground
- Compatible with CMOS logic family
- Pin-out identical to LM339

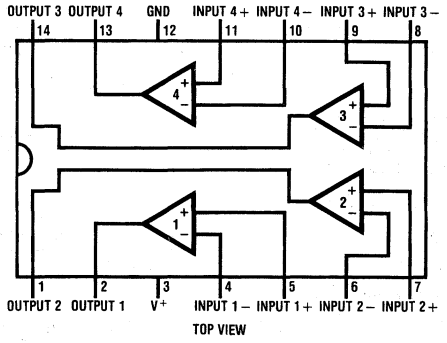
Features

- Ultra-low power supply current drain (60 μA)—independent of the supply voltage (75 μW/comparator at +5 V_{DC})
- Low input biasing current 3 nA
- Low input offset current ±0.5 nA
- Low input offset voltage ±2 mV
- Input common-mode voltage includes ground
- Output voltage compatible with MOS and CMOS logic
- High output sink current capability (30 mA at V_O=2 V_{DC})
- Supply Input protected against reverse voltages

Schematic and Connection Diagrams



TL/H/5226–1



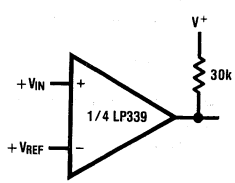
TL/H/5226–2

Order Number LP339M for S.O. Package
See NS Package Number M14A

Order Number LP339N for Dual-In-Line Package
See NS Package Number N14A

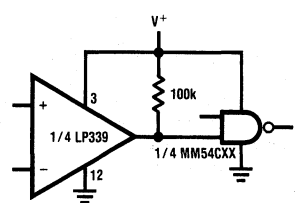
Typical Applications (V^+ = 5.0 V_{DC})

Basic Comparator



TL/H/5226–3

Driving CMOS



TL/H/5226–4

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	36 V_{DC} or ±18 V_{DC}
Differential Input Voltage	±36 V_{DC}
Input Voltage	−0.3 V_{DC} to 36 V_{DC}
Power Dissipation (Note 1) Molded DIP	570 mW
Output Short Circuit to GND (Note 2)	Continuous
Input Current $V_{IN} < -0.3$ V_{DC} (Note 3)	50 mA
Operating Temperature Range	0°C to +70°C
Storage Temperature Range	−65° to +150°C
Soldering Information:	
Dual-In-Line Package (10 sec.)	+260°C
S.O. Package:	
Vapor Phase (60 sec.)	+215°C
Infrared (15 sec.)	+220°C

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

Electrical Characteristics ($V+ = 5$ V_{DC}, Note 4)

Parameter	Conditions	Min	Typ	Max	Units
Input Offset Voltage	$T_A = 25°C$ (Note 9)		±2	±5	mV_{DC}
Input Bias Current	$I_{IN}(+)$ or $I_{IN}(-)$ with the Output in the Linear Range, $T_A = 25°C$ (Note 5)		2.5	25	nA_{DC}
Input Offset Current	$I_{IN}(+) - I_{IN}(-)$, $T_A = 25°C$		±0.5	±5	nA_{DC}
Input Common Mode Voltage Range	$T_A = 25°C$ (Note 6)	0		V+ −1.5	V_{DC}
Supply Current	R_L = Infinite on all Comparators, $T_A = 25°C$		60	100	μA_{DC}
Voltage Gain	V_O = 1 V_{DC} to 11 V_{DC}, $R_L = 15$ kΩ, $V+ = 15$ V_{DC}, $T_A = 25°C$		500		V/mV
Large Signal Response Time	V_{IN} = TTL Logic Swing, $V_{REF} = 1.4$ V_{DC}, $V_{RL} = 5$ V_{DC}, $R_L = 5.1$ kΩ, $T_A = 25°C$		1.3		µSec
Response Time	$V_{RL} = 5$ V_{DC}, $R_L = 5.1$ kΩ, $T_A = 25°C$ (Note 7)		8		µSec
Output Sink Current	$V_{IN}(-) = 1$ V_{DC}, $V_{IN}(+) = 0$, $V_O = 2$ V_{DC}, $T_A = 25°C$ (Note 11)	15	30		mA_{DC}
	$V_O = 0.4$ V_{DC}	0.20	0.70		mA_{DC}
Output Leakage Current	$V_{IN}(+) = 1$ V_{DC}, $V_{IN}(-) = 0$, $V_O = 5$ V_{DC}, $T_A = 25°C$		0.1		nA_{DC}
Input Offset Voltage	(Note 9)			±9	mV_{DC}
Input Offset Current	$I_{IN}(+) - I_{IN}(-)$		±1	±15	nA_{DC}
Input Bias Current	$I_{IN}(+)$ or $I_{IN}(-)$ with Output in Linear Range		4	40	nA_{DC}
Input Common Mode Voltage Range	Single Supply	0		V+ −2.0	V_{DC}
Output Sink Current	$V_{IN}(-) = 1$ V_{DC}, $V_{IN}(+) = 0$, $V_O = 2$ V_{DC}	10			mA_{DC}
Output Leakage Current	$V_{IN}(+) = 1$ V_{DC}, $V_{IN}(-) = 0$, $V_O = 30$ V_{DC}			1.0	μA_{DC}
Differential Input Voltage	All V_{IN}'s ≥ 0 V_{DC} (or V− on split supplies) (Note 8)			36	V_{DC}

Note 1: For elevated temperature operation, T_j max is 125°C for the LP339. θ_{ja} (junction to ambient) is 175°C/W for the LP339N and 120°C/W for the LP339M when either device is soldered in a printed circuit board in a still air environment. The low bias dissipation and the "ON-OFF" characteristic of the outputs keeps the chip dissipation very small ($P_D \leq 100$ mW), provided the output transistors are allowed to saturate.

Note 2: Short circuits from the output to V+ can cause excessive heating and eventual destruction. The maximum output current is approximately 50 mA.

Note 3: This input current will only exist when the voltage at any of the input leads is driven negative. It is due to the collector-base junction of the input PNP transistors becoming forward biased and thereby acting as input clamp diodes. In addition to this diode action, there is also lateral NPN parasitic transistor action on the IC chip. This transistor action can cause the output voltage of the comparators to go to the V+ voltage level (or to ground for a large input overdrive) for the time duration that an input is driven negative. This is not destructive and normal output states will re-establish when the input voltage, which is negative, again returns to a value greater than −0.3 V_{DC} ($T_A = 25°C$).

Note 4: These specifications apply for $V+ = 5V_{DC}$ and $0°C \leq T_A \leq 70°$ C, unless otherwise stated. The temperature extremes are guaranteed but not 100% production tested. These parameters are not used to calculate outgoing AQL.

Note 5: The direction of the input current is out of the IC due to the PNP input stage. This current is essentially constant, independent of the state of the output, so no loading change exists on the reference or the input lines as long as the common-mode range is not exceeded.

Note 6: The input common-mode voltage or either input voltage should not be allowed to go negative by more than 0.3V. The upper end of the common-mode voltage range is V+ −1.5V ($T_A = 25°C$), but either or both inputs can go to 30 V_{DC} without damage.

Note 7: The response time specified is for a 100 mV input step with 5 mV overdrive. For larger overdrive signals 1.3 µs can be obtained. See Typical Performance Characteristics section.

Electrical Characteristics ($V+ = 5\ V_{DC}$, Note 4) (Continued)

Note 8: Positive excursions of input voltage may exceed the power supply level. As long as the other voltage remains within the common-mode range, the comparator will provide a proper output state. The low input voltage state must not be less than $-0.3\ V_{DC}$ (or $0.3\ V_{DC}$ below the magnitude of the negative power supply, if used) at $T_A = 25°C$.

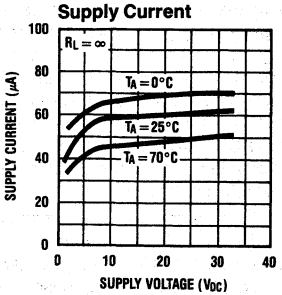
Note 9: At output switch point, $V_O = 1.4V$, $R_S = 0\Omega$ with $V+$ from $5\ V_{DC}$; and over the full input common-mode range ($0\ V_{DC}$ to $V+ - 1.5\ V_{DC}$).

Note 10: For input signals that exceed $V+$, only the overdriven comparator is affected. With a 5V supply, V_{IN} should be limited to 25V maximum, and a limiting resistor should be used on all inputs that might exceed the positive supply.

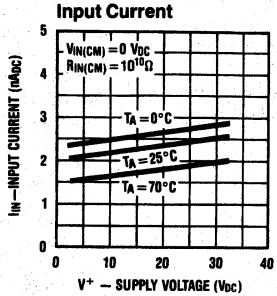
Note 11: The output sink current is a function of the output voltage. The LP339 has a bi-modal output section which allows it to sink large currents via a Darlington connection at output voltages greater than approximately $1.5\ V_{DC}$ and sink lower currents below this point. (See typical characteristics section and applications section).

Typical Performance Characteristics

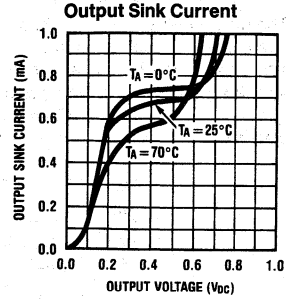
Supply Current



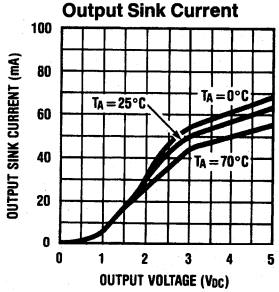
Input Current



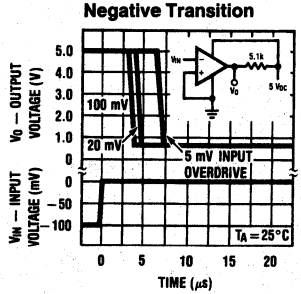
Output Sink Current



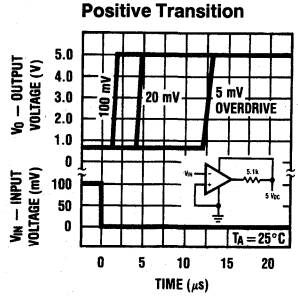
Output Sink Current



Response Times for Various Input Overdrives — Negative Transition



Response Times for Various Input Overdrives — Positive Transition



TL/H/5226–10

Application Hints

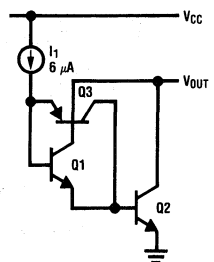
All pins of any unused comparators should be grounded.

The bias network of the LP339 establishes a drain current which is independent of the magnitude of the power supply voltage over the range of from 2 V_{DC} to 30 V_{DC}.

It is usually unnecessary to use a bypass capacitor across the power supply line.

The differential input voltage may be larger than V+ without damaging the device. Protection should be provided to prevent the input voltages from going negative more than −0.3 V_{DC} (at 25°C). An input clamp diode can be used as shown in the application section.

The output section of the LP339 has two distinct modes of operation-a Darlington mode and a grounded emitter mode. This unique drive circuit permits the LP339 to sink 30 mA at $V_O = 2\ V_{DC}$ (Darlington mode) and 700 μA at $V_O = 0.4\ V_{DC}$ (grounded emitter mode). *Figure 1* is a simplified schematic diagram of the LP339 output section.



TL/H/5226–11

FIGURE 1

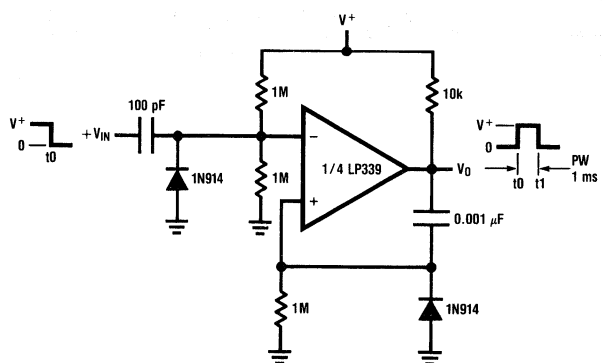
Notice that the output section is configured in a Darlington connection (ignoring Q3). Therefore, if the output voltage is held high enough ($V_O \geq 1\ V_{DC}$), Q1 is not saturated and the output current is limited only by the product of the betas of Q1, Q2 and I1 (and the 60Ω R_{SAT} of Q2). The LP339 is thus capable of driving LED's, relays, etc. in this mode while maintaining an ultra-low power supply current of typically 60 μA.

If transistor Q3 were omitted, and the output voltage allowed to drop below about 0.8 V_{DC}, transistor Q1 would saturate and the output current would drop to zero. The circuit would, therefore, be unable to 'pull' low current loads down to ground (or the negative supply, if used). Transistor Q3 has been included to bypass transistor Q1 under these conditions and apply the current I1 directly to the base of Q2. The output sink current is now approximately I1 times the beta of Q2 (700 μA at $V_O = 0.4\ V_{DC}$). The output of the LP339 exhibits a bi-modal characteristic with a smooth transition between modes. (See Output Sink Current graphs in Typical Performance Characteristics section.)

It is also important to note that in both cases the output is an uncommitted collector. Therefore, many collectors can be tied together to provide an output OR'ing function. An output pull-up resistor can be connected to any available power supply voltage within the permitted power supply voltage range and there is no restriction on this voltage due to the magnitude of the voltage which is applied to the V+ terminal of the LP339 package.

Typical Applications ($V^+ = 15\ V_{DC}$)

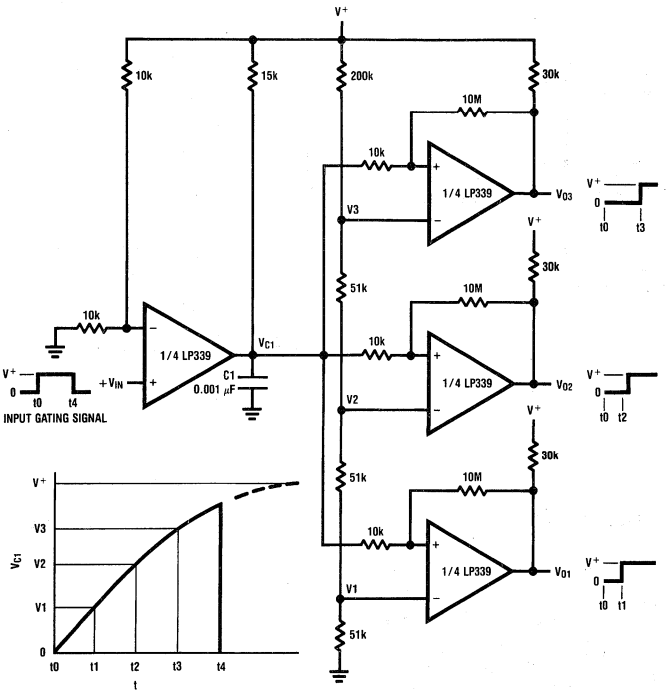
One-Shot Multivibrator



TL/H/5226–13

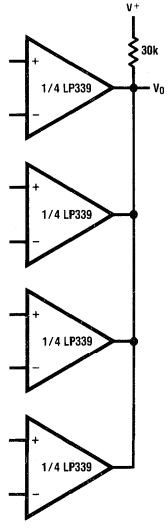
Typical Applications ($V^+ = 15\ V_{DC}$)

Time Delay Generator



TL/H/5226–15

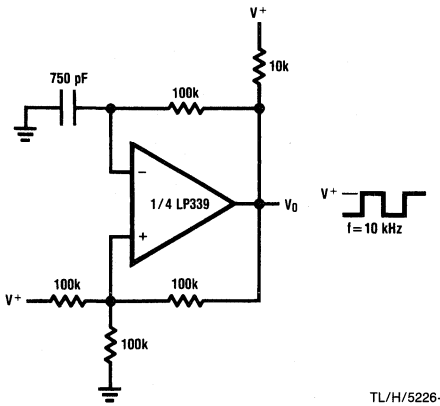
ORing the Outputs



TL/H/5226–16

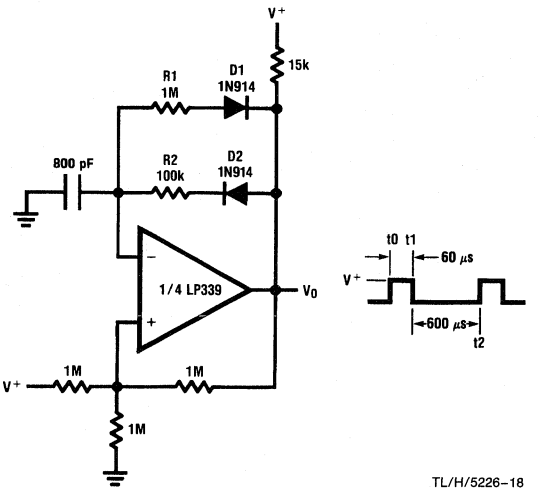
Typical Applications (Continued) ($V^+ = 15\ V_{DC}$)

Squarewave Oscillator



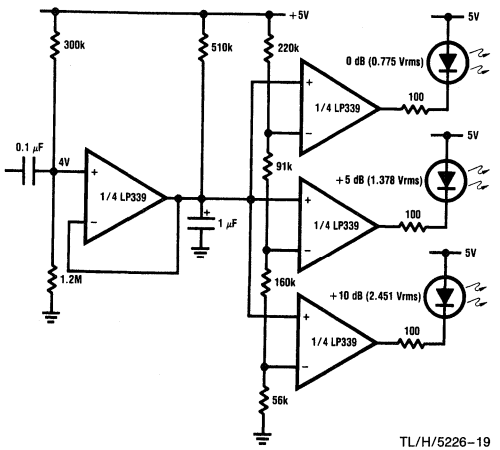
TL/H/5226–17

Pulse Generator



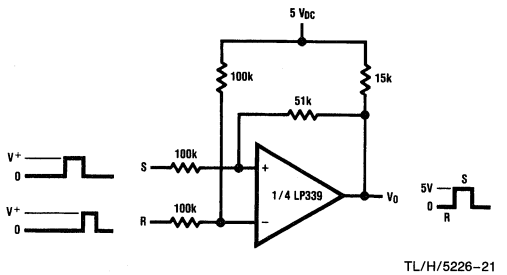
TL/H/5226–18

Three Level Audio Peak Indicator



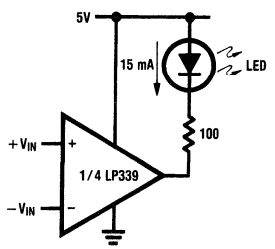
TL/H/5226–19

Bi-Stable Multivibrator



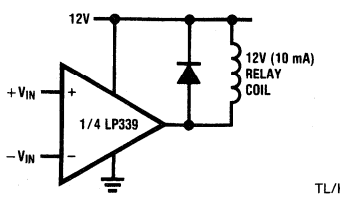
TL/H/5226–21

LED Driver



TL/H/5226–22

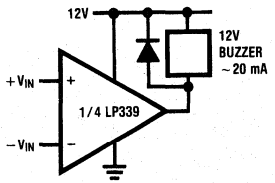
Relay Driver



TL/H/5226–23

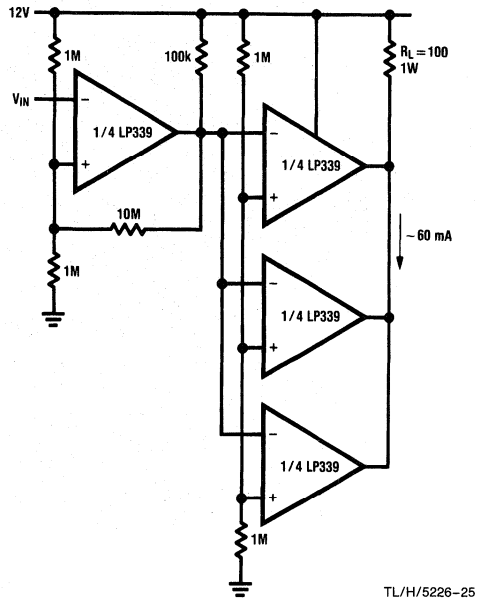
Typical Applications (Continued) (Single Supply)

Buzzer Driver



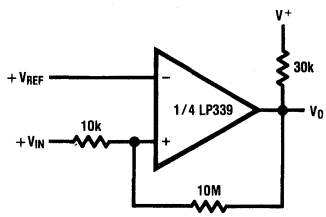
TL/H/5226–24

Comparator With 60 mA Sink Capability



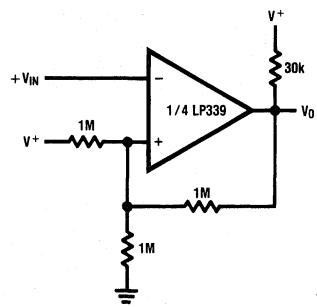
TL/H/5226–25

Non-Inverting Comparator with Hysteresis



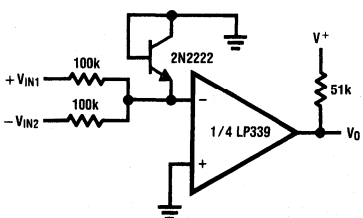
TL/H/5226–26

Inverting Comparator with Hysteresis



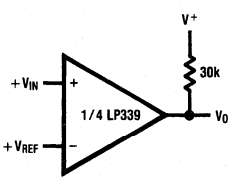
TL/H/5226–27

Comparing Input Voltages of Opposite Polarity



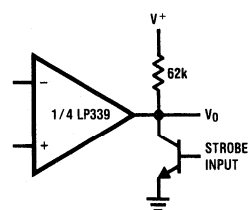
TL/H/5226–28

Basic Comparator



TL/H/5226–29

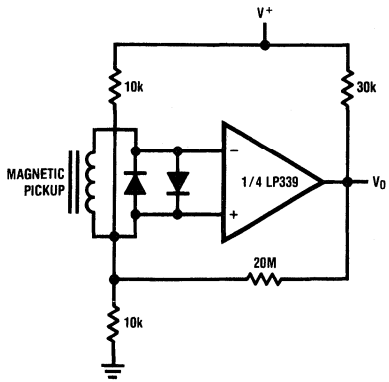
Output Strobing



TL/H/5226–30

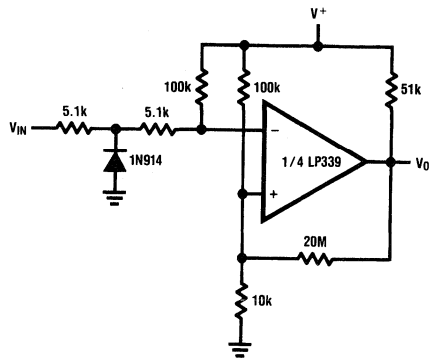
Typical Applications (Continued) (Single Supply)

Transducer Amplifier



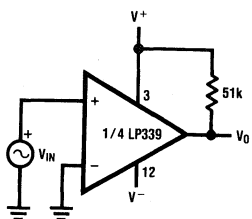
TL/H/5226–31

Zero Crossing Detector (Single Power Supply)



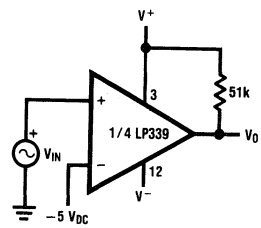
TL/H/5226–32

Split-Supply Applications
Zero Crossing Detector



TL/H/5226–33

Comparator With a Negative Reference



TL/H/5226–34

Section 4

Instrumentation Amplifiers

Section 4 Contents

National Semiconductor

LH0036 Instrumentation Amplifier

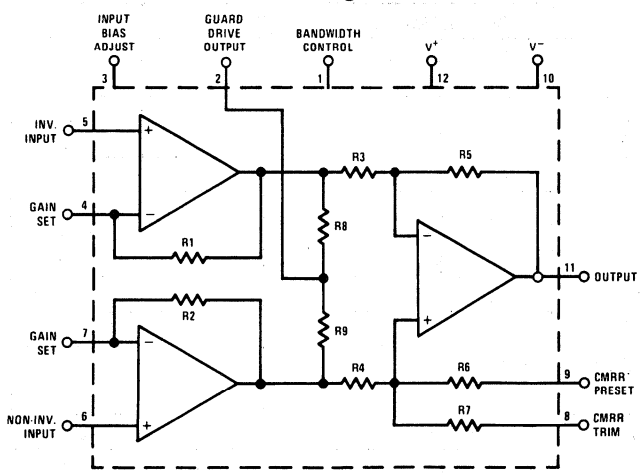
General Description

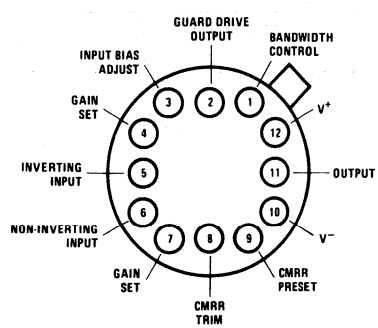
The LH0036C is a micro power instrumentation amplifier designed for precision differential signal processing. Extremely high accuracy can be obtained due to the 300 MΩ input impedance and excellent 100 dB common mode rejection ratio. It is packaged in a hermetic TO-8 package. Gain is programmable from 1 to 1000 with a single external resistor. Power supply operating range is between ±1V and ±18V. Input bias current and output bandwidth are both externally adjustable or can be set by internally set values. The LH0036C is specified for operation over the −25°C to +85°C temperature range.

Features

- High input impedance — 300 MΩ
- High CMRR — 100 dB
- Single resistor gain adjust — 1 to 1000
- Low power — 90 μW
- Wide supply range — ±1V to ±18V
- Adjustable input bias current
- Adjustable output bandwidth
- Guard drive output

Equivalent Circuit and Connection Diagrams





TOP VIEW

TL/H/5545–1

Order Number LH0036CG
See NS Package Number G12B

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications. (Note 5)

Supply Voltage	±18V
Differential Input Voltage	±30V
Input Voltage Range	$\pm V_S$
Shield Drive Voltage	$\pm V_S$
CMRR Preset Voltage	$\pm V_S$
CMRR Trim Voltage	$\pm V_S$
Power Dissipation (Note 3)	1.5W
Short Circuit Duration	Continuous
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec.)	260°C

Operating Temperature Range

LH0036C	−25°C to +85°C

ESD rating to be determined.

Electrical Characteristics (Notes 1 and 2)

Parameter	Conditions	Limits			Units
		LH0036C			
		Min	Typ	Max	
Input Offset Voltage	R_S = 1.0 kΩ, T_A = 25°C		1.0	2.0	mV
(V_{IOS})	R_S = 1.0 kΩ			3.0	mV
Output Offset Voltage	R_S = 1.0 kΩ, T_A = 25°C		5.0	10	mV
(V_{OOS})	R_S = 1.0 kΩ			12	mV
Input Offset Voltage Tempco ($\Delta V_{IOS}/\Delta T$)	$R_S \leq$ 1.0 kΩ		10		μV/°C
Output Offset Voltage Tempco ($\Delta V_{OOS}/\Delta T$)			15		μV/°C
Overall Offset Referred to Input (V_{OS})	A_V = 1.0		6.0		mV
	A_V = 10 A_V = 100 A_V = 1000		1.5 1.05 1.005		mV mV mV
Input Bias Current (I_B)	T_A = 25°C		50	125	nA
				200	nA
Input Offset Current (I_{OS})	T_A = 25°C		20	50	nA
				100	nA
Input Voltage Range	Differential	±10	±12		V
	Common Mode	±10	±12		V
Gain Nonlinearity			0.03		%
Deviation From Gain Equation Formula	A_V = 1 to 1000 (Note 4)		±1.0	±3.0	%

Electrical Characteristics (Notes 1 and 2) (Continued)

Parameter	Conditions	Limits			Units
		LH0036C			
		Min	Typ	Max	
PSRR	$\pm 5.0V \le V_S \le \pm 15V$, $A_V = 1.0$ $\pm 5.0V \le V_S \le \pm 15V$, $A_V = 100$		1.0 0.10	5.0 0.50	mV/V mV/V
CMRR	$A_V = 1.0$ DC to $A_V = 10$ 100 Hz $A_V = 100$ $\Delta R_S = 1.0k$		2.5 0.25 50	5.0 0.50 100	mV/V mV/V μV/V
Output Voltage	$V_S = \pm 15V$, $R_L = 10\ k\Omega$ $V_S = \pm 1.5V$, $R_L = 100\ k\Omega$	±10 ±0.6	±13.5 ±0.8		V V
Output Resistance			0.5		Ω
Supply Current			400	600	μA
Small Signal Bandwidth	$A_V = 1.0$, $R_L = 10\ k\Omega$ $A_V = 10$, $R_L = 10\ k\Omega$ $A_V = 100$, $R_L = 10\ k\Omega$ $A_V = 1000$, $R_L = 10\ k\Omega$		350 35 3.5 350		kHz kHz kHz Hz
Full Power Bandwidth	$V_{IN} = \pm 10V$, $R_L = 10k$, $A_V = 1$		5.0		kHz
Equivalent Input Noise Voltage	0.1 Hz < f < 10 kHz, $R_S < 50\Omega$		20		μV/p-p
Slew Rate	$\Delta V_{IN} = \pm 10V$, $R_L = 10\ k\Omega$, $A_V = 1.0$		0.3		V/μS
Settling Time	To ±10 mV, $R_L = 10\ k\Omega$, $\Delta V_{OUT} = 1.0V$ $A_V = 1.0$ $A_V = 100$		 3.8 180		 μS μS

Note 1: Unless otherwise specified, all specifications apply for $V_S = \pm 15V$, Pins 1, 3, and 9 grounded, −25°C to +85°C.

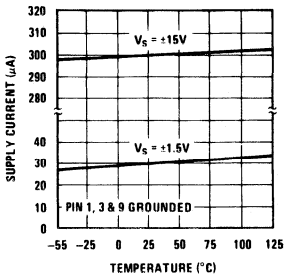
Note 2: All typical values are for $T_A = 25°C$.

Note 3: The maximum junction temperature is 150°C. For operation at elevated temperature derate the G package on a thermal resistance of 90°C/W.

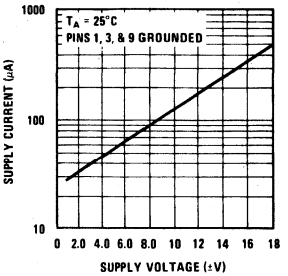
Note 4: $A_V = 1000$ guaranteed by design and testing at $A_V = 100$.

Typical Performance Characteristics

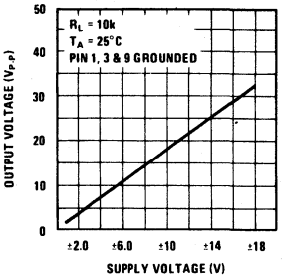
Supply Current vs Temperature



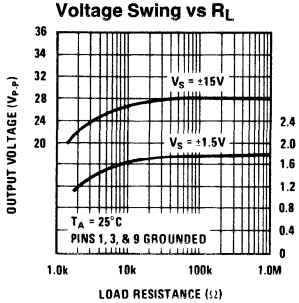
Supply Current vs Supply Voltage



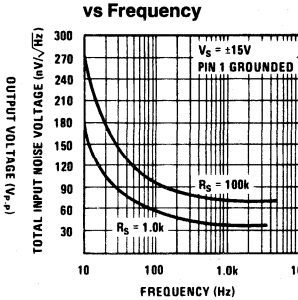
Output Voltage Swing vs Supply Voltage



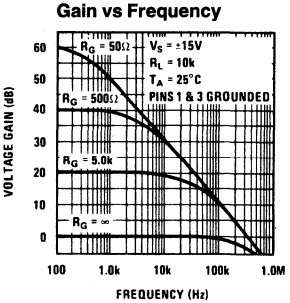
Peak to Peak Output Voltage Swing vs R_L



Total Input Noise Voltage* vs Frequency

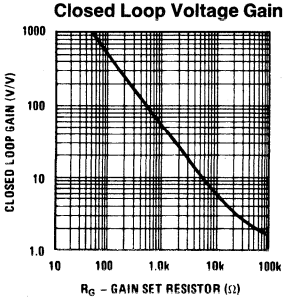


Closed Loop Voltage Gain vs Frequency

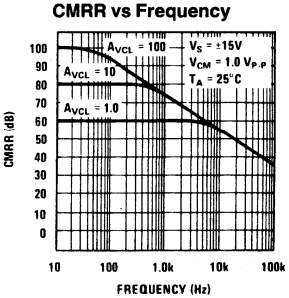


*Noise voltage includes contribution from source resistance

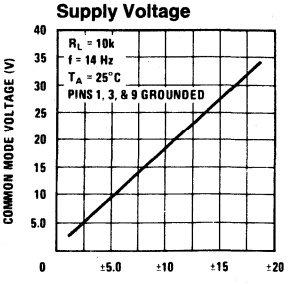
Closed Loop Voltage Gain



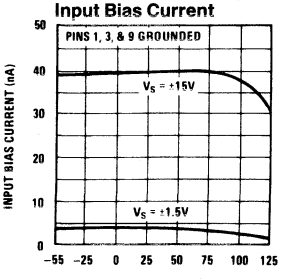
CMRR vs Frequency



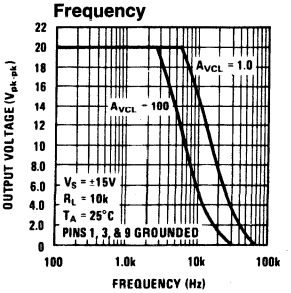
Common Mode Voltage vs Supply Voltage



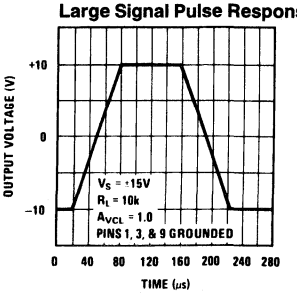
Input Bias Current



Output Voltage Swing vs Frequency



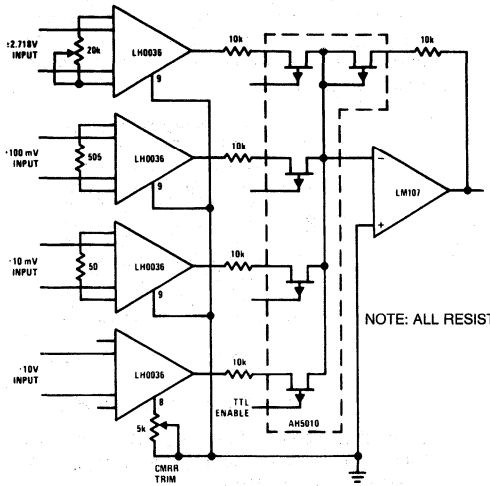
Large Signal Pulse Response



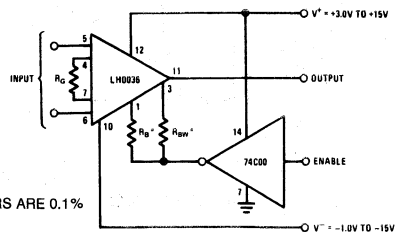
TL/H/5545- 2

Typical Applications

Pre MUX Signal Conditioning

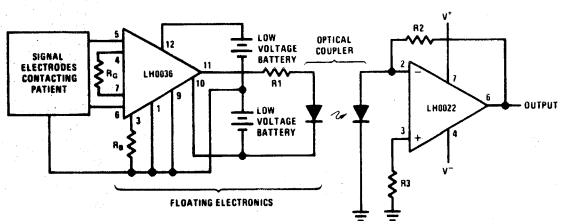


Instrumentation Amplifier with Logic Controlled Shut-Down

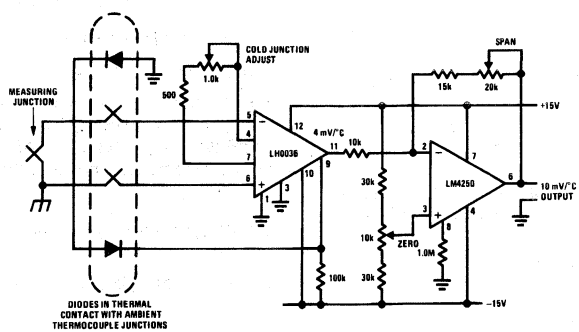


*R_{BW} AND R_B ARE OPTIONAL BANDWIDTH AND INPUT BIAS CURRENT CONTROLLING RESISTORS.

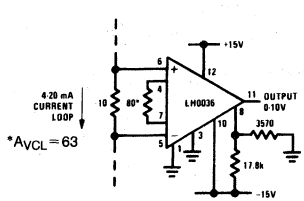
Isolation Amplifier for Medical Telemetry



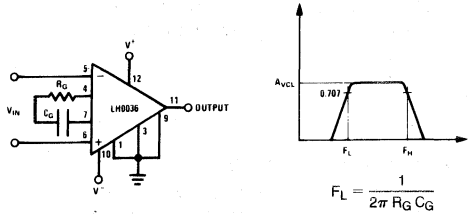
Thermocouple Amplifier with Cold Junction Compensation



Process Control Interface



High Pass Filter



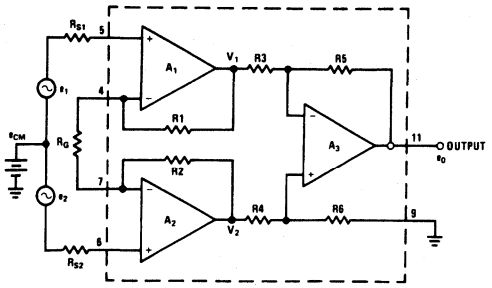
$$F_L = \frac{1}{2\pi R_G C_G}$$

TL/H/5545–3

F_H = A FUNCTION OF SELECTED A_{VCL}, R_S AND R_{SW}

Applications Information

THEORY OF OPERATION



TL/H/5545–4

FIGURE 1. Simplified LH0036

The LH0036 is a 2 stage amplifier with a high input impedance gain stage comprised of A_1 and A_2 and a differential to single-ended unity gain stage, A_3. Operational amplifier, A_1, receives differential input signal, e_1, and amplifies it by a factor equal to $(R1 + R_G)/R_G$.

A_1 also receives input e_2 via A_2 and R2. e_2 is seen as an inverting signal with a gain of $R1/R_G$. A_1 also receives the common mode signal e_{CM} and processes it with a gain of $+1$.

Hence:

$$V_1 = \frac{R1+R_G}{R_G} e_1 - \frac{R1}{R_G} e_2 + e_{CM} \quad (1)$$

By similar analysis V_2 is seen to be:

$$V_2 = \frac{R2 + R_G}{R_G} e_2 - \frac{R2}{R_G} e_1 + e_{CM} \quad (2)$$

For $R1 = R2$:

$$V_2 - V_1 = \left[\left(\frac{2R1}{R_G}\right) + 1\right](e_2 - e_1) \quad (3)$$

Also, for $R3 = R5 = R4 = R6$, the gain of $A_3 = 1$, and:

$$e_0 = (1)(V_2 - V_1) = (e_2 - e_1)\left[1 + \left(\frac{2R1}{R_G}\right)\right] \quad (4)$$

As can be seen for identically matched resistors, e_{CM} is cancelled out, and the differential gain is dictated by equation (4).

For the LH0036, equation (4) reduces to:

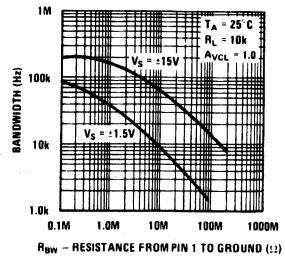
$$A_{VCL} = \frac{e_0}{e_2 - e_1} = 1 + \frac{50k}{R_G} \quad (5a)$$

The closed loop gain may be set to any value from 1 ($R_G = \infty$) to 1000 ($R_G \cong 50\Omega$). Equation (5a) re-arranged in more convenient form may be used to select R_G for a desired gain:

$$R_G = \frac{50k}{A_{VCL} - 1} \quad (5b)$$

USE OF BANDWIDTH CONTROL (pin 1)

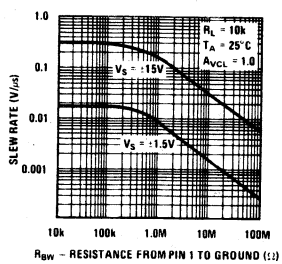
In the standard configuration, pin 1 of the LH0036 is simply grounded. The amplifier's slew rate in this configuration is typically $0.3V/\mu S$ and small signal bandwidth 350 kHz for $A_{VCL} = 1$. In some applications, particularly at low frequency, it may be desirable to limit bandwidth in order to minimize the overall noise bandwidth of the device. A resistor R_{BW} may be placed between pin 1 and ground to accomplish this purpose. *Figure 2* shows typical small signal bandwidth versus R_{BW}.



TL/H/5545–5

FIGURE 2. Bandwidth vs R_{BW}

It also should be noted that large signal bandwidth and slew rate may be adjusted down by use of R_{BW}. *Figure 3* is plot of slew rate versus R_{BW}.



TL/H/5545–6

FIGURE 3. Output Slew Rate vs R_{BW}

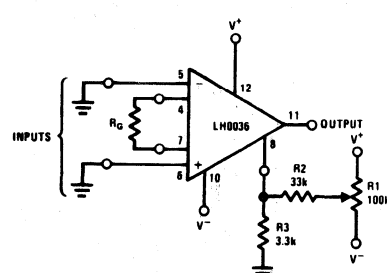
CMRR CONSIDERATIONS

Use of Pin 9, CMRR Preset

Pin 9 should be grounded for nominal operation. An internal factory trimmed resistor, R6, will yield a CMRR in excess of 80 dB (for $A_{VCL} = 100$). Should a higher CMRR be desired, pin 9 should be left open and the procedure, in this section followed.

DC Off-set Voltage and Common Mode Rejection Adjustments

Off-set may be nulled using the circuit shown in *Figure 4*.

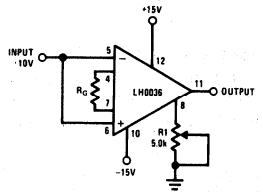


TL/H/5545–7

FIGURE 4. V_{OS} Adjustment Circuit

Applications Information (Continued)

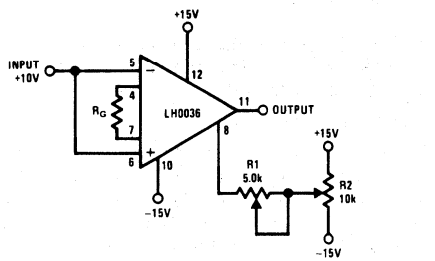
Pin 8 is also used to improve the common mode rejection ratio as shown in *Figure 5*. Null is achieved by alternately applying ±10V (for V^+ & V^- = 15V) to the inputs and adjusting R1 for minimum change at the output.



TL/H/5545–8

FIGURE 5. CMRR Adjustment Circuit

The circuits of *Figure 4* and *5* may be combined as shown in *Figure 6* to accomplish both V_{OS} and CMRR null. However, the V_{OS} and CMRR adjustment are interactive and several iterations are required. The procedure for null should start with the inputs grounded.

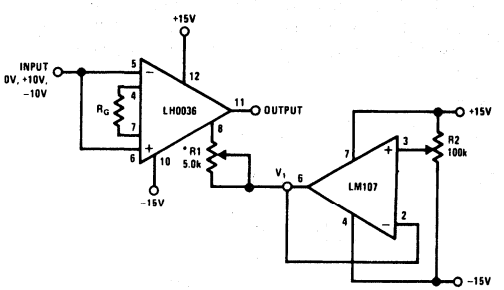


TL/H/5545–10

FIGURE 6. Combined CMRR, V_{OS} Adjustment Circuit

R2 is adjusted for V_{OS} null. An input of +10V is then applied and R1 is adjusted for CMRR null. The procedure is then repeated until the optimum is achieved.

A circuit which overcomes adjustment interaction is shown in *Figure 7*. In this case, R2 is adjusted first for output null of the LH0036. R1 is then adjusted for output null with +10V input. It is always a good idea to check CMRR null with a −10V input. The optimum null achievable will yield the highest CMRR over the amplifiers common mode range.



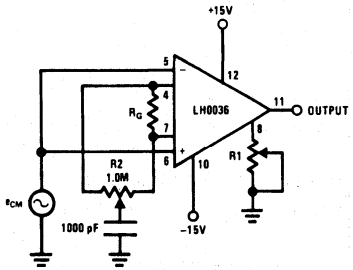
TL/H/5545–11

*Note: Nominal value R1 to Achieve Optimum CMRR is 3.0 kΩ

FIGURE 7. Improved V_{OS}, CMRR Nulling Circuit

AC CMRR Considerations

The ac CMRR may be improved using the circuit of *Figure 8*.



TL/H/5545–9

FIGURE 8. Improved AC CMRR Circuit

After adjusting R1 for best dc CMRR as before, R2 should be adjusted for minimum peak-to-peak voltage at the output while applying an ac common mode signal of the maximum amplitude and frequency of interest.

INPUT BIAS CURRENT CONTROL

Under nominal operating conditions (pin 3 grounded), the LH0036 requires input currents of 40 nA. The input current may be reduced by inserting a resistor (R_B) between 3 and ground or, alternatively, between 3 and V^-. For R_B returned to ground, the input bias current may be predicted by:

$$I_{BIAS} \cong \frac{V^+ - 0.5}{4 \times 10^8 + 800\, R_B} \qquad (6a)$$

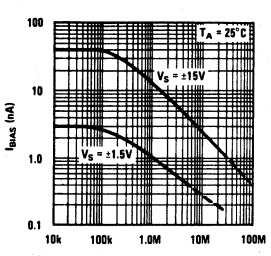
or

$$R_B = \frac{V^+ - 0.5 - (4 \times 10^8)\,(I_{BIAS})}{800\, I_{BIAS}} \qquad (6b)$$

Where:

I_{BIAS} = Input Bias Current (nA)
R_B = External Resistor connected between pin 3 and ground (Ohms)
V^+ = Positive Supply Voltage (Volts)

Figure 9 is a plot of input bias current versus R_B.



TL/H/5545–12

FIGURE 9. Input Bias Current as a Function of R_B

As indicated above, R_B may be returned to the negative supply voltage. Input bias current may then be predicted by:

$$I_{BIAS} \cong \frac{(V^+ - V^-) - 0.5}{4 \times 10^8 + 800\, R_B}$$

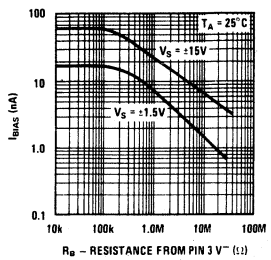
Applications Information (Continued)

or

$$R_B \cong \frac{(V^+ - V^-) - 0.5 - (4 \times 10^8)(I_{BIAS})}{800\ I_{BIAS}} \quad (8)$$

Where:

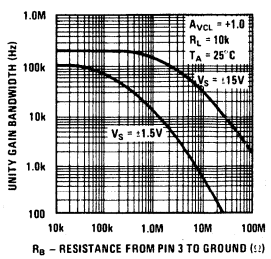
I_{BIAS} = Input Bias Current (nA)
R_B = External resistor connected between pin 3 and V^- (Ohms)
V^+ = Positive Supply Voltage (Volts)
V^- = Negative Supply Voltage (Volts)



TL/H/5545–13

FIGURE 10. Input Bias Current as a Function of R_B

Figure 10 is a plot of input bias current versus R_B returned to V^- it should be noted that bandwidth is affected by changes in R_B. *Figure 11* is a plot of bandwidth versus R_B.

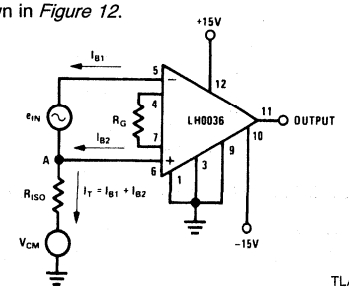


TL/H/5545–14

FIGURE 11. Unity Gain Bandwidth as a Function of R_B

BIAS CURRENT RETURN PATH CONSIDERATIONS

The LH0036 exhibits input bias currents typically in the 40 nA region in each input. This current must flow through R_{ISO} as shown in *Figure 12*.



TL/H/5545–16

FIGURE 12. Bias Current Return Path

In a typical application, $V_S = \pm 15V$, $I_{B1} \cong I_{B2} \cong 40$ nA, the total current, I_T, would flow through R_{ISO} causing a voltage rise at point A. For values of $R_{ISO} \geq 150$ MΩ, the voltage at point A exceeds the +12V common range of the device. Clearly, for $R_{ISO} = \infty$, the LH0036 would be driven to positive saturation.

The implication is that a finite impedance must be supplied between the input and power supply ground. The value of the resistor is dictated by the maximum input bias current, and the common mode voltage. Under worst case conditions:

$$R_{ISO} \leq \frac{V_{CMR} - V_{CM}}{I_T} \quad (9)$$

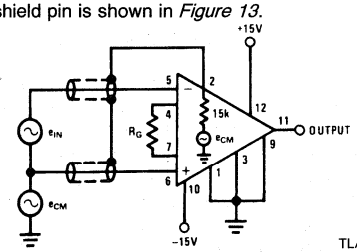
Where:

V_{CMR} = Common Mode Range (10V for the LH0036)
V_{CM} = Common Mode Voltage
$I_T = I_{B1} + I_{B2}$

In applications in which the signal source is floating, such as a thermocouple, one end of the source may be grounded directly or through a resistor.

GUARD OUTPUT

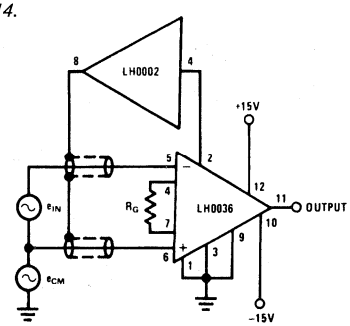
Pin 2 of the LH0036 is provided as a guard drive pin in those stringent applications which require very low leakage and minimum input capacitance. Pin 2 will always be biased at the input common mode voltage. The source impedance looking into pin 2 is approximately 15 kΩ. Proper use of the guard/shield pin is shown in *Figure 13*.



TL/H/5545–15

FIGURE 13. Use of Guard

For applications requiring a lower source impedance than 15 kΩ, a unity gain buffer, such as the LH0002 may be inserted between pin 2 and the input shields as shown in *Figure 14*.



TL/H/5545–17

FIGURE 14. Guard Pin With Buffer

Definition of Terms

Bandwidth: The frequency at which the voltage gain is reduced to 0.707 of the low frequency (dc) value.

Closed Loop Gain, A_{VCL}: The ratio of the output voltage swing to the input voltage swing determined by $A_{VCL} = 1 + (50k/R_G)$. Where: R_G = Gain Set Resistor.

Common Mode Rejection Ratio: The ratio of input voltage range to the peak-to-peak change in offset voltage over this range.

Gain Equation Accuracy: The deviation of the actual closed loop gain from the predicted closed loop gain, $A_{VCL} = 1 + (50k/R_G)$ for the specified closed loop gain.

Input Bias Current: The current flowing at pin 5 and 6 under the specified operating conditions.

Input Offset Current: The difference between the input bias current at pins 5 and 6; i.e. $I_{OS} = |I_5 - I_6|$.

Input Stage Offset Voltage, V_{IOS}: The voltage which must be applied to the input pins to force the output to zero volts for $A_{VCL} = 100$.

Output Stage Offset Voltage, V_{OOS}: The voltage which must be applied to the input of the output stage to produce zero output voltage. It can be measured by measuring the overall offset at unity gain and subtracting V_{IOS}.

$$V_{OOS} = \left[V_{OS}\Big|_{A_{VCL}=1}\right] - \left[V_{OS}\Big|_{A_{VCL}=1000}\right]$$

Overall Offset Voltage:

$$V_{OS} = V_{IOS} + \frac{V_{OOS}}{A_{VCL}}$$

Power Supply Rejection Ratio: The ratio of the change in offset voltage, V_{OS}, to the change in supply voltage producing it.

Resistor, R_B: An optional resistor placed between pin 3 of the LH0036 and ground (or V^-) to reduce the input bias current.

Resistor, R_{BW}: An optional resistor placed between pin 1 of the LH0036 and ground (or V^-) to reduce the bandwidth of the output stage.

Resistor, R_G: A gain setting resistor connected between pins 4 and 7 of the LH0036 in order to program the gain from 1 to 1000.

Settling Time: The time between the initiation of an input step function and the time when the output voltage has settled to within a specified error band of the final output voltage.

National Semiconductor

LM221/LM321 Precision Preamplifiers

General Description

The LM221 series are precision preamplifiers designed to operate with general purpose operational amplifiers to drastically decrease dc errors. Drift, bias current, common mode and supply rejection are more than a factor of 50 better than standard op amps alone. Further, the added dc gain of the LM221 decreases the closed loop gain error.

The LM221 series operates with supply voltages from ±3V to ±20V and has sufficient supply rejection to operate from unregulated supplies. The operating current is programmable from 5 μA to 200 μA so bias current, offset current, gain and noise can be optimized for the particular application while still realizing very low drift. Super-gain transistors are used for the input stage so input error currents are lower than conventional amplifiers at the same operating current. Further, the initial offset voltage is easily nulled to zero.

The extremely low drift of the LM221 will improve accuracy on almost any precision dc circuit. For example, instrumentation amplifier, strain gauge amplifiers and thermocouple amplifiers now using chopper amplifiers can be made with the LM221. The full differential input and high common-mode rejection are another advantage over choppers. For applications where low bias current is more important than drift, the operating current can be reduced to low values. High operating currents can be used for low voltage noise with low source resistance. The programmable operating current of the LM221 allows tailoring the input characteristics to match those of specialized op amps.

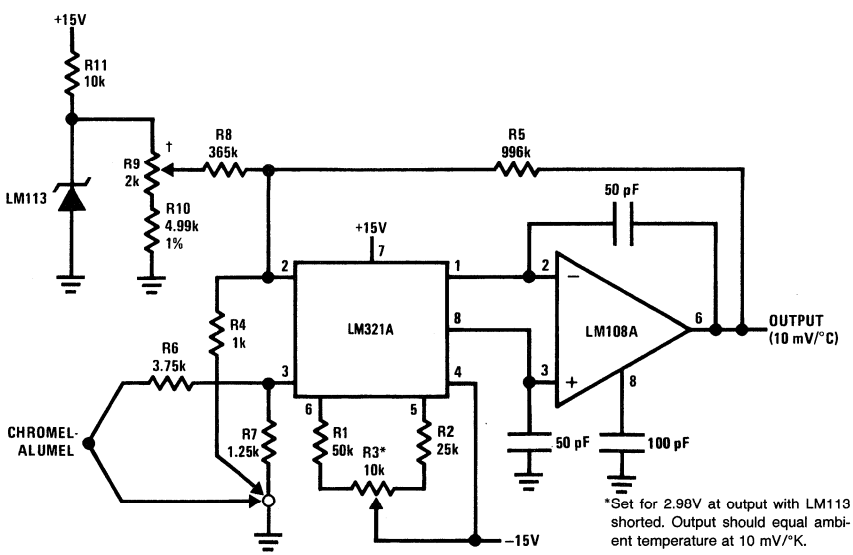
The LM221 is specified over a −25°C to +85°C range and the LM321 over a 0°C to +70°C temperature range.

Features

- Guaranteed drift of LM321A—0.2 μV/°C
- Guaranteed drift of LM221 series—1 μV/°C
- Offset voltage less than 0.4 mV
- Bias current less than 10 nA at 10 μA operating current
- CMRR 126 dB minimum
- 120 dB supply rejection
- Easily nulled offset voltage

Typical Applications

Thermocouple Amplifier with Cold Junction Compensation



*Set for 2.98V at output with LM113 shorted. Output should equal ambient temperature at 10 mV/°K.

†Adjust for output reading in °C.

TL/H/7769–1

Absolute Maximum Ratings

Supply Voltage	±20V
Power Dissipation (Note 1)	500 mW
Differential Input Voltage (Notes 2 and 3)	±15V
Input Voltage (Note 3)	±15V

Operating Temperature Range LM321A	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec.)	300°C

ESD rating to be determined.

Electrical Characteristics (Note 4) LM321A

Parameter	Conditions	LM321A			Units
		Min	Typ	Max	
Input Offset Voltage	T_A = 25°C, 6.4k ≤ R_{SET} ≤ 70k		0.2	0.4	mV
Input Offset Current	T_A = 25°C, R_{SET} = 70k R_{SET} = 6.4k		 0.3	 0.5 5	 nA nA
Input Bias Current	T_A = 25°C, R_{SET} = 70k R_{SET} = 6.4k		 5 50	 15 150	 nA nA
Input Resistance	T_A = 25°C, R_{SET} = 70k R_{SET} = 6.4k	 2 0.2	 8		 MΩ MΩ
Supply Current	T_A = 25°C, R_{SET} = 70k		0.8	2.2	mA
Input Offset Voltage	6.4k ≤ R_{SET} ≤ 70k		0.5	0.65	mV
Input Bias Current	R_{SET} = 70k R_{SET} = 6.4k		15 150	25 250	nA nA
Input Offset Current	R_{SET} = 70k R_{SET} = 6.4k		0.5 5	1 10	nA nA
Input Offset Current Drift	R_{SET} = 70k		3		pA/°C
Average Temperature	R_S ≤ 200Ω, 6.4k ≤ R_{SET} ≤ 70k				
Coefficient of Input Offset Voltage	Offset Voltage Nulled		0.07	0.2	μV/°C
Long Term Stability			3		μV/yr
Supply Current			1	3.5	mA
Input Voltage Range	V_S = ±15V, (Note 5) R_{SET} = 70k R_{SET} = 6.4k	 ±13 +7, −13			 V V
Common-Mode Rejection Ratio	R_{SET} = 70k R_{SET} = 6.4k	126 120	140 130		dB dB
Supply Voltage Rejection Ratio	R_{SET} = 70k R_{SET} = 6.4k	118 114	126 120		dB dB
Voltage Gain	T_A = 25°C, R_{SET} = 70k, R_L > 3 MΩ	 12	 20		 V/V
Noise	R_{SET} = 70k, R_{SOURCE} = 0		8		nV/√Hz

Note 1: The maximum junction temperature of the LM321A is 85°C. For operating at elevated temperature, devices in the H08 package must be derated based on a thermal resistance of 150°C/W, junction to ambient, or 18°C/W, junction to case.

Note 2: The inputs are shunted with back-to-back diodes in series with a 500Ω resistor for overvoltage protection. Therefore, excessive current will flow if a differential input voltage in excess of 1V is applied between the inputs.

Note 3: For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

Note 4: These specifications apply for ±5 ≤ V_S ≤ ±20V and −55°C ≤ T_A ≤ +125°C, unless otherwise specified. With the LM221A, however all temperature specifications are limited to −25°C ≤ T_A ≤ +85°C, and for the LM321A the specifications apply over a 0°C to +70°C temperature range.

Note 5: External precision resistor —0.1%— can be placed from pins 1 and 8 to 7 increase positive common-mode range.

Note 6: See RETS121X for LM121H/883 military specs and RET121AX for LM121AH/883 military specs.

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	±20V
Power Dissipation (Note 1)	500 mW
Differential Input Voltage (Notes 2 and 3)	±15V
Input Voltage (Note 3)	±15V
Operating Temperature Range	
LM221, LM121A (-883), LM121 (-883)	−25°C to +85°C
LM321, LM321A	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec.)	260°C
ESD rating to be determined.	

Electrical Characteristics (Note 4) LM221, LM321

Parameter	Conditions	LM221			LM321			Units
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	$T_A = 25°C$, $6.4k \le R_{SET} \le 70k$			0.7			1.5	mV
Input Offset Current	$T_A = 25°C$,							
	$R_{SET} = 70k$			1			2	nA
	$R_{SET} = 6.4k$			10			20	nA
Input Bias Current	$T_A = 25°C$,							
	$R_{SET} = 70k$			10			18	nA
	$R_{SET} = 6.4k$			100			180	nA
Input Resistance	$T_A = 25°C$,							
	$R_{SET} = 70k$	4			2			MΩ
	$R_{SET} = 6.4k$	0.4			0.2			MΩ
Supply Current	$T_A = 25°C$, $R_{SET} = 70k$			1.5			2.2	mA
Input Offset Voltage	$6.4k \le R_{SET} \le 70k$			1.0			2.5	mV
Input Bias Current	$R_{SET} = 70k$			30			28	nA
	$R_{SET} = 6.4k$			300			280	nA
Input Offset Current	$R_{SET} = 70k$			3			4	nA
	$R_{SET} = 6.4k$			30			40	nA
Input Offset Current Drift	$R_{SET} = 70k$		3			3		pA/°C
Average Temperature Coefficient of Input Offset Voltage	$R_S \le 200\Omega$, $6.4k \le R_{SET} \le 70k$ Offset Voltage Nulled			1			1	μV/°C
Long Term Stability			5			5		μV/yr
Supply Current				2.5			3.5	mA
Input Voltage Range	$V_S = \pm 15V$, (Note 5)							
	$R_{SET} = 70k$	±13			±13			V
	$R_{SET} = 6.4k$	+7, −13			+7, −13			V
Common-Mode Rejection Ratio	$R_{SET} = 70k$	120			114			dB
	$R_{SET} = 6.4k$	114			114			dB
Supply Voltage Rejection Ratio	$R_{SET} = 70k$	120			114			dB
	$R_{SET} = 6.4k$	114			114			dB
Voltage Gain	$T_A = 25°C$, $R_{SET} = 70k$, $R_L > 3\ M\Omega$	16			12			V/V
Noise	$R_{SET} = 70k$, $R_{SOURCE} = 0$		8			8		$nV/\sqrt{Hz}$

Note 1: The maximum junction temperature of the LM221 is 100°C. The maximum junction temperature of the LM321 is 85°C. For operating at elevated temperature, devices in the H08 package must be derated based on a thermal resistance of 150°C/W, junction to ambient, or 18°C/W, junction to case.

Note 2: The inputs are shunted with back-to-back diodes in series with a 500Ω resistor for overvoltage protection. Therefore, excessive current will flow if a differential input voltage in excess of 1V is applied between the inputs.

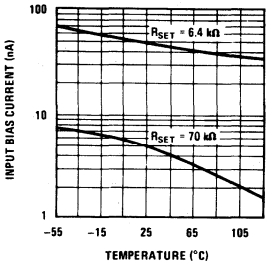
Note 3: For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

Note 4: These specifications apply for $\pm 5 \le V_S \le \pm 20V$ and $-55°C \le T_A \le +125°C$, unless otherwise specified. With the LM221, however all temperature specifications are limited to $-25°C \le T_A \le +85°C$, and for the LM321 the specifications apply over a 0°C to +70°C temperature range.

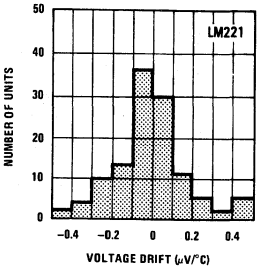
Note 5: External precision resistor —0.1%— can be placed from pins 1 and 8 to 7 increase positive common-mode range.

Typical Performance Characteristics

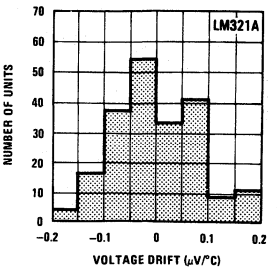
Input Bias Current



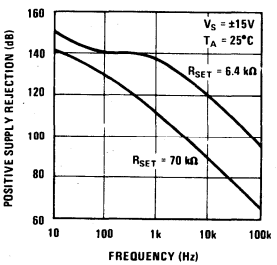
Distribution of Offset Voltage Drift (Nulled)



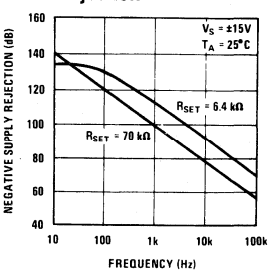
Distribution of Offset Voltage Drift (Nulled)



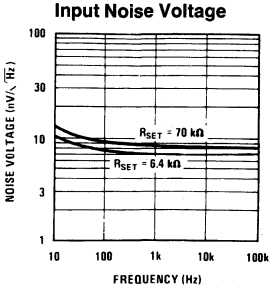
Positive Power Supply Rejection



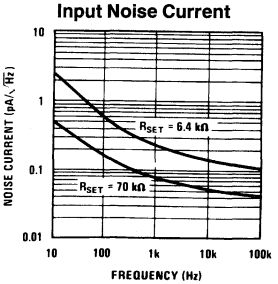
Negative Power Supply Rejection



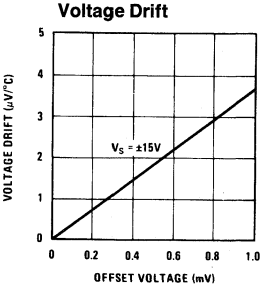
Input Noise Voltage



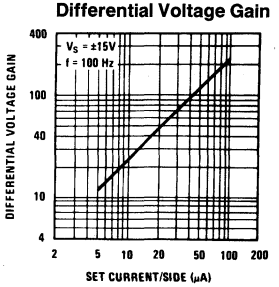
Input Noise Current



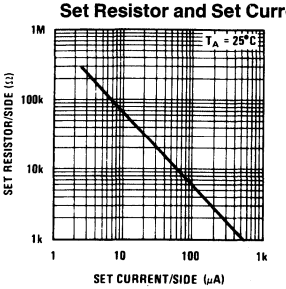
Voltage Drift



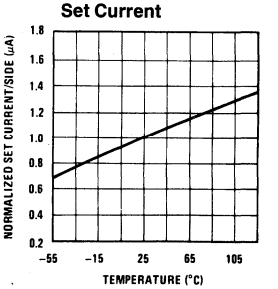
Differential Voltage Gain



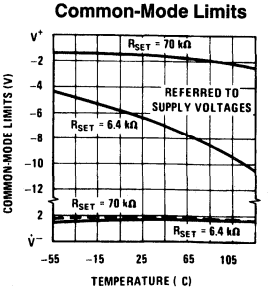
Set Resistor and Set Current



Set Current



Common-Mode Limits



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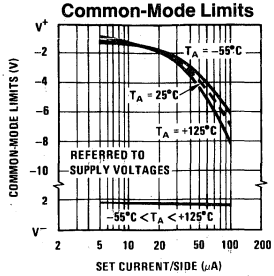
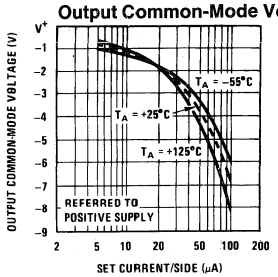
Typical Performance Characteristics (Continued)

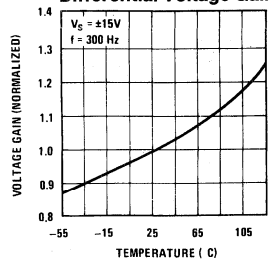
Common-Mode Limits



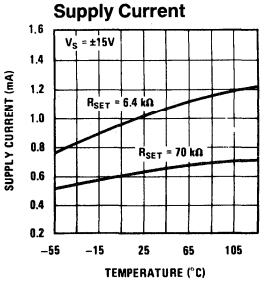
Output Common-Mode Voltage



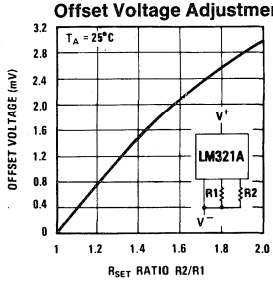
Differential Voltage Gain



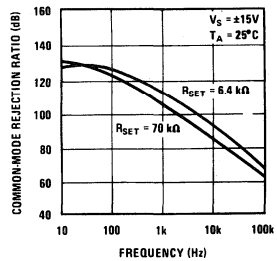
Supply Current



Offset Voltage Adjustment



Common-Mode Rejection Ratio



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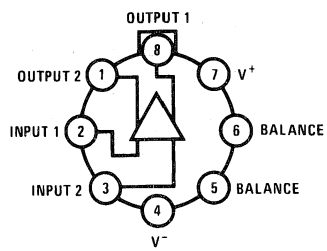
Connection Diagram

Metal Can Package



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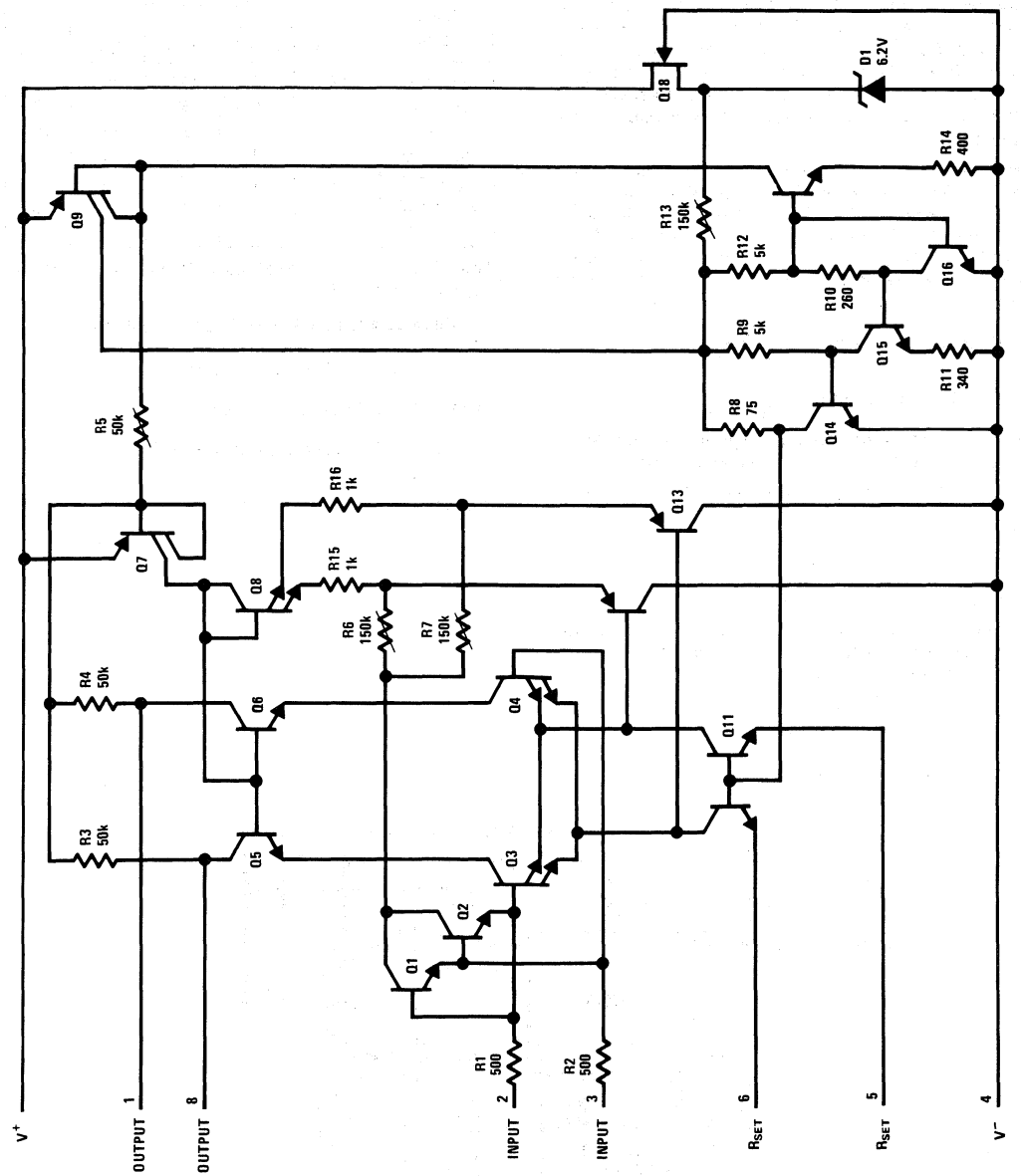
Top View

Note: Pin 4 connected to case.

Order Number LM121AH/883, LM121H/883, LM221H, LM321H or LM321AH
See NS Package Number H08C

Note: Outputs are inverting from the input of the same number.

Schematic Diagram



Frequency Compensation

UNIVERSAL COMPENSATION

The additional gain of the LM321 preamplifier when used with an operational amplifier usually necessitates additional frequency compensation. When the closed loop gain of the op amp with the LM321 is less than the gain of the LM321 alone, more compensation is needed. The worst case situation is when there is 100% feedback—such as a voltage follower or integrator—and the gain of the LM321 is high. When high closed loop gains are used—for example A_V = 1000—and only an addition gain of 200 is inserted by the LM321, the frequency compensation of the op amp will usually suffice.

The frequency compensation shown here is designed to operate with any unity-gain stable op amp. *Figure 1* shows the basic configuration of frequency stabilizing network. In operation the output of the LM321 is rendered single ended by a 0.01 μF bypass capacitor to ground. Overall frequency compensation then is achieved by an integrating capacitor around the op amp.

$$\text{Bandwidth at unity-gain} \cong \frac{12}{2\pi R_{SET} C}$$

$$\text{for 0.5 MHz bandwidth } C = \frac{4}{10^6 R_{SET}}$$

For use with higher frequency op amps such as the LM118 the bandwidth may be increased to about 2 MHz.

If the closed loop gain is greater than unity, "C" may be decreased to:

$$C = \frac{4}{10^6 A_{CL} R_{SET}}$$

ALTERNATE COMPENSATION

The two compensation capacitors can be made equal for improved power supply rejection. In this case the formula for the compensation capscitor is:

$$C = \frac{8}{10^6 A_{CL} R_{SET}}$$

Table I shows typical values for the two compensating capacitors for various gains and operating currents.

TABLE I

Closed Loop Gain	Current Set Resistor				
	120 kΩ	60 kΩ	30 kΩ	12 kΩ	6 kΩ
A_V = 1	68	130	270	680	1300
A_V = 5	15	27	56	130	270
A_V = 10	10	15	27	68	130
A_V = 50	1	3	5	15	27
A_V = 100	–	1	3	5	10
A_V = 500	–	–	1	1	3
A_V = 1000	–	–	–	–	–

This table applies for the LM108, LM101A, LM741, LM118. Capacitance is in pF.

DESIGN EQUATIONS FOR THE LM321 SERIES

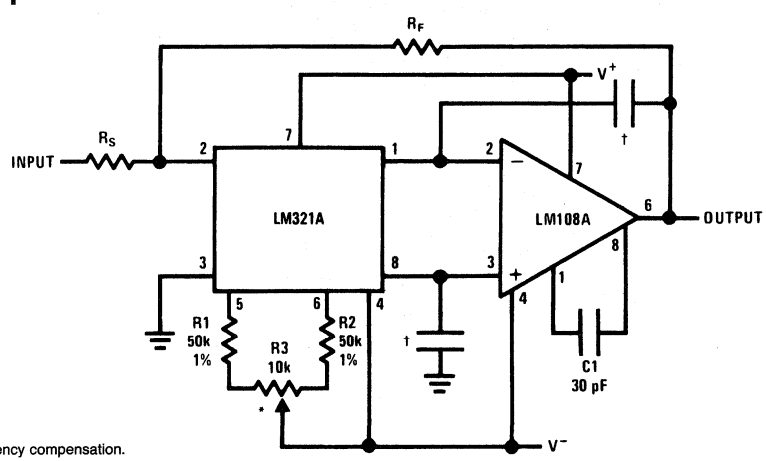
$$\text{Gain } A_V \approx \frac{1.2 \times 10^6}{R_{SET}}$$

Null Pot Value should be 10% of R_{SET}

$$\text{Operating Current} \approx \frac{2 \times 0.65V}{R_{SET}}$$

$$\text{Positive Common-Mode Limit} \approx V^+ - \left[0.6 - \frac{0.65V \times 50k}{R_{SET}}\right]$$

Typical Applications



*Offset adjust.

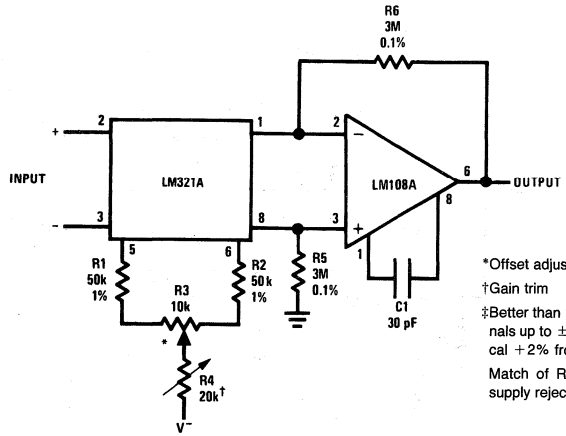
†See table for frequency compensation.

TL/H/7769–2

FIGURE 1. Low Drift Op Amp Using the LM321A as a Preamp

Typical Applications (Continued)

Gain of 1000 Instrumentation Amplifier‡



*Offset adjust

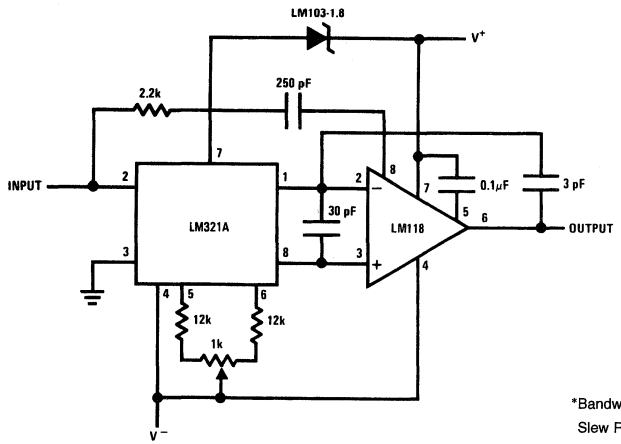
†Gain trim

‡Better than 1% linearity for input signals up to ±10 mV gain stability typical +2% from −55 to +125°C.

Match of R5 and R6 effect power supply rejection

TL/H/7769–3

High Speed* Inverting Amplifier with Low Drift

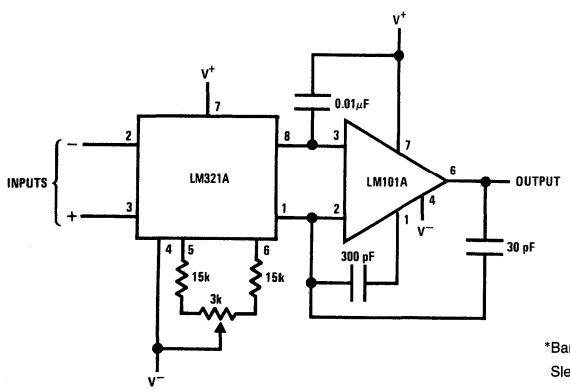


*Bandwidth = 10 MHz

Slew Rate = 40 V/μs

TL/H/7769–4

Medium Speed* General Purpose Amplifier



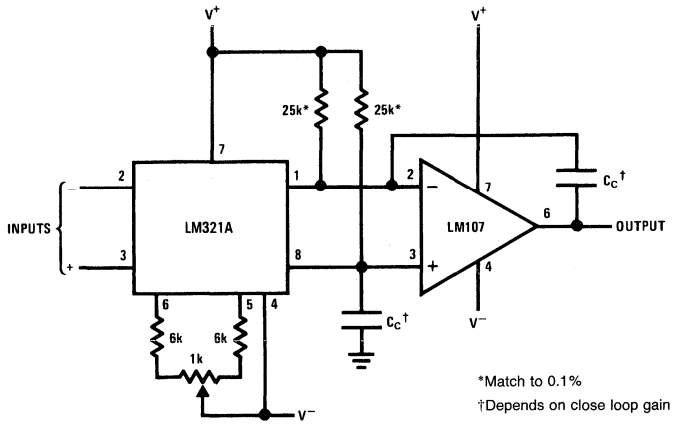
*Bandwidth = 3.5 MHz

Slew Rate = 1.1 V/μs

TL/H/7769–5

Typical Applications (Continued)

Increased Common-Mode Range at High Operating Currents



*Match to 0.1%

†Depends on close loop gain

TL/H/7769–6

Section 5

Surface Mount

Section 5 Contents

National Semiconductor

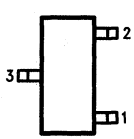
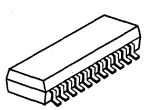
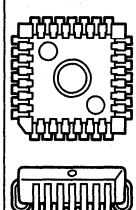
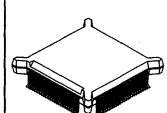
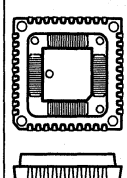
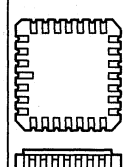
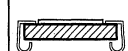
Surface Mount

SURFACE MOUNT PACKAGING AT NATIONAL

To meet the growing demand for smaller packaging, National has developed a line of surface mount packages. Ranging in lead counts from 3 to 360, the package offerings are summarized in Table I.

Lead center spacing keeps shrinking with each new generation of surface mount package. Traditional packages (e.g., DIPs) have a 100 mil lead center spacing. Surface mount packages currently in production (e.g., SOT, SOIC, PCC, LCC, LDCC) have a 50 mil lead center spacing. Surface mount packages in production release (e.g., PQFP) have a 25 mil lead center spacing. Surface mount packages in development (e.g., TAPEPAK®) will have a lead center spacing of only 12–20 mils.

TABLE I. Surface Mount Packages from National

Package Type	Small Outline Transistor (SOT)	Small Outline IC (SOIC)	Plastic Chip Carrier (PCC)	Plastic Quad Flat Pack (PQFP)	TAPEPAK® (TP)	Leadless Chip Carrier (LCC) (LDCC)	Leaded Chip Carrier
							
Package Material	Plastic	Plastic	Plastic	Plastic	Plastic	Ceramic	Ceramic
Lead Bend	Gull Wing	Gull Wing	J-Bend	Gull Wing	Gull Wing	—	Gull Wing
Lead Center Spacing	50 Mils	50 Mils	50 Mils	25 Mils	20, 15, 12 Mils	50 Mils	50 Mils
Tape & Reel Option	Yes	Yes	Yes	tbd	tbd	No	No
Lead Counts	SOT-23 High Profile SOT-23 Low Profile	SO-8(*) SO-14(*) SO-14 Wide(*) SO-16(*) SO-16 Wide(*) SO-20(*) SO-24(*) SO-28(*)	PCC-20(*) PCC-28(*) PCC-44(*) PCC-68 PCC-84 PCC-124	PQFP-84 PQFP-100 PQFP-132 PQFP-196(*) PQFP-244	TP-40 (*) TP-68 TP-84 TP-132 TP-172 TP-220 TP-284 TP-360	LCC-18 LCC-20(*) LCC-28 LCC-32 LCC-44 (*) LCC-48 LCC-52 LCC-68 LCC-84 LCC-124	LDCC-44 LDCC-68 LDCC-84 LDCC-124

*In production (or planned) for linear products.

5

LINEAR PRODUCTS IN SURFACE MOUNT

Linear functions available in surface mount include:

- Op amps
- Comparators
- Regulators
- References
- Data conversion
- Industrial
- Consumer
- Automotive

A representative list of linear part numbers in surface mount is presented in Table III. Refer to the datasheet in the appropriate chapter of this databook for a complete description of the device. In addition, National has other products and is continually expanding the list of devices offered in surface mount. If the functions you need do not appear in Table III, contact the sales office or distributor branch nearest you for additional information.

Automated manufacturers can improve their cost savings by using Tape-and-Reel for surface mount devices. Simplified handling results because hundreds-to-thousands of semiconductors are carried on a single Tape-and-Reel pack (see ordering and shipping information—printed later in this section—for a comparison of devices/reel vs. devices/rail for those surface mount package types being used for linear products). With this higher device count per reel (when compared with less than a 100 devices per rail), pick-and-place machines have to be re-loaded less frequently and lower labor costs result.

With Tape-and-Reel, manufacturers save twice—once from using surface mount technology for automated PC board assembly and again from less device handling during shipment and machine set-up.

BOARD CONVERSION

Besides new designs, many manufacturers are converting existing printed circuit board designs to surface mount. The resulting PCB will be smaller, lighter and less expensive to manufacture; but there is one caveat—be careful about the thermal dissipation capability of the surface mount package.

Because the surface mount package is smaller than the traditional dual-in-line package, the surface mount package is not capable of conducting as much heat away as the DIP (i.e., the surface mount package has a higher thermal resistance—see Table II).

The silicon for most National devices can operate up to a 150°C junction temperature (check the datasheet for the rare exception). Like the DIP, the surface mount package can actually withstand an ambient temperature of up to 125°C (although a commercial temperature range device will only be specified for a max ambient temperature of 70°C and an industrial temperature range device will only be specified for a max ambient temperature of 85°C). See AN-336, "Understanding Integrated Circuit Package Power Capabilities", (reprinted in the appendix of each linear databook volume) for more information.

TABLE II: Surface Mount Package Thermal Resistance Range*

Package	Thermal Resistance** (θ_{jA}, °C/W)
SO-8	120–175
SO-14	100–140
SO-14 Wide	70–110
SO-16	90–130
SO-16 Wide	70–100
SO-20	60–90
SO-24	55–85
SO-28	TBD
PCC-20	70–100
PCC-28	60–90
PCC-44	40–60

*Actual thermal resistance for a particular device depends on die size. Refer to the datasheet for the actual θ_{jA} value.

**Test conditions: PCB mount (FR4 material), still air (room temperature), copper traces (150 × 20 × 10 mils).

Given a max junction temperature of 150°C and a maximum allowed ambient temperature, the surface mount device will be able to dissipate less power than the DIP device. This factor must be taken into account for new designs.

For board conversion, the DIP and surface mount devices would have to dissipate the same power. This means the surface mount circuit would have a lower maximum allowable ambient temperature than the DIP circuit. For DIP circuits where the maximum ambient temperature required is substantially lower than the maximum ambient temperature allowed, there may be enough margin for safe operation of the surface mount circuit with its lower maximum allowable ambient temperature. But where the maximum ambient temperature required of the DIP current is close to the maximum allowable ambient temperature, the lower maximum ambient temperature allowed for the surface mount circuit may fall below the maximum ambient temperature required. The circuit designer must be aware of this potential pitfall so that an appropriate work-around can be found to keep the surface mount package from being thermally overstressed in the application.

SURFACE MOUNT LITERATURE

National has published extensive literature on the subject of surface mount packaging. Engineers from packaging, quality, reliability, and surface mount applications have pooled their experience to provide you with practical hands-on knowledge about the construction and use of surface mount packages.

The applications note AN-450 "Surface Mounting Methods and their Effect on Product Reliability" is referenced on each SMD datasheet. In addition, "Wave Soldering of Surface Mount Components" is reprinted in this section for your information.

TABLE III. Linear Surface Mount Selected Device Listing

Amplifiers and Comparators

Part Number	Part Number
LF451CM	LMC6022IM
LF453CM	LMC6024IM
LM10CWM	LMC6032IM
LM10CLWM	LMC6034IM
LM318M	LMC6041IM
LM3080M	LMC6042IM
LM4250M	LMC6044IM
LM611CM	LMC6084IM
LM612IM	LMC6064IM
LM613CWM	LMC6061IM
LM614CWM	LMC6081IM
LM615IWM	LMC6062IM
LM6181IM	LMC6082IM
LM6218WM	LMC6484IM
LM6321M	LMC6482IM
LM6361M	LPC660IM
LM6362M	LPC661IM
LM6364M	LPC662IM
LM6365M	
LMC660CM	
LMC662CM	

Peripheral Drivers

Part Number	Part Number
DS2001CM	DS2004TM
DS2001TM	DS3680M
DS2002CM	DS75451M
DS2002TM	DS75452M
DS2003CM	DS75453M
DS2003TM	DS75454M
DS2004CM	

Regulators and References

Part Number	Part Number
LM317LM	LM2577M—12
LM337LM	LM2577M—15
LM431ACM	LM2577M—ADJ
LM723CM	LM2578AM
LM2574M—3.3	LM2931AM—5.0
LM2574M—5.0	LM2931M—5.0
LM2574M—12	LM2931CM
LM2574M—15	LM2936M—5.0
LM2574M—ADJ	LM3524DM
LM2574HVM—3.3	LM3578AM
LM2574HVM—5.0	LM78L05ACM
LM2574HVM—12	LM78L12ACM
LM2574HVM—15	LM78L15ACM
LM2574HVM—ADJ	LM79L05ACM
LM2575M—5.0	LM79L12ACM
LM2575M—12	LM79L15ACM
LM2575M—15	LP2951ACM
LM2575M—ADJ	LP2951CM
LM2575HVM—5.0	LP2952AIM
LM2575HVM—12	LP2952IM
LM2575HVM—15	LP2953AIM
LM2575HVM—ADJ	LP2953IM

Data Acquisition Products

Part Number	Part Number
ADC08061/2/4/8	DAC0854
ADC08161/4/8	LM12454/8
ADC08031/2/4/8	LM34
ADC08131/4/8	LM35
ADC08231/4/8	LM4040
ADC0851/58	LM4041
ADC10061/2/4	LM4431
ADC10154/8	LMF100
ADC1034/8	LMF380
ADC10461/2/4	LMF40
ADC1061	LMF60
ADC10662/4	LMF90
ADC12030/2/4/8	

Industrial Functions

Part Number	Part Number
AH5012CM	LM13600M
LF13331M	LM13700M
LF13509M	LMC555CM
LF13333M	LM567CM
LM555CM	MF4CWM-50
LM556CM	MF4CWM-100
LM567CM	MF6CWM-50
LM1496M	MF10CCWM
LM2917M	MF6CWM-100
LM3046M	MF5CWM
LM3086M	LMC568CM
LM3146M	LMC567CM

Commercial and Automotive

Part Number	Part Number
LM386M-1	LM1851M
LM831M	LM1865M
LM832M	LM1877M
LM833M	LM1894M
LM837M	LM1882CM
LMC835V	LM1964V
LM1201M	LMC1982CIV
LM1204V	LMC1983CIV
	LM3361AM
	LM1881M
	LM3914V

A FINAL WORD

National is a world leader in the design and manufacture of surface mount components.

Because of design innovations such as perforated copper leadframes, our small outline package is as reliable as our DIP—the laws of physics would have meant that a straight "junior copy" of the DIP would have resulted in an "S.O." package of lower reliability. You benefit from this equivalence of reliability. In addition, our ongoing vigilance at each step of the production process assures that the reliability we designed in stays in so that only devices of the highest quality and reliability are shipped to your factory.

Our surface mount applications lab at our headquarters site in Santa Clara, California continues to research (and publish) methods to make it even easier for you to use surface mount technology. Your problems are our problems.

When you think "Surface Mount"—think "National"!

Ordering and Shipping Information

When you order a surface mount semiconductor, it will be in one of the several available surface mount package types. Specifying the Tape-and-Reel method of shipment means that you will receive your devices in the following quantities per Tape-and-Reel pack: SMD devices can also be supplied in conventional conductive rails.

When ordering bulk S.O.—specify "M".

When ordering S.O. Tape & Reel—specify "MX".

Package	Package Designator	Max/Rail	Per Reel*
SO-8	M	100	2500
SO-14	M	50	2500
SO-14 Wide	WM	50	1000
SO-16	M	50	2500
SO-16 Wide	WM	50	1000
SO-20	M	40	1000
SO-24	M	30	1000
SO-28	M	26	1000
PCL-20	V	50	1000
PCL-28	V	40	1000
PCL-44	V	25	500
PQFP-196	VF	TBD	—
TP-40	TP	100	TBD
LCC-20	E	50	—
LCC-44	E	25	—

*Incremental ordering quantities. (National Semiconductor reserves the right to provide a smaller quantity of devices per Tape-and-Reel pack to preserve lot or date code integrity. See example below.)

Example: You order 5,000 LM324MXICs shipped in Tape-and-Reel.

- Case 1: All 5,000 devices have the same date code
  - You receive 2 SO-14 (Narrow) Tape-and-Reel packs, each having 2500 LM324M ICs
- Case 2: 3,000 devices have date code A and 2,000 devices have date code B
  - You receive 3 SO-14 (Narrow) Tape-and-Reel packs as follows:

    Pack #1 has 2,500 LM324MXICs with date code A

    Pack #2 has 500 LM324MXICs with date code A

    Pack #3 has 2,000 LM324MXICs with date code B

Short-Form Procurement Specification

TAPE FORMAT

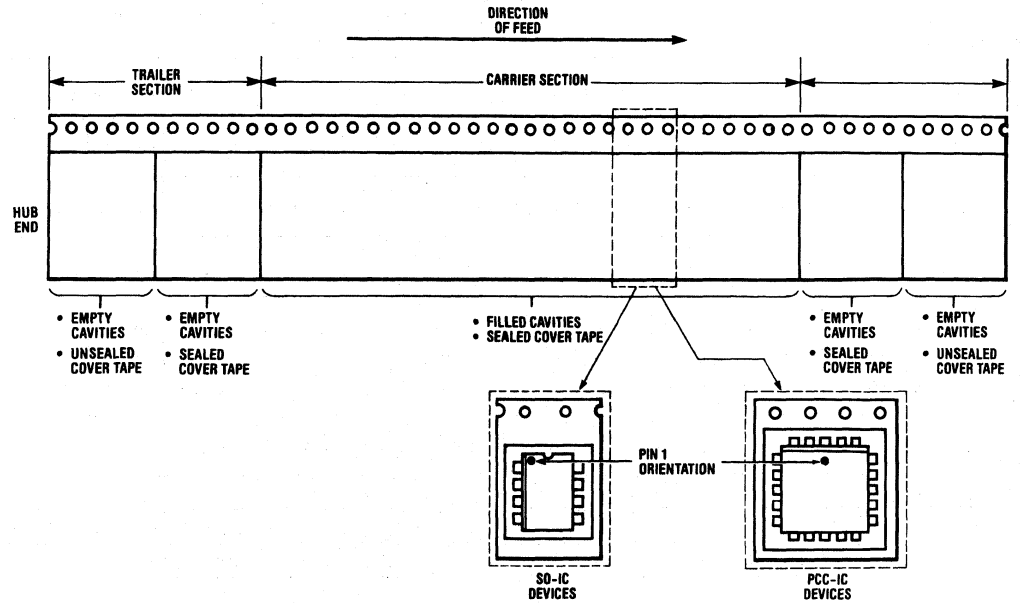
→ Direction of Feed

	Trailer (Hub End)*		Carrier*	Leader (Start End)*	
	Empty Cavities, min (Unsealed Cover Tape)	Empty Cavities, min (Sealed Cover Tape)	Filled Cavities (Sealed Cover Tape)	Empty Cavities, min (Sealed Cover Tape)	Empty Cavities, min (Unsealed Cover Tape)
Small Outline IC					
SO-8 (Narrow)	2	2	2500	5	5
SO-14 (Narrow)	2	2	2500	5	5
SO-14 (Wide)	2	2	1000	5	5
SO-16 (Narrow)	2	2	2500	5	5
SO-16 (Wide)	2	2	1000	5	5
SO-20 (Wide)	2	2	1000	5	5
SO-24 (Wide)	2	2	1000	5	5
SO-28 (Wide)	0	25	1000	42	0
Plastic Chip Carrier IC					
PCC-20	2	2	1000	5	5
PCC-28	2	2	750	5	5
PCC-44	2	2	500	5	5

***The following diagram identifies these sections of the tape and Pin #1 device orientation.**

Short-Form Procurement Specification (Continued)

DEVICE ORIENTATION



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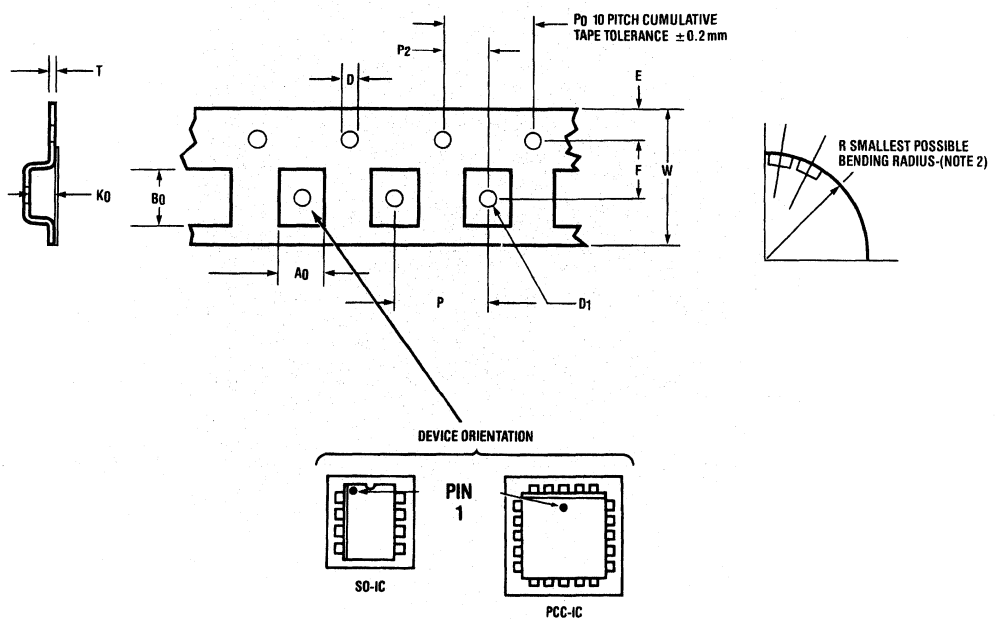
MATERIALS

- Cavity Tape: Conductive PVC (less than 10^5 Ohms/Sq)
- Cover Tape: Polyester
  - (1) Conductive cover available
- Reel:
  - (1) Solid 80 pt fibreboard (standard)
  - (2) Conductive fibreboard available
  - (3) Conductive plastic (PVC) available

TAPE DIMENSIONS (24 Millimeter Tape or Less)



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Short-Form Procurement Specification (Continued)

	W	P	F	E	P_2	P_0	D	T	A_0	B_0	K_0	D_1	R
Small Outline IC													
SO-8 (Narrow)	12±.30	8.0±.10	5.5±.05	1.75±.10	2.0±.05	4.0±.10	1.55±.05	.30±.10	6.4±.10	5.2±.10	2.1±.10	1.55±.05	30
SO-14 (Narrow)	16±.30	8.0±.10	7.5±.10	1.75±.10	2.0±.05	4.0±.10	1.55±.05	.30±.10	6.5±.10	9.0±.10	2.1±.10	1.55±.05	40
SO-14 (Wide)	16±.30	12.0±.10	7.5±.10	1.75±.10	2.0±.05	4.0±.10	1.55±.05	.30±.10	10.9±.10	9.5±.10	3.0±.10	1.55±.05	40
SO-16 (Narrow)	16±.30	8.0±.10	7.5±.10	1.75±.10	2.0±.05	4.0±.10	1.55±.05	.30±.10	6.5±.10	10.3±.10	2.1±.10	1.55±.05	40
SO-16 (Wide)	16±.30	12.0±.10	7.5±.10	1.75±.10	2.0±.05	4.0±.10	1.55±.05	.30±.10	10.9±.10	10.76±.10	3.0±.10	1.55±.05	40
SO-20 (Wide)	24±.30	12.0±.10	11.5±.10	1.75±.10	2.0±.05	4.0±.10	1.55±.05	.30±.10	10.9±.10	13.3±.10	3.0±.10	2.05±.05	50
SO-24 (Wide)	24±.30	12.0±.10	11.5±.10	1.75±.10	2.0±.05	4.0±.10	1.55±.05	.30±.10	10.9±.10	15.85±.10	3.0±.10	2.05±.05	50
Plastic Chip Carrier IC													
PCC-20	16±.30	12.0±.10	7.5±.10	1.75±.10	2.0±.05	4.0±.10	1.55±.05	.30±.10	9.3±.10	9.3±.10	4.9±.10	1.55±.05	40
PCC-28	24±.30	16.0±.10	11.5±.10	1.75±.10	2.0±.05	4.0±.10	1.55±.05	.30±.10	13.0±.10	13.0±.10	4.9±.10	2.05±.05	50

Note 1: A_0, B_0 and K_0 dimensions are measured 0.3 mm above the inside wall of the cavity bottom.

Note 2: Tape with components shall pass around a mandril radius R without damage.

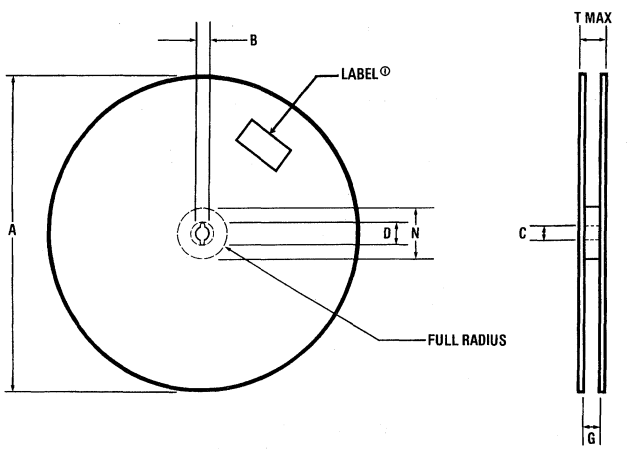
Note 3: Cavity tape material shall be PVC conductive (less than 10^5 Ohms/Sq).

Note 4: Cover tape material shall be polyester (30–65 grams peel-back force).

Note 5: D_1 Dimension is centered within cavity.

Note 6: All dimensions are in millimeters.

REEL DIMENSIONS



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STAR™* Surface Mount Tape and Reel

Short-Form Procurement Specifications (Continued)

		A (Max)	B (Min)	C	D (Min)	N (Min)	G	T (Max)
12 mm Tape	SO-8 (Narrow)	(13.00) (330)	.059 1.5	.512±.002 13±0.05	.795 20.2	1.969 50	$0.488^{+.078}_{-.000}$ 12.4^{+2}_{-0}	.724 18.4
16 mm Tape	SO-14 (Narrow) SO-14 (Wide) SO-16 (Narrow) SO-16 (Wide) PCC-20	(13.00) (330)	.059 1.5	.512±.002 13±0.05	.795 20.2	1.969 50	$0.646^{+.078}_{-.000}$ 16.4^{+2}_{-0}	.882 22.4
24 mm Tape	SO-20 (Wide) SO-24 (Wide) PCC-28	(13.00) (330)	.059 1.5	.512±.002 13±0.05	.795 20.2	1.969 50	$0.960^{+.078}_{-.000}$ 24.4^{+2}_{-0}	1.197 30.4
32 mm Tape	PCC-44	(13.00) (330)	.059 1.5	.512±.002 13±0.05	.795 20.2	1.969 50	$1.276^{+.078}_{-.000}$ 32.4^{+2}_{-0}	1.512 38.4

Units: Inches / Millimeters

Material: Paperboard (Non-Flaking)

LABEL

Human and Machine Readable Label is provided on reel. A variable (C.P.I) density code 39 is available. NSC STD label (7.6 C.P.I.)

FIELD

Lot Number

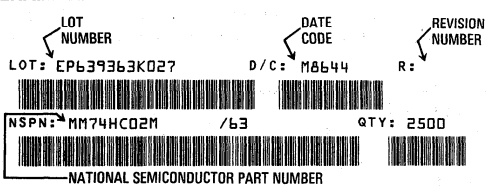
Date Code

Revision Level

National Part No. I.D.

Qty.

EXAMPLE



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Fields are separated by at least one blank space.

Future Tape-and-Reel packs will also include a smaller-size bar code label (high-density code 39) at the beginning of the tape. (This tape label is not available on current production.)

National Semiconductor will also offer additional labels containing information per your specific specification.

Wave Soldering of Surface Mount Components

ABSTRACT

In facing the upcoming surge of "surface mount technology", many manufacturers of printed circuit boards have taken steps to convert some portions of their boards to this new process. However, as the availability of surface mount components is still limited, may have taken to mixing the lead-inserted standard dual-in-line packages (DIPs) with the surface mounted devices (SMDs). Furthermore, to take advantage of using both sides of the board, surface-mounted components are generally adhered to the bottom side of the board while the top side is reserved for the conventional lead-inserted packages. If processed through a wave solder machine, the semiconductor components are now subjected to extra thermal stresses (now that the components are totally immersed into the molten solder).

A discussion of the effect of wave soldering on the reliability of plastic semiconductor packages follows. This is intended to highlight the limitations which should be understood in the use of wave soldering of surface mounted components.

ROLE OF WAVE-SOLDERING IN APPLICATION OF SMDs

The generally acceptable methods of soldering SMDs are vapor phase reflow soldering and IR reflow soldering, both requiring application of solder paste on PW boards prior to placement of the components. However, sentiment still exists for retaining the use of the old wave-soldering machine.

Wave Soldering of Surface Mount Components (Continued)

The reasons being:

1) Most PC Board Assembly houses already possess wave soldering equipment. Switching to another technology such as vapor phase soldering requires substantial investment in equipment and people.
2) Due to the limited number of devices that are surface mount components, it is necessary to mix both lead inserted components and surface mount components on the same board.
3) Some components such as relays and switches are made of materials which would not be able to survive the temperature exposure in a vapor phase or IR furnace.

PW BOARD ASSEMBLY PROCEDURES

There are two considerations in which through-hole ICs may be combined with surface mount components on the PW Board:

a) Whether to mount ICs on one or both sides of the board.
b) The sequence of soldering using Vapor Phase, IR or Wave Soldering singly or combination of two or more methods.

The various processes that may be employed are:

A) Wave Solder before Vapor/IR reflow solder.
   1. Components on the same side of PW Board.
      Lead insert standard DIPS onto PW Board Wave solder (conventional)
      Wash and lead trim
      Dispense solder paste on SMD pads
      Pick and place SMDs onto PW Board
      Bake
      Vapor phase/IR reflow
      Clean
   2. Components on opposite side of PW Board.
      Lead insert standard DIPs onto PW Board
      Wave Solder (conventional)
      Clean and lead trim
      Invert PW Board
      Dispense solder paste on SMD pads
      Dispense drop of adhesive on SMD sites (optional for smaller components)
      Pick and place SMDs onto board
      Bake/Cure
      Invert board to rest on raised fixture
      Vapor/IR reflow soldering
      Clean

B) Vapor/IR reflow solder then Wave Solder.
   1. Components on the same side of PW Board.
      Solder paste screened on SMD side of Printed Wire Board
      Pick and place SMDs
      Bake
      Vapor/IR reflow
      Lead insert on same side as SMDs
      Wave solder
      Clean and trim underside of PCB

C) Vapor/IR reflow only.
   1. Components on the same side of PW Board.
      Trim and form standard DIPs in "gull wing" configuration
      Solder paste screened on PW Board
      Pick and place SMDs and DIPs
      Bake
      Vapor/IR reflow
      Clean
   2. Components on opposite sides of PW Board.
      Solder paste screened on SMD-side of Printed Wire Board
      Adhesive dispensed at central location of each component
      Pick and place SMDs
      Bake
      Solder paste screened on all pads on DIP-side or alternatively apply solder rings (performs) on leads
      Lead insert DIPs
      Vapor/IR reflow
      Clean and lead trim

D) Wave Soldering Only
   1. Components on opposite sides of PW Board.
      Adhesive dispense on SMD side of PW Board
      Pick and place SMDs
      Cure adhesive
      Lead insert top side with DIPs
      Wave solder with SMDs down and into solder bath
      Clean and lead trim

All of the above assembly procedures can be divided into three categories for I.C. Reliability considerations:

1) Components are subjected to both a vapor phase/IR heat cycle then followed by a wave-solder heat cycle or vice versa.
2) Components are subjected to only a vapor phase/IR heat cycle.
3) Components are subjected to wave-soldering only and SMDs are subjected to heat by immersion into a solder pot.

Of these three categories, the last is the most severe regarding heat treatment to a semiconductor device. However, note that semiconductor molded packages generally possess a coating of solder on their leads as a final finish for solderability and protection of base leadframe material. Most semiconductor manufacturers solder-plate the component leads, while others perform hot solder dip. In the latter case the packages may be subjected to total immersion into a hot solder bath under controlled conditions (manual operation) or be partially immersed while in a 'pallet' where automatic wave or DIP soldering processes are used. It is, therefore, possible to subject SMDs to solder heat under certain conditions and not cause catastrophic failures.

Wave Soldering of Surface Mount Components (Continued)

THERMAL CHARACTERISTICS OF MOLDED INTEGRATED CIRCUITS

Since Plastic DIPs and SMDs are encapsulated with a thermoset epoxy, the thermal characteristics of the material generally correspond to a TMA (Thermo-Mechanical Analysis) graph. The critical parameters are (a) its Linear thermal expansion characteristics and (b) its glass transition temperature after the epoxy has been fully cured. A typical TMA graph is illustrated in *Figure 1*. Note that the epoxy changes to a higher thermal expansion once it is subjected to temperatures exceeding its glass transition temperature. Metals (as used on lead frames, for example) do not have this characteristic and generally will have a consistent Linear thermal expansion over the same temperature range.

In any good reliable plastic package, the choice of lead frame material should be such to match its thermal expansion properties to that of the encapsulating epoxy. In the event that there is a mismatch between the two, stresses can build up at the interface of the epoxy and metal. There now exists a tendency for the epoxy to separate from the metal lead frame in a manner similar to that observed on bimetallic thermal range.

In most cases when the packages are kept at temperatures below their glass transition, there is a small possibility of separation at the expoxy-metal interface. However, if the package is subjected to temprature above its glass-transition temperature, the epoxy will begin to expand much faster than the metal and the probability of separation is greatly increased.

CONVENTIONAL WAVE-SOLDERING

Most wave-soldering operations occur at temperatures between 240–260°C. Conventional epoxies for encapsulation have glass-transition temperature between 140–170°C. An I.C. directly exposed to these temperatures risks its long term functionality due to epoxy/metal separation.

Fortunately, there are factors that can reduce that element of risk:

1) The PW board has a certain amount of heat-sink effect and tends to shield the components from the temperature of the solder (if they were placed on the top side of the board). In actual measurements, DIPs achieve a temperature between 120–150°C in a 5-second pass over the solder. This accounts for the fact that DIPs mounted in the conventional manner are reliable.
2) In conventional soldering, only the tip of each lead in a DIP would experience the solder temperature because the epoxy and die are standing above the PW board and out of the solder bath.

EFFECT ON PACKAGE PERFORMANCE BY EPOXY-METAL SEPARATION

In wave soldering, it is necessary to use fluxes to assist the solderability of the components and PW boards. Some facilities may even process the boards and components through some form of acid cleaning prior to the soldering temperature. If separation occurs, the flux residues and acid residues (which may be present owing to inadequate cleaning) will be forced into the package mainly by capillary action as the residues move away from the solder heat source. Once the package is cooled, these contaminants are now trapped within the package and are available to diffuse with moisture from the epoxy over time. It should be noted that electrical tests performed immediately after soldering generally will give no indication of this potential problem. In any case, the end result will be corrosion of the chip metallization over time and premature failure of the device in the field.

VAPOR PHASE/IR REFLOW SOLDERING

In both vapor phase and IR reflow soldering, the risk of separation between epoxy/metal can also be high. Operating temperatures are 215°C (vapor phase) or 240°C (IR) and duration may also be longer (30 sec–60 sec). On the same theoretical basis, there should also be separation. However, in both these methods, solder paste is applied to the pads of the boards; no fluxes are used. Also, the devices are not immersed into the hot solder. This reduces the possibility of solder forcing itself into the epoxy-lead frame interface. Furthermore, in the vapor phase system, the soldering environment is "oxygen-free" and considered "contaminant free". Being so, it could be visualized that as far as reliability with respect to corrosion, both of these methods are advantageous over wave soldering.

BIAS MOISTURE TEST

A bias moisture test was designed to determine the effect on package performance. In this test, the packages are pressured in a stream chamber to accelerate penetration of moisture into the package. An electrical bias is applied on the device. Should there be any contaminants trapped within the package, the moisture will quickly form an electrolyte and cause the electrodes (which are the lead fingers), the gold wire and the aluminum bond-pads of the silicon device to corrode. The aluminum bond-pads, being the weakest link of the system, will generally be the first to fail.

This proprietary accelerated bias/moisture pressure-test is significant in relation to the life test condition at 85°C and

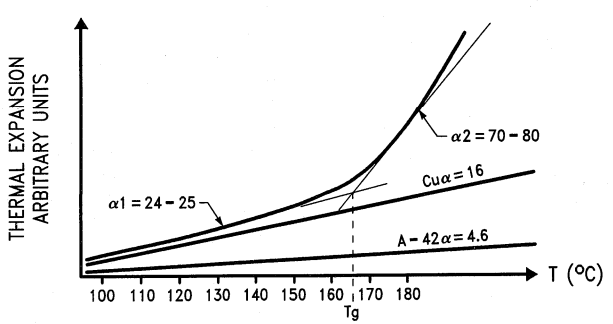

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FIGURE 1. Thermal Expansion and Glass Transition Temperature

Wave Soldering of Surface Mount Components (Continued)

85% relative humidity. Once cycle of approximately 100 hours has been shown to be equivalent to 2000 hours in the 85/85 condition. Should the packages start to fail within the first cycle in the test, it is anticipated that the boards with these components in the harsh operating environment (85°C/85% RH) will experience corrosion and eventual electrical failures within its first 2000 hours of operation.

Whether this is significant to a circuit board manufacturer will obviously be dependent on the products being manufactured and the workmanship or reliability standards. Generally in systems with a long warranty and containing many components, it is advisable both on a reputation and cost basis to have the most reliable parts available.

TEST RESULTS

The comparison of vapor phase and wave-soldering upon the reliability of molded Small-Outline packages was performed using the bias moisture test (see Table IV). It is clearly seen that vapor phase reflow soldering gave more consistent results. Wave-soldering results were based on manual operation giving variations in soldering parameters such as temperature and duration.

TABLE IV. Vapor Phase vs. Wave Solder

1. Vapor phase (60 sec. exposure @ 215°C)
   = 9 failures/1723 samples
   = 0.5% (average over 32 sample lots)
2. Wave solder (2 sec total immersion @ 260°C)
   = 16 failures/1201 samples
   = 1.3% (average over 27 sample lots)

Package: SO-14 lead
Test: Bias moisture test 85% R.H., 85°C for 2000 hours
Device: LM324M

In Table V we examine the tolerance of the Small-Outlined (SOIC) package to varying immersion time in a hot solder pot. SO-14 lead molded packages were subjected to the bias moisture test after being treated to the various soldering conditions and repeated four (4) times. End point was an electrical test after an equivalent of 4000 hours 85/85 test. Results were compared for packages by itself against packages which were surface-mounted onto a FR-4 printed wire board.

TABLE V. Summary of Wave Solder Results (85% R.H./85°C Bias Moisture Test, 2000 hours) (# Failures/Total Tested)

	Unmounted	Mounted
Control/Vapor Phase 15 sec @ 215°C	0/114	0/84
Solder Dip 2 sec @ 260°C	2/144 (1.4%)	0/85
Solder Dip 4 sec @ 260°C	—	0/83
Solder Dip 6 sec @ 260°C	13/248 (5.2%)	1/76 (1.3%)
Solder Dip 10 sec @ 260°C	14/127 (11.0%)	3/79 (3.8%)
Package: SO-14 lead Device: LM324M		

Since the package is of very small mass and experiences a rather sharp thermal shock followed by stresses created by the mismatch in expansion, the results show the package being susceptible to failures after being immersed in excess of 6 seconds in a solder pot. In the second case where the packages were mounted, the effect of severe temperature excursion was reduced. In the second case where the packages were mounted, the effect of severe temperature excursion was reduced. In any case, because of the repeated treatment, the package had failures when subjected in excess of 6 seconds immersion in hot solder. The safety margin is therefore recommended as maximum 4 seconds immersion. If packages were immersed longer than 4 seconds, there is a probable chance of finding some long term reliability failures even though the immediate electrical test data could be acceptable.

Finally, Table VI examines the bias moisture test performed on surface mount (SOIC) components manufactured by various semiconductor houses. End point was an electrical test after an equivalent of 6000 hours in a 85/85 test. Failures were analyzed and corrosion was checked for in each case to detect flaws in package integrity.

TABLE VI. U.S. Manufacturers Integrated Circuits Reliability in Various Solder Environments (# Failure/Total Tested)

Package SO-8	Vapor Phase 30 sec	Wave Solder 2 sec	Wave Solder 4 sec	Wave Solder 6 sec	Wave Solder 10 sec
Manuf A	8/30*	1/30*	0.30	12/30*	16/30*
Manuf B	2/30*	8/30*	2/30*	22/30*	20/30*
Manuf C	0/30	0/29	0/29	0/30	0/30
Manuf D	1/30*	0/30	12/30*	14/30*	2/30*
Manuf E	1/30**	0/30	0/30	0/30	0/30
Manuf F	0/30	0/30	0/30	0/30	0/30
Manuf G	0/30	0/30	0/30	0/30	0/30

*Corrosion-failures

**No Visual Defects—Non-corrosion failures

Test: Accelerated Bias Moisture Test; 85% R.H./85°C, 6000 equivalent hours.

SUMMARY

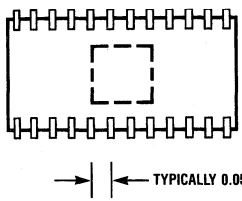
Based on the results presented, it is noted that surface-mounted components are as reliable as standard molded DIP packages. Whereas DIPs were never processed by being totally immersed in a hot solder wave during printed circuit board soldering, surface mounted components such as SOICs (Small Outline) are expected to survive a total immersion in the hot solder in order to capitalize on maximum population on boards. Being constructed from a thermoset plastic of relatively low Tg compared to the soldering temperature, the ability of the package to survive is dependent on the time of immersion and also the cleanliness of material. The results indicate that one should limit the immersion time of package in the solder wave to a maximum of 4 seconds in order to truly duplicate the reliability of a DIP. As the package size is reduced, as in a SO-8 lead, the requirement becomes even more critical. This is shown by the various manufacturers' performance. Results indicate there is room for improvement since not all survived the hot solder immersion without compromise to lower reliability.

Small Outline (SO) Package Surface Mounting Methods— Parameters and Their Effect on Product Reliability

The SO (small outline) package has been developed to meet customer demand for ever-increasing miniaturization and component density.

COMPONENT SIZE COMPARISON

S.O. Package



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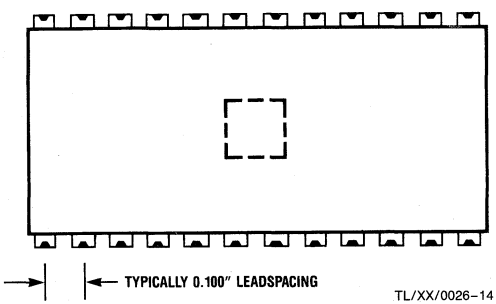
Standard DIP Package



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Because of its small size, reliability of the product assembled in SO packages needs to be carefully evaluated.

SO packages at National were internally qualified for production under the condition that they be of comparable reliability performance to a standard dual in line package under all accelerated environmental tests. *Figure A* is a summary of accelarated bias moisture test performance on 30V bipolar and 15V CMOS product assembled in SO and DIP (control) packages.

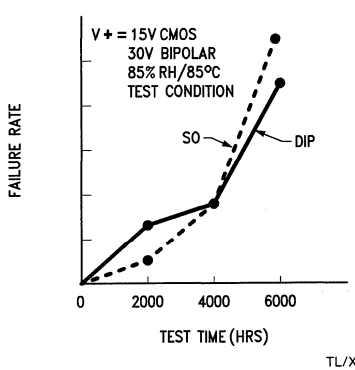

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FIGURE A

In order to achieve reliability performance comparable to DIPs—SO packages are designed and built with materials and processes that effectively compensate for their small size.

All SO packages tested on 85%RA, 85°C were assembled on PC conversion boards using vapor-phase reflow soldering. With this approach we are able to measure the effect of surface mounting methods on reliability of the process. As illustrated in *Figure A* no significant difference was detected between the long term reliability performance of surface mounted S.O. packages and the DIP control product for up to 6000 hours of accelerated 85%/85°C testing.

SURFACE-MOUNT PROCESS FLOW

The standard process flowcharts for basic surface-mount operation and mixed-lead insertion/surface-mount operations, are illustrated on the following pages.

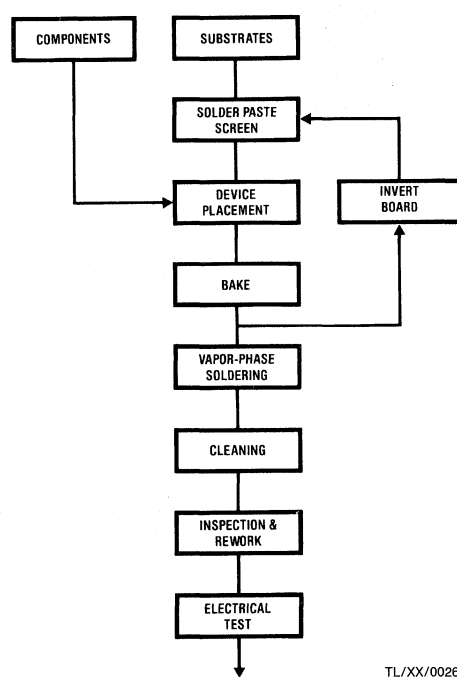
Usual variations encountered by users of SO packages are:

- Single-sided boards, surface-mounted components only.
- Single-sided boards, mixed-lead inserted and surface-mounted components.
- Double-sided boards, surface-mounted components only.
- Double-sided boards, mixed-lead inserted and surface-mounted components.

In consideration of these variations, it became necessary for users to utilize techniques involving wave soldering and adhesive applications, along with the commonly-used vapor-phase solder reflow soldering technique.

PRODUCTION FLOW

Basic Surface-Mount Production Flow



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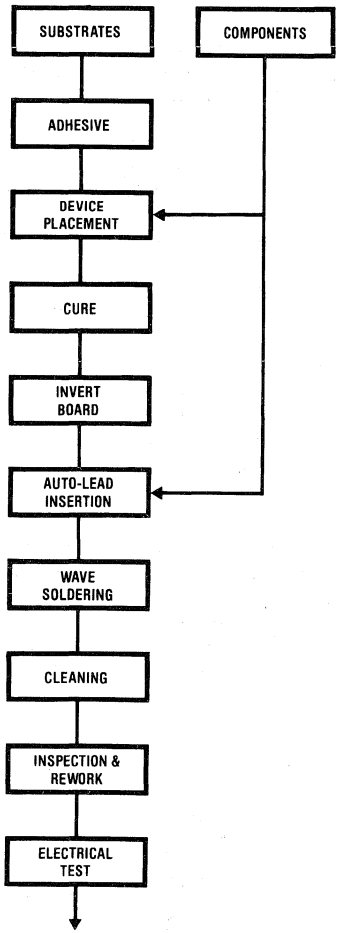
Mixed Surface-Mount and Axial-Leaded Insertion Components Production Flow



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Thermal stress of the packages during surface-mounting processing is more severe than during standard DIP PC board mounting processes. *Figure B* illustrates package temperature versus wave soldering dwell time for surface mounted packages (components are immersed into the molten solder) and the standard DIP wave soldering process. (Only leads of the package are immersed into the molten solder).

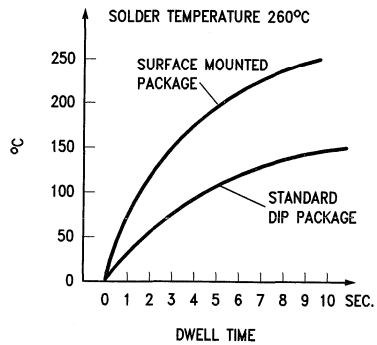

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FIGURE B

For an ideal package, the thermal expansion rate of the encapsulant should match that of the leadframe material in order for the package to maintain mechanical integrity during the soldering process. Unfortunately, a perfect matchup of thermal expansion rates with most presently used packaging materials is scarce. The problem lies primarily with the epoxy compound.

Normally, thermal expansion rates for epoxy encapsulant and metal lead frame materials are linear and remain fairly close at temperatures approaching 160°C, *Figure C*. At lower temperatures the difference in expansion rate of the two materials is not great enough to cause interface separation. However, when the package reaches the glass-transition temperature (T_g) of epoxy (typically 160–165°C), the thermal expansion rate of the encapsulant increases sharply, and the material undergoes a transition into a plastic state. The epoxy begins to expand at a rate three times or more greater than the metal leadframe, causing a separation at the interface.

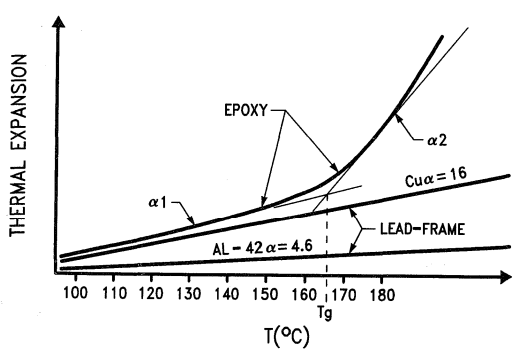

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FIGURE C

When this happens during a conventional wave soldering process using flux and acid cleaners, process residues and even solder can enter the cavity created by the separation and become entrapped when the material cools. These contaminants can eventually diffuse into the interior of the package, especially in the presence of moisture. The result is die contamination, excessive leakage, and even catastrophic failure. Unfortunately, electrical tests performed immediately following soldering may not detect potential flaws.

Most soldering processes involve temperatures ranging up to 260°C, which far exceeds the glass-transition temperature of epoxy. Clearly, circuit boards containing SMD packages require tighter process controls than those used for boards populated solely by DIPs.

Figure D is a summary of accelerated bias moisture test performance on the 30V bipolar process.

Group 1 — Standard DIP package

Group 2 — SO packages vapor-phase reflow soldered on PC boards

Group 3–6 SO packages wave soldered on PC boards

Group 3 — dwell time 2 seconds

4 — dwell time 4 seconds

5 — dwell time 6 seconds

6 — dwell time 10 seconds

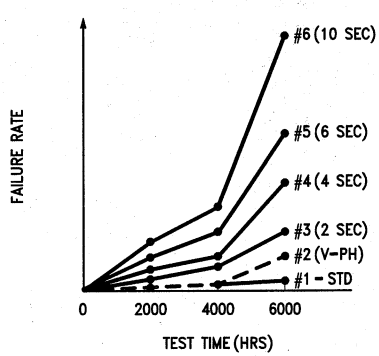

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FIGURE D

It is clear based on the data presented that SO packages soldered onto PC boards with the vapor phase reflow process have the best long term bias moisture performance and this is comparable to the performance of standard DIP packages. The key advantage of reflow soldering methods is the clean environment that minimized the potential for contamination of surface mounted packages, and is preferred for the surface-mount process.

When wave soldering is used to surface mount components on the board, the dwell time of the component under molten solder should be no more than 4 seconds, preferrably under 2 seconds in order to prevent damage to the component. Non-Halide, or (organic acid) fluxes are highly recommended.

PICK AND PLACE

The choice of automatic (all generally programmable) pick-and-place machines to handle surface mounting has grown considerably, and their selection is based on individual needs and degree of sophistication.

The basic component-placement systems available are classified as:

(a) In-line placement

— Fixed placement stations

— Boards indexed under head and respective components placed

(b) Sequential placement

— Either a X-Y moving table system or a θ, X-Y moving pickup system used

—Individual components picked and placed onto boards

(c) Simultaneous placement

— Multiple pickup heads

— Whole array of components placed onto the PCB at the same time

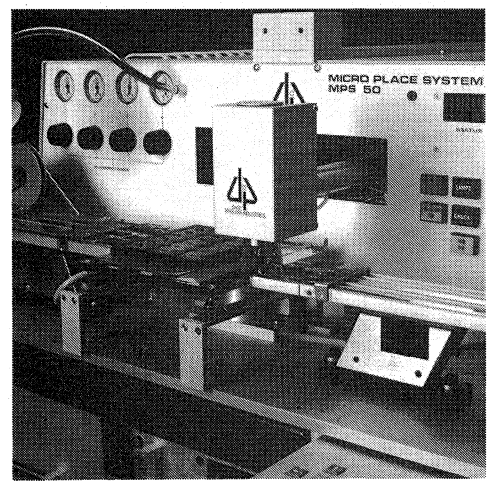
(d) Sequential/simultaneous placement

— X–Y moving table, multiple pickup heads system

— Components placed on PCB by successive or simultaneous actuation of pickup heads

The SO package is treated almost the same as surface-mount, passive components requiring correct orientation in placement on the board.

Pick and Place Action



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BAKE

This is recommended, despite claims made by some solder paste suppliers that this step be omitted.

The functions of this step are:

- Holds down the solder globules during subsequent reflow soldering process and prevents expulsion of small solder balls.
- Acts as an adhesive to hold the components in place during handling between placement to reflow soldering.
- Holds components in position when a double-sided surface-mounted board is held upside down going into a vapor-phase reflow soldering operation.
- Removes solvents which might otherwise contaminate other equipment.
- Initiates activator cleaning of surfaces to be soldered.
- Prevents moisture absorption.

The process is moreover very simple. The usual schedule is about 20 minutes in a 65°C–95°C (dependent on solvent system of solder paste) oven with adequate venting. Longer bake time is not recommended due to the following reasons:

- The flux will degrade and affect the characteristics of the paste.
- Solder globules will begin to oxidize and cause solderability problems.
- The paste will creep and after reflow, may leave behind residues between traces which are difficult to remove and vulnerable to electro-migration problems.

REFLOW SOLDERING

There are various methods for reflowing the solder paste, namely:

- Hot air reflow
- Infrared heating (furnaces)
- Convectional oven heating
- Vapor-phase reflow soldering
- Laser soldering

For SO applications, hot air reflow/infrared furnace may be used for low-volume production or prototype work, but vapor-phase soldering reflow is more efficient for consistency and speed. Oven heating is not recommended because of "hot spots" in the oven and uneven melting may result. Laser soldering is more for specialized applications and requires a great amount of investment.

HOT GAS REFLOW/INFRARED HEATING

A hand-held or table-mount air blower (with appropriate orifice mask) can be used.

The boards are preheated to about 100°C and then subjected to an air jet at about 260°C. This is a slow process and results may be inconsistent due to various heat-sink properties of passive components.

Use of an infrared furnace is the next step to automating the concept, except that the heating is promoted by use of IR lamps or panels. The main objection to this method is that certain materials may heat up at different rates under IR radiation and may result in damage to these components (usually sockets and connectors). This could be minimized by using far-infrared (non-focused) system.

VAPOR-PHASE REFLOW SOLDERING

Currently the most popular and consistent method, vapor-phase soldering utilizes a fluoroinert fluid with excellent heat-transfer properties to heat up components until the solder paste reflows. The maximum temperature is limited by the vapor temperature of the fluid.

The commonly used fluids (supplied by 3M Corp) are:

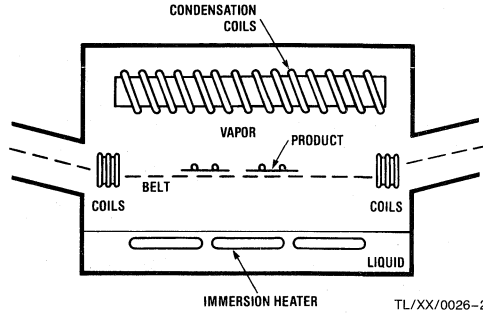
- FC-70, 215°C vapor (most applications) or FX-38
- FC-71, 253°C vapor (low-lead or tin-plate)

HTC, Concord, CA, manufactures equipment that utilizes this technique, with two options:

- Batch systems, where boards are lowered in a basket and subjected to the vapor from a tank of boiling fluid.
- In-line conveyorized systems, where boards are placed onto a continuous belt which transports them into a concealed tank where they are subjected to an environment of hot vapor.

Dwell time in the vapor is generally on the order of 15–30 seconds (depending on the mass of the boards and the loading density of boards on the belt).

In-Line Conveyorized Vapor-Phase Soldering



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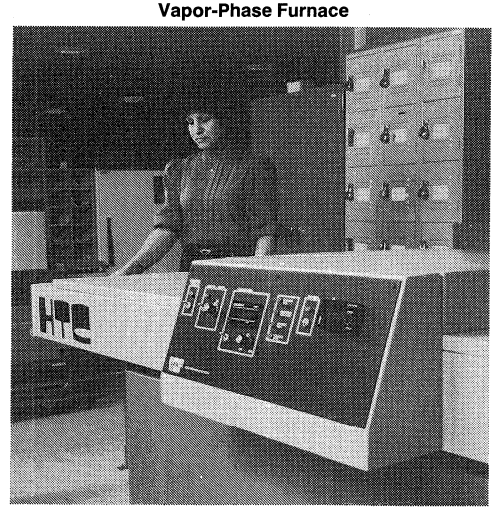
The question of thermal shock is asked frequently because of the relatively sharp increase in component temperature from room temperature to 215°C. SO packages mounted on representative boards have been tested and have shown little effect on the integrity of the packages. Various packages, such as cerdips, metal cans and TO-5 cans with glass seals, have also been tested.

Vapor-Phase Furnace



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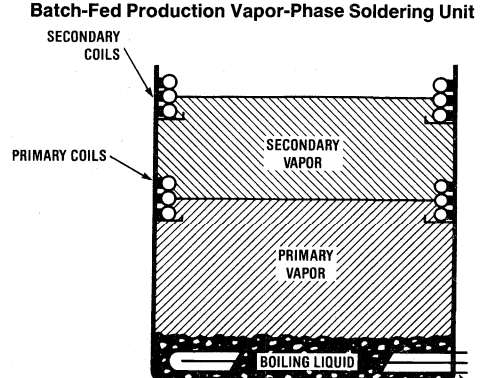
Batch-Fed Production Vapor-Phase Soldering Unit



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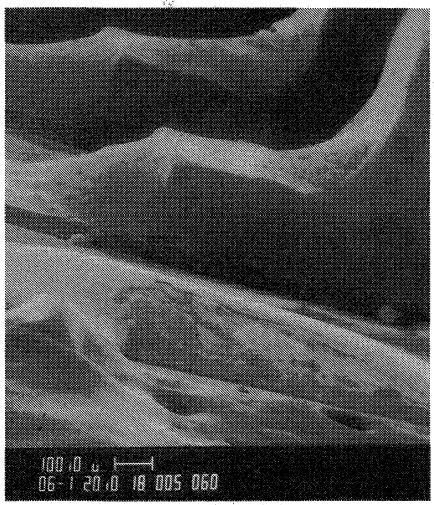
Solder Joints on a SO-14 Package on PCB



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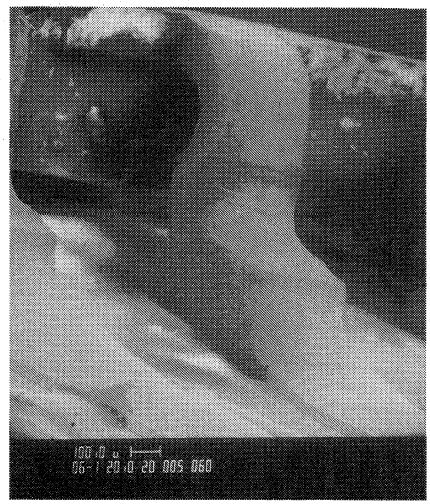
Solder Joints on a SO-14 Package on PCB



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PRINTED CIRCUIT BOARD

The SO package is molded out of clean, thermoset plastic compound and has no particular compatibility problems with most printed circuit board substrates.

The package can be reliably mounted onto substrates such as:

- G10 or FR4 glass/resin
- FR5 glass/resin systems for high-temperature applications
- Polymide boards, also high-temperature applications
- Ceramic substrates

General requirements for printed circuit boards are:

- Mounting pads should be solder-plated whenever applicable.
- Solder masks are commonly used to prevent solder bridging of fine lines during soldering.

  The mask also protects circuits from processing chemical contamination and corrosion.

  If coated over pre-tinned traces, residues may accumulate at the mask/trace interface during subsequent reflow, leading to possible reliability failures.

  Recommended application of solder resist on bare, clean traces prior to coating exposed areas with solder.

  General requirements for solder mask:

  — Good pattern resolution.

  — Complete coverage of circuit lines and resistance to flaking during soldering.

  — Adhesion should be excellent on substrate material to keep off moisture and chemicals.

  — Compatible with soldering and cleaning requirements.

SOLDER PASTE SCREEN PRINTING

With the initial choice of printed circuit lithographic design and substrate material, the first step in surface mounting is the application of solder paste.

The typical lithographic "footprints" for SO packages are illustrated below. Note that the 0.050″ lead center-center spacing is not easily managed by commercially-available air pressure, hand-held dispensers.

Using a stainless-steel, wire-mesh screen stencilled with an emulsion image of the substrate pads is by far the most common and well-tried method. The paste is forced through the screen by a V-shaped plastic squeegee in a sweeping manner onto the board placed beneath the screen.

The setup for SO packages has no special requirement from that required by other surface-mounted, passive components. Recommended working specifications are:

- Use stainless-steel, wire-mesh screens, #80 or #120, wire diameter 2.6 mils. Rule of thumb: mesh opening should be approximately 2.5–5 times larger than the average particle size of paste material.
- Use squeegee of Durometer 70.
- Experimentation with squeegee travel speed is recommended, if available on machine used.
- Use solder paste of mesh 200–325.
- Emulsion thickness of 0.005″ usually used to achieve a solder paste thickness (wet) of about 0.008″ typical.
- Mesh pattern should be 90 degrees, square grid.
- Snap-off height of screen should not exceed 1/8″, to avoid damage to screens and minimize distortion.

SOLDER PASTE

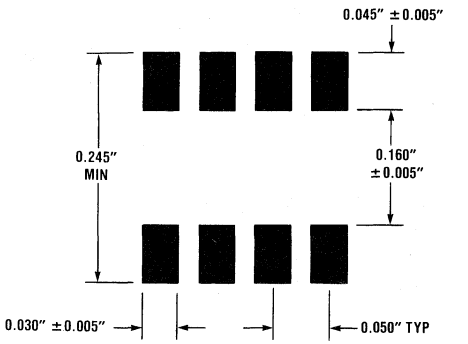
Selection of solder paste tends to be confusing, due to numerous formulations available from various manufacturers. In general, the following guidelines are sufficient to qualify a particular paste for production:

- Particle sizes (see photographs below). Mesh 325 (approximately 45 microns) should be used for general purposes, while larger (solder globules) particles are preferred for leadless components (LCC). The larger particles can easily be used for SO packages.

- Uniform particle distribution. Solder globules should be spherical in shape with uniform diameters and minimum amount of elongation (visual under 100/200 × magnification). Uneven distribution causes uneven melting and subsequent expulsion of smaller solder balls away from their proper sites.
- Composition, generally 60/40 or 63/37 Sn/Pb. Use 62/36 Sn/Pb with 2% Ag in the presence of Au on the soldering area. This formulation reduces problems of metal leaching from soldering pads.
- RMA flux system usually used.
- Use paste with aproximately 88–90% solids.

RECOMMENDED SOLDER PADS FOR SO PACKAGES

SO-8, SO-14, SO-16



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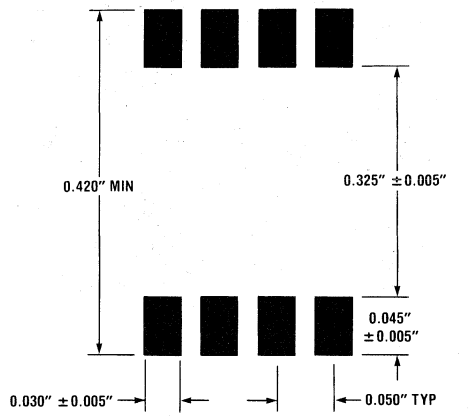
SO-16L, SO-20



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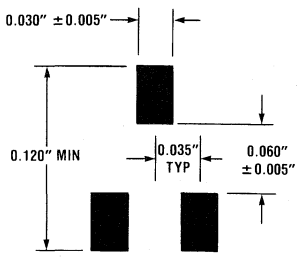
SOT-23



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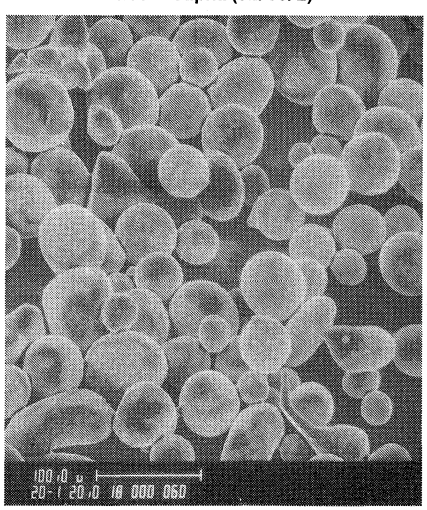
Comparison of Particle Size/Shape of Various Solder Pastes

200 × Alpha (62/36/2)



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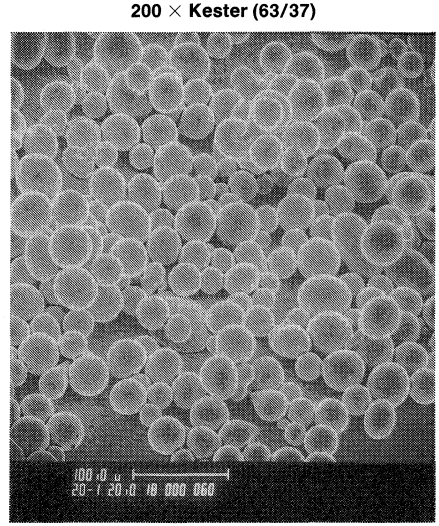
200 × Kester (63/37)



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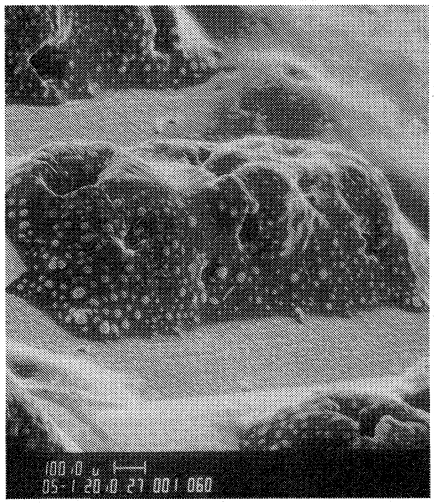
Comparison of Particle Size/Shape of Various Solder Pastes (Continued)

Solder Paste Screen on Pads



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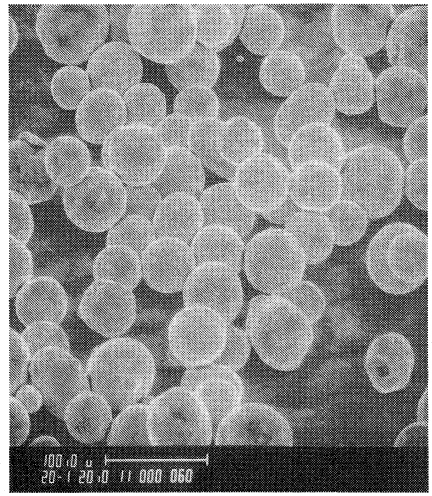
200 × Fry Metal (63/37)



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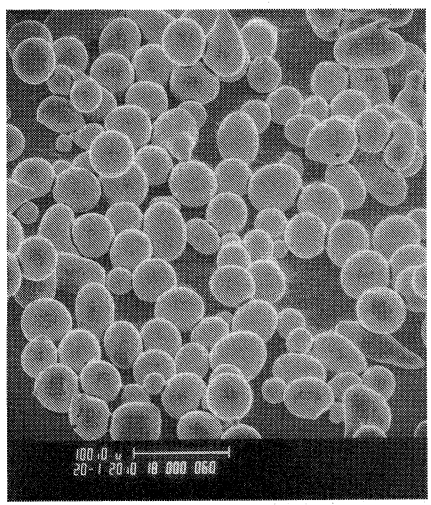
200 ESL (63/37)



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CLEANING

The most critical process in surface mounting SO packages is in the cleaning cycle. The package is mounted very close to the surface of the substrate and has a tendency to collect residue left behind after reflow soldering.

Important considerations in cleaning are:

- Time between soldering and cleaning to be as short as possible. Residue should not be allowed to solidify on the substrate for long periods of time, making it difficult to dislodge.
- A low surface tension solvent (high penetration) should be employed. Solvents commercially available are:

  Freon TMS (general purpose)
  Freon TE35/TP35 (cold-dip cleaning)
  Freon TES (general purpose)

  It should also be noted that these solvents generally will leave the substrate surface hydrophobic (moisture repellent), which is desirable.

  Prelete or 1,1,1-Trichloroethane
  Kester 5120/5121
- A defluxer system which allows the workpiece to be subjected to a solvent vapor, followed by a rinse in pure solvent and a high-pressure spray lance are the basic requirments for low-volume production.
- For volume production, a conveyorized, multiple hot solvent spray/jet system is recommended.
- Rosin, being a natural occurring material, is not readily soluble in solvents, and has long been a stumbling block to the cleaning process. In recent developments, synthetic flux (SA flux), which is readily soluble in Freon TMS solvent, has been developed. This should be explored where permissible.

The dangers of an inadequate cleaning cycle are:

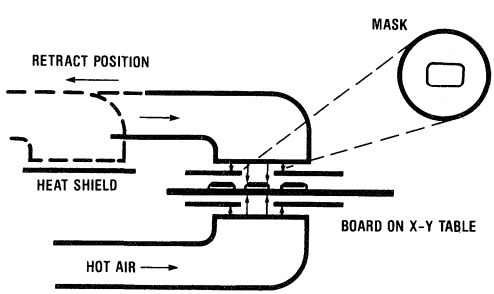
- Ion contamination, where ionic residue left on boards would cause corrosion to metallic components, affecting the performance of the board.
- Electro-migration, where ionic residue and moisture present on electrically-biased boards would cause dentritic growth between close spacing traces on the substrate, resulting in failures (shorts).

REWORK

Should there be a need to replace a component or re-align a previously disturbed component, a hot air system with appropriate orifice masking to protect surrounding components may be used.

When rework is necessary in the field, specially-designed tweezers that thermally heat the component may be used to remove it from its site. The replacement can be fluxed at the lead tips or, if necessary, solder paste can be dispensed onto the pads using a varimeter. After being placed into position, the solder is reflowed by a hot-air jet or even a standard soldering iron.

Hot-Air Solder Rework Station



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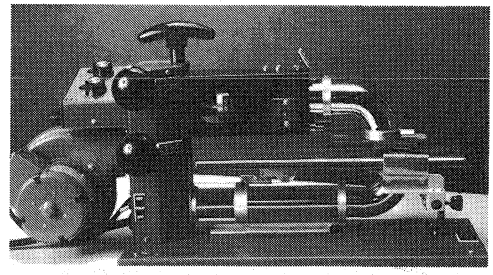
Hot-Air Rework Machine



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WAVE SOLDERING

In a case where lead insertions are made on the same board as surface-mounted components, there is a need to include a wave-soldering operation in the process flow.

Two options are used:

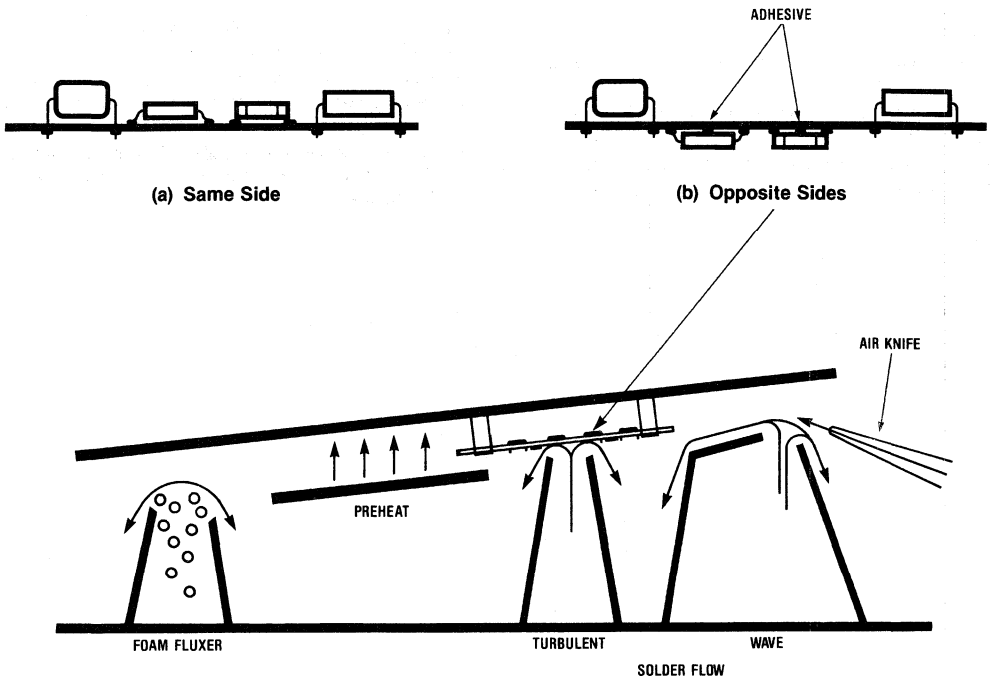
- Surface mounted components are placed and vapor phase reflowed before auto-insertion of remaining components. The board is carried over a standard wave-solder system and the underside of the board (only lead-inserted leads) soldered.
- Surface-mounted components are placed in position, but no solder paste is used. Instead, a drop of adhesive about 5 mils maximum in height with diameter not exceeding 25% width of the package is used to hold down the package. The adhesive is cured and then proceeded to auto-insertion on the reverse side of the board (surface-mounted side facing down). The assembly is then passed over a "dual wave" soldering system. Note that the surface-mounted components are immersed into the molten solder.

Lead trimming will pose a problem after soldering in the latter case, unless the leads of the insertion components are pre-trimmed or the board specially designed to localize certain areas for easy access to the trim blade.

The controls required for wave soldering are:

- Solder temperature to be 240–260°C. The dwell time of components under molten solder to be short (preferably kept under 2 seconds), to prevent damage to most components and semiconductor devices.
- RMA (Rosin Mildly Activated) flux or more aggressive OA (Organic Acid) flux are applied by either dipping or foam fluxing on boards prior to preheat and soldering. Cleaning procedures are also more difficult (aqueous, when OA flux is used), as the entire board has been treated by flux (unlike solder paste, which is more or less localized). Non-halide OA fluxes are highly recommended.
- Preheating of boards is essential to reduce thermal shock on components. Board should reach a temperature of about 100°C just before entering the solder wave.
- Due to the closer lead spacings (0.050″ vs 0.100″ for dual-in-line packages), bridging of traces by solder could occur. The reduced clearance between packages also causes "shadowing" of some areas, resulting in poor solder coverage. This is minimized by dual-wave solder systems.

Mixed Surface Mount and Lead Insertion



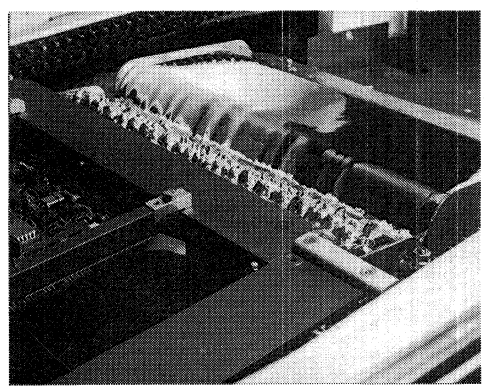
TL/XX/0026–37

A typical dual-wave system is illustrated below, showing the various stages employed. The first wave typically is in turbulence and given a transverse motion (across the motion of the board). This covers areas where "shadowing" occurs. A second wave (usually a broad wave) then proceeds to perform the standard soldering. The departing edge from the solder is such to reduce "icicles," and is still further reduced by an air knife placed close to the final soldering step. This air knife will blow off excess solder (still in the fluid stage) which would otherwise cause shorts (bridging) and solder bumps.

AQUEOUS CLEANING

- For volume production, a conveyorized system is often used with a heated recirculating spray wash (water temperature 130°C), a final spray rinse (water temperature 45–55°C), and a hot (120°C) air/air-knife drying section.
- For low-volume production, the above cleaning can be done manually, using several water rinses/tanks. Fast-drying solvents, like alcohols that are miscible with water, are sometimes used to help the drying process.
- Neutralizing agents which will react with the corrosive materials in the flux and produce material readily soluble in water may be used; the choice depends on the type of flux used.
- Final rinse water should be free from chemicals which are introduced to maintain the biological purity of the water. These materials, mostly chlorides, are detrimental to the assemblies cleaned because they introduce a fresh amount of ionizable material.

Dual Wave



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CONFORMAL COATING

Conformal coating is recommended for high-reliability PCBs to provide insulation resistance, as well as protection against contamination and degradation by moisture.

Requirements:

- Complete coating over components and solder joints.
- Thixotropic material which will not flow under the packages or fill voids, otherwise will introduce stress on solder joints on expansion.
- Compatibility and possess excellent adhesion with PCB material/components.
- Silicones are recommended where permissible in application.

SMD Lab Support

FUNCTIONS

Demonstration—Introduce first-time users to surface-mounting processes.

Service—Investigate problems experienced by users on surface mounting.

Reliability Builds—Assemble surface-mounted units for reliability data acquisition.

Techniques—Develop techniques for handling different materials and processes in surface mounting.

Equipment—In conjunction with equipment manufacturers, develop customized equipments to handle high density, new technology packages developed by National.

In-House Expertise—Availability of in-house expertise on semiconductor research/development to assist users on packaging queries.

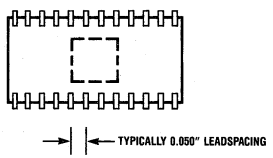
Small Outline (SO) Package Surface Mounting Methods-Parameters and Their Effect on Product Reliability

National Semiconductor
Application Note 450
Josip Huljev
W. K. Boey

The SO (small outline) package has been developed to meet customer demand for ever-increasing miniaturization and component density.

COMPONENT SIZE COMPARISON

S.O. Package



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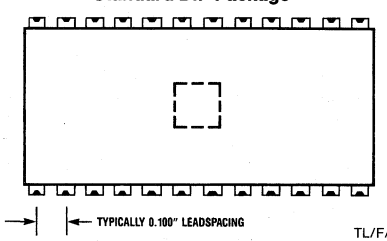
Standard DIP Package



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Because of its small size, reliability of the product assembled in SO packages needs to be carefully evaluated.

SO packages at National were internally qualified for production under the condition that they be of comparable reliability performance to a standard dual in line package under all accelerated environmental tests. *Figure A* is a summary of accelarated bias moisture test performance on 30V bipolar and 15V CMOS product assembled in SO and DIP (control) packages.

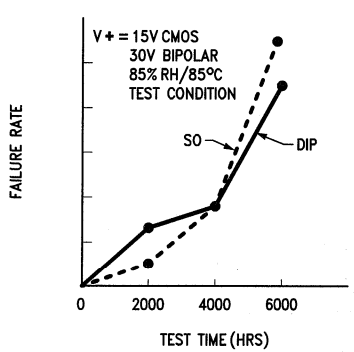

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FIGURE A

In order to achieve reliability performance comparable to DIPs—SO packages are designed and built with materials and processes that effectively compensate for their small size.

All SO packages tested on 85%RA, 85°C were assembled on PC conversion boards using vapor-phase reflow soldering. With this approach we are able to measure the effect of surface mounting methods on reliability of the process. As illustrated in *Figure A* no significant difference was detected between the long term reliability performance of surface mounted S.O. packages and the DIP control product for up to 6000 hours of accelerated 85%/85°C testing.

SURFACE-MOUNT PROCESS FLOW

The standard process flowcharts for basic surface-mount operation and mixed-lead insertion/surface-mount operations, are illustrated on the following pages.

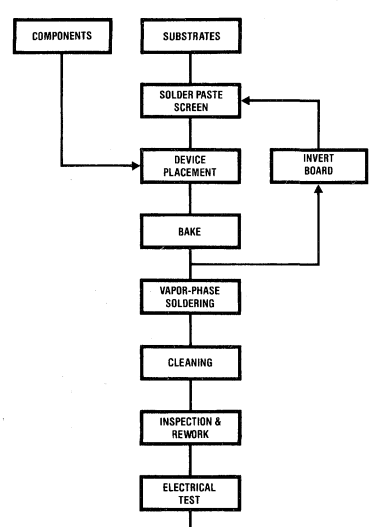
Usual variations encountered by users of SO packages are:

- Single-sided boards, surface-mounted components only.
- Single-sided boards, mixed-lead inserted and surface-mounted components.
- Double-sided boards, surface-mounted components only.
- Double-sided boards, mixed-lead inserted and surface-mounted components.

In consideration of these variations, it became necessary for users to utilize techniques involving wave soldering and adhesive applications, along with the commonly-used vapor-phase solder reflow soldering technique.

PRODUCTION FLOW

Basic Surface-Mount Production Flow



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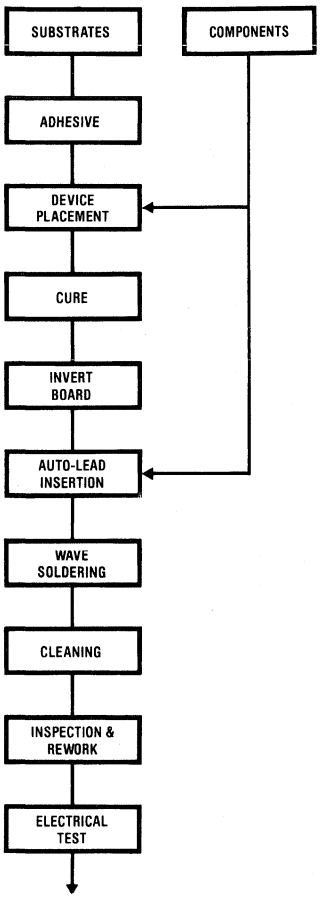
Mixed Surface-Mount and Axial-Leaded Insertion Components Production Flow



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Thermal stress of the packages during surface-mounting processing is more severe than during standard DIP PC board mounting processes. *Figure B* illustrates package temperature versus wave soldering dwell time for surface mounted packages (components are immersed into the molten solder) and the standard DIP wave soldering process. (Only leads of the package are immersed into the molten solder).

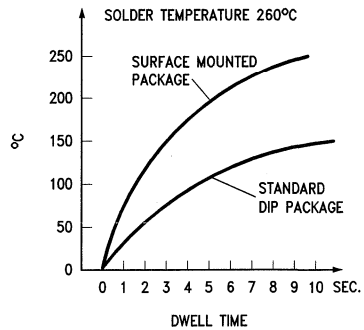

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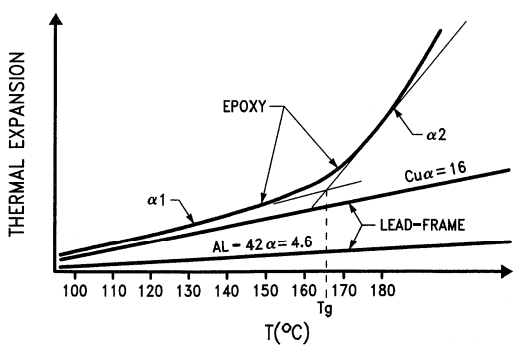
FIGURE B

For an ideal package, the thermal expansion rate of the encapsulant should match that of the leadframe material in order for the package to maintain mechanical integrity during the soldering process. Unfortunately, a perfect matchup of thermal expansion rates with most presently used packaging materials is scarce. The problem lies primarily with the epoxy compound.

Normally, thermal expansion rates for epoxy encapsulant and metal lead frame materials are linear and remain fairly close at temperatures approaching 160°C, *Figure C.* At lower temperatures the difference in expansion rate of the two materials is not great enough to cause interface separation. However, when the package reaches the glass-transition temperature (T_g) of epoxy (typically 160–165°C), the thermal expansion rate of the encapsulant increases sharply, and the material undergoes a transition into a plastic state. The epoxy begins to expand at a rate three times or more greater than the metal leadframe, causing a separation at the interface.



TL/F/8766–26

FIGURE C

When this happens during a conventional wave soldering process using flux and acid cleaners, process residues and even solder can enter the cavity created by the separation and become entrapped when the material cools. These contaminants can eventually diffuse into the interior of the package, especially in the presence of moisture. The result is die contamination, excessive leakage, and even catastrophic failure. Unfortunately, electrical tests performed immediately following soldering may not detect potential flaws.

Most soldering processes involve temperatures ranging up to 260°C, which far exceeds the glass-transition temperature of epoxy. Clearly, circuit boards containing SMD packages require tighter process controls than those used for boards populated solely by DIPs.

Figure D is a summary of accelerated bias moisture test performance on the 30V bipolar process.

Group 1 — Standard DIP package

Group 2 — SO packages vapor-phase reflow soldered on PC boards

Group 3–6 SO packages wave soldered on PC boards

Group 3 — dwell time 2 seconds

4 — dwell time 4 seconds

5 — dwell time 6 seconds

6 — dwell time 10 seconds

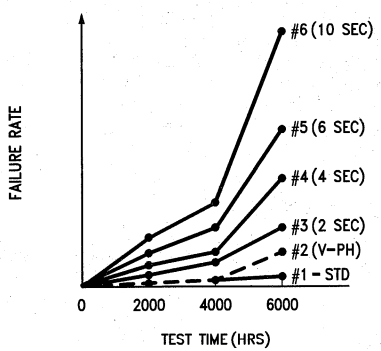


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FIGURE D

It is clear based on the data presented that SO packages soldered onto PC boards with the vapor phase reflow process have the best long term bias moisture performance and this is comparable to the performance of standard DIP packages. The key advantage of reflow soldering methods is the clean environment that minimized the potential for contamination of surface mounted packages, and is preferred for the surface-mount process.

When wave soldering is used to surface mount components on the board, the dwell time of the component under molten solder should be no more than 4 seconds, preferrably under 2 seconds in order to prevent damage to the component. Non-Halide, or (organic acid) fluxes are highly recommended.

PICK AND PLACE

The choice of automatic (all generally programmable) pick-and-place machines to handle surface mounting has grown considerably, and their selection is based on individual needs and degree of sophistication.

The basic component-placement systems available are classified as:

(a) In-line placement

— Fixed placement stations

— Boards indexed under head and respective components placed

(b) Sequential placement

— Either a X-Y moving table system or a θ, X-Y moving pickup system used

—Individual components picked and placed onto boards

(c) Simultaneous placement

— Multiple pickup heads

— Whole array of components placed onto the PCB at the same time

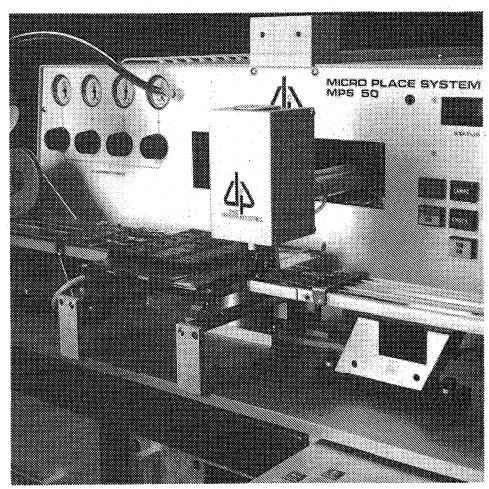
(d) Sequential/simultaneous placement

— X–Y moving table, multiple pickup heads system

— Components placed on PCB by successive or simultaneous actuation of pickup heads

The SO package is treated almost the same as surface-mount, passive components requiring correct orientation in placement on the board.

Pick and Place Action



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BAKE

This is recommended, despite claims made by some solder paste suppliers that this step be omitted.

The functions of this step are:

- Holds down the solder globules during subsequent reflow soldering process and prevents expulsion of small solder balls.
- Acts as an adhesive to hold the components in place during handling between placement to reflow soldering.
- Holds components in position when a double-sided surface-mounted board is held upside down going into a vapor-phase reflow soldering operation.
- Removes solvents which might otherwise contaminate other equipment.
- Initiates activator cleaning of surfaces to be soldered.
- Prevents moisture absorption.

The process is moreover very simple. The usual schedule is about 20 minutes in a 65°C–95°C (dependent on solvent system of solder paste) oven with adequate venting. Longer bake time is not recommended due to the following reasons:

- The flux will degrade and affect the characteristics of the paste.
- Solder globules will begin to oxidize and cause solderability problems.
- The paste will creep and after reflow, may leave behind residues between traces which are difficult to remove and vulnerable to electro-migration problems.

REFLOW SOLDERING

There are various methods for reflowing the solder paste, namely:

- Hot air reflow
- Infrared heating (furnaces)
- Convectional oven heating
- Vapor-phase reflow soldering
- Laser soldering

For SO applications, hot air reflow/infrared furnace may be used for low-volume production or prototype work, but vapor-phase soldering reflow is more efficient for consistency and speed. Oven heating is not recommended because of "hot spots" in the oven and uneven melting may result. Laser soldering is more for specialized applications and requires a great amount of investment.

HOT GAS REFLOW/INFRARED HEATING

A hand-held or table-mount air blower (with appropriate orifice mask) can be used.

The boards are preheated to about 100°C and then subjected to an air jet at about 260°C. This is a slow process and results may be inconsistent due to various heat-sink properties of passive components.

Use of an infrared furnace is the next step to automating the concept, except that the heating is promoted by use of IR lamps or panels. The main objection to this method is that certain materials may heat up at different rates under IR radiation and may result in damage to these components (usually sockets and connectors). This could be minimized by using far-infrared (non-focused) system.

VAPOR-PHASE REFLOW SOLDERING

Currently the most popular and consistent method, vapor-phase soldering utilizes a fluoroinert fluid with excellent heat-transfer properties to heat up components until the solder paste reflows. The maximum temperature is limited by the vapor temperature of the fluid.

The commonly used fluids (supplied by 3M Corp) are:

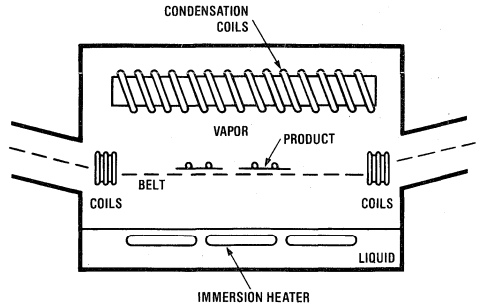
- FC-70, 215°C vapor (most applications) or FX-38
- FC-71, 253°C vapor (low-lead or tin-plate)

HTC, Concord, CA, manufactures equipment that utilizes this technique, with two options:

- Batch systems, where boards are lowered in a basket and subjected to the vapor from a tank of boiling fluid.
- In-line conveyorized systems, where boards are placed onto a continuous belt which transports them into a concealed tank where they are subjected to an environment of hot vapor.

Dwell time in the vapor is generally on the order of 15–30 seconds (depending on the mass of the boards and the loading density of boards on the belt).

In-Line Conveyorized Vapor-Phase Soldering



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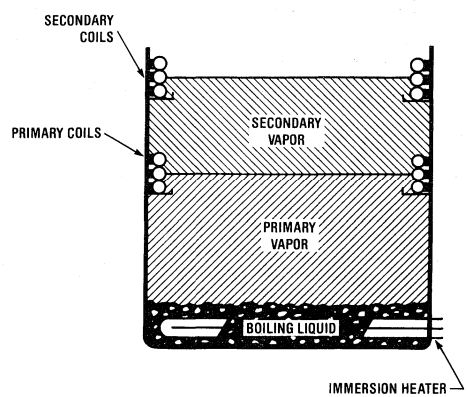
The question of thermal shock is asked frequently because of the relatively sharp increase in component temperature from room temperature to 215°C. SO packages mounted on representative boards have been tested and have shown little effect on the integrity of the packages. Various packages, such as cerdips, metal cans and TO-5 cans with glass seals, have also been tested.

Vapor-Phase Furnace

TL/F/8766–10

Batch-Fed Production Vapor-Phase Soldering Unit



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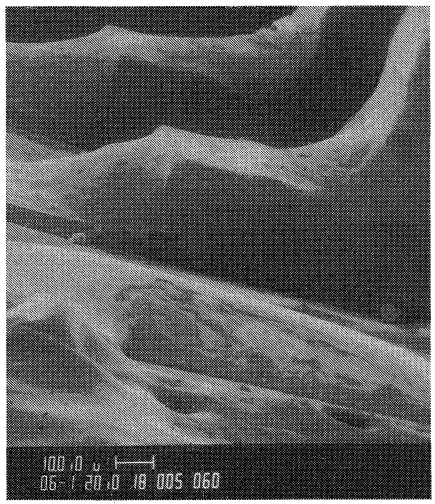
Solder Joints on a SO-14 Package on PCB



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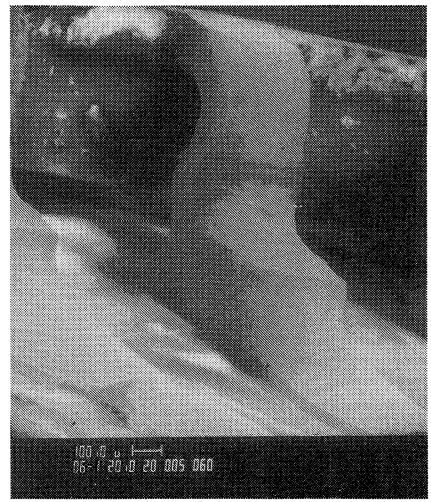
Solder Joints on a SO-14 Package on PCB



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PRINTED CIRCUIT BOARD

The SO package is molded out of clean, thermoset plastic compound and has no particular compatibility problems with most printed circuit board substrates.

The package can be reliably mounted onto substrates such as:

- G10 or FR4 glass/resin
- FR5 glass/resin systems for high-temperature applications
- Polymide boards, also high-temperature applications
- Ceramic substrates

General requirements for printed circuit boards are:

- Mounting pads should be solder-plated whenever applicable.
- Solder masks are commonly used to prevent solder bridging of fine lines during soldering.

  The mask also protects circuits from processing chemical contamination and corrosion.

  If coated over pre-tinned traces, residues may accumulate at the mask/trace interface during subsequent reflow, leading to possible reliability failures.

  Recommended application of solder resist on bare, clean traces prior to coating exposed areas with solder.

  General requirements for solder mask:

  — Good pattern resolution.

  — Complete coverage of circuit lines and resistance to flaking during soldering.

  — Adhesion should be excellent on substrate material to keep off moisture and chemicals.

  — Compatible with soldering and cleaning requirements.

SOLDER PASTE SCREEN PRINTING

With the initial choice of printed circuit lithographic design and substrate material, the first step in surface mounting is the application of solder paste.

The typical lithographic "footprints" for SO packages are illustrated below. Note that the 0.050″ lead center-center spacing is not easily managed by commercially-available air pressure, hand-held dispensers.

Using a stainless-steel, wire-mesh screen stencilled with an emulsion image of the substrate pads is by far the most common and well-tried method. The paste is forced through the screen by a V-shaped plastic squeegee in a sweeping manner onto the board placed beneath the screen.

The setup for SO packages has no special requirement from that required by other surface-mounted, passive components. Recommended working specifications are:

- Use stainless-steel, wire-mesh screens, #80 or #120, wire diameter 2.6 mils. Rule of thumb: mesh opening should be approximately 2.5–5 times larger than the average particle size of paste material.
- Use squeegee of Durometer 70.
- Experimentation with squeegee travel speed is recommended, if available on machine used.
- Use solder paste of mesh 200–325.
- Emulsion thickness of 0.005″ usually used to achieve a solder paste thickness (wet) of about 0.008″ typical.
- Mesh pattern should be 90 degrees, square grid.
- Snap-off height of screen should not exceed $\frac{1}{8}$″, to avoid damage to screens and minimize distortion.

SOLDER PASTE

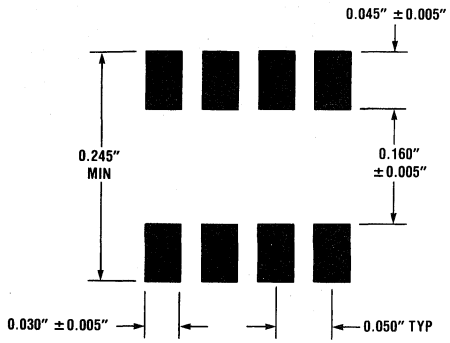
Selection of solder paste tends to be confusing, due to numerous formulations available from various manufacturers. In general, the following guidelines are sufficient to qualify a particular paste for production:

- Particle sizes (see photographs below). Mesh 325 (approximately 45 microns) should be used for general purposes, while larger (solder globules) particles are preferred for leadless components (LCC). The larger particles can easily be used for SO packages.

- Uniform particle distribution. Solder globules should be spherical in shape with uniform diameters and minimum amount of elongation (visual under 100/200 × magnification). Uneven distribution causes uneven melting and subsequent expulsion of smaller solder balls away from their proper sites.
- Composition, generally 60/40 or 63/37 Sn/Pb. Use 62/36 Sn/Pb with 2% Ag in the presence of Au on the soldering area. This formulation reduces problems of metal leaching from soldering pads.
- RMA flux system usually used.
- Use paste with aproximately 88–90% solids.

RECOMMENDED SOLDER PADS FOR SO PACKAGES

SO-8, SO-14, SO-16



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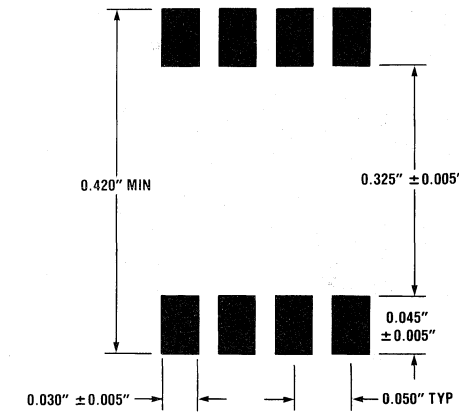
SO-16L, SO-20



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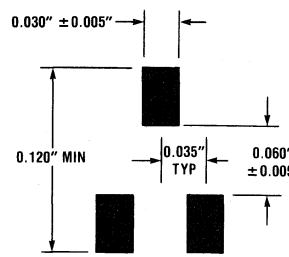
SOT-23



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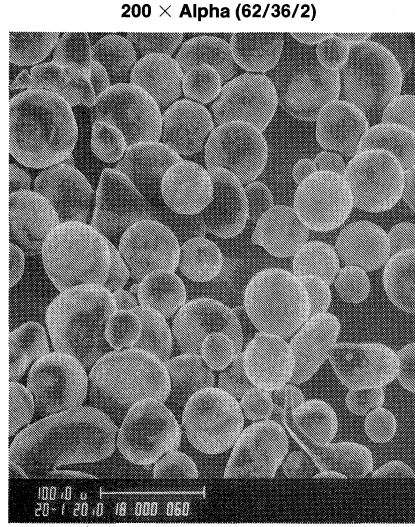
Comparison of Particle Size/Shape of Various Solder Pastes

200 × Alpha (62/36/2)



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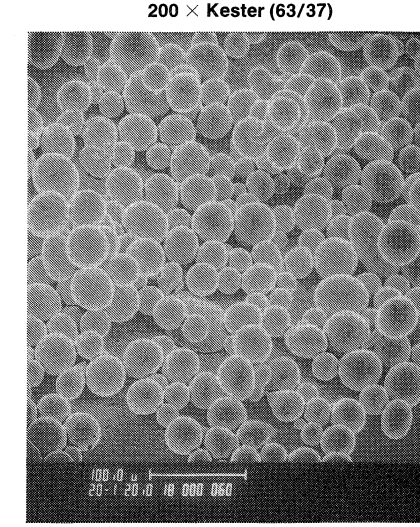
200 × Kester (63/37)



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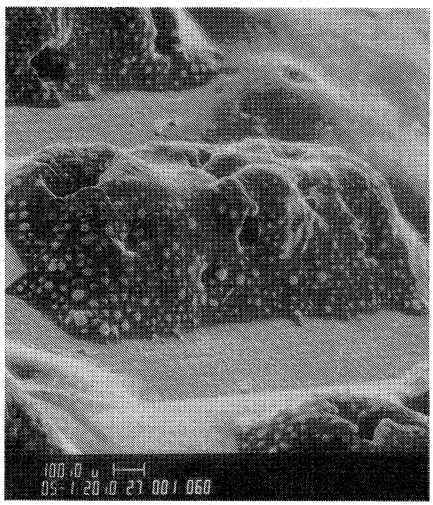
Comparison of Particle Size/Shape of Various Solder Pastes (Continued)

Solder Paste Screen on Pads



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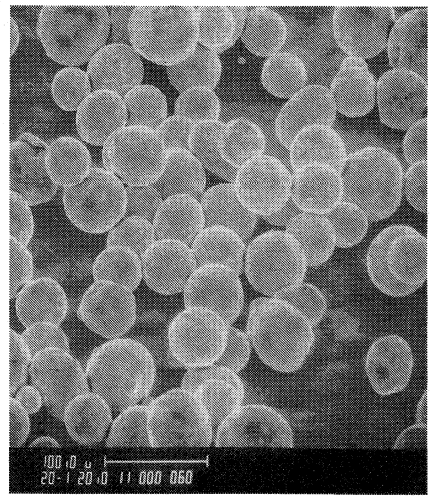
200 × Fry Metal (63/37)



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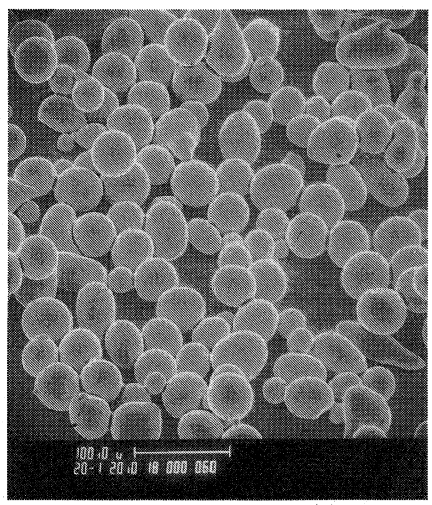
200 ESL (63/37)



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CLEANING

The most critical process in surface mounting SO packages is in the cleaning cycle. The package is mounted very close to the surface of the substrate and has a tendency to collect residue left behind after reflow soldering.

Important considerations in cleaning are:

- Time between soldering and cleaning to be as short as possible. Residue should not be allowed to solidify on the substrate for long periods of time, making it difficult to dislodge.
- A low surface tension solvent (high penetration) should be employed. Solvents commercially available are:

  Freon TMS (general purpose)
  Freon TE35/TP35 (cold-dip cleaning)
  Freon TES (general purpose)

  It should also be noted that these solvents generally will leave the substrate surface hydrophobic (moisture repellent), which is desirable.

  Prelete or 1,1,1-Trichloroethane
  Kester 5120/5121
- A defluxer system which allows the workpiece to be subjected to a solvent vapor, followed by a rinse in pure solvent and a high-pressure spray lance are the basic requirments for low-volume production.
- For volume production, a conveyorized, multiple hot solvent spray/jet system is recommended.
- Rosin, being a natural occurring material, is not readily soluble in solvents, and has long been a stumbling block to the cleaning process. In recent developments, synthetic flux (SA flux), which is readily soluble in Freon TMS solvent, has been developed. This should be explored where permissible.

The dangers of an inadequate cleaning cycle are:

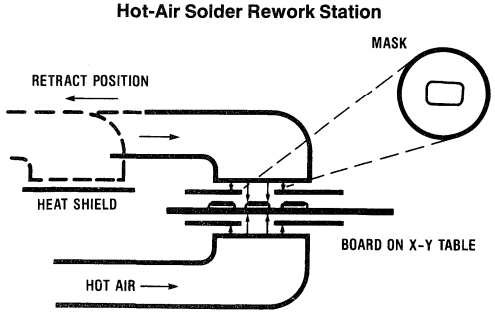
- Ion contamination, where ionic residue left on boards would cause corrosion to metallic components, affecting the performance of the board.
- Electro-migration, where ionic residue and moisture present on electrically-biased boards would cause dentritic growth between close spacing traces on the substrate, resulting in failures (shorts).

REWORK

Should there be a need to replace a component or re-align a previously disturbed component, a hot air system with appropriate orifice masking to protect surrounding components may be used.

When rework is necessary in the field, specially-designed tweezers that thermally heat the component may be used to remove it from its site. The replacement can be fluxed at the lead tips or, if necessary, solder paste can be dispensed onto the pads using a varimeter. After being placed into position, the solder is reflowed by a hot-air jet or even a standard soldering iron.

Hot-Air Solder Rework Station



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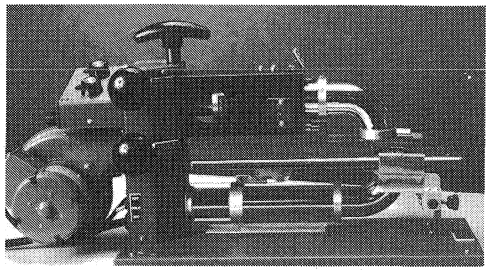
Hot-Air Rework Machine



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WAVE SOLDERING

In a case where lead insertions are made on the same board as surface-mounted components, there is a need to include a wave-soldering operation in the process flow.

Two options are used:

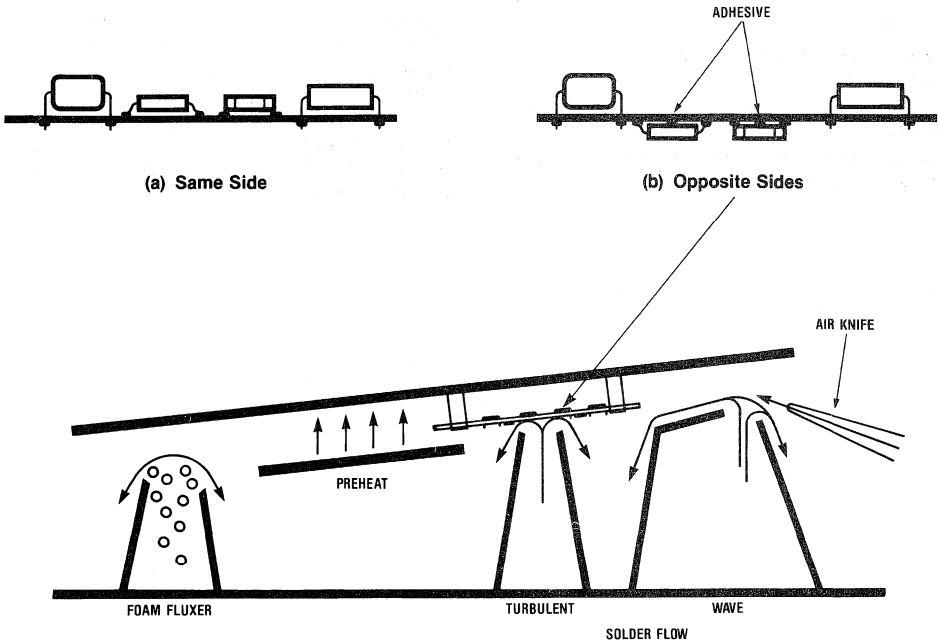
- Surface mounted components are placed and vapor phase reflowed before auto-insertion of remaining components. The board is carried over a standard wave-solder system and the underside of the board (only lead-inserted leads) soldered.
- Surface-mounted components are placed in position, but no solder paste is used. Instead, a drop of adhesive about 5 mils maximum in height with diameter not exceeding 25% width of the package is used to hold down the package. The adhesive is cured and then proceeded to auto-insertion on the reverse side of the board (surface-mounted side facing down). The assembly is then passed over a "dual wave" soldering system. Note that the surface-mounted components are immersed into the molten solder.

Lead trimming will pose a problem after soldering in the latter case, unless the leads of the insertion components are pre-trimmed or the board specially designed to localize certain areas for easy access to the trim blade.

The controls required for wave soldering are:

- Solder temperature to be 240–260°C. The dwell time of components under molten solder to be short (preferably kept under 2 seconds), to prevent damage to most components and semiconductor devices.
- RMA (Rosin Mildly Activated) flux or more aggressive OA (Organic Acid) flux are applied by either dipping or foam fluxing on boards prior to preheat and soldering. Cleaning procedures are also more difficult (aqueous, when OA flux is used), as the entire board has been treated by flux (unlike solder paste, which is more or less localized). Non-halide OA fluxes are highly recommended.
- Preheating of boards is essential to reduce thermal shock on components. Board should reach a temperature of about 100°C just before entering the solder wave.
- Due to the closer lead spacings (0.050″ vs 0.100″ for dual-in-line packages), bridging of traces by solder could occur. The reduced clearance between packages also causes "shadowing" of some areas, resulting in poor solder coverage. This is minimized by dual-wave solder systems.

Mixed Surface Mount and Lead Insertion



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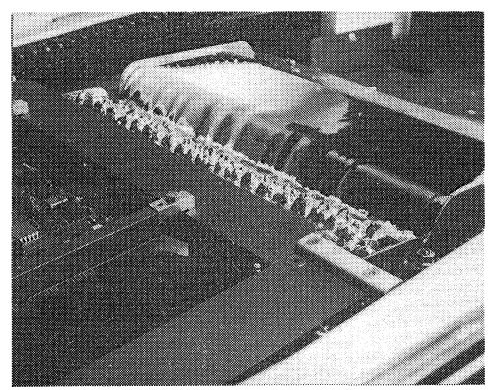
A typical dual-wave system is illustrated below, showing the various stages employed. The first wave typically is in turbulence and given a transverse motion (across the motion of the board). This covers areas where "shadowing" occurs. A second wave (usually a broad wave) then proceeds to perform the standard soldering. The departing edge from the solder is such to reduce "icicles," and is still further reduced by an air knife placed close to the final soldering step. This air knife will blow off excess solder (still in the fluid stage) which would otherwise cause shorts (bridging) and solder bumps.

Dual Wave



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AQUEOUS CLEANING

- For volume production, a conveyorized system is often used with a heated recirculating spray wash (water temperature 130°C), a final spray rinse (water temperature 45–55°C), and a hot (120°C) air/air-knife drying section.
- For low-volume production, the above cleaning can be done manually, using several water rinses/tanks. Fast-drying solvents, like alcohols that are miscible with water, are sometimes used to help the drying process.
- Neutralizing agents which will react with the corrosive materials in the flux and produce material readily soluble in water may be used; the choice depends on the type of flux used.
- Final rinse water should be free from chemicals which are introduced to maintain the biological purity of the water. These materials, mostly chlorides, are detrimental to the assemblies cleaned because they introduce a fresh amount of ionizable material.

CONFORMAL COATING

Conformal coating is recommended for high-reliability PCBs to provide insulation resistance, as well as protection against contamination and degradation by moisture.

Requirements:

- Complete coating over components and solder joints.
- Thixotropic material which will not flow under the packages or fill voids, otherwise will introduce stress on solder joints on expansion.
- Compatibility and possess excellent adhesion with PCB material/components.
- Silicones are recommended where permissible in application.

5

SMD Lab Support

FUNCTIONS

Demonstration—Introduce first-time users to surface-mounting processes.

Service—Investigate problems experienced by users on surface mounting.

Reliability Builds—Assemble surface-mounted units for reliability data acquisition.

Techniques—Develop techniques for handling different materials and processes in surface mounting.

Equipment—In conjunction with equipment manufacturers, develop customized equipments to handle high density, new technology packages developed by National.

In-House Expertise—Availability of in-house expertise on semiconductor research/development to assist users on packaging queries.

Section 6

Appendices/ Physical Dimensions

Section 6 Contents

National Semiconductor

Appendix A
General Product Marking & Code Explanation

LF 356 N /A+

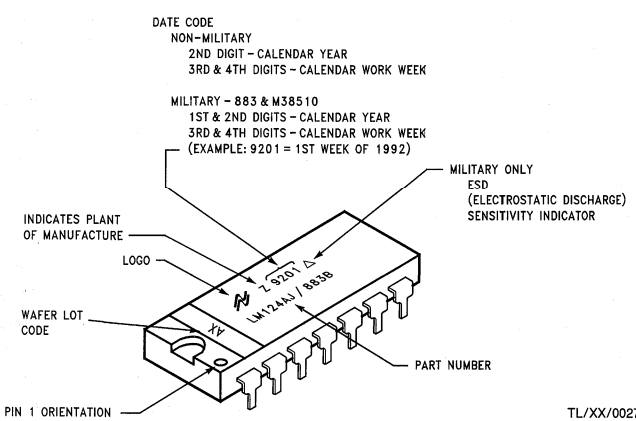
- /A+ — Reliability Program (Optional) (Refer to Appendix C)
- N — Package Type (See Right)
- 356 — Device Number (Generic Type) and Suffix Letter (Optional)
  - A or B: Improved Electrical Specification
  - C, I, E or M: Temperature Range
- LF — Device Family (See Below)

Device Family

ADC	Data Conversion
AF	Active Filter
AH	Analog Switch (Hybrid)
DAC	Data Conversion
DM	Digital (Monolithic)
HS	Hybrid
LF	Linear (Bifet)
LH	Linear (Hybrid)
LM	Linear (Monolithic)
LMC	Linear CMOS
LMD	Linear DMOS
LP	Linear (Low Power)
LPC	Linear CMOS (Low Power)
MF	Linear (Monolithic Filter)
LMF	Linear Monolithic Filter

Package Type

D	Glass/Metal DIP
E	Ceramic Leadless Chip Carrier (LCC)
F	Glass/Metal Flat Pak (1/4" x 1/4")
G	12 Lead TO-8 Metal Can (M/C)
H	Multi-Lead Metal Can (M/C)
H-05	4 Lead M/C (TO-5) } Shipped with
H-46	4 Lead M/C (TO-46) } Thermal Shield
J	Lo-Temp Ceramic DIP
J-8	8 Lead Ceramic DIP ("MiniDIP")
J-14	14 Lead Ceramic DIP (-14 used only when product is also available in -8 pkg).
K	TO-3 M/C in Steel, except LM309K which is shipped in Aluminum
KC	TO-3 M/C (Aluminum)
K Steel	TO-3 M/C (Steel)
M	Small Outline Package
M3	3-Lead Small Outline Package
N	Molded DIP (EPOXY B)
N-01	Molded DIP (Epoxy B) with Staggered Leads
N-8	8 Lead Molded DIP (Epoxy B) ("Mini-DIP")
N-14	14 Lead Molded DIP (Epoxy B) (-14 used only when product is also available in -8 pkg).
P	3 Lead TO-202 Power Pkg
Q	Cerdip with UV Window
T	3,5,11,15 & 23 Lead TO-220 PWR Pkg (Epoxy B)
V	Multi-lead Plastic Chip Carrier (PCC)
W	Lo-Temp Ceramic Flat Pak
WM	Wide Body Small Outline Package



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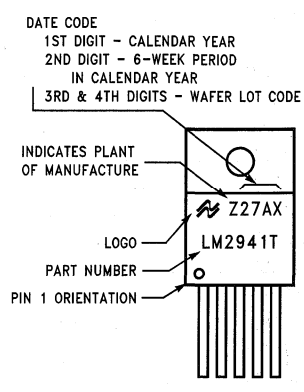

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National Semiconductor

Appendix B
Device/Application Literature Cross-Reference

Device Number	Application Literature
ADCXXXX	AN-156
ADC80	AN-360
ADC0801	AN-233, AN-271, AN-274, AN-280, AN-281, AN-294, LB-53
ADC0802	AN-233, AN-274, AN-280, AN-281, LB-53
ADC0803	AN-233, AN-274, AN-280, AN-281, LB-53
ADC08031	AN-460
ADC0804	AN-233, AN-274, AN-276, AN-280, AN-281, AN-301, AN-460, LB-53
ADC0805	AN-233, AN-274, AN-280, AN-281, LB-53
ADC0808	AN-247, AN-280, AN-281
ADC0809	AN-247, AN-280
ADC0816	AN-193, AN-247, AN-258, AN-280
ADC0817	AN-247, AN-258, AN-280
ADC0820	AN-237
ADC0831	AN-280, AN-281
ADC0832	AN-280, AN-281
ADC0833	AN-280, AN-281
ADC0834	AN-280, AN-281
ADC0838	AN-280, AN-281
ADC1001	AN-276, AN-280, AN-281
ADC1005	AN-280
ADC10461	AN-769
ADC10462	AN-769
ADC10464	AN-769
ADC10662	AN-769
ADC10664	AN-769
ADC1210	AN-245
ADC12441	AN-769
ADC12451	AN-769
ADC3501	AN-200, AN-202
ADC3511	AN-200
ADC3701	AN-200
ADC3711	AN-200
AH0014	AN-38
AH0019	AN-38
CD4016	AB-10
DACXXXX	AN-156
DAC0800	AN-693
DAC0830	AN-284
DAC0831	AN-271, AN-284
DAC0832	AN-271, AN-284
DAC1000	AN-271, AN-275, AN-277, AN-284
DAC1001	AN-271, AN-275, AN-277, AN-284
DAC1002	AN-271, AN-275, AN-277, AN-284

Device/Application Literature Cross-Reference (Continued)

Device Number	Application Literature
DAC1006	AN-271, AN-275, AN-277, AN-284
DAC1007	AN-271, AN-275, AN-277, AN-284
DAC1008	AN-271, AN-275, AN-277, AN-284
DAC1020	AN-263, AN-269, AN-2293, AN-294, AN-299
DAC1021	AN-269
DAC1022	AN-269
DAC1208	AN-271, AN-284
DAC1209	AN-271, AN-284
DAC1210	AN-271, AN-284
DAC1218	AN-293
DAC1219	AN-693
DAC1220	AN-253, AN-269
DAC1221	AN-269
DAC1222	AN-269
DAC1230	AN-284
DAC1231	AN-271, AN-284
DAC1232	AN-271, AN-284
DAC1280	AN-261, AN-263
DH0034	AN-253
DH0035	AN-49
Digitalker	AN-252, LB-54
DM8890	Appendix B
DS8606	AN-381, AN-382
DS8608	AN-382
DT1058	AN-287
DT1060	AN-287
DTSW250E2	AN-287
DTSW250GI	AN-287
INS8070	AN-260
LF111	LB-39
LF155	AN-263, AN-447
LF198	AN-245, AN-294
LF311	AN-301
LF347	AN-256, AN-262, AN-263, AN-265, AN-266, AN-301, AN-344, AN-447, LB-44
LF351	AN-242, AN-263, AN-266, AN-271, AN-275, AN-293, AN-447, Appendix C
LF351A	AN-240
LF351B	Appendix D
LF353	AN-256, AN-258, AN-262, AN-263, AN-264, AN-266, AN-271, AN-285, AN-293, AN-447, LB-44, Appendix D
LF356	AN-253, AN-258, AN-260, AN-263, AN-266, AN-271, AN-272, AN-275, AN-293, AN-294, AN-295, AN-301, AN-447, AN-693
LF357	AN-263, AN-447, LB-42
LF398	AN-247, AN-258, AN-266, AN-294, AN-298, LB-45
LF400	AN-428, AN-447
LF411	AN-294, AN-301, AN-344, AN-447
LF412	AN-272, AN-299, AN-301, AN-344, AN-447
LF441	AN-301, AN-447
LF13006	AN-344
LF13007	AN-344
LF13331	AN-294, AN-447
LF13508	AN-289, AN-360, AN-447
LF13509	AN-289, AN-295, AN-447

Device/Application Literature Cross-Reference (Continued)

Device Number	Application Literature
LH0002	AN-13, AN-63, AN-227, AN-244, AN-263, AN-272, AN-301
LH0005	AN-13
LH0022	AN-63, AN-75
LH0023	AN-245, AN-360
LH0024	AN-253
LH0032	AN-242, AN-244, AN-253
LH0033	AN-48, AN-115, AN-227, AN-253
LH0042	AN-63
LH0043	AN-245
LH0052	AN-63
LH0053	AN-245
LH0062	AN-75
LH0063	AN-227
LH0070	AN-301
LH0071	AN-245
LH0082	AN-244, AN-266
LH0086	AN-245, AN-360
LH0091	AN-180
LH0094	AN-301
LH0101	AN-261
LH1605	AN-343
LM10	AN-211, AN-247, AN-258, AN-271, AN-288, AN-299, AN-300, AN-460, AN-693
LM11	AN-241, AN-242, AN-260, AN-266, AN-271
LM12	AN-446, AN-693, AN-706
LM101	AN-4, AN-13, AN-20, AN-24, AN-75, LB-42, Appendix A
LM101A	AN-29, AN-30, AN-31, AN-79, AN-241 AN-711, LB-1, LB-2, LB-4, LB-8, LB-14, LB-16, LB-19, LB-28
LM102	AN-4, AN-13, AN-30, LB-1, LB-5, LB-6, LB-11
LM103	AN-110, LB-41
LM104	AN-21, LB-3, LB-7, LB-10, LB-40
LM105	AN-21, AN-23, AN-110, LB-3, LB-7, LB-10
LM106	AN-41, LB-6, LB-12
LM107	AN-20, AN-31, LB-1, LB-12, LB-19, Appendix A
LM108	AN-29, AN-30, AN-31, AN-63, AN-79, AN-211, AN-241, LB-14, LB-15, LB-21
LM108A	AN-260, LB-15, LB-19
LM109	AN-42, LB-15
LM109A	LB-15
LM110	LB-11, LB-42
LM111	AN-41, AN-103, LB-12, LB-16, LB-32, LB-39
LM112	AN-63, LB-19
LM113	AN-56, AN-110, LB-21, LB-24, LB-28, LB-37
LM117	AN-178, AN-181, AN-182, LB-46, LB-47
LM117HV	LB-46, LB-47
LM118	LB-17, LB-19, LB-21, LB-23, Appendix A
LM119	AN-115, LB-23
LM120	AN-182
LM121	AN-79, AN-104, AN-184, AN-260, LB-22
LM121A	LB-32
LM122	AN-97, LB-38
LM125	AN-82
LM126	AN-82

Device/Application Literature Cross-Reference (Continued)

Device Number	Application Literature
LM129	AN-173, AN-178, AN-262, AN-266
LM131	AN-210, AN-460, Appendix D
LM131A	AN-210
LM134	LB-41, AN-460
LM135	AN-225, AN-262, AN-292, AN-298, AN-460
LM137	LB-46
LM137HV	LB-46
LM138	LB-46
LM139	AN-74
LM143	AN-127, AN-271
LM148	AN-260
LM150	LB-46
LM158	AN-116
LM160	AN-87
LM161	AN-87, AN-266
LM163	AN-295
LM194	AN-222, LB-21
LM195	AN-110
LM199	AN-161, AN-260, AN-360
LM199A	AN-161
LM211	LB-39
LM216A	LB-37
LM231	AN-210
LM231A	AN-210
LM235	AN-225
LM239	AN-74
LM258	AN-116
LM260	AN-87
LM261	AN-87
LM34	AN-460
LM35	AN-460
LM301A	AN-178, AN-181, AN-222
LM304	LB-40
LM308	AN-88, AN-184, AN-272, LB-22, LB-28, Appendix D
LM308A	AN-225, LB-24
LM309	AN-178, AN-182
LM311	AN-41, AN-103, AN-260, AN-263, AN-288, AN-294, AN-295, AN-307, LB-12, LB-16, LB-18, LB-39
LM313	AN-263
LM316	AN-258
LM317	AN-178, LB-35, LB-46
LM317H	LB-47
LM318	AN-115, AN-299, LB-21
LM319	AN-115, AN-271, AN-293
LM320	AN-288
LM321	LB-24
LM324	AN-88, AN-258, AN-274, AN-284, AN-301, LB-44, AB-25, Appendix C
LM329	AN-256, AN-263, AN-284, AN-295, AN-301
LM329B	AN-225
LM330	AN-301
LM331	AN-210, AN-240, AN-265, AN-278, AN-285, AN-311, LB-45, Appendix C, Appendix D
LM331A	AN-210, Appendix C

Device/Application Literature Cross-Reference (Continued)

Device Number	Application Literature
LM334	AN-242, AN-256, AN-284
LM335	AN-225, AN-263, AN-295
LM336	AN-202, AN-247, AN-258
LM337	LB-46
LM338	LB-49, LB-51
LM339	AN-74, AN-245, AN-274
LM340	AN-103, AN-182
LM340L	AN-256
LM342	AN-288
LM346	AN-202, LB-54
LM348	AN-202, LB-42
LM349	LB-42
LM358	AN-116, AN-247, AN-271, AN-274, AN-284, AN-298, Appendix C
LM358A	Appendix D
LM359	AN-278, AB-24
LM360	AN-87
LM361	AN-87, AN-294
LM363	AN-271
LM380	AN-69, AN-146
LM381	AN-64, AN-104
LM382	AN-147
LM385	AN-242, AN-256, AN-301, AN-344, AN-460, AN-693, AN-777
LM386	LB-54
LM389	AN-256, AN-263, AN-264, AN-274
LM391	AN-272
LM392	AN-274, AN-286
LM393	AN-271, AN-274, AN-293, AN-694
LM394	AN-262, AN-263, AN-264, AN-271, AN-293, AN-299, AN-311, LB-52
LM395	AN-178, AN-181, AN-262, AN-263, AN-266, AN-301, AN-460, LB-28
LM399	AN-184
LM555	AN-694, AB-7
LM556	AB-7
LM565	AN-46, AN-146
LM566	AN-146
LM604	AN-460
LM628	AN-693, AN-706
LM629	AN-693, AN-694, AN-706
LM709	AN-24, AN-30
LM710	AN-41, LB-12
LM725	LB-22
LM741	AN-75, AN-79, LB-19, LB-22
LM832	AN-386, AN-390
LM833	AN-346
LM1036	AN-390
LM1310	AN-81
LM1458	AN-116
LM1524	AN-272, AN-288, AN-292, AN-293
LM1558	AN-116
LM1578A	AB-30
LM1807	Appendix B

Device/Application Literature Cross-Reference (Continued)

Device Number	Application Literature
LM1808	Appendix B
LM1820	LB-29
LM1828	Appendix B
LM1830	AB-10
LM1845	Appendix B
LM1865	AN-382, AN-390
LM1894	AN-384, AN-386, AN-390
LM2577	AN-776, AN-777
LM2878	AN-147
LM2907	AN-162
LM2917	AN-162
LM2931	AB-12
LM2931CT	AB-11
LM3045	AN-286
LM3046	AN-146, AN-299
LM3064	Appendix B
LM3065	Appendix B
LM3070	Appendix B
LM3071	Appendix B
LM3089	AN-147
LM3524	AN-272, AN-288, AN-292, AN-293
LM3525A	AN-694
LM3578A	AB-30
LM3900	AN-72, AN-263, AN-274, AN-278, LB-20, AB-24
LM3909	AN-154
LM3911	LB-27, AN-460
LM3914	AN-460, LB-48, AB-25
LM3915	AN-386
LM3999	AN-161
LM4250	AN-88, LB-34
LM7800	AN-178
LM78L12	AN-146
LM78S40	AN-711
LMC555	AN-460
LMC835	AN-435
LMD18200	AN-694
LM18293	AN-706
LP324	AN-284
LP395	AN-460

Device/Application Literature Cross-Reference (Continued)

Device Number	Application Literature
MF10	AN-307
MM2716	LB-54
MM54104	AN-252, AN-287, LB-54
MM57110	AN-382
MM74C00	AN-88
MM74C02	AN-88
MM74C04	AN-88
MM74C948	AN-193
MM74LS138	LB-54
MM53200	AN-290
2N4339	AN-32

National Semiconductor

Appendix C
Summary of Commercial Reliability Programs

General

National Semiconductor Commercial Reliability Programs provide a broad range of off-the-shelf enhanced semiconductor products that supply an extra measure of quality and reliability needed in high-stress or difficult to service applications.

National's A+ and B+ programs allow each individual customer to:

- Minimize the need for incoming electrical inspection
- Eliminate the need and associated costs of using independent testing laboratories
- Reduction in infant mortality rate
- Reduction in reworked board costs
- Reduction in warranty and service costs

A+ Product Enhancement

The A+ Product Enhancement incorporates the benefits of the Multiple-Pass and Elevated Temperature along with "BURN-IN."

The A+ Program provides:

- 100% Temperature Cycling
- 100% Electrical Testing at Room and High Temperature
- 100% Burn-In Testing Combining Increased Temperature with Applied Voltage
- Acceptable Quality Levels Greater than Industry Norm

Typical A+ Flow is:

- SEM
- Assembly and Seal
- Four Hour 150°C Bake
- Five Temperature Cycles (0°C to +100°C)
- High Temperature Electrical Test
- Electrical Test
- Burn-In (160 hours at a minimum junction temperature of 125°C)
- DC Parametric and Function Tests
- Tightened Quality Control Inspection Plans

Note: Certain products may follow slightly different process flows dictated by specific capabilities and device characteristics, consult NSC.

P+ Product Enhancement

The P+ product enhancement program applies to power devices and offers an added advantage. P+ involves dynamic tests that screen out assembly related and silicon defects that can lead to infant mortality and/or reduce the survivability of the device under high stress conditions. This includes but is not limited to the following devices:

Device	Package Types					
	TO-3 K STEEL	TO-39 (H)	TO-220 (T)	TO-202 (P)	DIP (N)	SO (M)
LM12	X					
LM109/309	X	X				
LM117/317	X	X	X	X		
LM117HV/317HV	X	X				
LM120/320	X	X	X	X		
LM123/323	X					
LM133/333	X		X			
LM137/337	X	X	X	X		
LM137HV/337HV	X	X				
LM138/338	X		X			
LM140/340	X		X			
LM145/345	X					
LM150/350	X		X			
LM195/395	X	X	X	X		
LM196/396	X					
LM2930/2935/2984			X			
LM2937			X			
LM2940/2941			X			
LM2990/2991			X			
LM2575/2575HV			X		X	X
LM2576			X			
LM2577			X		X	X
LMD18200/18201			X			
LM18298			X			

National Semiconductor

Appendix D
Military Aerospace Programs from National Semiconductor

This appendix is intended to provide a brief overview of military products available from National Semiconductor. For further information, refer to our 1987 Reliability Handbook.

National Semiconductor's Military/Aerospace Program is founded on dedication to excellence. National offers complete support across the broadest range of products with the widest selection of qualification levels and screening flows. These flows include:

Process Flows (Integrated Circuits)	Description
JAN S	QPL products processed to MIL-M-38510 Level S for space level applications.
JAN B	QPL products processed to MIL-M-38510 Level B for military applications.
SMD	Standard Military Drawing products processed to Level B with Table I Electricals controlled by DESC. (Formally called DESC Drawing.)
883	Products processed to MIL-STD-883 Level B for military applications.
MLP	Products processed on the Monitored Line (Program) developed by the Air Force for space level applications.
MIL S	Non-JAN products processed to Level S to negotiated electrical specifications for space level applications.
-MIL	Similar to MIL-STD-883 with exceptions noted on Certificate of Conformance.
MSP	Military Screening Program for initial release of advanced products.

- **MIL-M-38510:** The MIL-M-38510 Program, which is sometimes called the JAN IC Program, is administered by the Defense Electronics Supply Center (DESC). The purpose of this program is to provide the military community with standardized products that have been manufactured and screened to government-controlled specifications in government certified facilities. All 38510 manufacturers must be formally qualified and their products listed on DESC's Qualified Products List (QPL) before devices can be marked and shipped as JAN product.

  There are two processing levels specified within MIL-M-38510: Class S and B. Class S is typically specified for space flight applications, while Class B is used for aircraft, naval and ground systems. National is a major supplier of both classes of devices. Screening requirements are outlined in Table III.

  Tables I and II explain the JAN device marking system.

  Copies of MIL-M-38510, the QPL and other related documents may be obtained from:

  Naval Publications and Forms Center
  5801 Tabor Avenue
  Philadelphia, PA 19120
  (212) 697-2179

- **Standard Military Drawings (SMD):** SMD's are issued to provide standardized versions of devices which are not available as JAN product. MIL-STD-883 Class B screening is coupled with tightly controlled electrical specifications which have been written to allow a manufacturer to use his standard electrical tests. A current listing of National's SMD offerings can be obtained from our authorized distributors, sales offices or DESC. DESC is located in Dayton, Ohio.

- **MIL-STD-883:** Although originally intended to establish uniform test methods and procedures, MIL-STD-883 has also become the general specification for non-JAN military product. Revision D of this document defines the minimum requirements for a device to be marked and advertised as 883-compliant. Included are design and construction criteria, documentation controls, electrical and mechanical screening requirements, and quality control procedures. Details can be found in paragraph 1.2.1 of MIL-STD-883.

  National offers both 883 Class B and 883 Class S product. The screening requirements for both classes of product are outlined in Table III.

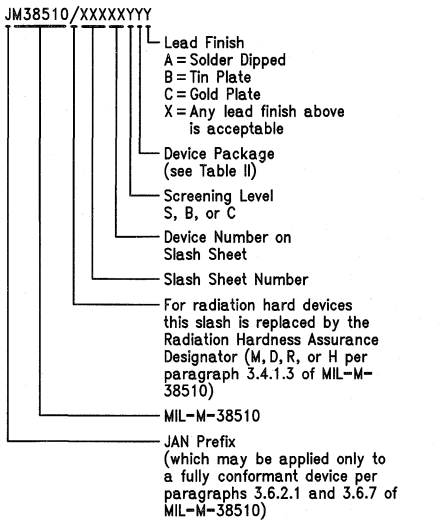
  As with SMDs a manufacturer is allowed to use his standard electrical tests provided that all critical parameters are tested. Also, the electrical test parameters, test conditions, test limits and test temperatures must be clearly documented. At National Semiconductor, this information is available via our Table I (formerly RETS, Reliability Electrical Test Specification Program). The Table I document is a complete description of the electrical tests performed and is controlled by our QA department. Individual copies are available upon request.

  Some of National's products are produced on a flow similar to MIL-STD-883. These devices are screened to the same stringent requirements as 883 product, but are marked as **-MIL**; specific reasons for prevention of compliancy are clearly defined in the Certificate of Conformance (C of C) shipped with the product.

- **Monitored Line Program (MLP):** is a non JAN Level S program developed by the Air Force. Monitored Line product usually provides the shortest cycle time, and is acceptable for application in several space level programs. Lockheed Missiles and Space Company in Sunnyvale, California, under an Air Force contract, provides "on-site" monitoring of product processing, and as appropriate, program management. Monitored Line orders generally do not allow "customizing", and most flows do not include quality conformance inspection. Drawing control is maintained by the Lockheed Company.

- **Military Screening Program (MSP):** National's Military Screening Program was developed to make screened versions of advanced products such as gate arrays and microprocessors available more quickly than is possible for JAN and 883 devices. Through this program, screened product is made available for prototypes and breadboards prior to or during the JAN or 883 qualification activities. MSP products receive the 100% screening of Table III, but are not subjected to Group C and D quality conformance testing. Other criteria such as electrical testing and temperature range will vary depending upon individual device status and capability.

TABLE I. The MIL-M-38510 Part Marking



TL/XX/0030–1

TABLE II. JAN Package Codes

38510 Package Designation	Microcircuit Industry Description
A	14-pin 1/4" x 1/4" (Metal) Flatpak
B	14-pin 3/16" x 1/4" (Metal) Flatpak
C	14-pin 1/4" x 3/4" Dual-In-Line
D	14-pin 1/4" x 3/8" (Ceramic) Flatpak
E	16-pin 1/4" x 7/8" Dual-In-Line
F	16-pin 1/4" x 3/8" (Metal or Ceramic) Flatpak
G	8-pin TO-99 Can or Header
H	10-pin 1/4" x 1/4" (Metal) Flatpak
I	10-pin TO-100 Can or Header
J	24-pin 1/2" x 1 1/4" Dual-In-Line
K	24-pin 3/8" x 5/8" Flatpak
L	24-pin 1/4" x 1 1/4" Dual-In-Line
M	12-pin TO-101 Can or Header
N	(Note 1)
P	8-pin 1/4" x 3/8" Dual-In-Line
Q	40-pin 3/16" x 2 1/16" Dual-In-Line
R	20-pin 1/4" x 1 1/16" Dual-In-Line
S	20-pin 1/4" x 1/2" Flatpak
T	(Note 1)
U	(Note 1)
V	18-pin 3/8" x 15/16" Dual-In-Line
W	22-pin 3/8" x 1 1/8" Dual-In-Line
X	(Note 1)
Y	(Note 1)
Z	(Note 1)
2	20-terminal 0.350" x 0.350" Chip Carrier
3	28-terminal 0.450" x 0.450" Chip Carrier

Note 1: These letters are assigned to packages by individual MIL-M-38510 detail specifications and may be assigned to different packages in different specifications.

TABLE III. 100% Screening Requirements

	Screen	Class S		Class B	
		Method	Reqmt	Method	Reqmt
1.	Wafer Lot Acceptance	5007	All Lots		
2.	Nondestructive Bond Pull (Note 14)	2023	100%		
3.	Internal Visual (Note 1)	2020, Condition A	100%	2010, Condition B	100%
4.	Stabilization Bake (Note 16)	1008, Condition C, Min 24 Hrs. Min	100%	1008, Condition C, Min 24 Hrs. Min	100%
5.	Temperature Cycling (Note 2)	1010, Condition C	100%	1010, Condition C	100%
6.	Constant Acceleration	2001, Condition E Min Y_1 Orientation Only	100%	2001, Condition E Min Y_1 Orientation Only	100%
7.	Visual Inspection (Note 3)		100%		100%
8.	Particle Impact Noise Detection (PIND)	2010, Condition A (Note 4)	100%		
9.	Serialization	(Note 5)	100%		
10.	Interim (Pre-Burn-In) Electrical Parameters	Per Applicable Device Specification (Note 13)	100%	Per Applicable Device Specification (Note 6)	

TABLE III. 100% Screening Requirements (Continued)

	Screen	Class S		Class B	
		Method	Reqmt	Method	Reqmt
11.	Burn-In Test	1015 240 Hrs. @ 125°C Min (Cond. F Not Allowed)	100%	1015 160 Hrs. @ 125°C Min	100%
12.	Interim (Post Burn-In) Electrical Parameters	Per Applicable Device Specification (Note 3)	100%		
13.	Reverse Bias Burn-In (Note 7)	1015; Test Condition A, C, 72 Hrs. @ 150°C Min (Cond. F Not Allowed)	100%		
14.	Interim (Post-Burn-In) Electrical Parameters	Per Applicable Device Specification (Note 13)	100%	Per Applicable Device Specification	100%
15.	PDA Calculation	5% Parametric (Note 14), 3% Functional	All Lots	5% Parametric (Note 14)	All Lots
16.	Final Electrical Test (Note 15) a) Static Tests 1) 25°C (Subgroup 1, Table I, 5005) 2) Max & Min Rated Operating Temp. (Subgroups 2, 3, Table I, 5005) b) Dynamic Tests or Functional Tests 1) 25°C (Subgroup 4 or 7) 2) Max and Min Rated Operating Temp. (Subgroups 5 and 6 or 8, Table I, 5005) c) Switching Tests 25°C (Subgroup 9, Table I, 5005)	Per Applicable Device Specification	 100% 100% 100% 100% 100%	Per Applicable Device Specification	 100% 100% 100% 100% 100%
17.	Seal Fine, Gross	1014	100% (Note 8)	1014	100% (Note 9)
18.	Radiographic (Note 10)	2012 Two Views	100%		
19.	Qualification or Quality Conformance Inspection Test Sample Selection	(Note 11)	Samp.	(Note 11)	Samp.
20.	External Visual (Note 12)	2009	100%		100%

Note 1: Unless otherwise specified, at the manufacturer's option, test samples for Group B, bond strength (Method 5005) may be randomly selected prior to or following internal visual (Method 5004), prior to sealing provided all other specification requirements are satisfied (e.g., bond strength requirements shall apply to each inspection lot, bond failures shall be counted even if the bond would have failed internal visual).

Note 2: For Class B devices, this test may be replaced with thermal shock Method 1011, Test Condition A, minimum.

Note 3: At the manufacturer's option, visual inspection for catastrophic failures may be conducted after each of the thermal/mechanical screens, after the sequence or after seal test. Catastrophic failures are defined as missing leads, broken packages, or lids off.

Note 4: The PIND test may be performed in any sequence after step 6 and prior to step 16. See MIL-M-38510, paragraph 4.6.3.

Note 5: Class S devices shall be serialized prior to interim electrical parameter measurements.

Note 6: When specified, all devices shall be tested for those parameters requiring delta calculations.

Note 7: Reverse bias burn-in is a requirement only when specified in the applicable device specification. The order of performing burn-in and reverse bias burn-in may be inverted.

Note 8: For Class S devices, the seal test may be performed in any sequence between step 16 and step 19, but it shall be performed after all shearing and forming operations on the terminals.

Note 9: For Class B devices, the fine and gross seal tests shall be performed separately or together in any sequence and order between step 6 and step 20 except that they shall be performed after all shearing and forming operations on the terminals. When 100% seal screen cannot be performed after shearing and forming (e.g., flatpaks and chip carriers) the seal screen shall be done 100% prior to these operations and a sample test (LTPD = 5) shall be performed on each inspection lot following these operations. If the sample fails, 100% rescreening shall be required.

Note 10: The radiographic screen may be performed in any sequence after step 9.

Note 11: Samples shall be selected for testing in accordance with the specific device class and lot requirements of Method 5005.

Note 12: External Visual shall be performed on the lot any time after step 19 and prior to shipment.

Note 13: Read and record is required at steps 10 and 12 only for those parameters for which post-burn-in delta measurements are specified. All parameters shall be read and recorded at step 14.

Note 14: The PDA shall apply to all subgroup 1 parameters at 25°C and all delta parameters.

Note 15: Only one view is required for flat packages and leadless chip carriers with leads on all four sides.

Note 16: May be performed at any time prior to step 10.

Military Analog Products Available from National Semiconductor

Device	Package Styles (Note 1)	Description	Process Flows (Note 2)	SMD/JAN (Note 3)
HIGH PERFORMANCE AMPLIFIERS AND BUFFERS				
LF147	D, J	Wide BW Quad JFET Op Amp	SMD/JAN	/11906
LF155	J, W, H	JFET Input Op Amp	883/JAN	/11401
LF155A	H	JFET Input Op Amp	883	—
LF156	J, W, H	JFET Input Op Amp	883/JAN	/11402
LF156A	H	JFET Input Op Amp	883	—
LF157	H	JFET Input Op Amp	883	—
LF157A	H	JFET Input Op Amp	883	—
LF411M	H, J	Low Offset, Low Drift JFET Input	883/JAN	/11904
LF412M	H, J	Low Offset, Low Drift JFET Input-Dual	883/JAN	/11905
LF441M	H	Low Power JFET Input	883	—
LF442M	H	Low Power JFET Input-Dual	883	—
LF444M	D	Low Power JFET Input-Quad	883	—
LH0002	H	Buffer Amp	883/MIL	7801301
LH0021	K	1.0 Amp Power Op Amp	883/SMD	85088
LH0024	H	High Slew Rate Op Amp	"-MIL"	—
LH0032	G	Ultra Fast FET-Input Op Amp	883/SMD	80013
LH0041	G	0.2 Amp Power Op Amp	883/SMD	85087
LH0061	K	0.5 Amp Wide Bandwidth Op Amp	"-MIL"	—
LH0101	K	Power Op Amp	883/SMD	85089
LH4118	G	Low Gain Wide Band RF Amp	"-MIL"	—
LH4161	H	Trimmed LM6161 VIP Amp	"-MIL"	—
LH4162	H	Dual LH4161	"-MIL"	—
LM10	H	Super-Block™ Micropower Op Amp/Ref	883/SMD	5962-87604
LM101A	J, H, W	General Purpose Op Amp	883/JAN	/10103
LM108A	J, H, W	Precision Op Amp	883/JAN	/10104
LM118	J, H, W	Fast Op Amp	883/JAN	/10107
LM124	J, E, W	Low Power Quad Op Amp	883/JAN	/11005
LM124A	J, W	Low Power Quad	883/JAN	/11006
LM146	J	Quad Programmable Op Amp	883	—
LM148	J, E, W	Quad 741 Op amp	883/JAN	/11001
LM158A	J, H	Low Power Dual Op Amp	883/SMD	5962-8771002
LM158	J, H	Low Power Dual Op Amp	883/SMD	5962-8771001
LM604AM	J	Super-Block 4 Channel Mux Amp	883/SMD	5962-89639
LM611AM	J	Super-Block Op Amp/Reference	883/SMD	TBD
LM613AM	J, E	Super-Block Dual Op Amp/Dual Comp/Ref	883/SMD	TBD
LM614AM	J	Super-Block Quad Op Amp/Ref	883/SMD	TBD
LM709A	H, J, W	General Purpose Op Amp	883/SMD	7800701
LM741	J, H, W	General Purpose Op Amp	883/JAN	/10101
LM747	J, H, W	General Purpose Dual Op Amp	883/JAN	/10102
LM6118	J, E	VIP Dual Op Amp	883/SMD	5962-91565
LM6121	H	VIP Buffer	883/SMD	5962-90812
LM6125	H	VIP Buffer with Error Flag	883/SMD	5962-90815
LM6161	J, E, W	VIP Op Amp (Unity Gain)	883/SMD	5962-89621
LM6164	J, E, W	VIP Op Amp ($A_V > 5$)	883/SMD	5962-89624
LM6165	J, E, W	VIP Op Amp ($A_V > 25$)	883/SMD	5962-89625
LM6162	J, E, W	VIP Op Amp ($A_V > 2, -1$)	883/SMD	5962-92165
LMC660AM	J	Low Power CMOS Quad Op Amp	883/SMD	TBD
LMC662AM	J	Low Power CMOS Dual Op Amp	883/SMD	TBD
LPC660AM	J	Micropower CMOS Quad Op Amp	883/SMD	TBD
LPC662AM	J	Micropower CMOS Dual Op Amp	883/SMD	TBD
OP07	H	Precision Op Amp	SMD/JAN	/13502

Military Analog Products Available from National Semiconductor (Continued)

Device	Package Styles (Note 1)	Description	Process Flows (Note 2)	SMD/JAN (Note 3)
COMPARATORS				
LF111	H	Voltage Comparator	"-MIL"	—
LH2111	J, W	Dual Voltage Comparator	883/JAN	/10305
LM106	H, W	Voltage Comparator	883/SMD	8003701
LM111	J, H, E, W	Voltage Comparator	883/JAN	/10304
LM119	J, H, E, W	High Speed Dual Comparator	883/JAN	/10306
LM139	J, E, W	Quad Comparator	883/JAN	/11201
LM139A	J	Precision Quad Comparator	883/SMD	5962-87739
LM160	J, H	High Speed Differential Comparator	883/SMD	8767401
LM161	J, H	High Speed Differential Comparator	883/SMD	5962-87572
LM193A	J, H	Dual Comparator	883/JAN	/11202
LM612AM	J	Dual-Channel Comparator/Reference	883/SMD	TBD
LM613AM	J, E	Super-Block Dual Comparator/ Dual Op Amp/Adj Reference	883/SMD	TBD
LM615AM	J	Quad Comparator/Adjustable Reference	883/SMD	TBD
LM710A*	J, H, W	Voltage Comparator	883/JAN	/10301
LM711A*	J, H, W	Dual LM710	883/JAN	/10302
LM760	J, H	High Speed Differential Comparator	883/JAN	5962-87545
LINEAR REGULATORS				
Positive Voltage Regulators				
LH0075	G	Precision Voltage Regulator	"-MIL"	—
LM105	H	Adjustable Voltage Regulator	883/SMD	5962-89588
LM109	H	5V Regulator, I_O = 20 mA	883/JAN	/10701BXA
LM109	K	5V Regulator, I_O = 1A	883/JAN	/10701BYA
LM117	H, E, K	Adjustable Regulator	883/JAN	/11703, /11704
LM117A	H	Precision Adjustable Regulator, I_O = 0.5A	883/SMD	7703405XA
LM117A	K	Precision Adjustable Regulator, I_O = 1.5A	883/SMD	7703405YA
LM117HV	H	Adjustable Regulator, I_O = 0.5A	883/SMD	7703402XA
LM117HV	K	Adjustable Regulator, I_O = 1.5A	883/SMD	7703402YA
LM123	K	3A Voltage Regulator	883	—
LM138	K	5A Adjustable Regulator	"-MIL"	—
LM140H-5.0	H	0.5A Fixed 5V Regulator	883/JAN	/10702
LM140H-6.0	H	0.5A Fixed 6V Regulator	883	—
LM140H-8.0	H	0.5A Fixed 8V Regulator	883	—
LM140H-12	H	0.5A Fixed 12V Regulator	883/JAN	/10703
LM140H-15	H	0.5A Fixed 15V Regulator	883/JAN	/10704
LM140H-24	H	0.5A Fixed 24V Regulator	883	—
LM140AK-5.0	K	1.0A Fixed 5V Regulator	883	—
LM140AK-12	K	1.0A Fixed 12V Regulator	883	—
LM140AK-15	K	1.0A Fixed 15V Regulator	883	—
LM140K-5.0	K	1.0A Fixed 5V Regulator	883/JAN	/10706
LM140K-12	K	1.0A Fixed 12V Regulator	883/JAN	/10707
LM140K-15	K	1.0A Fixed 15V Regulator	883/JAN	/10708
LM140K-24	K	1.2A Fixed 24V Regulator	883/JAN	/10709
LM140LAH-5.0	H	100 mA Fixed 5V Regulator	883	—
LM140LAH-12	H	100 mA Fixed 12V Regulator	883	—
LM140LAH-15	H	100 mA Fixed 15V Regulator	883	—
LM150	K	3A Adjustable Power Regulator	883	—
LM2940K-5.0	K	5V Low Dropout Regulator	883/SMD	5962-89587
LM2940K-8.0	K	8V Low Dropout Regulator	883/SMD	5962-90883
LM2940K-12	K	12V Low Dropout Regulator	883/SMD	5962-90884
LM2940K-15	K	15V Low Dropout Regulator	883/SMD	5962-90885
LM2941K	K	Adjustable Low Dropout Regulator	883/SMD	TBD
LM723	H, J, E	Precision Adjustable Regulator	883/JAN	/10201
LM78MG	H	Adjustable Regulator	883	—
LP2951	H, E, J	Adjustable Micropower LDO	883/SMD	5962-38705
LP2953AM	J	250 mA Adj. Micropower LDO	883	—

*Formerly manufactured by Fairchild Semiconductor as part numbers μA710 and μA711.

Military Analog Products Available from National Semiconductor (Continued)

Device	Package Styles (Note 1)	Description	Process Flows (Note 2)	SMD/JAN (Note 3)
LINEAR REGULATORS (Continued)				
Negative Voltage Regulators				
LH0076	G	Precision Programmable Regulator	"-MIL"	—
LM104	H	Precision Negative Regulator	883/SMD	5962-87605
LM120H-5.0	H	Fixed 0.5A Regulator, $V_{OUT} = -5V$	883/JAN	/11501
LM120H-8.0	H	Fixed 0.5A Regulator, $V_{OUT} = -8V$	883	—
LM120H-12	H	Fixed 0.5A Regulator, $V_{OUT} = -12V$	883/JAN	/11502
LM120H-15	H	Fixed 0.5A Regulator, $V_{OUT} = -15V$	883/JAN	/11503
LM120K-5.0	K	Fixed 1.0A Regulator, $V_{OUT} = -5V$	883/JAN	/11505
LM120K-12	K	Fixed 1.0A Regulator, $V_{OUT} = -12V$	883/JAN	/11506
LM120K-15	K	Fixed 1.0A Regulator, $V_{OUT} = -15V$	883/JAN	/11507
LM137A	H	Precision Adjustable Regulator	883/SMD	7703406XA
LM137A	K	Precision Adjustable Regulator	883/SMD	7703406YA
LM137	H, K	Adjustable Regulator	883/JAN	/11803, /11804
LM137HV	H	Adjustable (High Voltage) Regulator	883/SMD	7703404XA
LM137HV	K	Adjustable (High Voltage) Regulator	883/SMD	7703404YA
LM145K-5.0	K	Negative 3 Amp Regulator	883/SMD	5962-90645
LM145K-5.2	K	Negative 3 Amp Regulator	883	—
LM79MG	H	Adjustable Regulator	883	—
SWITCHING REGULATORS				
LM1575-5	K	Simple Switcher™ Step-Down, $V_{OUT} = 5V$	883/SMD	TBD
LM1575-12	K	Simple Switcher Step-Down, $V_{OUT} = 12V$	883/SMD	TBD
LM1575-15	K	Simple Switcher Step-Down, $V_{OUT} = 15V$	883/SMD	TBD
LM1575-ADJ	K	Simple Switcher Step-Down, Adj V_{OUT}	883/SMD	TBD
LM1575HV-5	K	Simple Switcher Step-Down, $V_{OUT} = 5V$	883/SMD	TBD
LM1575HV-12	K	Simple Switcher Step-Down, $V_{OUT} = 12V$	883/SMD	TBD
LM1575HV-15	K	Simple Switcher Step-Down, $V_{OUT} = 15V$	883/SMD	TBD
LM1575HV-ADJ	K	Simple Switcher Step-Down, Adj V_{OUT}	883/SMD	TBD
LM1577-12	K	Simple Switcher Step-Up, $V_{OUT} = 12V$	883/SMD	TBD
LM1577-15	K	Simple Switcher Step-Up, $V_{OUT} = 15V$	883/SMD	TBD
LM1577-ADJ	K	Simple Switcher Step-Up, Adj V_{OUT}	883/SMD	TBD
LM1578	H	750 mA Switching Regulator	883/SMD	5962-89586
LM78S40*	J	Universal Switching Regulator Subsystem	883/SMD	5962-88761

*Formerly manufactured by Fairchild Semiconductor as the μA78S40DMQB.

VOLTAGE REFERENCES				
LM103-3.0	H	Reference Diode, BV = 3.0V	883/SMD	7702806
LM103-3.3	H	Reference Diode, BV = 3.3V	883/SMD	7702807
LM103-3.6	H	Reference Diode, BV = 3.6V	883/SMD	7702808
LM103-3.9	H	Reference Diode, BV = 3.9V	883/SMD	7702809
LM113	H	Reference Diode with 5% Tolerance	883/SMD	5962-8671101
LM113-1	H	Reference Diode with 1% Tolerance	883/SMD	5962-8671102
LM113-2	H	Reference Diode with 2% Tolerance	883/SMD	5962-8671103
LM129A	H	Precision Reference, 10 ppm/°C Drift	883/SMD	5962-8992101XA
LM129B	H	Precision Reference, 20 ppm/°C Drift	883/SMD	5962-8992102XA
LM136A-2.5	H	2.5V Reference Diode, 1% V_{OUT} Tolerance	883	—
LM136A-5.0	H	5V Reference Diode, 1% V_{OUT} Tolerance	883/SMD	8418001
LM136-2.5	H	2.5V Reference Diode, 2% V_{OUT} Tolerance	883	—
LM136-5.0	H	5V Reference Diode, 2% V_{OUT} Tolerance	883	—

Military Analog Products Available from National Semiconductor (Continued)

Device	Package Styles (Note 1)	Description	Process Flows (Note 2)	SMD/JAN (Note 3)
VOLTAGE REFERENCES (Continued)				
LM169	H	10V Precision Reference, Low Tempco 0.05% Tolerance	883/SMD	TBD
LM185	H, E	Adjustable Micropower Voltage Reference	883	—
LM185BXH2.5	H	2.5V Micropower Reference Diode, Ultralow Drift	883/SMD	5962-8759404
LM185BY	H	Adjustable Micropower Voltage Reference	883	—
LM185BYH1.2	H	1.2V Micropower Reference Diode, Low Drift	883/SMD	5962-8759405
LM185BYH2.5	H	2.5V Micropower Reference Diode, Low Drift	883/SMD	5962-8759406
LM185-1.2	H, E	1.2V Micropower Reference Diode, Low Drift	883/SMD	5962-8759401
LM185-2.5	H, E	2.5V Micropower Reference Diode, Low Drift	883/SMD	5962-8759402
LM199	H	Precision Reference, Low Tempco	883/SMD	5962-8856102
LM199A	H	Precision Reference, Ultralow Tempco	883/SMD	5962-8856101
LM199A-20	H	Precision Reference, Ultralow Tempco	883	—
LM611AM	J	Super-Block Op Amp/Reference	883/SMD	TBD
LM612AM	J	Super-Block Dual-Channel Comparator/Reference	883/SMD	TBD
LM613AM	J, E	Super-Block Dual Op Amp/DualComp/Dual Ref	883/SMD	TBD
LM614AM	J	Super-Block Quad Op Amp/Reference	883/SMD	TBD
LM615AM	J	Super-Block Quad Comparator/Reference	883/SMD	TBD
LH0070-0	H	Precision BCD Buffered Reference	"-MIL"	—
LH0070-1	H	Precision BCD Buffered Reference	"-MIL"	—
LH0070-2	H	Precision BCD Buffered Reference	"-MIL"	—
DATA ACQUISITION				
ADC08020L	J	8-Bit μP-Compatible	883/SMD	5962-90966
ADC0851	J	8-Bit Analog Data Acquisition & Monitoring System	883/SMD	TBD
ADC0858	J	8-Bit Analog Data Acquisition & Monitoring System	883/SMD	TBD
ADC1241CM	J	12-Bit Plus Sign Self-Calibrating with Sample/Hold Function	883/SMD	TBD
ADC12441CM	J	Dynamically-Tested ADC1241	883/SMD	TBD
ADC1251CM	J	12-Bit Plus Sign Self-Calibrating with Sample/Hold Function	883/SMD	TBD
ADC12451CM	J	Dynamically-Tested ADC1251	883/SMD	TBD
ADC10061CM	J	10-Bit Multistep ADC	883/SMD	TBD
ADC10062CM	J	10-Bit Multistep ADC w/Dual Input Multiplexer	883/SMD	TBD
ADC10064CM	J	10-Bit Multistep ADC w/Quad Input Multiplexer	883/SMD	TBD
ADC08061CM	J	8-Bit Multistep ADC	883/SMD	TBD
ADC08062CM	J	8-Bit Multistep ADC w/Dual Input Multiplexer	883/SMD	TBD
ADC08064CM	J	8-Bit Multistep ADC w/Quad Input Multiplexer	883/SMD	TBD
ADC08068CM	J	8-Bit Multistep ADC w/Octal Input Multiplexer	883/SMD	TBD

Military Analog Products Available from National Semiconductor (Continued)

Device	Package Styles (Note 1)	Description	Process Flows (Note 2)	SMD/JAN (Note 3)
DATA ACQUISITION SUPPORT				
Switched Capacitor Filters				
LMF60CMJ50	J	6th Order Butterworth Lowpass	883/SMD	5962-90967
LMF60CMJ100	J	6th Order Butterworth Lowpass	883/SMD	5962-90967
LMF90CM	J	4th Order Elliptic Notch	883/SMD	5962-90968
LMF100A	J, E	Dual 2nd Order General Purpose	883/SMD	TBD
Sample and Hold				
LF198	H	Monolithic Sample and Hold	SMD/JA	5962-87608 /12501

Note 1: D: Side-Brazed DIP
E: Leadless Ceramic Chip Carrier
G: Metal Can (TO-8)
H: Metal Can (TO-39, TO-5, TO-99, TO-100)
J: Ceramic DIP
K: Metal Can (TO-3)
W: Flatpak

Note 2: Process Flows
JAN = JM38510, Level B
SMD = Standard Military Drawing
883 = MIL-STD-883 Rev C
-MIL = Exceptions to 883C noted on Certificate of Conformance

Note 3: Please call your local sales office to determine price and availability of space-level products. All "LM" prefix products in this guide are availble with space-level processing.

National Semiconductor

Appendix E
Understanding Integrated Circuit Package Power Capabilities

INTRODUCTION

The short and long term reliability of National Semiconductor's interface circuits, like any integrated circuit, is very dependent on its environmental condition. Beyond the mechanical/environmental factors, nothing has a greater influence on this reliability than the electrical and thermal stress seen by the integrated circuit. Both of these stress issues are specifically addressed on every interface circuit data sheet, under the headings of Absolute Maximum Ratings and Recommended Operating Conditions.

However, through application calls, it has become clear that electrical stress conditions are generally more understood than the thermal stress conditions. Understanding the importance of electrical stress should never be reduced, but clearly, a higher focus and understanding must be placed on thermal stress. Thermal stress and its application to interface circuits from National Semiconductor is the subject of this application note.

FACTORS AFFECTING DEVICE RELIABILITY

Figure 1 shows the well known "bathtub" curve plotting failure rate versus time. Similar to all system hardware (mechanical or electrical) the reliability of interface integrated circuits conform to this curve. The key issues associated with this curve are infant mortality, failure rate, and useful life.

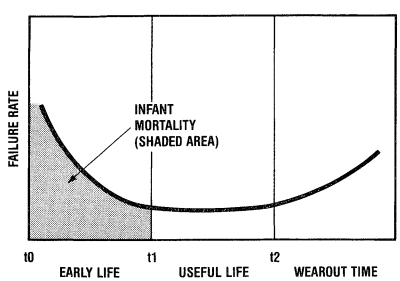


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FIGURE 1. Failure Rate vs Time

Infant mortality, the high failure rate from time t0 to t1 (early life), is greatly influenced by system stress conditions other than temperature, and can vary widely from one application to another. The main stress factors that contribute to infant mortality are electrical transients and noise, mechanical maltreatment and excessive temperatures. Most of these failures are discovered in device test, burn-in, card assembly and handling, and initial system test and operation. Although important, much literature is available on the subject of infant mortality in integrated circuits and is beyond the scope of this application note.

Failure rate is the number of devices that will be expected to fail in a given period of time (such as, per million hours). The mean time between failure (MTBF) is the average time (in hours) that will be expected to elapse after a unit has failed before the next unit failure will occur. These two primary "units of measure" for device reliability are inversely related:

$$\text{MTBF} = \frac{1}{\text{Failure Rate}}$$

Although the "bathtub" curve plots the overall failure rate versus time, the useful failure rate can be defined as the percentage of devices that fail per-unit-time during the flat portion of the curve. This area, called the useful life, extends between t1 and t2 or from the end of infant mortality to the onset of wearout. The useful life may be as short as several years but usually extends for decades if adequate design margins are used in the development of a system.

Many factors influence useful life including: pressure, mechanical stress, thermal cycling, and electrical stress. However, die temperature during the device's useful life plays an equally important role in triggering the onset of wearout.

FAILURE RATES vs TIME AND TEMPERATURE

The relationship between integrated circuit failure rates and time and temperature is a well established fact. The occurrence of these failures is a function which can be represented by the Arrhenius Model. Well validated and predominantly used for accelerated life testing of integrated circuits, the Arrhenius Model assumes the degradation of a performance parameter is linear with time and that MTBF is a function of temperature stress. The temperature dependence is an exponential function that defines the probability of occurrence. This results in a formula for expressing the lifetime or MTBF at a given temperature stress in relation to another MTBF at a different temperature. The ratio of these two MTBFs is called the acceleration factor F and is defined by the following equation:

$$F = \frac{X1}{X2} = \exp\left[\frac{E}{K}\left(\frac{1}{T2} - \frac{1}{T1}\right)\right]$$

Where: X1 = Failure rate at junction temperature T1
X2 = Failure rate at junction temperature T2
T = Junction temperature in degrees Kelvin
E = Thermal activation energy in electron volts (ev)
K = Boltzman's constant

However, the dramatic acceleration effect of junction temperature (chip temperature) on failure rate is illustrated in a plot of the above equation for three different activation energies in *Figure 2*. This graph clearly demonstrates the importance of the relationship of junction temperature to device failure rate. For example, using the 0.99 ev line, a 30° rise in junction temperature, say from 130°C to 160°C, results in a 10 to 1 increase in failure rate.

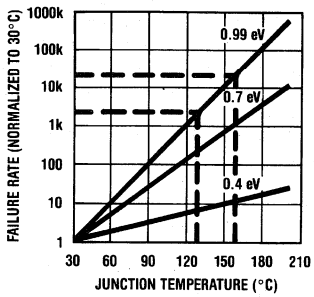

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FIGURE 2. Failure Rate as a Function of Junction Temperature

DEVICE THERMAL CAPABILITIES

There are many factors which affect the thermal capability of an integrated circuit. To understand these we need to understand the predominant paths for heat to transfer out of the integrated circuit package. This is illustrated by *Figures 3* and *4*.

Figure 3 shows a cross-sectional view of an assembled integrated circuit mounted into a printed circuit board.

Figure 4 is a flow chart showing how the heat generated at the power source, the junctions of the integrated circuit flows from the chip to the ultimate heat sink, the ambient environment. There are two predominant paths. The first is from the die to the die attach pad to the surrounding package material to the package lead frame to the printed circuit board and then to the ambient. The second path is from the package directly to the ambient air.

Improving the thermal characteristics of any stage in the flow chart of *Figure 4* will result in an improvement in device thermal characteristics. However, grouping all these characteristics into one equation determining the overall thermal capability of an integrated circuit/package/environmental condition is possible. The equation that expresses this relationship is:

$$T_J = T_A + P_D (\theta_{JA})$$

Where: T_J = Die junction temperature

T_A = Ambient temperature in the vicinity device

P_D = Total power dissipation (in watts)

θ_{JA} = Thermal resistance junction-to-ambient

θ_{JA}, the thermal resistance from device junction-to-ambient temperature, is measured and specified by the manufacturers of integrated circuits. National Semiconductor utilizes special vehicles and methods to measure and monitor this parameter. All circuit data sheets specify the thermal characteristics and capabilities of the packages available for a given device under specific conditions—these package power ratings directly relate to thermal resistance junction-to-ambient or θ_{JA}.

Although National provides these thermal ratings, it is critical that the end user understand how to use these numbers to improve thermal characteristics in the development of his system using IC components.

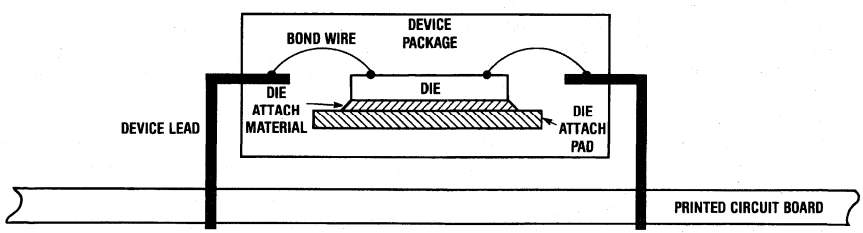

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FIGURE 3. Integrated Circuit Soldered into a Printed Circuit Board (Cross-Sectional View)

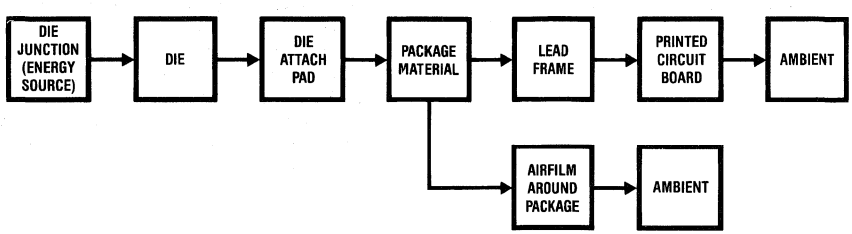

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FIGURE 4. Thermal Flow (Predominant Paths)

DETERMINING DEVICE OPERATING JUNCTION TEMPERATURE

From the above equation the method of determining actual worst-case device operating junction temperature becomes straightforward. Given a package thermal characteristic, θ_{JA}, worst-case ambient operating temperature, T_A(max), the only unknown parameter is device power dissipation, P_D. In calculating this parameter, the dissipation of the integrated circuit due to its own supply has to be considered, the dissipation within the package due to the external load must also be added. The power associated with the load in a dynamic (switching) situation must also be considered. For example, the power associated with an inductor or a capacitor in a static versus dynamic (say, 1 MHz) condition is significantly different.

The junction temperature of a device with a total package power of 600 mW at 70°C in a package with a thermal resistance of 63°C/W is 108°C.

$$T_J = 70°C + (63°C/W) \times (0.6W) = 108°C$$

The next obvious question is, "how safe is 108°C?"

MAXIMUM ALLOWABLE JUNCTION TEMPERATURES

What is an acceptable maximum operating junction temperature is in itself somewhat of a difficult question to answer. Many companies have established their own standards based on corporate policy. However, the semiconductor industry has developed some defacto standards based on the device package type. These have been well accepted as numbers that relate to reasonable (acceptable) device lifetimes, thus failure rates.

National Semiconductor has adopted these industry-wide standards. For devices fabricated in a molded package, the maximum allowable junction temperature is 150°C. For these devices assembled in ceramic or cavity DIP packages, the maximum allowable junction temperature is 175°C. The numbers are different because of the differences in package types. The thermal strain associated with the die package interface in a cavity package is much less than that exhibited in a molded package where the integrated circuit chip is in direct contact with the package material.

Let us use this new information and our thermal equation to construct a graph which displays the safe thermal (power) operating area for a given package type. *Figure 5* is an example of such a graph. The end points of this graph are easily determined. For a 16-pin molded package, the maximum allowable temperature is 150°C; at this point no power dissipation is allowable. The power capability at 25°C is 1.98W as given by the following calculation:

$$P_D @ 25°C = \frac{T_J(max) - T_A}{\theta_{JA}} = \frac{150°C - 25°C}{63°C/W} = 1.98W$$

The slope of the straight line between these two points is minus the inversion of the thermal resistance. This is referred to as the derating factor.

$$\text{Derating Factor} = -\frac{1}{\theta_{JA}}$$

As mentioned, *Figure 5* is a plot of the safe thermal operating area for a device in a 16-pin molded DIP. As long as the intersection of a vertical line defining the maximum ambient temperature (70°C in our previous example) and maximum device package power (600 mW) remains below the maximum package thermal capability line the junction temperature will remain below 150°C—the limit for a molded package. If the intersection of ambient temperature and package power fails on this line, the maximum junction temperature will be 150°C. Any intersection that occurs above this line will result in a junction temperature in excess of 150°C and is not an appropriate operating condition.

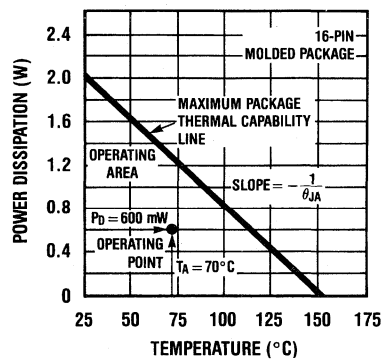

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FIGURE 5. Package Power Capability vs Temperature

The thermal capabilities of all integrated circuits are expressed as a power capability at 25°C still air environment with a given derating factor. This simply states, for every degree of ambient temperature rise above 25°C, reduce the package power capability stated by the derating factor which is expressed in mW/°C. For our example—a θ_{JA} of 63°C/W relates to a derating factor of 15.9 mW/°C.

FACTORS INFLUENCING PACKAGE THERMAL RESISTANCE

As discussed earlier, improving any portion of the two primary thermal flow paths will result in an improvement in overall thermal resistance junction-to-ambient. This section discusses those components of thermal resistance that can be influenced by the manufacturer of the integrated circuit. It also discusses those factors in the overall thermal resistance that can be impacted by the end user of the integrated circuit. Understanding these issues will go a long way in understanding chip power capabilities and what can be done to insure the best possible operating conditions and, thus, best overall reliability.

Die Size

Figure 6 shows a graph of our 16-pin DIP thermal resistance as a function of integrated circuit die size. Clearly, as the chip size increases the thermal resistance decreases—this relates directly to having a larger area with which to dissipate a given power.

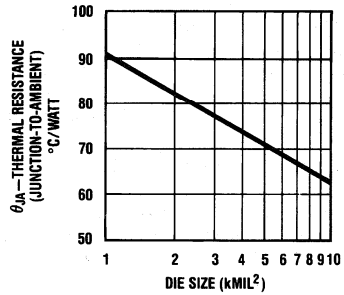

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FIGURE 6. Thermal Resistance vs Die Size

Lead Frame Material

Figure 7 shows the influence of lead frame material (both die attach and device pins) on thermal resistance. This graph compares our same 16-pin DIP with a copper lead frame, a Kovar lead frame, and finally an Alloy 42 type lead frame—these are lead frame materials commonly used in the industry. Obviously the thermal conductivity of the lead frame material has a significant impact in package power capability. Molded interface circuits from National Semiconductor use the copper lead frame exclusively.

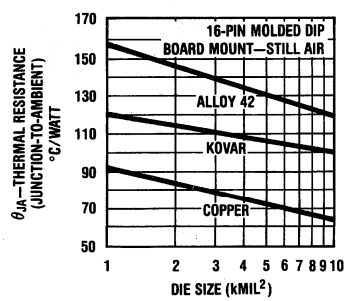

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FIGURE 7. Thermal Resistance vs Lead Frame Material

Board vs Socket Mount

One of the major paths of dissipating energy generated by the integrated circuit is through the device leads. As a result of this, the graph of *Figure 8* comes as no surprise. This compares the thermal resistance of our 16-pin package soldered into a printed circuit board (board mount) compared to the same package placed in a socket (socket mount). Adding a socket in the path between the PC board and the device adds another stage in the thermal flow path, thus increasing the overall thermal resistance. The thermal capabilities of National Semiconductor's interface circuits are specified assuming board mount conditions. If the devices are placed in a socket the thermal capabilities should be reduced by approximately 5% to 10%.

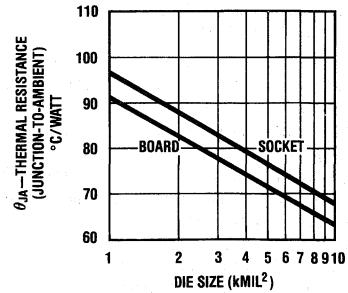

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FIGURE 8. Thermal Resistance vs Board or Socket Mount

Air Flow

When a high power situation exists and the ambient temperature cannot be reduced, the next best thing is to provide air flow in the vicinity of the package. The graph of *Figure 9* illustrates the impact this has on thermal resistance. This graph plots the relative reduction in thermal resistance normalized to the still air condition for our 16-pin molded DIP. The thermal ratings on National Semiconductor's interface circuits data sheets relate to the still air environment.

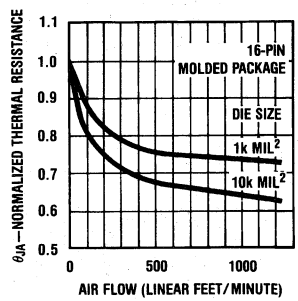

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FIGURE 9. Thermal Resistance vs Air Flow

Other Factors

A number of other factors influence thermal resistance. The most important of these is using thermal epoxy in mounting ICs to the PC board and heat sinks. Generally these techniques are required only in the very highest of power applications.

Some confusion exists between the difference in thermal resistance junction-to-ambient (θ_{JA}) and thermal resistance junction-to-case (θ_{JC}). The best measure of actual junction temperature is the junction-to-ambient number since nearly all systems operate in an open air environment. The only situation where thermal resistance junction-to-case is important is when the entire system is immersed in a thermal bath and the environmental temperature is indeed the case temperature. This is only used in extreme cases and is the exception to the rule and, for this reason, is not addressed in this application note.

NATIONAL SEMICONDUCTOR PACKAGE CAPABILITIES

Figures 10 and *11* show composite plots of the thermal characteristics of the most common package types in the National Semiconductor Linear Circuits product family. *Figure 10* is a composite of the copper lead frame molded package. *Figure 11* is a composite of the ceramic (cavity) DIP using poly die attach. These graphs represent board mount still air thermal capabilities. Another, and final, thermal resistance trend will be noticed in these graphs. As the number of device pins increase in a DIP the thermal resistance decreases. Referring back to the thermal flow chart, this trend should, by now, be obvious.

RATINGS ON INTERFACE CIRCUITS DATA SHEETS

In conclusion, all National Semiconductor Linear Products define power dissipation (thermal) capability. This information can be found in the Absolute Maximum Ratings section of the data sheet. The thermal information shown in this application note represents average data for characterization of the indicated package. Actual thermal resistance can vary from ±10% to ±15% due to fluctuations in assembly quality, die shape, die thickness, distribution of heat sources on the die, etc. The numbers quoted in the linear data sheets reflect a 15% safety margin from the average numbers found in this application note. Insuring that total package power remains under a specified level will guarantee that the maximum junction temperature will not exceed the package maximum.

The package power ratings are specified as a maximum power at 25°C ambient with an associated derating factor for ambient temperatures above 25°C. It is easy to determine the power capability at an elevated temperature. The power specified at 25°C should be reduced by the derating factor for every degree of ambient temperature above 25°C. For example, in a given product data sheet the following will be found:

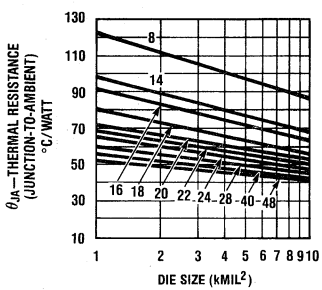
Maximum Power Dissipation* at 25°C
Cavity Package 1509 mW
Molded Package 1476 mW

* Derate cavity package at 10 mW/°C above 25°C; derate molded package at 11.8 mW/°C above 25°C.

If the molded package is used at a maximum ambient temperature of 70°C, the package power capability is 945 mW.

$$P_D @ 70°C = 1476\ mW - (11.8\ mW/°C) \times (70°C - 25°C)$$
$$= 945\ mW$$

Molded (N Package) DIP*
Copper Leadframe—HTP
Die Attach Board Mount—
Still Air



*Packages from 8- to 20-pin 0.3 mil width
22-pin 0.4 mil width
24- to 40-pin 0.6 mil width

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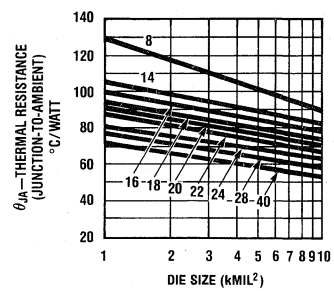
FIGURE 10. Thermal Resistance vs Die Size vs Package Type (Molded Package)

Cavity (J Package) DIP*
Poly Die Attach Board
Mount—Still Air



*Packages from 8- to 20-pin 0.3 mil width
22-pin 0.4 mil width
24- to 48-pin 0.6 mil width

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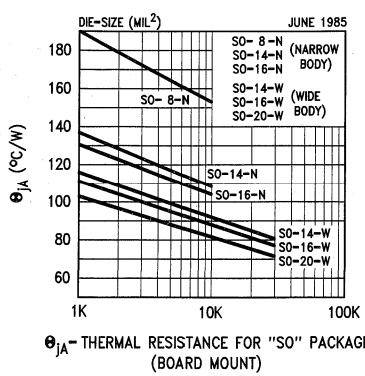
FIGURE 11. Thermal Resistance vs Die Size vs Package Type (Cavity Package)



Θ_{JA} – THERMAL RESISTANCE FOR "SO" PACKAGES (BOARD MOUNT)

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FIGURE 12

National Semiconductor

APPENDIX F
How to Get the Right Information From a Data Sheet

Not All Data Sheets Are Created Alike, and False Assumptions Could Cost an Engineer Time and Money

By Robert A. Pease

When a new product arrives in the marketplace, it hopefully will have a good, clear data sheet with it.

The data sheet can show the prospective user how to apply the device, what performance specifications are guaranteed and various typical applications and characteristics. If the data-sheet writer has done a good job, the user can decide if the product will be valuable to him, exactly how well it will be of use to him and what precautions to take to avoid problems.

SPECIFICATIONS

The most important area of a data sheet specifies the characteristics that are guaranteed—and the test conditions that apply when the tests are done. Ideally, all specifications that the users will need will be spelled out clearly. If the product is similar to existing products, one can expect the data sheet to have a format similar to other devices.

But, if there are significant changes and improvements that nobody has seen before, then the writer must clarify what is meant by each specification. Definitions of new phrases or characteristics may even have to be added as an appendix.

For example, when fast-settling operational amplifiers were first introduced, some manufacturers defined settling time as the time after slewing before the output finally enters and stays within the error-band; but other manufacturers included the slewing time in their definition. Because both groups made their definitions clear, the user was unlikely to be confused or misled.

However, the reader ought to be on the alert. In a few cases, the data-sheet writer is playing a specsmanship game, and is trying to show an inferior (to some users) aspect of a product in a light that makes it look superior (which it may be, to a couple of users).

GUARANTEES

When a data sheet specifies a guaranteed minimum value, what does it mean? An assumption might be made that the manufacturer has actually tested that specification and has great confidence that no part could fail that test and still be shipped. Yet that is not always the case.

For instance, in the early days of op amps (20 years ago), the differential-input impedance might have been guaranteed at 1 MΩ—but the manufacturer obviously did not measure the impedance. When a customer insisted, "I have to know how you measure this impedance," it had to be explained that the impedance was not measured, but that the base current was. The correlation between I_b and Z_{in} permitted the substitution of this simple dc test for a rather messy, noisy, hard-to-interpret test.

Every year, for the last 20 years, manufacturers have been trying to explain, with varying success, why they do not measure the Z_{in} *per se,* even though they do guarantee it.

In other cases, the manufacturer may specify a test that can be made only on the die as it is probed on the wafer, but cannot be tested after the die is packaged because that signal is not accessible any longer. To avoid frustrating and confusing the customer, some manufacturers are establishing two classes of guaranteed specifications:

- The tested limit represents a test that cannot be doubted, one that is actually performed directly on 100 percent of the devices, 100 percent of the time.
- The design limit covers other tests that may be indirect, implicit or simply guaranteed by the inherent design of the device, and is unlikely to cause a failure rate (on that test), even as high as one part per thousand.

Why was this distinction made? Not just because customers wanted to know which specifications were guaranteed by testing, but because the quality-assurance group insisted that it was essential to separate the tested guarantees from the design limits so that the AQL (assurance-quality level) could be improved from 0.1 percent to down below 100 ppm.

Some data sheets guarantee characteristics that are quite expensive and difficult to test (even harder than noise) such as long-term drift (20 ppm or 50 ppm over 1,000 hours).

The data sheet may not tell the reader if it is measured, tested or estimated. One manufacturer may perform a 100-percent test, while another states, "Guaranteed by sample testing." This is not a very comforting assurance that a part is good, especially in a critical case where only a long-term test can prove if the device did meet the manufacturer's specification. If in doubt, question the manufacturer.

TYPICALS

Next to a guaranteed specification, there is likely to be another in a column labeled "typical".

It might mean that the manufacturer once actually saw one part as good as that. It could indicate that half the parts are better than that specification, and half will be worse. But it is equally likely to mean that, five years ago, half the parts were better and half worse. It could easily signify that a few parts might be slightly better, and a few parts a lot worse; after all, if the noise of an amplifier is extremely close to the theoretical limit, one cannot expect to find anything much better than that, but there will always be a few noisy ones.

If the specification of interest happens to be the bias current (I_b) of an op amp, a user can expect broad variations. For example, if the specification is 200 nA maximum, there might be many parts where I_b is 40 nA on one batch (where the beta is high), and a month later, many parts where the I_b is 140 nA when the beta is low.

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Absolute Maximum Ratings (Note 11)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	+35V to −0.2V
Output Voltage	+6V to −1.0V
Output Current	10 mA
Storage Temperature,	
TO-46 Package	−76°F to +356°F
TO-92 Package	−76°F to +300°F
Lead Temp. (Soldering, 4 seconds) *	
TO-46 Package	+300°C
TO-92 Package	+260°C

Specified Operating Temp. Range (Note 2)

	T_{MIN} to T_{MAX}
LM34, LM34A	−50°F to +300°F
LM34C, LM34CA	−40°F to +230°F
LM34D	+32°F to +212°F

DC Electrical Characteristics (Note 1, **Note 6**)

Parameter	Conditions	LM34A			LM34CA			Units (Max)
		Typical	Tested Limit (Note 4)	Design Limit (Note 5)	Typical	Tested Limit (Note 4)	Design Limit (Note 5)	
Accuracy (Note 7)	T_A = +77°F	±0.4	±1.0		±0.4	±1.0		°F
	T_A = 0°F	±0.6			±0.6		±2.0	°F
	T_A = T_{MAX}	±0.8	±2.0		±0.8	±2.0		°F
	T_A = T_{MIN}	±0.8	±2.0		±0.8		±3.0	°F
Nonlinearity (Note 8)	$T_{MIN} \le T_A \le T_{MAX}$	**±0.35**		**±0.7**	**±0.30**		**±0.6**	°F
Sensor Gain (Average Slope)	$T_{MIN} \le T_A \le T_{MAX}$	**+10.0**	**+9.9, +10.1**		**+10.0**		**+9.9, +10.1**	mV/°F, min mV/°F, max
Load Regulation (Note 3)	T_A = +77°F	±0.4	±1.0		±0.4	±1.0		mV/mA
	$T_{MIN} \le T_A \le T_{MAX}$	**±0.5**		**±3.0**	**±0.5**		**±3.0**	mV/mA
	$0 \le I_L \le 1$ mA							
Line Regulation (Note 3)	T_A = +77°F	±0.01	±0.05		±0.01	±0.05		mV/V
	$5V \le V_S \le 30V$	**±0.02**		**±0.1**	**±0.02**		**±0.1**	mV/V
Quiescent Current (Note 9)	V_S = +5V, +77°F	75	90		75	90		µA
	V_S = +5V	**131**		**160**	**116**		**139**	µA
	V_S = +30V, +77°F	76	92		76	92		µA
	V_S = +30V	**132**		**163**	**117**		**142**	µA
Change of Quiescent Current (Note 3)	$4V \le V_S \le 30V$, +77°F	+0.5	2.0		0.5	2.0		µA
	$5V \le V_S \le 30V$	**+1.0**		**3.0**	**1.0**		**3.0**	µA
Temperature Coefficient of Quiescent Current		**+0.30**		**+0.5**	**+0.30**		**+0.5**	µA/°F
Minimum Temperature for Rated Accuracy	In circuit of *Figure 1*, I_L = 0	+3.0		+5.0	+3.0		+5.0	°F
Long-Term Stability	T_j = T_{MAX} for 1000 hours	±0.16			±0.16			°F

Note 1: Unless otherwise noted, these specifications apply: $-50°F \le T_j \le +300°F$ for the LM34 and LM34A; $-40°F \le T_j \le +230°F$ for the LM34C and LM34CA; and $+32°F \le T_j \le +212°F$ for the LM34D. V_S = +5 Vdc and I_{LOAD} = 50 µA in the circuit of *Figure 2;* +6 Vdc for LM34 and LM34A for $230°F \le T_j \le 300°F$. These specifications also apply from +5°F to T_{MAX} in the circuit of *Figure 1.*

Note 2: Thermal resistance of the TO-46 package is 292°F/W junction to ambient and 43°F/W junction to case. Thermal resistance of the TO-92 package is 324°F/W junction to ambient.

Note 3: Regulation is measured at constant junction temperature using pulse testing with a low duty cycle. Changes in output due to heating effects can be computed by multiplying the internal dissipation by the thermal resistance.

Note 4: Tested limits are guaranteed and 100% tested in production.

Note 5: Design limits are guaranteed (but not 100% production tested) over the indicated temperature and supply voltage ranges. These limits are not used to calculate outgoing quality levels.

Note 6: Specification in **BOLDFACE TYPE** apply over the full rated temperature range.

Note 7: Accuracy is defined as the error between the output voltage and 10 mV/°F times the device's case temperature at specified conditions of voltage, current, and temperature (expressed in °F).

Note 8: Nonlinearity is defined as the deviation of the output-voltage-versus-temperature curve from the best-fit straight line over the device's rated temperature range.

Note 9: Quiescent current is defined in the circuit of *Figure 1.*

Note 10: Contact factory for availability of LM34CAZ.

** **Note 11:** Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its rated operating conditions (see Note 1).

A Point-By-Point Look

Let's look a little more closely at the data sheet of the National Semiconductor LM34, which happens to be a temperature sensor.

Note 1 lists the nominal test conditions and test circuits in which all the characteristics are defined. Some additional test conditions are listed in the column "Conditions", but Note 1 helps minimize the clutter.

Note 2 gives the thermal impedance, (which may also be shown in a chart or table).

Note 3 warns that an output impedance test, if done with a long pulse, could cause significant self-heating and thus, error.

Note 6 is intended to show which specs apply at all rated temperatures.

Note 7 is the definition of the "Accuracy" spec, and Note 8 the definition for non-linearity. Note 9 states in what test circuit the quiescent current is defined. Note 10 indicates that one model of the family may not be available at the time of printing (but happens to be available now), and Note 11 is the definition of Absolute Max Ratings.

* Note—the "4 seconds" soldering time is a new standard for plastic packages.

** Note—the wording of Note 11 has been revised—this is the best wording we can devise, and we will use it on all future datasheets.

APPLICATIONS

Another important part of the data sheet is the applications section. It indicates the novel and conventional ways to use a device. Sometimes these applications are just little ideas to tweak a reader's mind. After looking at a couple of applications, one can invent other ideas that are useful. Some applications may be of no real interest or use.

In other cases, an application circuit may be the complete definition of the system's performance; it can be the test circuit in which the specification limits are defined, tested and guaranteed. But, in all other instances, the performance of a typical application circuit is not guaranteed, it is only typical. In many circumstances, the performance may depend on external components and their precision and matching. Some manufacturers have added a phrase to their data sheets:

"Applications for any circuits contained in this document are for illustration purposes only and the manufacturer makes no representation or warranty that such applications will be suitable for the use indicated without further testing or modification."

In the future, manufacturers may find it necessary to add disclaimers of this kind to avoid disappointing users with circuits that work well, much of the time, but cannot be easily guaranteed.

The applications section is also a good place to look for advice on quirks—potential drawbacks or little details that may not be so little when a user wants to know if a device will actually deliver the expected performance.

For example, if a buffer can drive heavy loads and can handle fast signals cleanly (at no load), the maker isn't doing anybody any favors if there is no mention that the distortion goes sky-high if the rated load is applied.

Another example is the application hint for the LF156 family:

"Exceeding the negative common-mode limit on either input will cause a reversal of the phase to output and force the amplifier output to the corresponding high or low state. Exceeding the negative common-mode limit on both inputs will force the amplifier output to a high state. In neither case does a latch occur, since raising the input back within the common-mode range again puts the input stage and, thus the amplifier, in a normal operating mode."

That's the kind of information a manufacturer should really give to a data-sheet reader because no one could ever guess it.

Sometimes, a writer slips a quirk into a characteristic curve, but it's wiser to draw attention to it with a line of text. This is because it's better to make the user sad before one gets started, rather than when one goes into production. Conversely, if a user is going to spend more than 10 minutes using a new product, one ought to spend a full five minutes reading the entire data sheet.

FINE PRINT

What other fine print can be found on a data sheet? Sometimes the front page may be marked "advance" or "preliminary." Then on the back page, the fine print may say something such as:

"This data sheet contains preliminary limits and design specifications. Supplemental information will be published at a later date. The manufacturer reserves the right to make changes in the products contained in this document in order to improve design or performance and to supply the best possible products. We also assume no responsibility for the use of any circuits described herein, convey no license under any patent or other right and make no representation that the circuits are free from patent infringement."

In fact, after a device is released to the marketplace in a preliminary status, the engineers love to make small improvements and upgrades in specifications and characteristics, and hate to degrade a specification from its first published value—but occasionally that is necessary.

Another item in the fine print is the manufacturer's telephone number. Usually it is best to refer questions to the local sales representative or field-applications engineer, because they may know the answer or they may be best able to put a questioner in touch with the right person at the factory.

Occasionally, the factory's applications engineers have all the information. Other times, they have to bring in product engineers, test engineers or marketing people. And sometimes the answer can't be generated quickly—data have to be gathered, opinions solidified or policies formulated before the manufacturer can answer the question. Still, the telephone number is the key to getting the factory to help.

ORIGINS OF DATA SHEETS

Of course, historically, most data sheets for a class of products have been closely modeled on the data sheet of the forerunner of that class. The first data sheet was copied to make new versions.

That's the way it happened with the UA709 (the first monolithic op amp) and all its copies, as well as many other similar families of circuits.

Even today, an attempt is made to build on the good things learned from the past and add a few improvements when necessary. But, it's important to have real improvements, not just change for the sake of change.

So, while it's not easy to get the format and everything in it exactly right to please everybody, new data sheets are continually surfacing with new features, applications ideas, specifications and aids for the user. And, if the users complain loudly enough about misleading or inadequate data sheets, they can help lead the way to change data sheets. That's how many of today's improvements came about—through customer demand.

Who writes data sheets? In some cases, a marketing person does the actual writing and engineers do the checking. In other companies, the engineer writes, while marketing people and other engineers check. Sometimes, a committee seems to be doing the writing. None of these ways is necessarily wrong.

For example, one approach might be: The original designer of the product writes the data sheet (inside his head) at the same time the product is designed. The concept here is, if one can't find the proper ingredients for a data sheet—good applications, convenient features for the user and nicely tested specifications as the part is being designed—then maybe it's not a very good product until all those ingredients are completed. Thus, the collection of raw materials for a good data sheet is an integral part of the design of a product. The actual assembly of these materials is an art which can take place later.

WHEN TO WRITE DATA SHEETS

A new product becomes available. The applications engineers start evaluating their application circuits and the test engineers examine their production test equipment.

But how can the users evaluate the new device? They have to have a data sheet—which is still in the process of being written. Every week, as the data sheet writer tries to polish and refine the incipient data sheet, other engineers are reporting, "These spec limits and conditions have to be revised," and, "Those application circuits don't work like we thought they would; we'll have one running in a couple of days." The marketing people insist that the data sheet must be finalized and frozen right away so that they can start printing copies to go out with evaluation samples.

These trying conditions may explain why data sheets always seem to have been thrown together under panic conditions and why they have so many rough spots. Users should be aware of the conflicting requirements: Getting a data sheet "as completely as possible" and "as accurately as possible" is compromised if one wants to get the data sheet "as quickly as possible."

The reader should always question the manufacturer. What are the alternatives? By not asking the right question, a misunderstanding could arise; getting angry with the manufacturer is not to anyone's advantage.

Robert Pease has been staff scientist at National Semiconductor Corp., Santa Clara, Calif., for eleven years. He has designed numerous op amps, data converters, voltage regulators and analog-circuit functions.

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Appendix G
Obsolete Product Replacement Guide

Some device types, individual temperature grades and package options have been discontinued. This guide is provided to help design engineers select and specify an appropriate alternative.

NSC Part Number	Replacement	Note
ADB1200	ADC3711	2
AF100	None	
AF121	None	
AF134	None	
DAC1200/1201	DAC1265	2
DH3467	None	
DH3725	None	
DS8627	None	
DS8628	None	
LF352	LM3631	2
LF400	None	
LF401	None	
LF13300	ADC3711	2
LF13741	None	
LH0001	LM4250	2
LH0005/LH0005A	LH0003	2
LH0020	LH0101	2
LH0022	AD506	2
LH0023	AD585	2
LH0037	LH0036	3
LH0038	None	
LH0043	AD583	2
LH0044	OP07	2
LH0045	None	
LH0052	OP100	2
LH0053	None	
LH0061	None	
LH0062	HA5162	2
LH0075	None	
LH0076	None	
LH0082	None	
LH0084	None	
LH0086	None	
LH0091	None	
LH0132	LH0032	2
LH2011	LM11	2
LH2101	LM101	2
LH2108	LM108	2
LH2110	LM110	2
LH2201A	LM201A	2

NSC Part Number	Replacement	Note
LH2208	LM208	2
LH2208A	LM208A	2
LH2301	LM301	2
LH2308	LM308	2
LH2310	LM310	2
LH4003	EL2031	2
LH4006	CLC110	2
LH4008	BB3553	2
LH4009	BB3553	2
LH4010	EL2004	2
LH4011	None	
LH4012	None	
LH4033	LH0033	2
LH4063	LH0063	2
LH4101	LM6313	2
LH4105	LM6218	2
LH4106	LM6313	2
LH4117	LM6181	2
LH4124	LM6181	2
LH4141	OPA654	2
LH4161	LM6361	2
LH4162	LM6361	2
LH4200	CLC104	2
LH4201	CLC104	2
LH4266	None	
LH4267	None	
LH4810	None	
LH4860	None	
LH7001	None	
LH7070	LH0070	2
LH24250	LM11	2
LM170/270/370	LM13600N	2
LM171/271/371	None	
LM172/272/372	None	
LM173/273/373	None	
LM174/274/374	None	
LM175/275/375	None	
LM216/316	LM11	2
LM363	None	
LM388N-2/N-3	LM388N-1	2
LM377N	LM2877P	3

Note 1: Pin for Pin replacement.

Note 2: FUNCTIONAL REPLACEMENT: Consult datasheet to determine suitability of the replacement for specific application.

Note 3: SIMILAR DEVICE with superior performance: Consult datasheet to determine suitability of the replacement for specific application.

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NSC Part Number	Replacement	Note
LM378N	LM2878P	3
LM379	LM2879T	3
LM322H	LM122H	2
LM565CH	LM565H	2
LM567CH	LM567H	2
LM592	None	
LM733	None	
LM776	None	
LM1014	None	
LM1017	None	
LM1019	None	
LM1800	None	
LM1801	None	
LM1822	LM1823	3
LM1812	None	
LM1837	None	
LM1863	LM1868	3
LM1866	None	
LM1870	None	
LM1871	None	
LM1872	None	

NSC Part Number	Replacement	Note
LM1877N-1/N-2/N-3	LM1877N-9	2
LM1880	None	
LM1884	None	
LM1889	None	
LM1895	LM1896	3
LM1897	None	
LM1965	LM1865	3
LM2002	None	
LM2005	None	
LM2065	LM1865	3
LM2895	LM2896	3
LM2905N	LM3905N	2
LM3011	None	
LM3064	None	
LM3075	None	
LM3820	None	
LM4500	None	
LM776	None	
LMC669	None	
MH0007	CTS0007	1
MM54240	None	

Note 1: Pin for Pin replacement

Note 2: FUNCTIONAL REPLACEMENT: Consult datasheet to determine suitability of the replacement for specific application.

Note 3: SIMILAR DEVICE with superior performance: Consult datasheet to determine suitability of the replacement for specific application.

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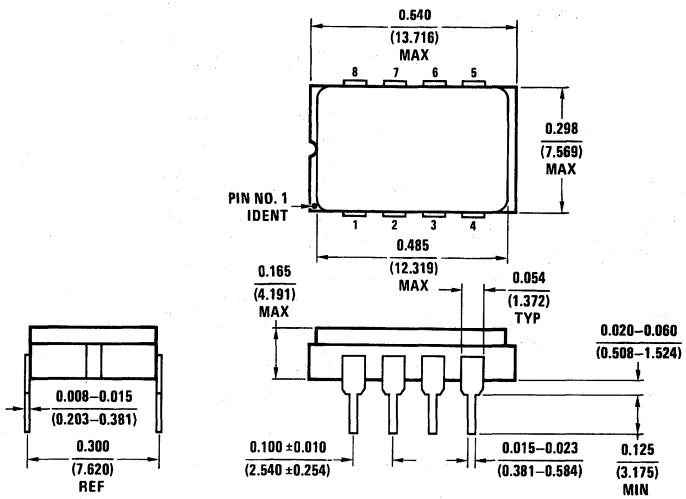
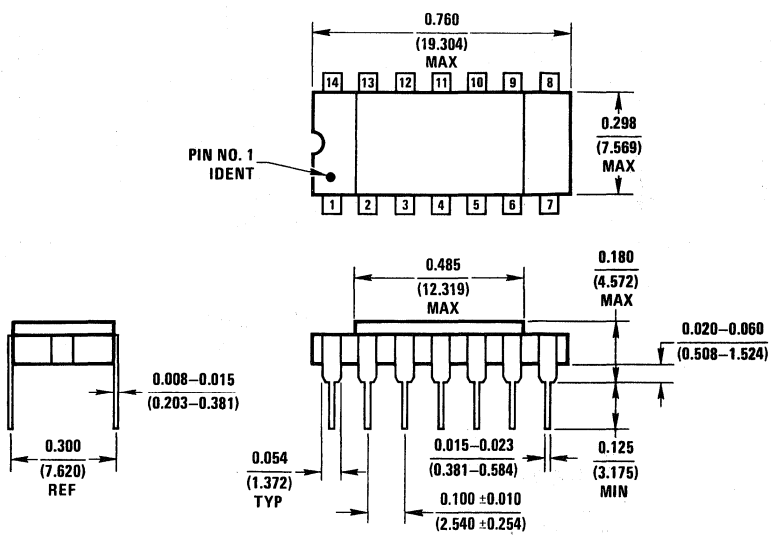
All dimensions are in inches (millimeters)

8 Lead Hermetic Dual-In-Line Package (D)
NS Package Number D08C



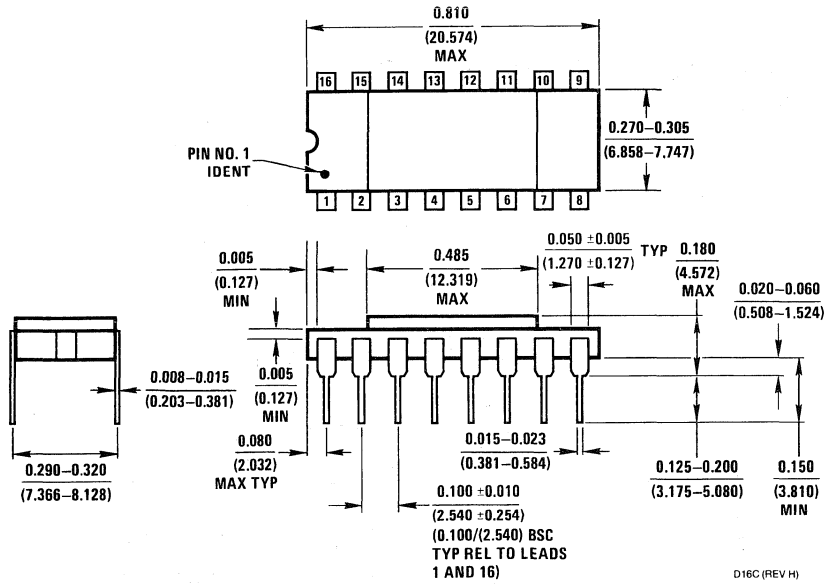
D08C (REV C)

14 Lead Hermetic Dual-In-Line Package (D)
NS Package Number D14E

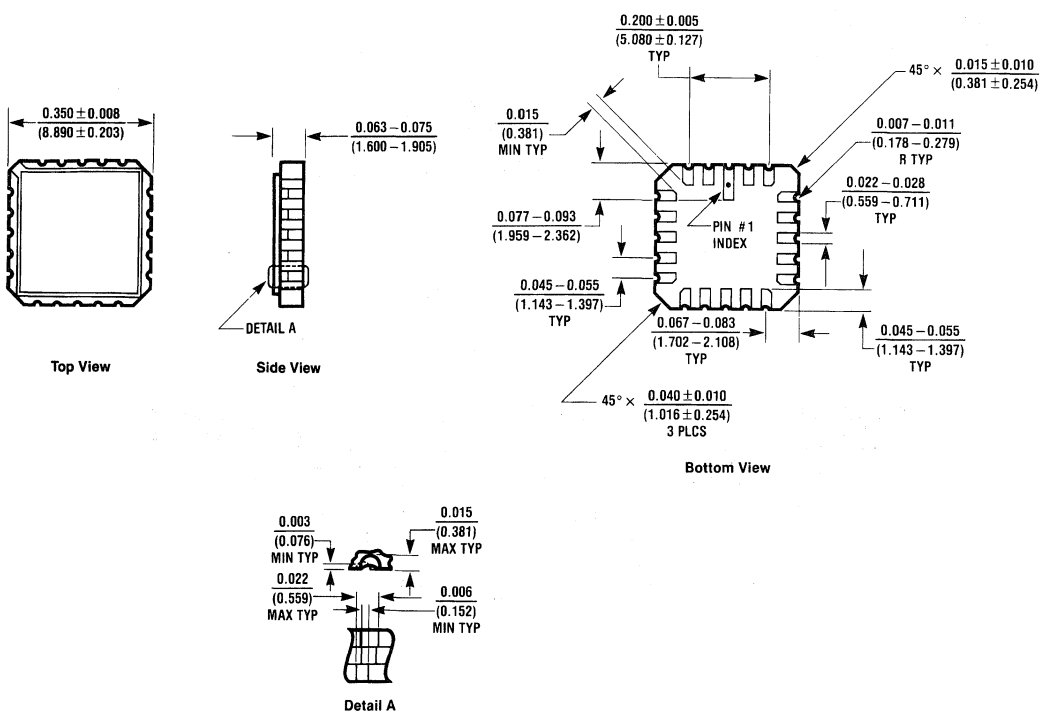


D14E (REV E)

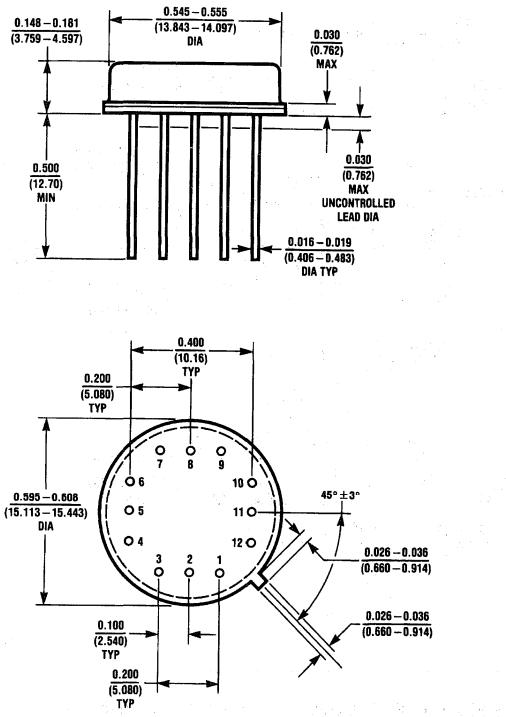
16 Lead Hermetic Dual-In-Line Package (D)
NS Package Number D16C



20 Terminal Ceramic Leadless Chip Carrier (LCC)
NS Package Number E20A

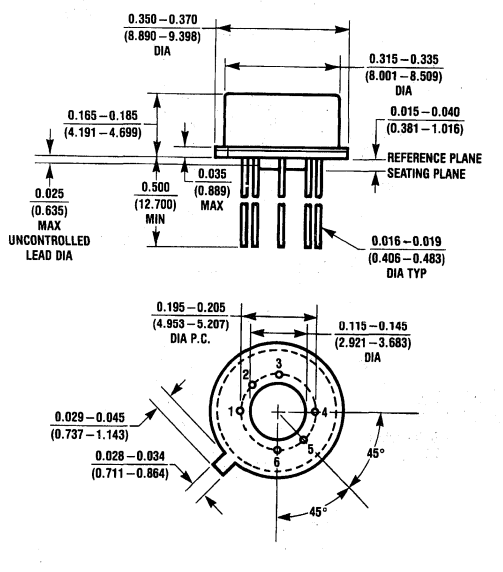


12 Lead (0.400" Square Pattern) Metal Can Package (G)
NS Package Number G12B



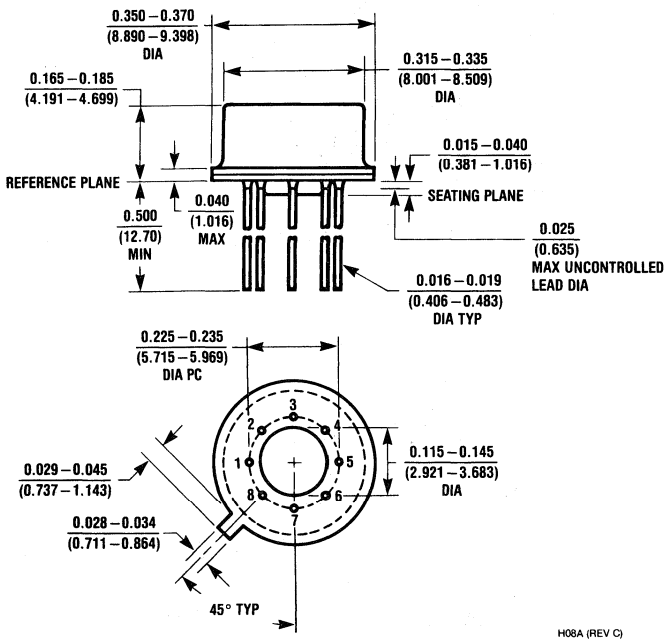
G12B (REV C)

6 Lead (0.200" Diameter P.C.) TO-99 Metal Can Package (H)
NS Package Number H06C



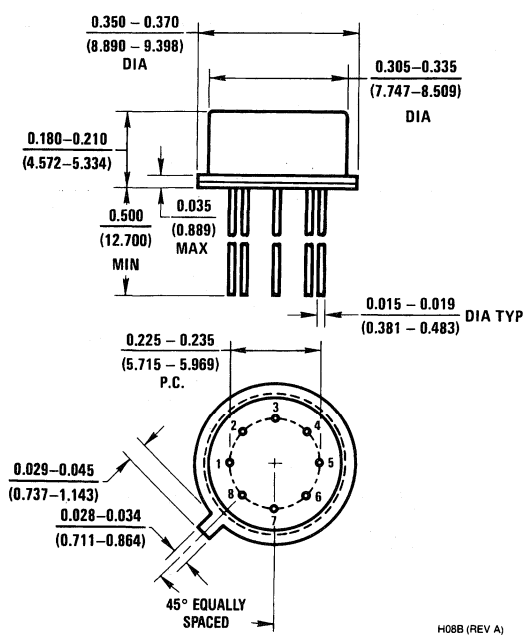
H06C (REV D)

8 Lead (0.230″ Diameter P.C.) Metal Can Package (H)
NS Package Number H08A



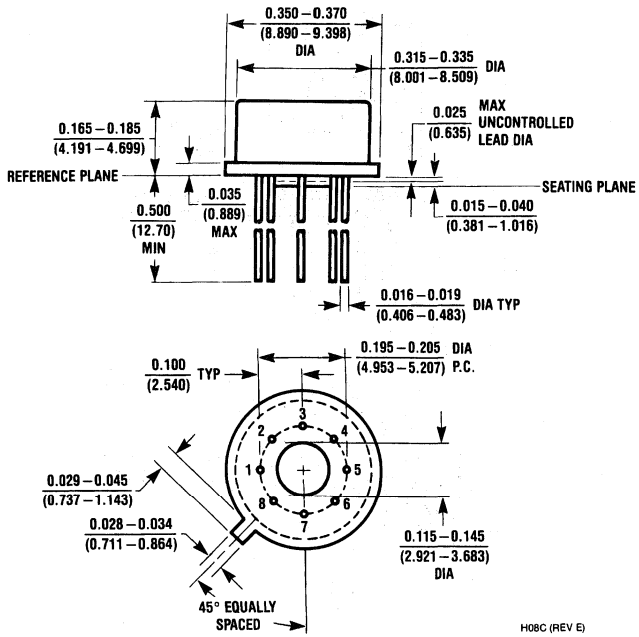
H08A (REV C)

8 Lead (0.230″ Diameter P.C.) Metal Can Package (H)
NS Package Number H08B

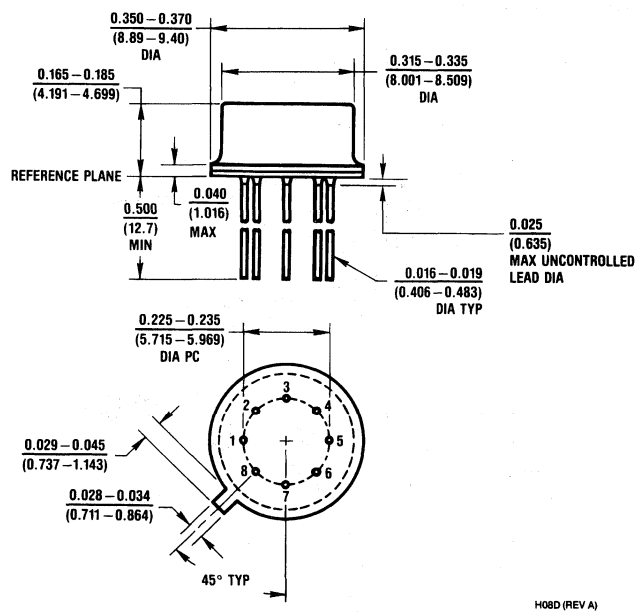


H08B (REV A)

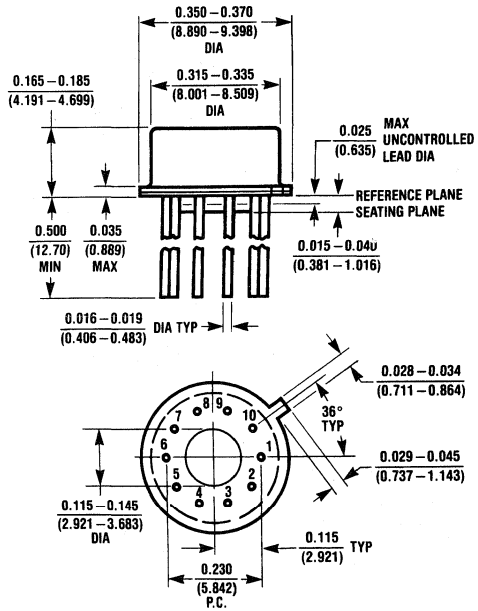
8 Lead (0.200" Diameter P.C.) TO-99 Metal Can Package (H)
NS Package Number H08C



8 Lead (0.230" Diameter P.C.) Metal Can Package (H)
NS Package Number H08D

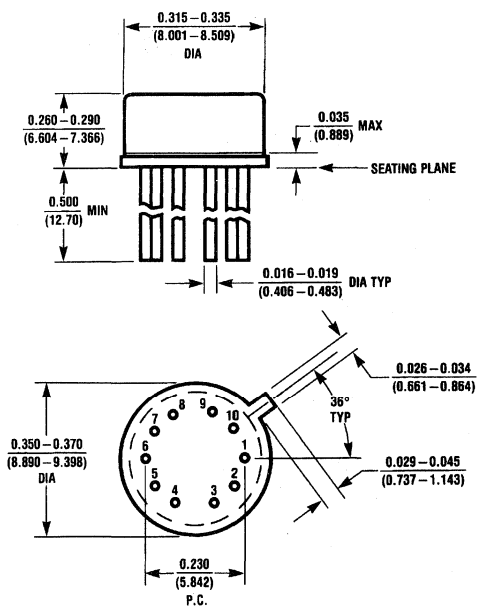


10 Lead (0.230″ Diameter P.C.) TO-100 Metal Can Package (H)
NS Package Number H10C



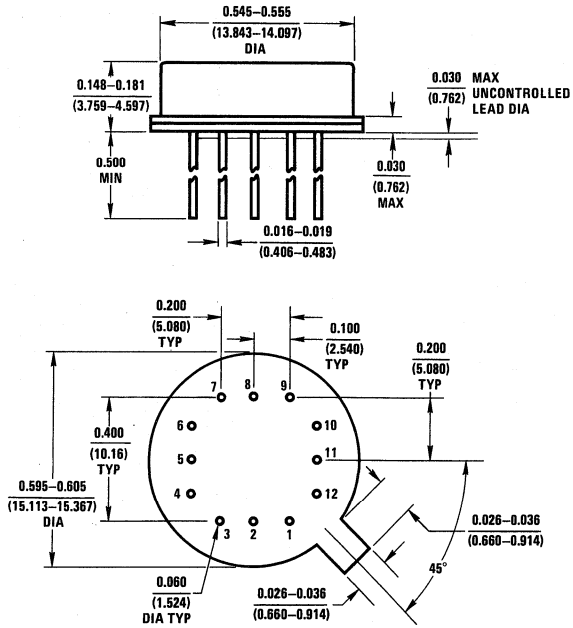
H10C (REV E)

10 Lead (0.230″ Diameter P.C.) Metal Can Package (H)
NS Package Number H10G



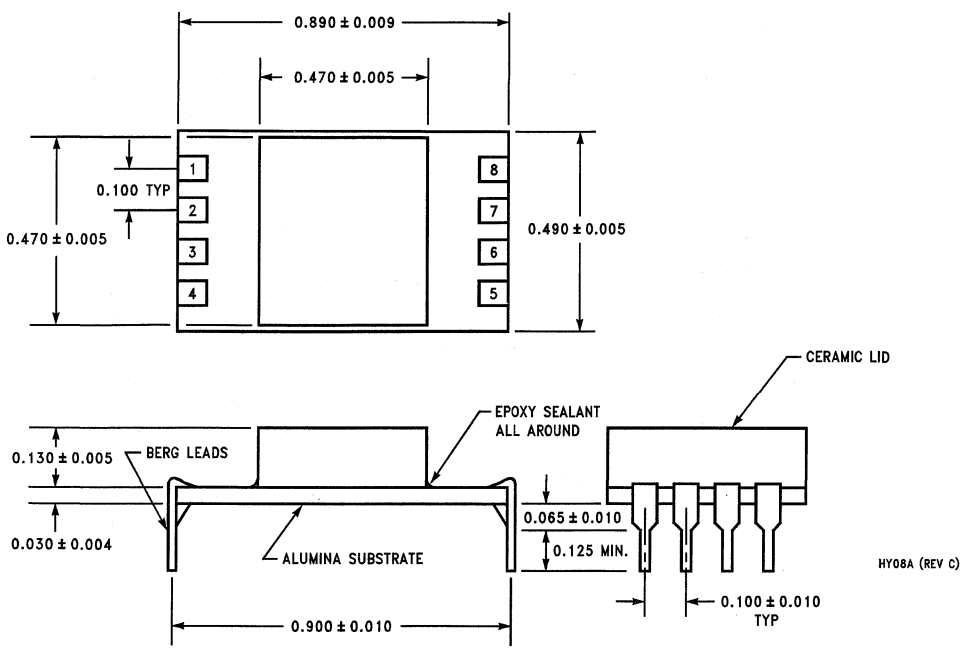
H10G (REV B)

12 Lead (0.230" Diameter P.C.) Metal Can Package (H)
NS Package Number H12B



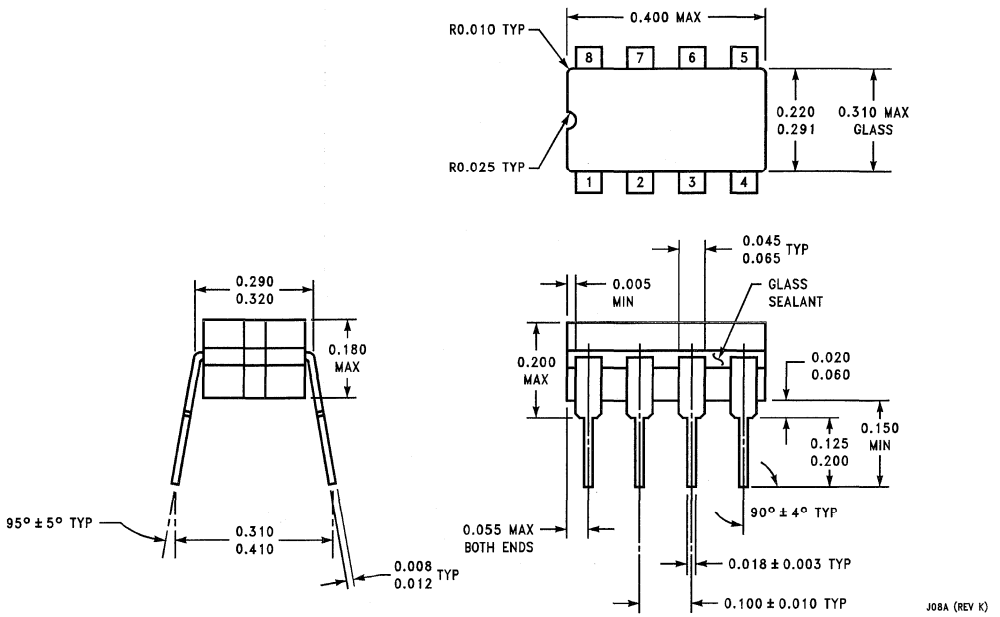
H12B (REV A)

8 Lead Dual-In-Line Hybrid Package (J)
NS Package Number HY08A

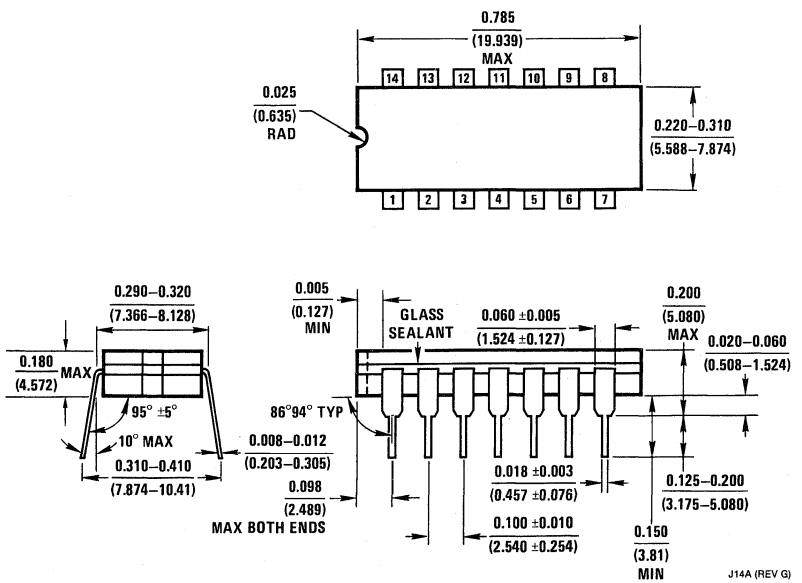


HY08A (REV C)

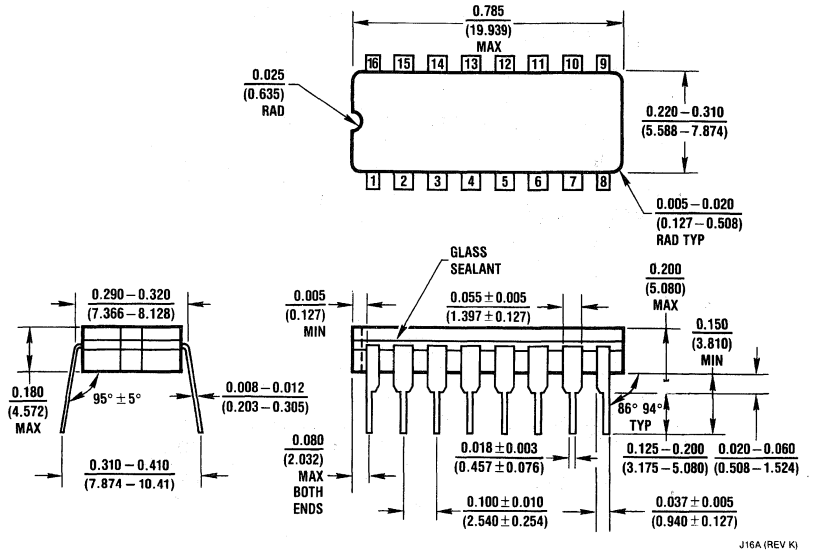
8 Lead Ceramic Dual-In-Line Package (J)
NS Package Number J08A



14 Lead Ceramic Dual-In-Line Package (J)
NS Package Number J14A

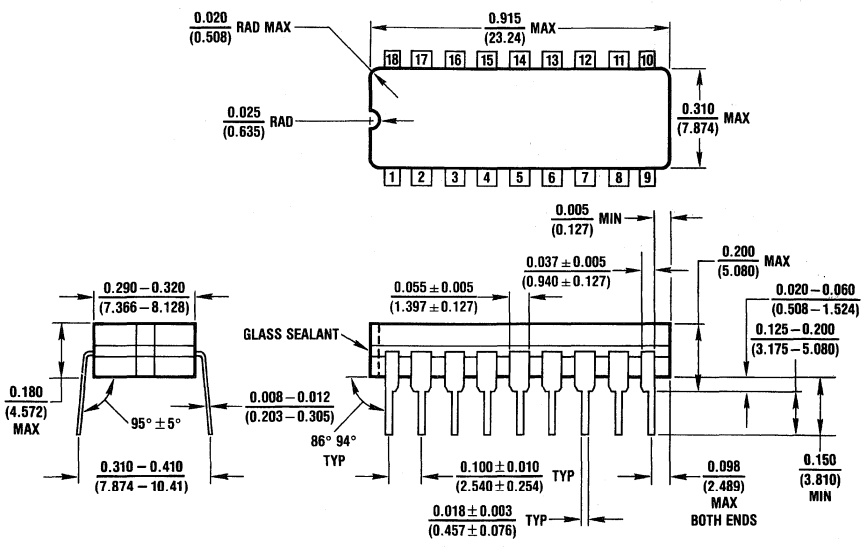


16 Lead Ceramic Dual-In-Line Package (J)
NS Package Number J16A



J16A (REV K)

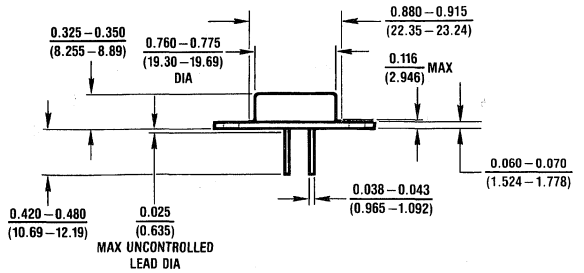
18 Lead Ceramic Dual-In-Line Package (J)
NS Package Number J18A

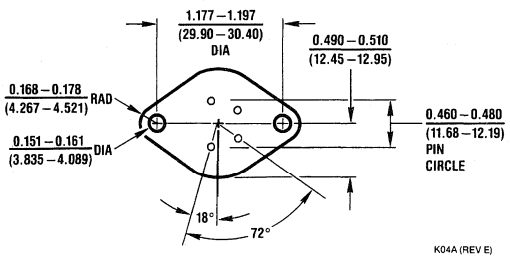


J18A (REV L)

6

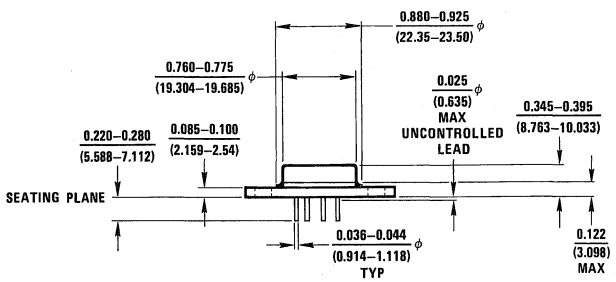
4 Lead TO-3 Metal Can Package (K)
NS Package Number K04A

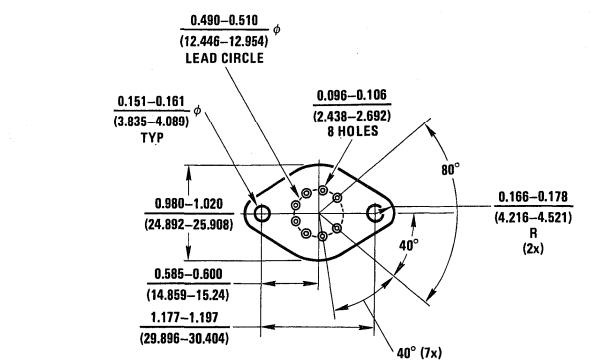




K04A (REV E)

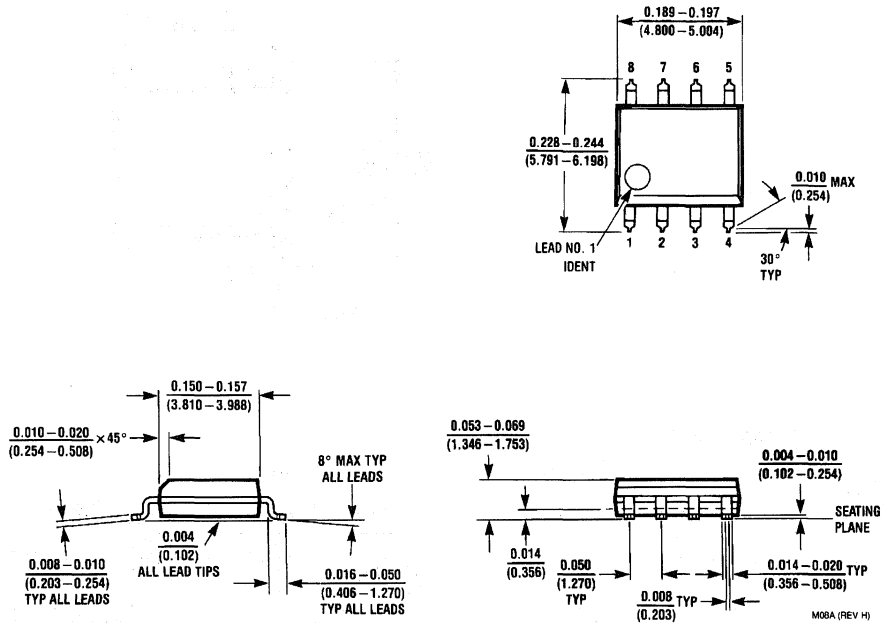
8 Lead TO-3 Metal Can Package (K)
NS Package Number K08A



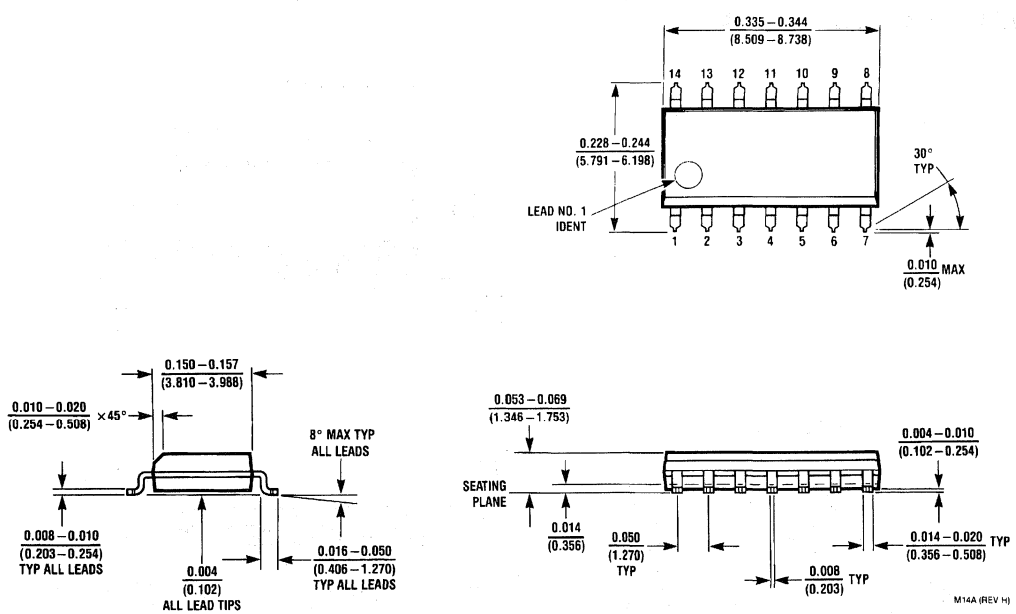


K08A (REV C)

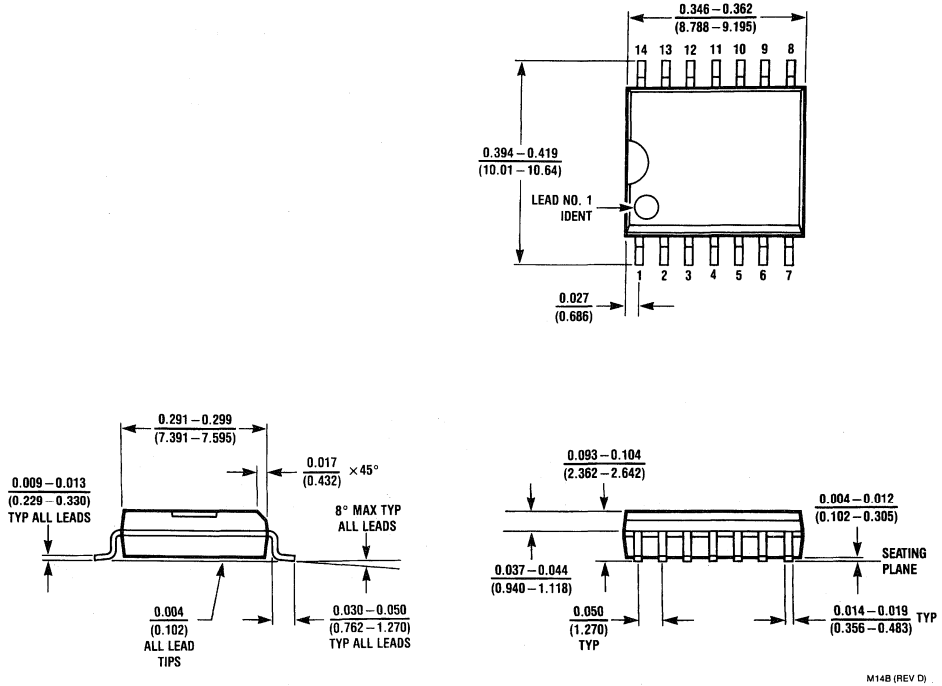
8 Lead (0.150" Wide) Small Outline Molded Package (M)
NS Package Number M08A



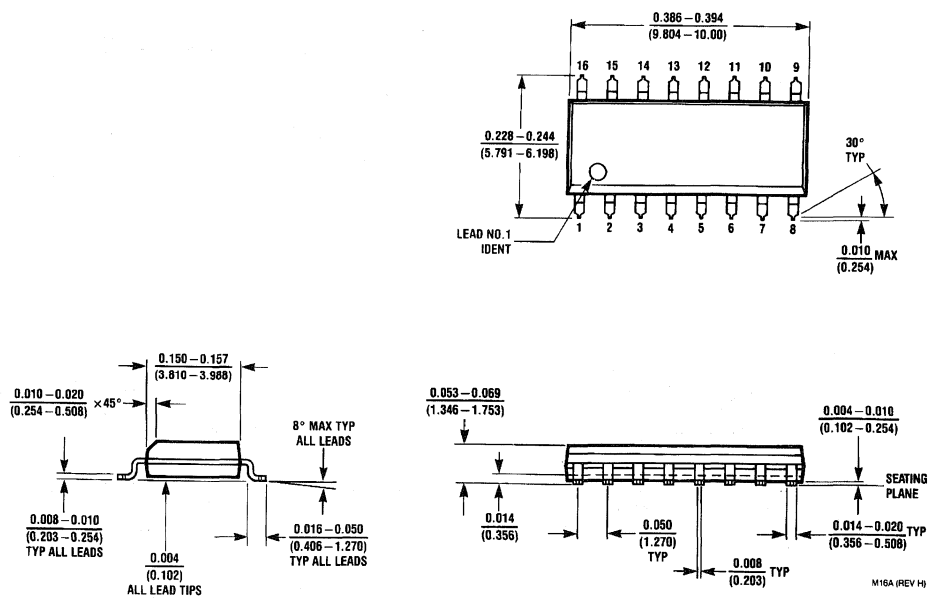
14 Lead (0.150" Wide) Small Outline Molded Package (M)
NS Package Number M14A



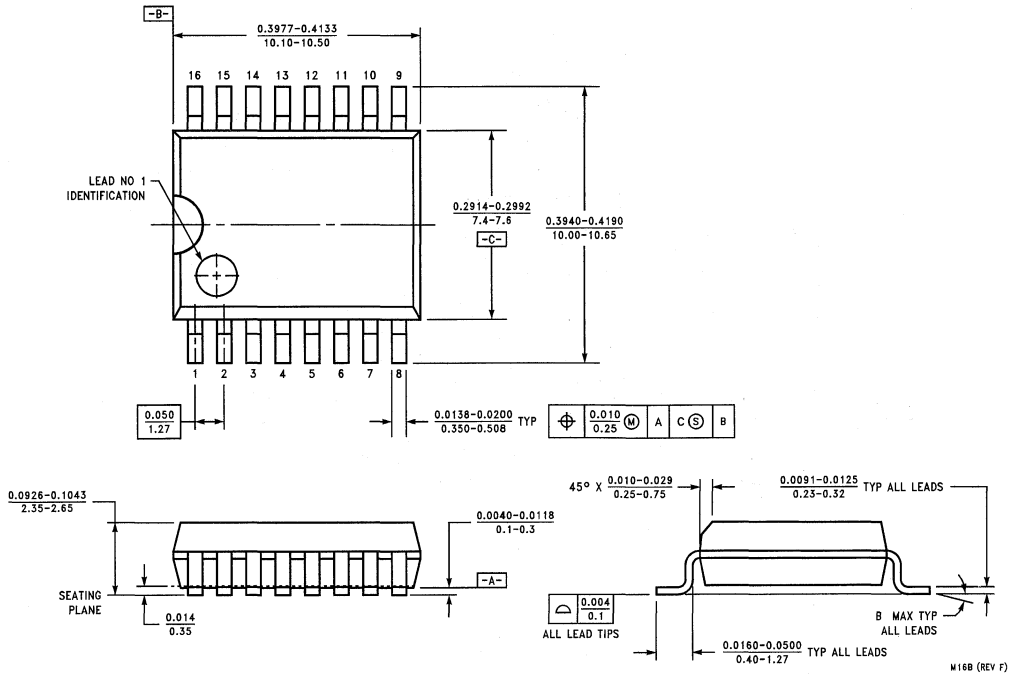
14 Lead (0.300" Wide) Small Outline Molded Package (M)
NS Package Number M14B



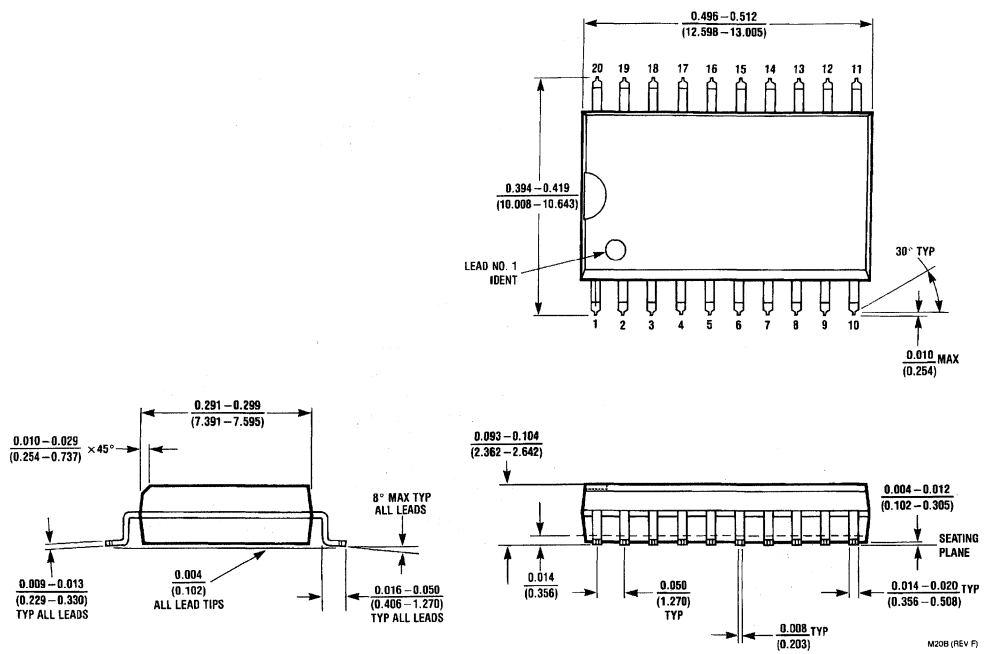
16 Lead (0.150" Wide) Small Outline Molded Package (M)
NS Package Number M16A



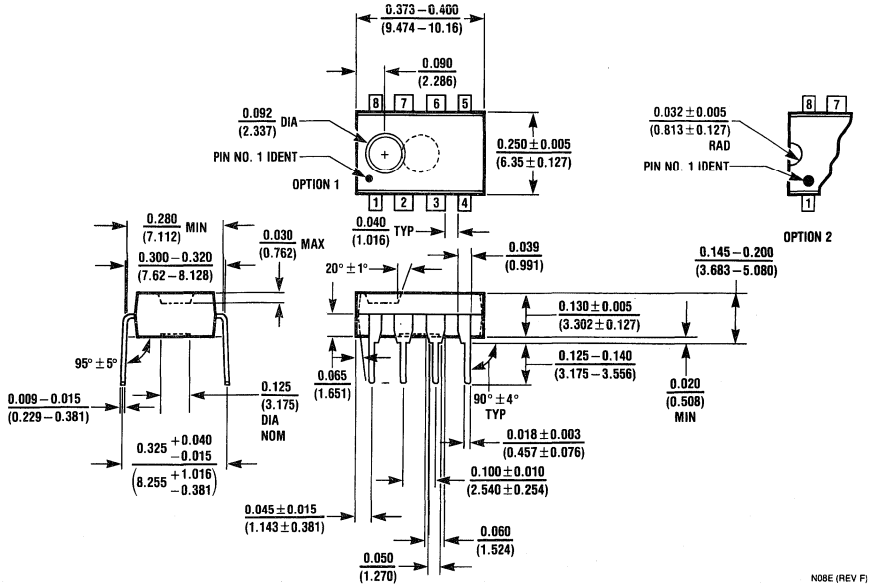
16 Lead (0.300" Wide) Small Outline Molded Package (M)
NS Package Number M16B



20 Lead (0.300" Wide) Small Outline Molded Package (M)
NS Package Number M20B

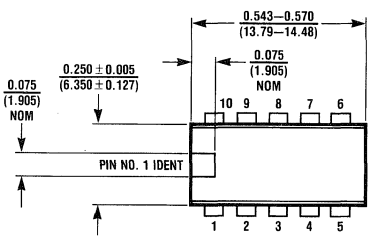


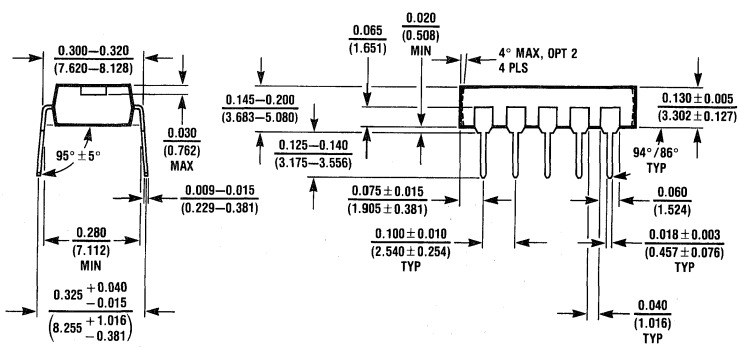
8 Lead Molded Dual-In-Line Package (N)
NS Package Number N08E



N08E (REV F)

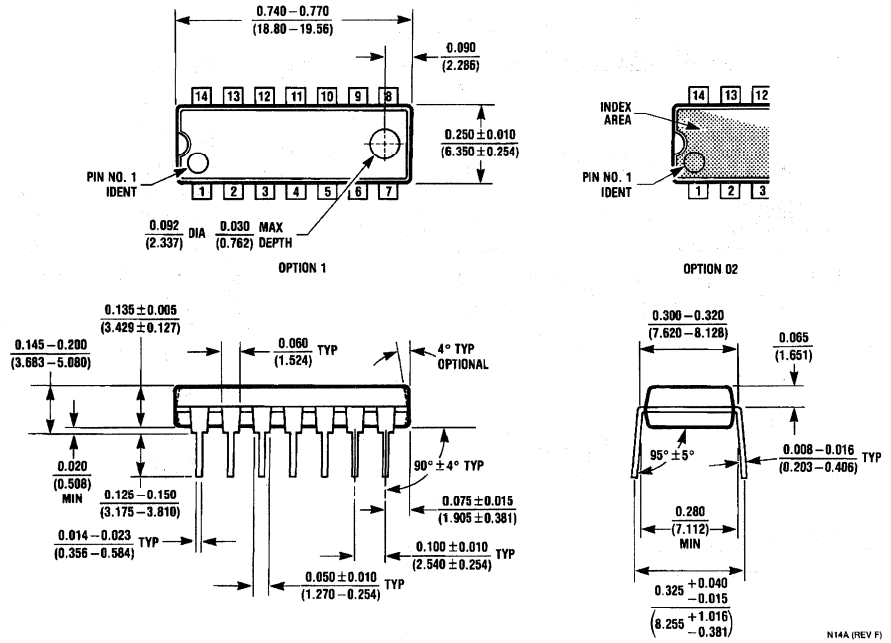
10 Lead Molded Dual-In-Line Package (N)
NS Package Number N10A



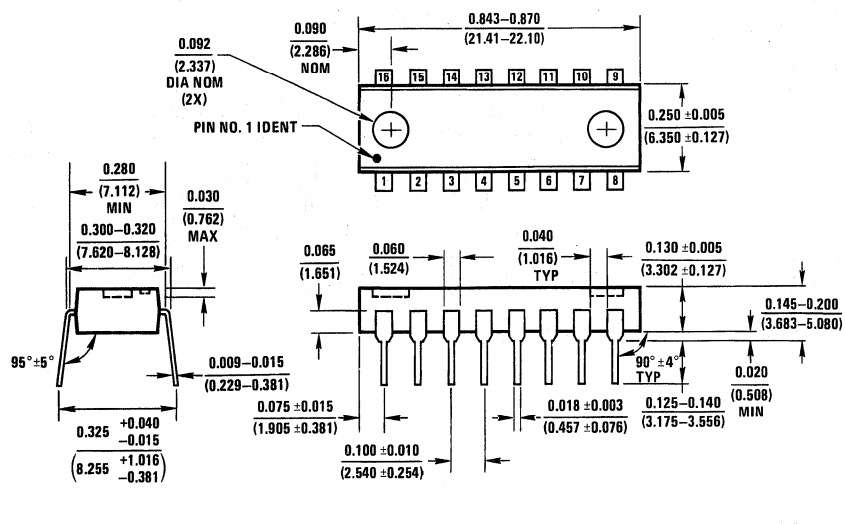


N10A (REV A)

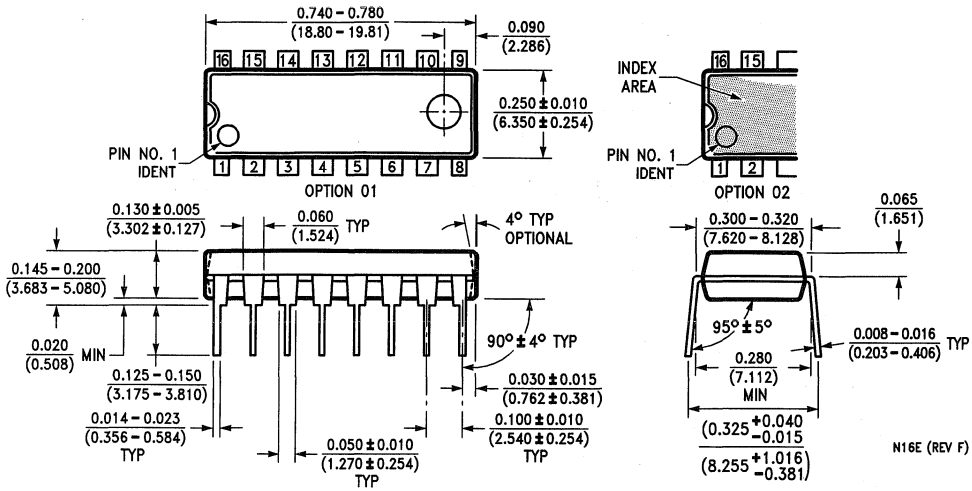
14 Lead Molded Dual-In-Line Package (N)
NS Package Number N14A



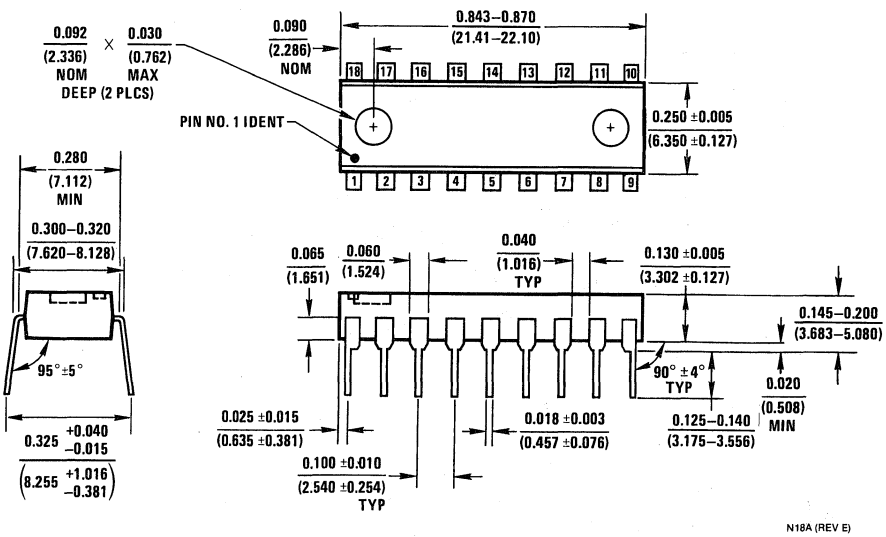
16 Lead Molded Dual-In-Line Package (N)
NS Package Number N16A



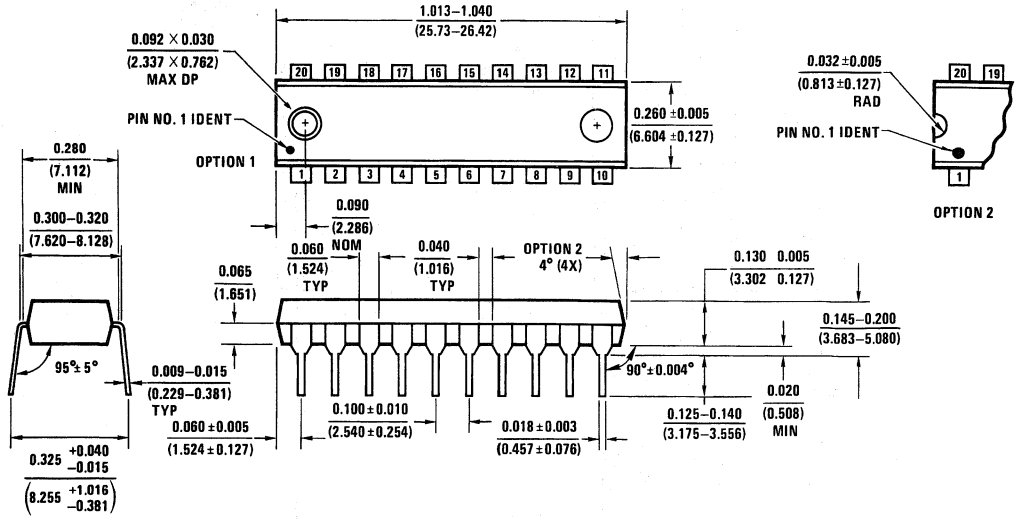
16 Lead Molded Dual-In-Line Package (N)
NS Package Number N16E



18 Lead Molded Dual-In-Line Package (N)
NS Package Number N18A

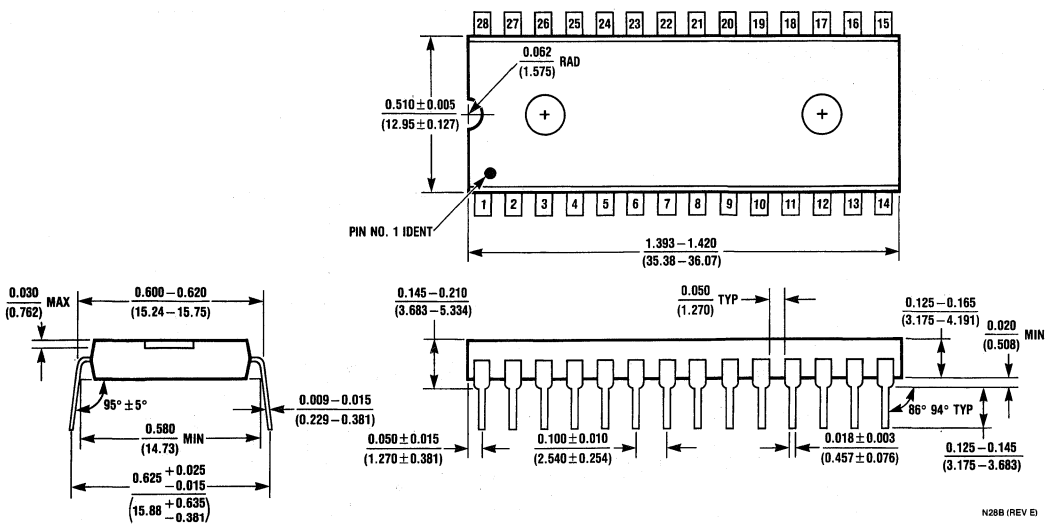


20 Lead Molded Dual-In-Line Package (N)
NS Package Number N20A



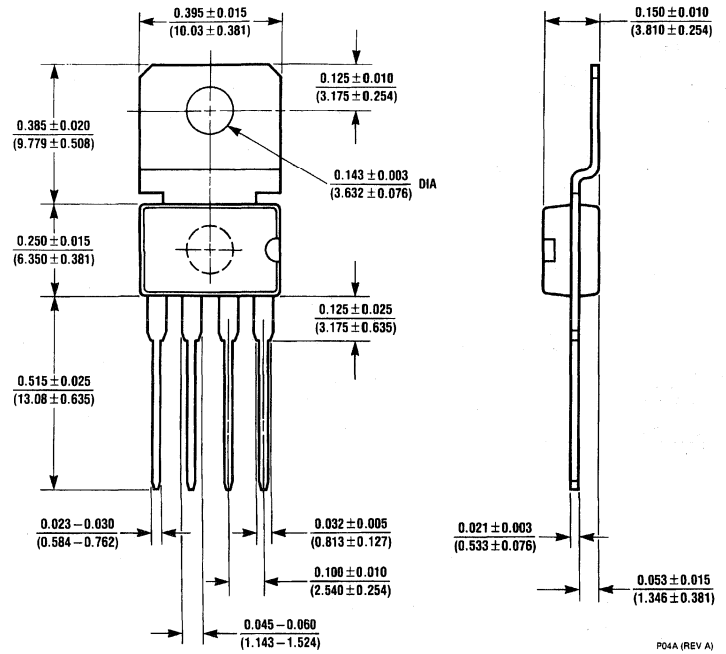
N20A (REV G)

28 Lead Molded Dual-In-Line Package (N)
NS Package Number N28B

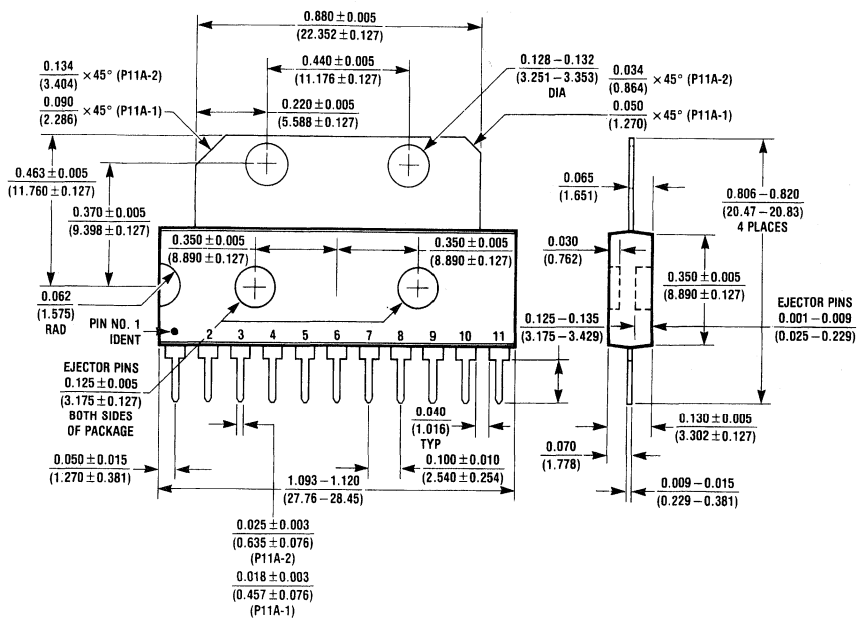


N28B (REV E)

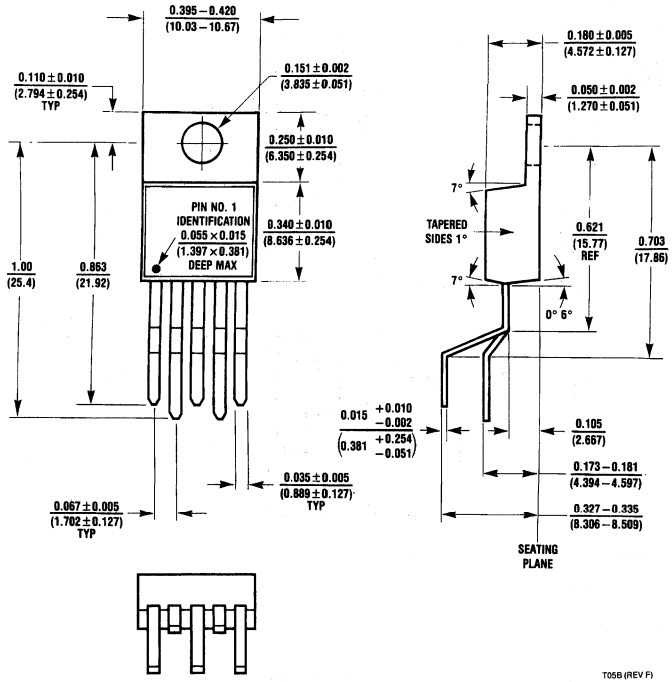
4 Lead TO-202 Molded Package (P)
NS Package Number P04A



11 Lead Molded Single In-Line Package (P)
NS Package Number P11A

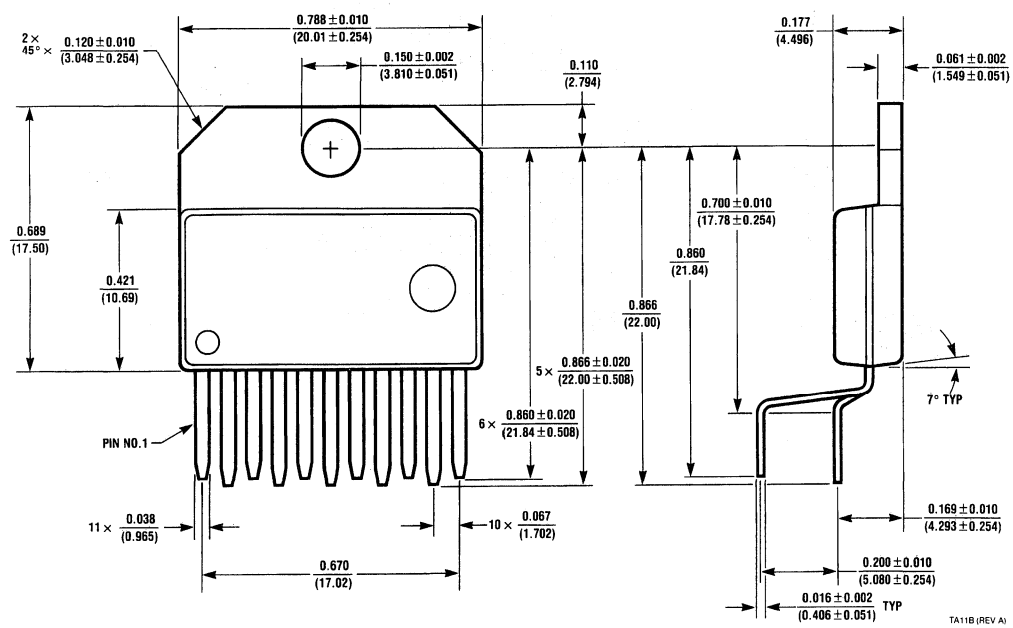


5 Lead TO-220 Molded Package (T)
NS Package Number T05B



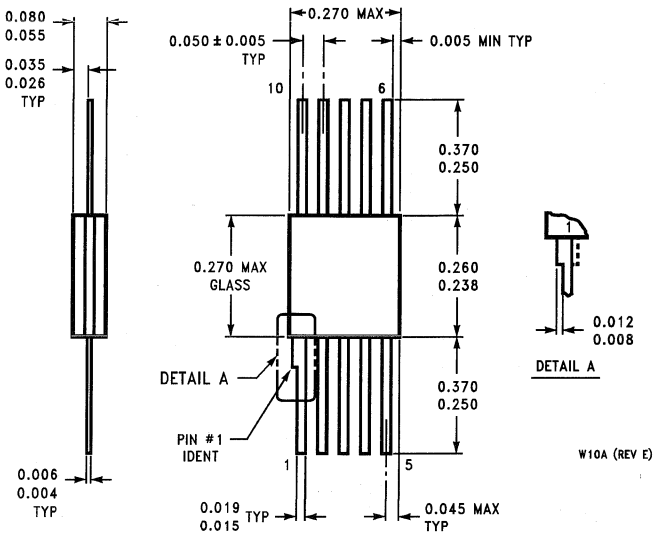
T05B (REV F)

11 Lead TO-220 Molded Package (T)
NS Package Number TA11B

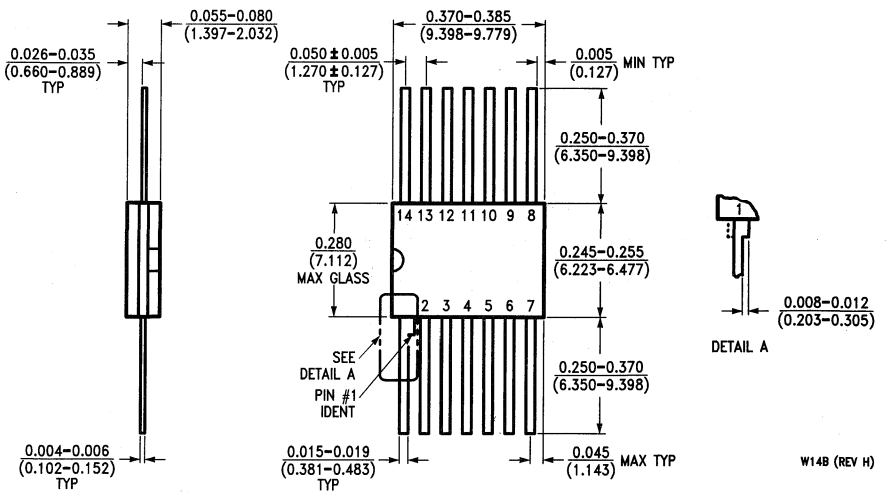


TA11B (REV A)

10 Lead Ceramic Flatpak (W)
NS Package Number W10A



14 Lead Ceramic Flatpak (W)
NS Package Number W14B



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